FRONT-END AND READ-OUT ELECTRONICS FOR THE UPGRADE OF THE NUMEN FPD

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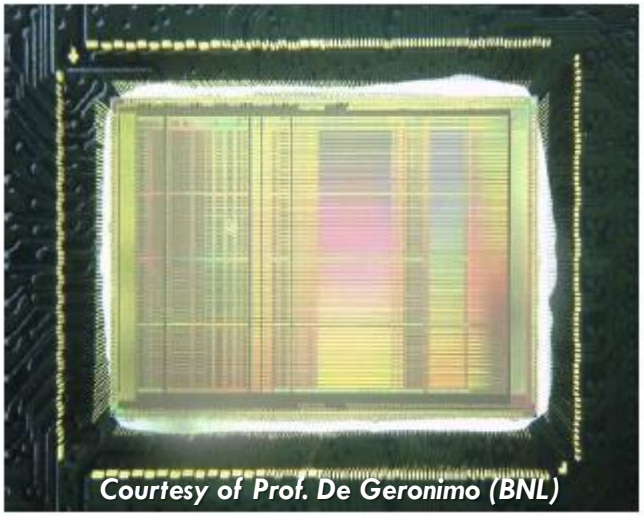
UPGRADE OF FOCAL PLANE DETECTOR (FPD) specifications

- *Tracker:*
  - *16 layers, 1 m width, segmented in 0,5 mm steps =32000 channels*
- *ΔE-ΔE-E Telescopes:*
  - *2500 SiC Telescopes (1x1 cm^2)= 7500 channels (2500x3 channels each telescope)*
- ***Foreseen event – rate after the upgrade of the cyclotron: 100 KHz/cm***

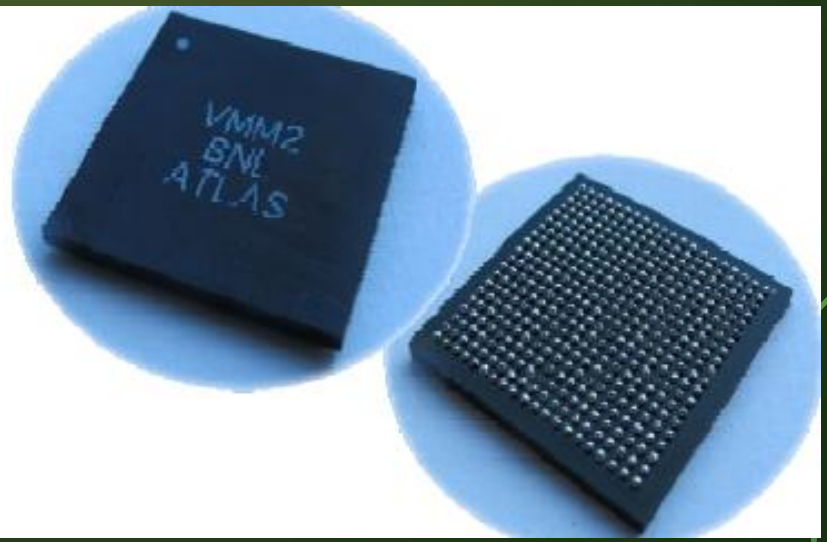
- ***Modularity***
- ***Ease of maintenance***
- ***Radiation Tolerance***
- ***Low Power***
- ***Low Cost***

VMM2 CHIP
BROOKHAVEN NATIONAL LABORATORIES

- *Selected after a deep survey between available front-end ASICs;*
- *Designed for MicroMegas detectors in ATLAS;*
- *Collaboration established with the designer: **Prof. G. De Geronimo**;*
- *Radiation Tolerant;*
- *New version VMM3 could take in account the NUMEN specifications;*
- *Available in the future in big volume;*
- *All digital read-out compliant with the foreseen event rate;*
- *Suitable for all the detector types foreseen in the final FPD:*
  - *Tracker (GEM, MicroMegas);*
  - *Calorimeter- particle identification (SiC ΔE-E);*
  - *APD.*



Courtesy of Prof. De Geronimo (BNL)



VMM2 CHIP
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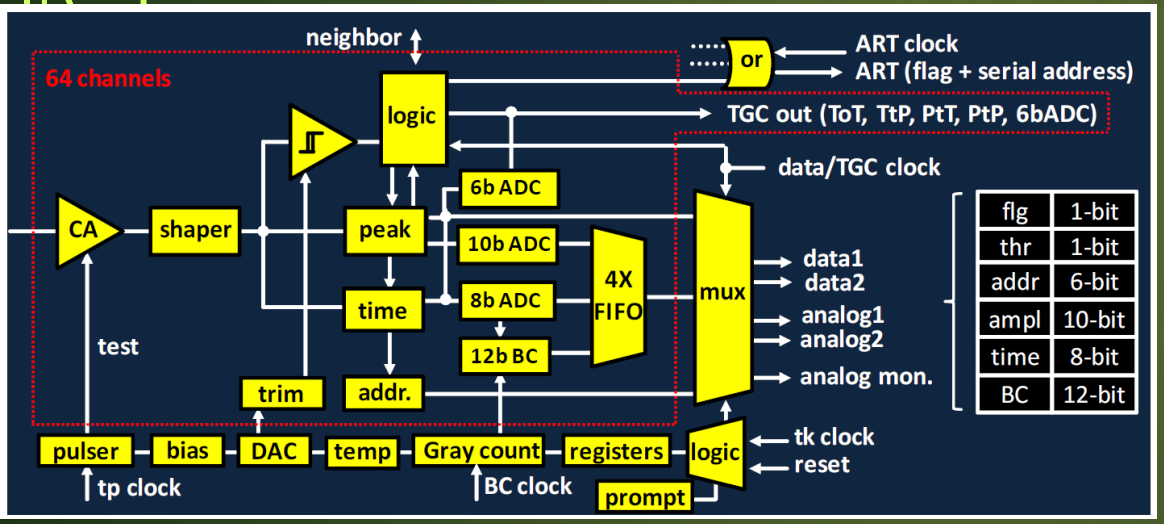
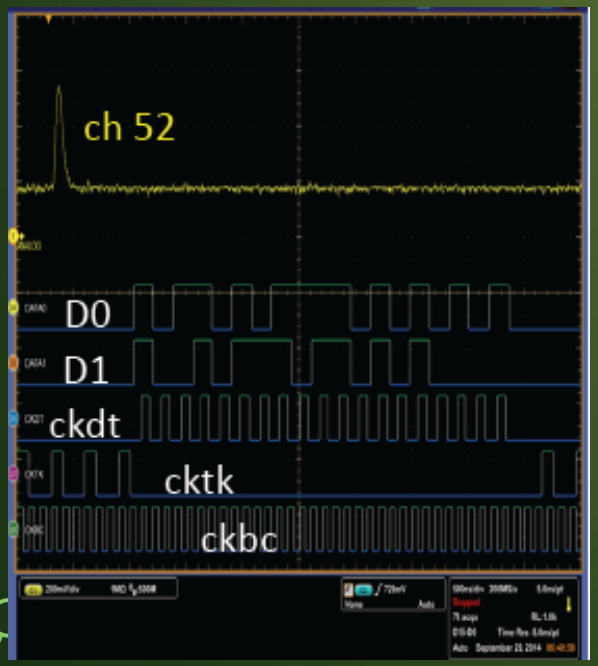


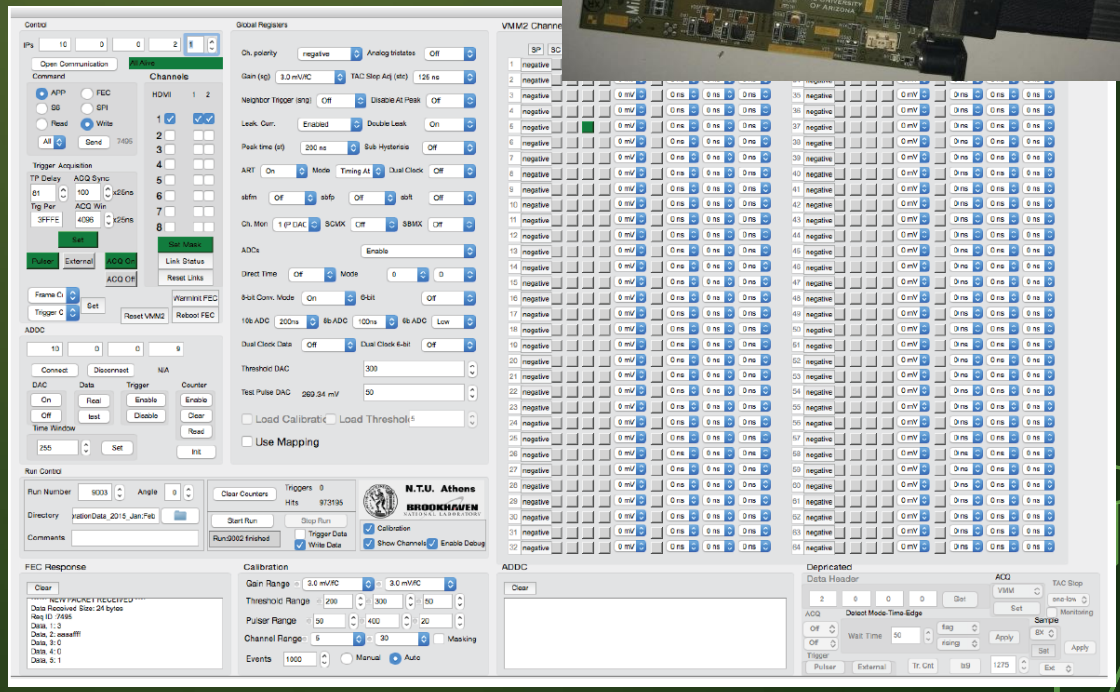
130nm 1.2V 8-metal CMOS technology from IBM
Courtesy of Prof. De Geronimo (BNL)

- *64 linear front-end channels:*
- *low-noise charge amplifier (CA) with adaptive feedback;*
- *test capacitor and pulse generator for calibration;*
- *adjustable polarity;*
- *optimized for a capacitance of 200pF and a peaking time of 25 ns.*
- *third-order shaper (DDF) - adjustable peaking time in four values (25, 50, 100, and 200 ns);*
- *Stabilized band-gap referenced baseline;*
- *Gain adjustable in eight values (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC).*
- *Many mode of operation, selected "continuous digital":*
  - *38 bit generated for each event read-out @ about 200 MHz;*
  - *Id channel-peak amplitude (10b) - time stamp (10b);*
  - *4-event deep de-randomizing FIFO per channel, read-out token ring;*
  - *8 LVDS digital channel required for the read-out and control of the chip;*
- *Power dissipation 4 mW per channel.*

VMM2 Test board

Thanks to the collaboration with G. De Geronimo a complete FE-RO chain for one VMM2 chip is available from sept 2015. Control and read-out software included.

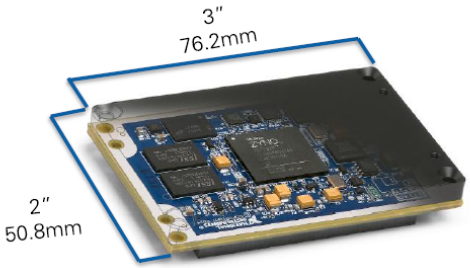




Continuous digital mode:
38 bit/event

flg	1-bit
thr	1-bit
addr	6-bit
ampl	10-bit
time	8-bit
BC	12-bit

NI System on Module (SOM) Specifications



Specifications

Processor SoC
Xilinx Zynq-7020 667 MH Dual-Core ARM Cortex-A9 Artix-7 FPGA Fabric
Size and Power
50.8mm x 78.2mm (2 in. X 3 in.) Typical Power: 3 W to 5 W
Memory
Nonvolatile: 512 MB DRAM: 512 MB
Operating Temperature
-40 °C to 85 °C Local Ambient

Read-out of VMMx chips will be performed by a SOM based board, custom designed for the experimental demands:

- *Low Power;*
- *Radiation Tolerance;*
- *Low Cost;*
- *Re-configurability;*

Measured Performance:

- ✓ *Sampling of 128 digital input SE @230MHz*
- ✓ *Sampling of 64 digital input SE @350MHz*

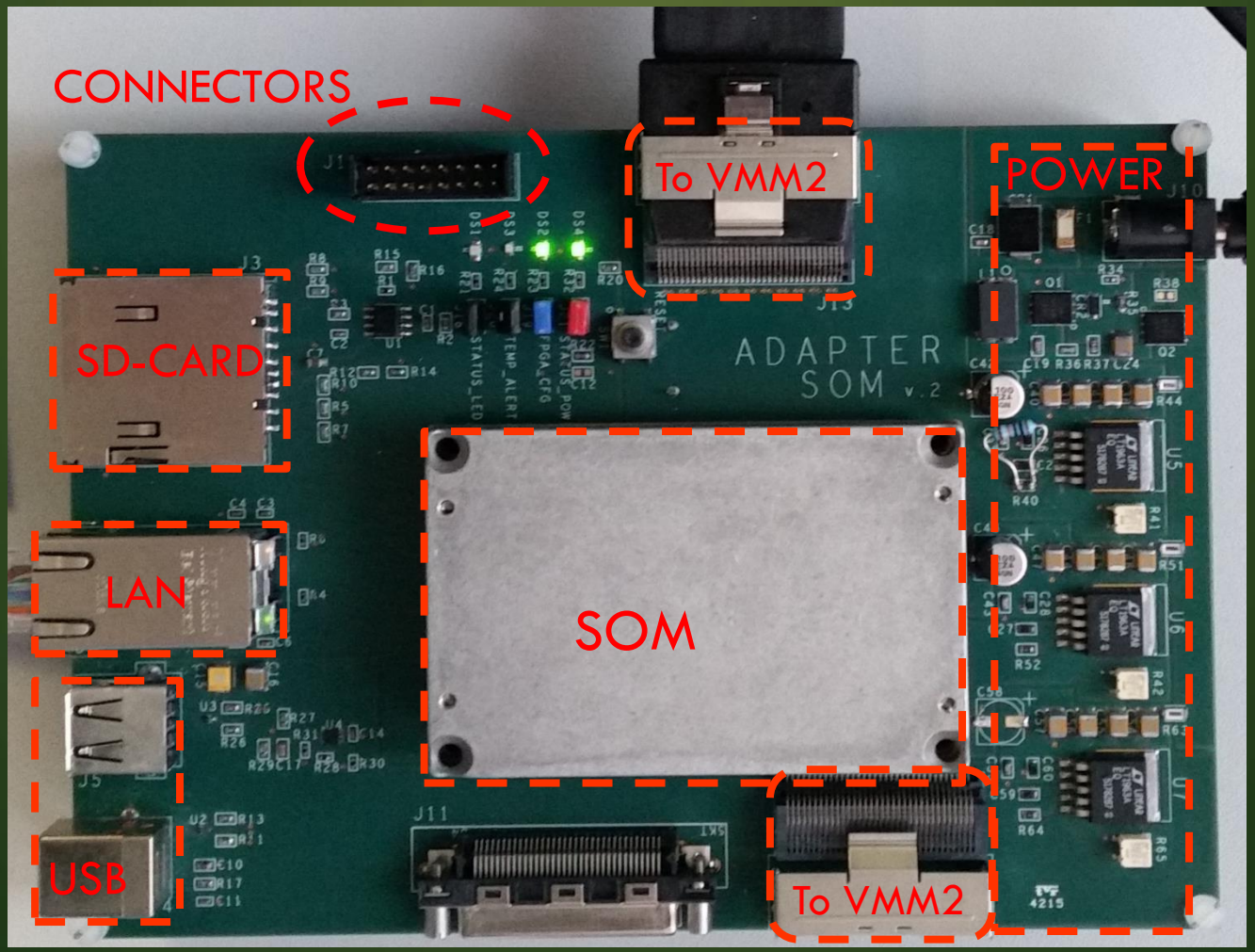
Applications:

- ✓ Real – Time characterization of a proton beam (position, size, fluence, energy);
- ✓ Imaging and radiography;
- ✓ Interfacing with:
  - ✓ DACs
  - ✓ ASICs (MAROC, VMM2)
  - ✓ SD – Cards, USB – HDD
  - ✓ High speed data transfer (Gigabit Ethernet)

Dedicated Processor I/O
Gigabit Ethernet
USB Host
USB Host/Device
SDHC
Serial TX/RX (console out)

FPGA I/O
16 SE fixed at 3.3V
144 SE/72 diff pairs with IO level selection
3 Banks with user supplied voltage
Configurable Peripherals: Gigabit Ethernet, RS232 x3, RS485 x2, CAN x2

Adapter SOM


CONNECTORS
To VMM2
POWER
SD-CARD
ADAPTER
SOM v.2
LAN
SOM
USB
To VMM2

Test SOM-VMM2

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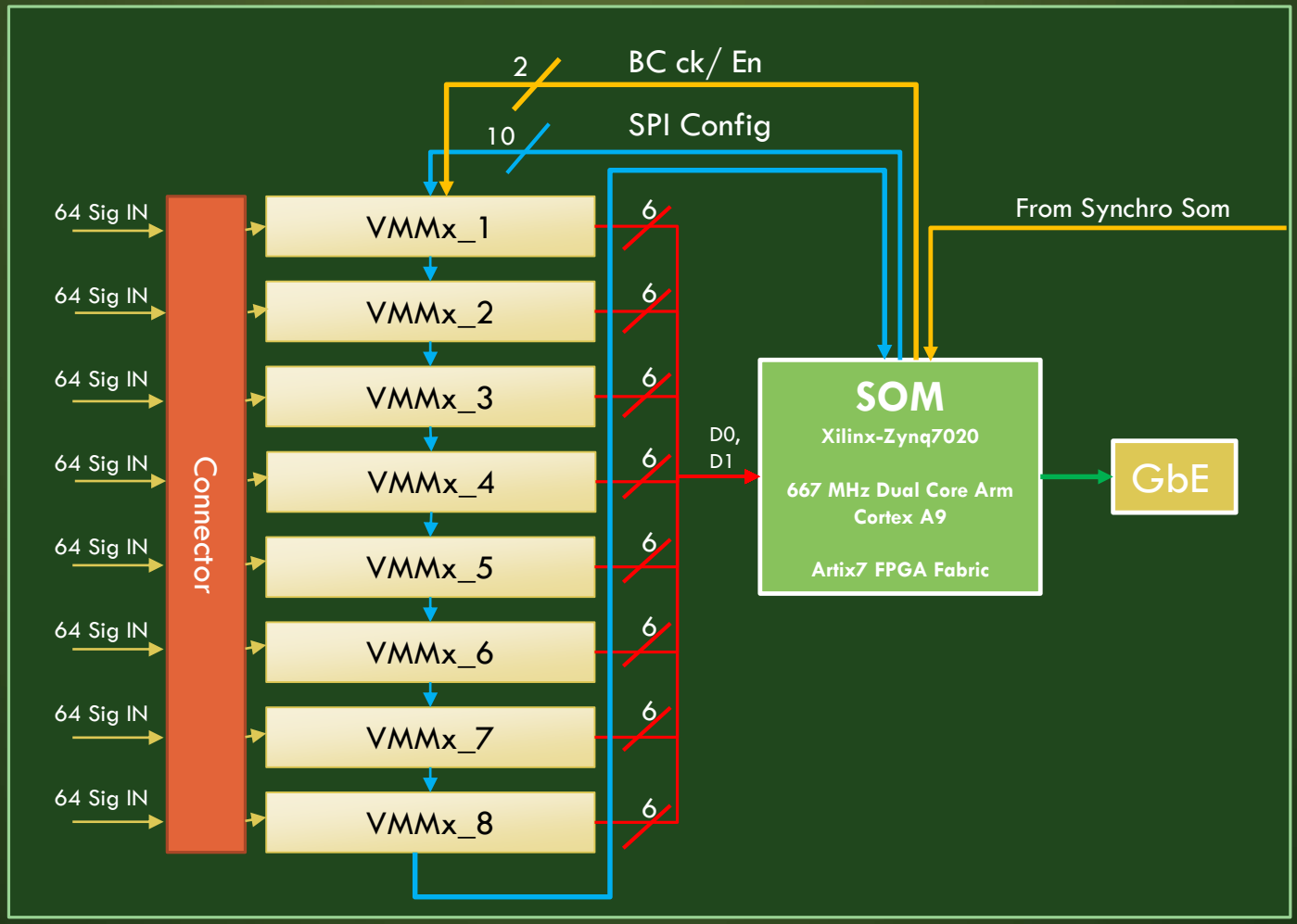
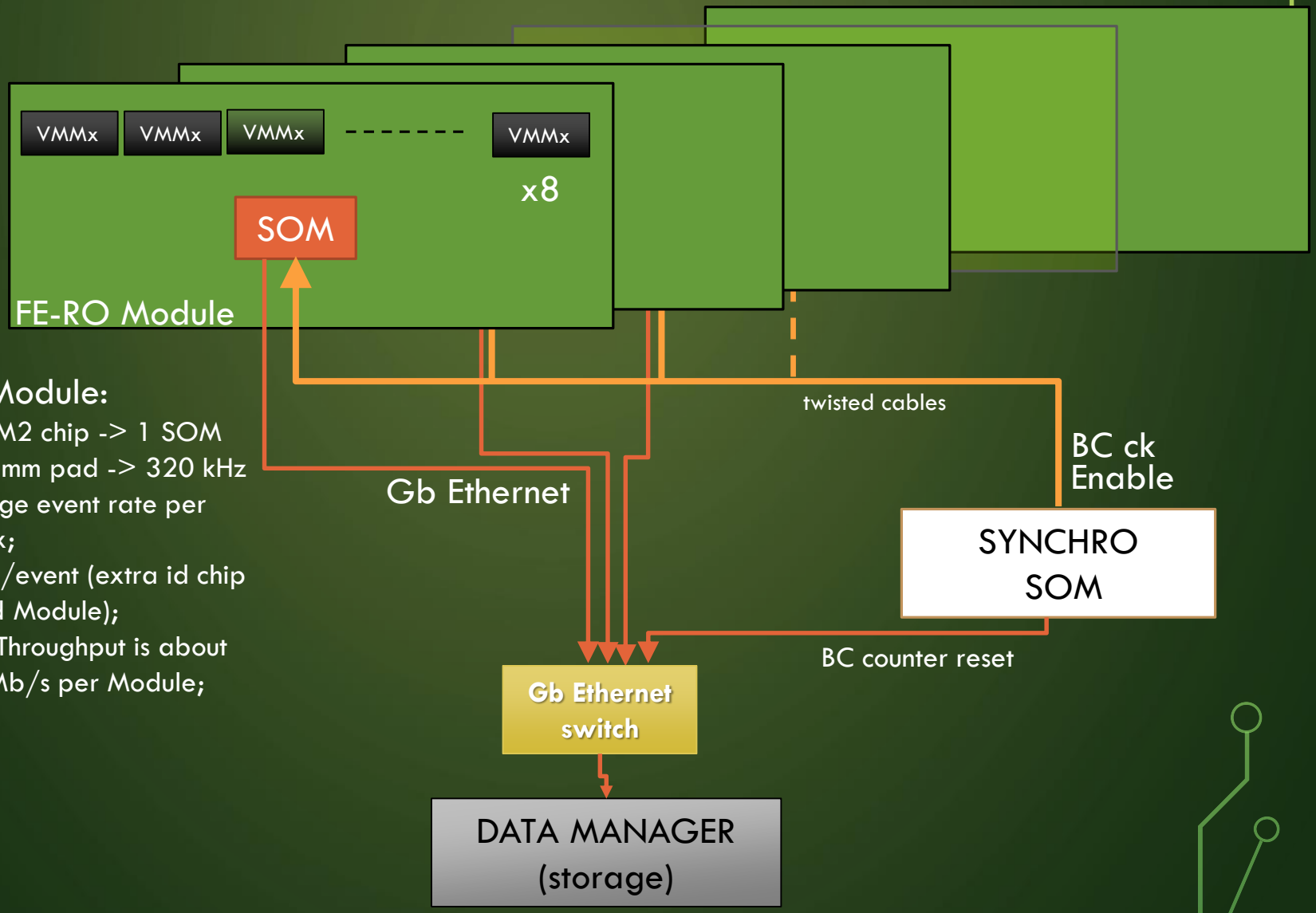
- SOM-VMM2 board fully functional:
- Firmware SOM ready for:
  - Configuration:
  - Calibration;
  - Synchronization:
  - Read-out;
- LabView GUI:
  - Slow control;
  - DAQ

FE-RO Module



- *8 VMMx chip read-out by 1 SOM is one FE-RO Module;*
- *Possible increase to 10 VMMx, to be confirmed!*

FE-RO ARCHITECTURE



FE-RO Module:

- 8 VMM2 chip -> 1 SOM
- If 0,5 mm pad -> 320 kHz average event rate per VMMx;
- 38 bit/event (extra id chip and id Module);
- Data Throughput is about 100 Mb/s per Module;

CONCLUSIONS

- A complete VMM2-SOM was successfully tested and is ready for interfacing with the prototype of some detector;
- For the FE-RO Module final design we need:
  - the VMM3 details:
    - Definition of the overall architecture;
  - The FPD tracker and telescopes final design:
    - Pitch, capacitance and interconnections;
    - (Vacuum sealing,…)

(ALMOST) EVERY NEW IDEA IS WELCOME…

THANK YOU

CONTACTS

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