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Operation of the Full Format DSSC Pixel Readout ASIC for the European XFEL

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Content :

The DSSC (DEPFET Sensor with Signal Compression) collaboration develops a hybrid pixelated X-ray photon detector with high frame rate and immediate amplitude digitization for experiments at the European XFEL.

We present measurements with the first full format 14.9x14mm² pixel readout ASIC for the DSSC detector. The DSSC system is able to record megapixel X-ray images with a frame rate of 4.5 MHz. The readout architecture is specially adapted to the burst structure of the XFEL (bursts with 2880 pulses spaced by down to 221 ns at a rate of 10 Hz) by in-pixel digitization and digital hit data storage and data transfer during the burst gaps.

The readout ASICs (130nm IBM CMOS technology) contain 64x64 pixels of 229x204μm² size and include per pixel two low noise front-end versions for DEPFET and silicon drift detectors (SDD), a single-slope 8-bit ADC and local SRAM storage. Particular challenges are the required single photon resolution and the high dynamic range of 10⁴ photons at 1 keV, requiring a non-linear characteristic. The DEPFET sensor provides signal compression at the sensor level. For the alternative SDD sensor, signal compression is achieved in the ASIC front-end.

The building blocks of the readout electronics and experimental results of the full format ASIC characteristics will be presented. Dispersion of ASIC parameters over the full matrix will be discussed and results of coupling ASICs to detector prototypes (DEPFET and SDD) will be shown.

Summary :

The DSSC camera is designed to detect single X-ray photons ranging from 0.5 keV to 6 keV. In the final system, there will be 256 ASICs reading out 16 sensor chips – in total 1024x1024 pixels.

A nonlinear system characteristic generates a high dynamic range up to several thousand photons. Front-end versions for DEPFET sensors with internal signal

compression and for SDD sensors with compression on the chip are available. Trapezoidal shaping is used to minimize 1/f noise. Full parallel 8-9 bit digitization and storage (800 words) until readout during the ~100ms burst gap are done in each pixel.

To minimize the power request of the electronics, the power supplies for the analog circuits and the ADCs on the chip are switched off during the gaps, only leaving the digital power supply for memory and readout circuits active. During the ~1 ms burst, the ASIC requests a peak current of 2.2 A on the analog supply. Events in the in-pixel memory can be discarded and reused by sending a veto telegram to the ASIC global control block. The total amount of data transferred during the ~100 ms burst gap is 3.7 MB per ASIC. The data stream is aggregated on $\frac{1}{4}$ megapixel level and amounts to ~36 Gbit/s per quadrant.

47 control bits per pixel provide flexible operation modes. Gain and offset settings of the analog front-end and the ADC can be trimmed in a wide range for each pixel. Dead pixels can be powered off. Signal integration time of the trapezoidal filter can be fine-tuned on ASIC level.

Power is distributed on the chip on ~15 mm long vertical busses. Horizontal power busses and row-wise reference circuits following the supply voltage drop reduce the effects. Results of these optimizations will be shown.

The noise and speed performance of the ASICs have been assessed in stand-alone tests and coupled to detector prototypes. Noise values down to 20 el. for 1 MHz operation have been measured for low-gain DEPFET types. Signal compression has been demonstrated for operation with DEPFET and SDD sensors.

By the time of the conference, results of wafer-scale ASIC testing will be available as well.

Collaboration :

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