High-Speed Serial Data Transmission - 2

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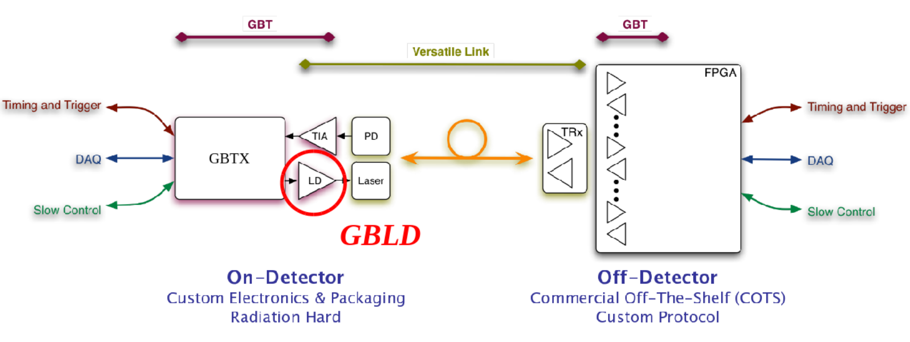
Case studies

- GBLD laser driver
- ALICE ALPIDE DTU

Case study : the GBLD laser driver



GBLD specifications

Laser diode type	EE or VCSEL	
Bit rate	5 Gb/s	
Modulation current	$2 \div 24$ mA	in 1.6 mA steps
Bias current	$2 \div 48$ mA	in 1.6 mA steps
Emphasis current	$0 \div 12$ mA	in 0.8 mA steps
Independently programmable pre/de emphasis		
Power supply	2.5 V	single supply
Random jitter	<1 ps	
Deterministic jitter	<25 ps	
Control interface	I^2C slave	
TID tolerance	>1 MGy	
SEU tolerance	TMR with self correction	
Technology	CMOS 0.13 μm	

Main issues

A laser driver circuit looks relatively simple, but...

- High driving currents and high speed are conflicting requirements:
  - High speed circuit $\longrightarrow$ small RC delays $\longrightarrow$ minimize R and/or C
  - Small resistors $\longrightarrow$ high power consumption
  - High I_{DS} current $\longrightarrow$ Large transistors $\longrightarrow$ High parasitic capacitances
  - Electromigration rules $\longrightarrow$ Large metal lines $\longrightarrow$ High parasitic capacitances
- Laser diodes voltage swing requires at least a 2.5 V supply:
  - Core transistors can sustain only up to 1.5 V
  - IO transistors are slower and less tolerant to radiation
  - Higher power consumption

GBLD flavours

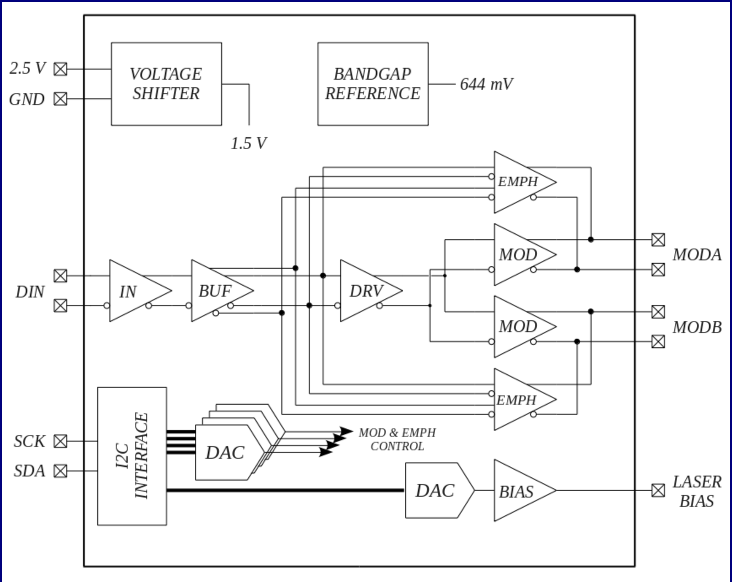
GBLD version 4

- Max modulation current : 24 mA
- Max bias current : 24 mA
- Power supply : single, 2.5 V
- Core supply current : 88.9 mA

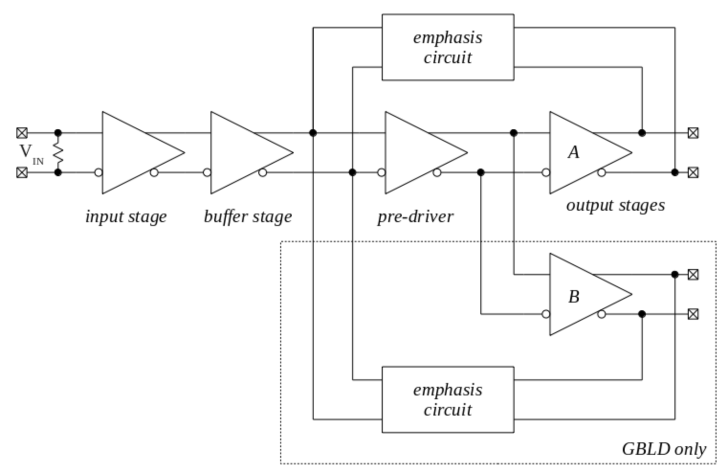
GBLD version 5

- Max modulation current : 12 mA
- Max bias current : 20 mA
- Power supply : single, 2.5 V or dual, 2.5 V and 1.5 V
- Core supply current : 55.3 mA

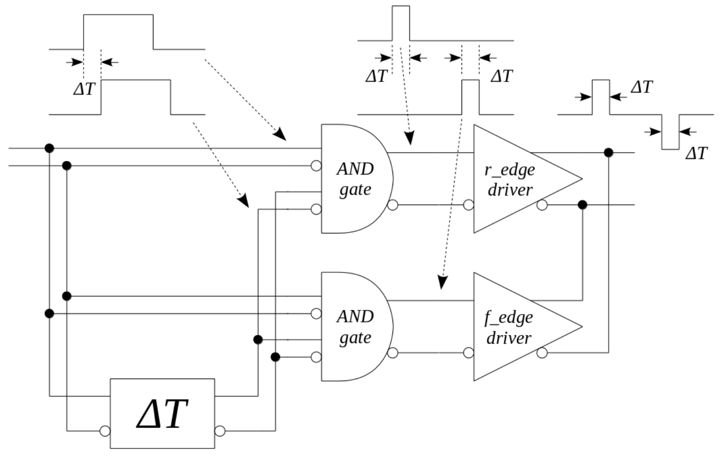
GBLD architecture



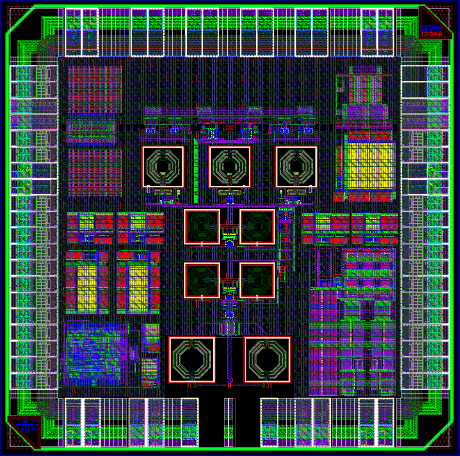
Modulator architecture

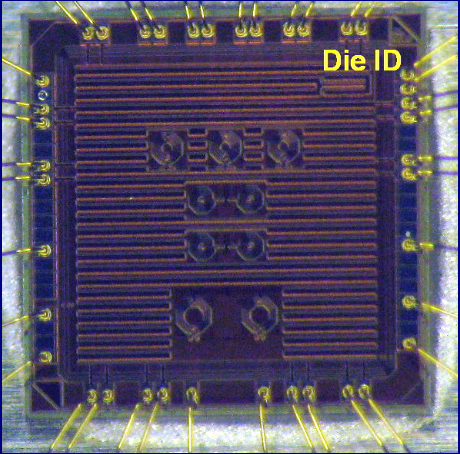


Emphasis architecture



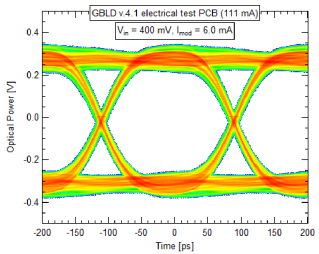
GBLD die

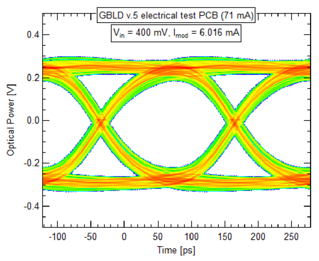


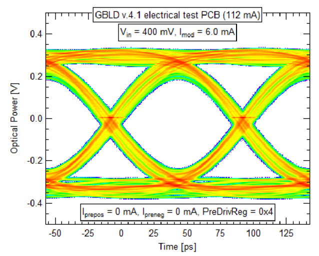


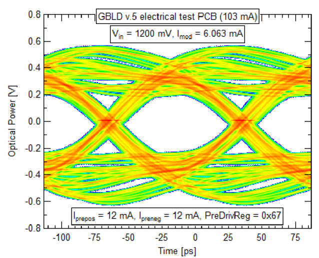
Die size 2×2 mm^2.
CMOS 0.13 μm technology.

Optical eye diagrams

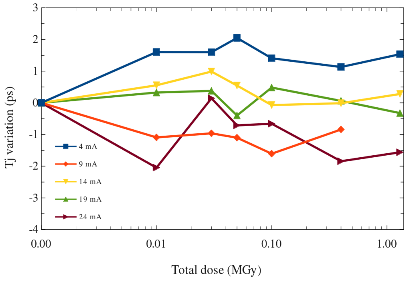


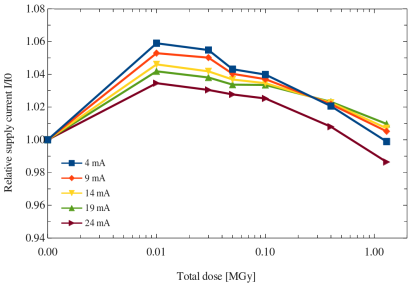


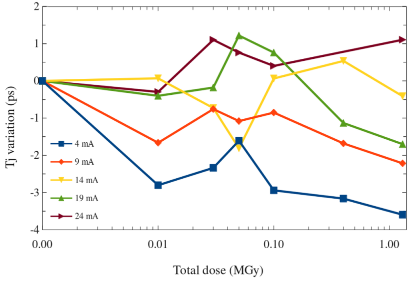


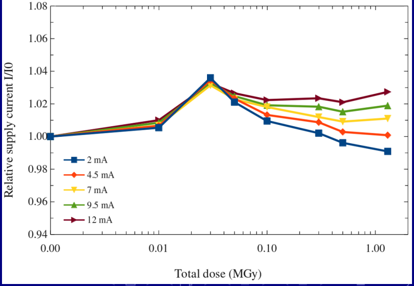


TID results

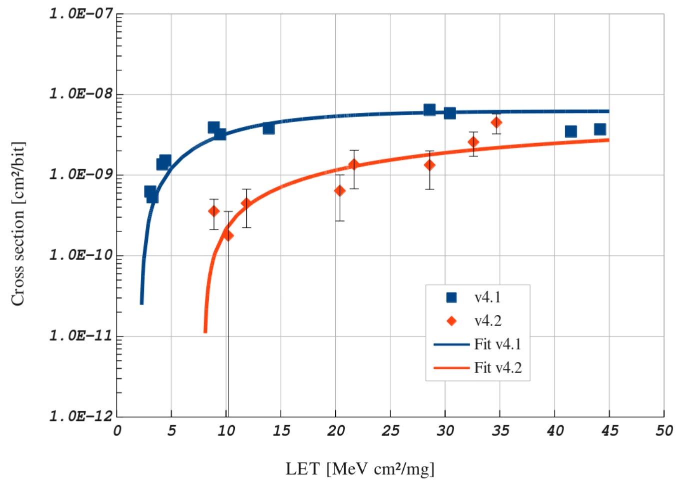

Tj variation (ps)
Total dose (MGy)
4 mA
9 mA
14 mA
19 mA
24 mA


Relative supply current I/I0
Total dose [MGy]
4 mA
9 mA
14 mA
19 mA
24 mA


Tj variation (ps)
Total dose (MGy)
4 mA
9 mA
14 mA
19 mA
24 mA


Relative supply current I/I0
Total dose (MGy)
2 mA
4.5 mA
7 mA
9.5 mA
12 mA

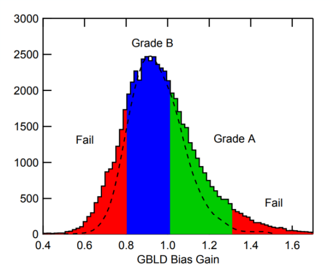
SEU test results



Difference between v4.1 and v4.2 : asynchronous reset net.

GBLD production

- 76 GBLD wafers
- 91000 GBLD dies
- Yield $> 99\%$
- ...much more than needed
- Biggest issues were contact problems

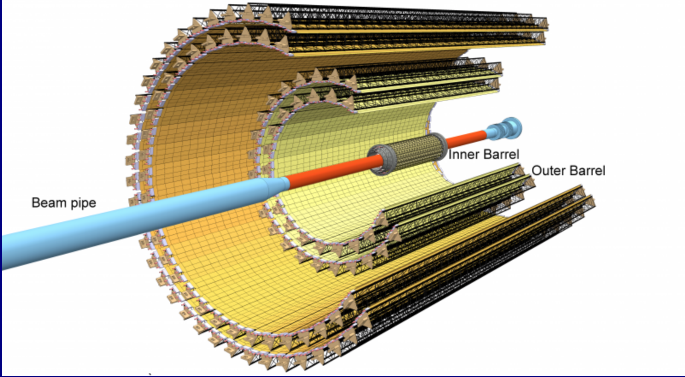


Bias Gain = real bias current / bias current setting
→ ideally always 1

- Problem : large spread in the bias currents
- Solution 1 : use the bias current control DAC
- Solution 2 : select only GBLDs within $\pm 20\%$ from nominal value.
- "Choosy" solution has been selected

Data from L. Olantera presentation at ACES 2018

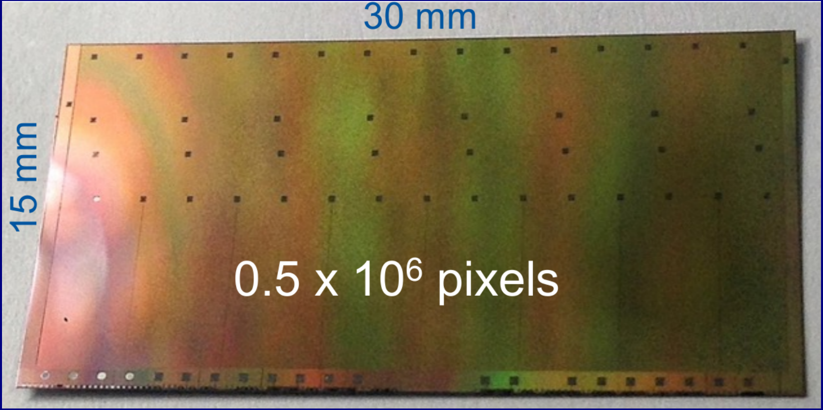
Case study : ALICE ITS upgrade



- 3 Inner Barrel layers (IB)
- 4 Outer Barrel layers (OB)

- Based on high resistivity epi layer MAPS
- Radiation levels (IB layer 0) : 270 kGy
- Radial coverage : 21-400 mm
- $\approx$10 m^2

ALPIDE ASIC

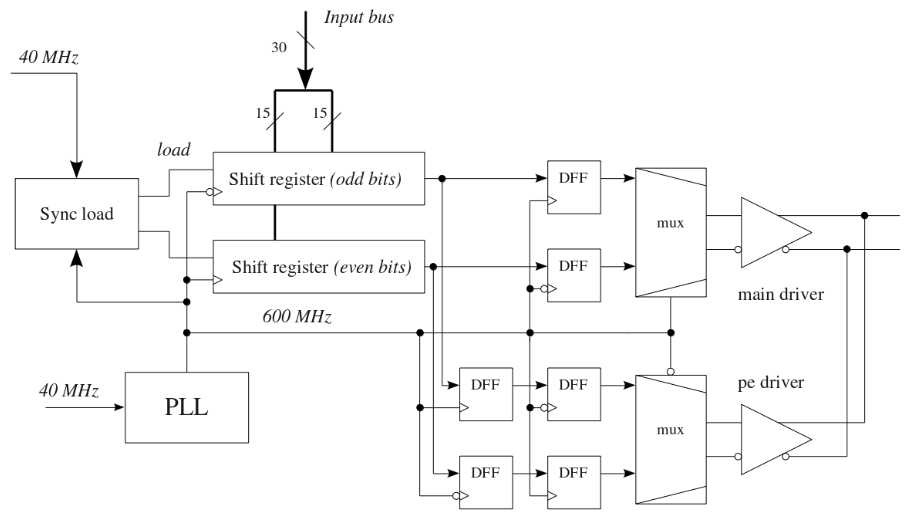


- Pixel size : $29 \times 27\ \mu\text{m}^2$ with low power FE (40 nW)
- Power density : $\approx$300 nW/pixel
- Chip area : $30 \times 15\ \text{mm}^2$
- Active area : $30 \times 13.9\ \text{mm}^2$

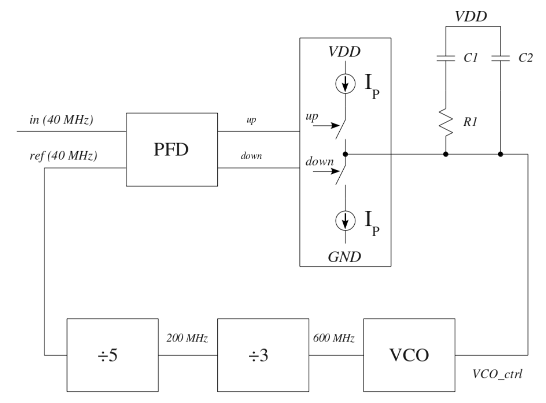
ALPIDE Data Transmission Unit (DTU) specifications

Input clock	40 MHz
Transmission clock	600 MHz
Transmission type	DDR
Data/Line rate	0.96/1.2 Gb/s (IB)
Data/Line rate	320/400 Mb/s (OB)
Data encoding	8b10b
Electrical protocol	pseudo LVDS
Technology	CIS 0.18 μm

DTU scheme


Input bus
30
40 MHz
15
15
load
Shift register (odd bits)
DFF
Sync load
mux
Shift register (even bits)
DFF
main driver
600 MHz
DFF
DFF
pe driver
40 MHz
PLL
mux
DFF
DFF

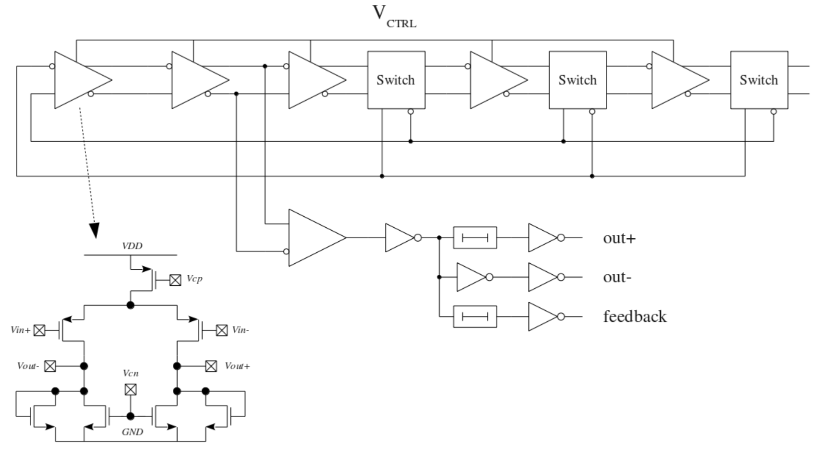
PLL scheme



- Input : 40 MHz
- Output : 600 MHz
- Lock time : $\approx$10 μs
- Power : 15.4 mW

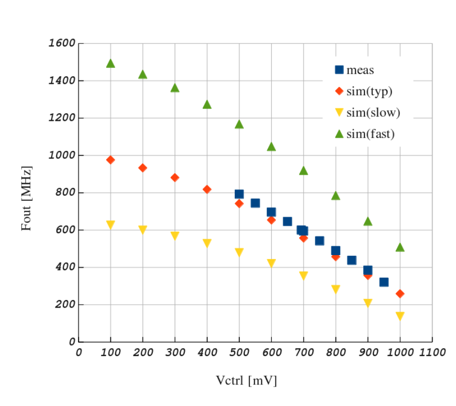
- Area : 1.059×0.12 mm^2 *(owing to floorplan requirements)*
- Differential ring oscillator VCO (range 500-700 MHz)
- SEU tolerant frequency divider

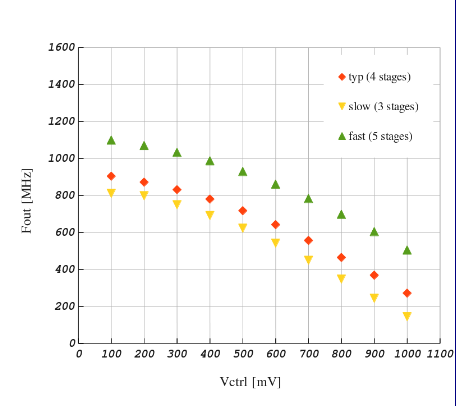
VCO scheme



Reference : J. Maneatis
Low-Jitter Process-Independent DLL and PLL Based on Self-Bias Techniques
IEEE J. Solid-State Circ., Vol. 31, No. 11, Nov 1996

VCO frequency spread

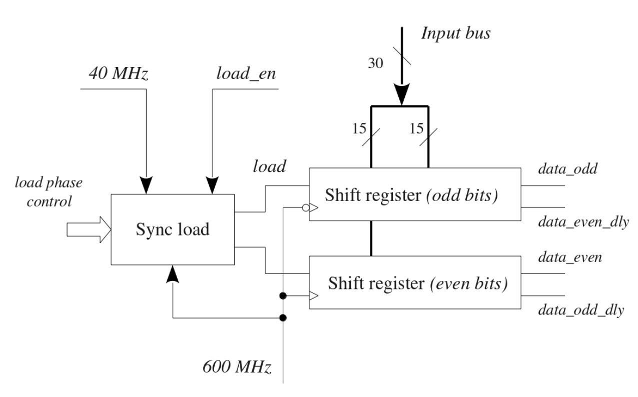




VCO with 4 stages
(sim & measurements)

VCO with 3-4-5 stages
(sim only)

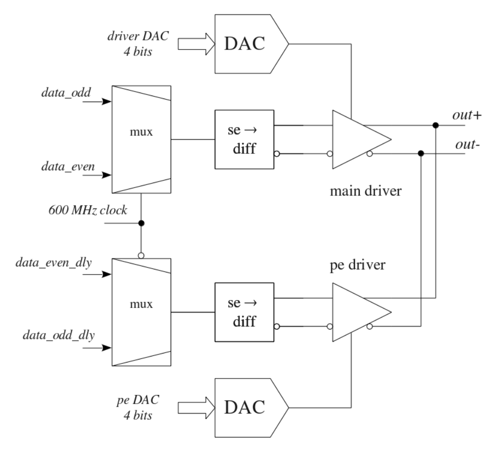
Serializer scheme



- Double Data Rate
- Pre-emphasis
- Power : 22.56 mW

- TMR-based SEU protection
- Programmable phase control synchronization

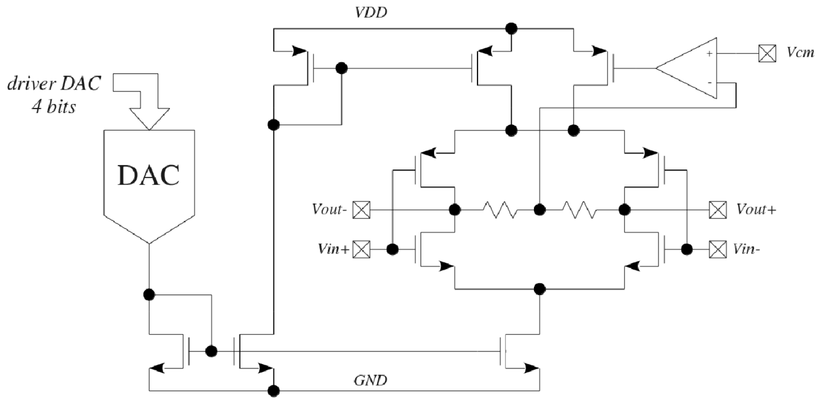
Driver scheme



- Pseudo-LVDS driver
- $V_{CM} = 900$ mV
- Power : 17.06 mW

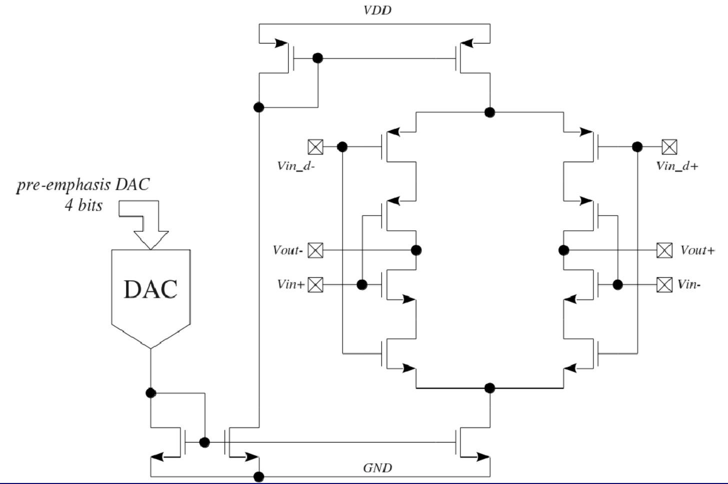
- Output current : 0÷5 mA in 312 μA steps (4 bits)
- Pre-emphasis current : 0÷2.5 mA in 156 μA steps (4 bits)
- Pre-emphasis time width : $0.5 \times T_{CK}$

Main current driver



- DAC controlled driver current
- Feedback common mode control
- pseudo-LVDS architecture (V_{CM} reduced to 900 mV).

Pre-emphasis current driver



- Control signals from the serializer

PLL test summary - 1

- Input frequency : 40 MHz
- Input frequency range : 30÷50 MHz
- Main output frequency : 600 MHz ($f_{IN} \times 15$)
- Main output frequency : 200 MHz ($f_{IN} \times 5$)

	Mean	σ
clock period	1.667 ns	6.86 ps
clock frequency	600.01 MHz	2.47 MHz
duty cycle	50.79%	0.0896%

Random jittter	4.736 ps	r.m.s.
Periodic jitter	46.342 ps	pk-pk

PLL test summary - 2

Figure: Oscilloscope waveforms

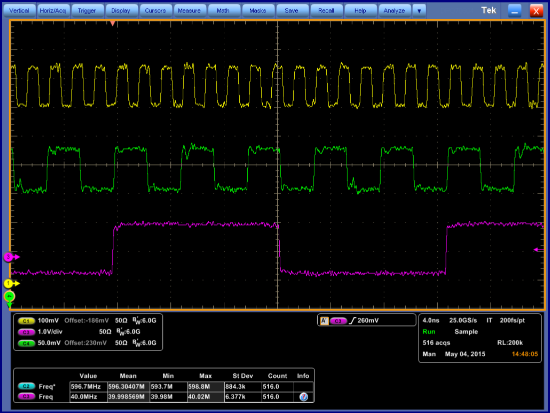
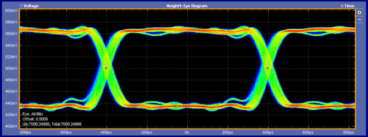


Figure: Eye diagram



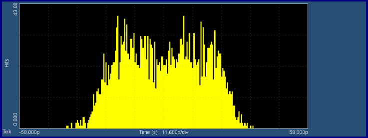


Figure: Jitter

DTU electrical tests

Figure: No pre-emphasis

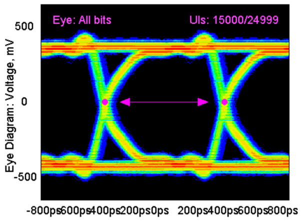


Figure: Pre-emphasis 12%

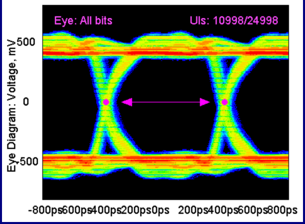
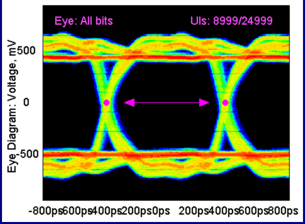


Figure: Pre-emphasis 25%



	PE 0	PE 12%	PE 25%
Eye width	0.822 UI	0.826 UI	0.835 UI
Rj	11.4 ps	10.9 ps	12.0 ps
Dj	48.8 ps	52.8 ps	57.4 ps

Test with 30 MeV protons

Figure: Flux 10^8 protons cm^{-2} s^{-1}

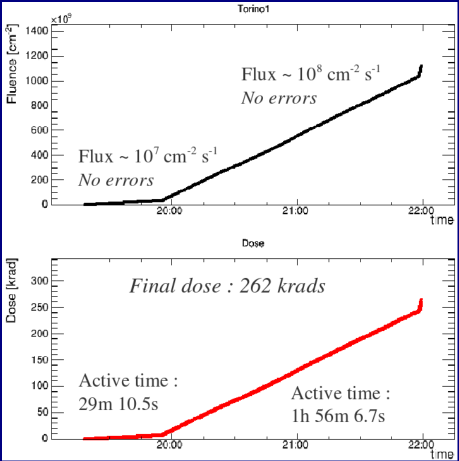
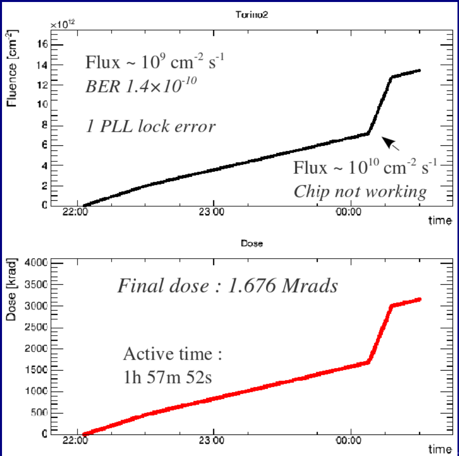
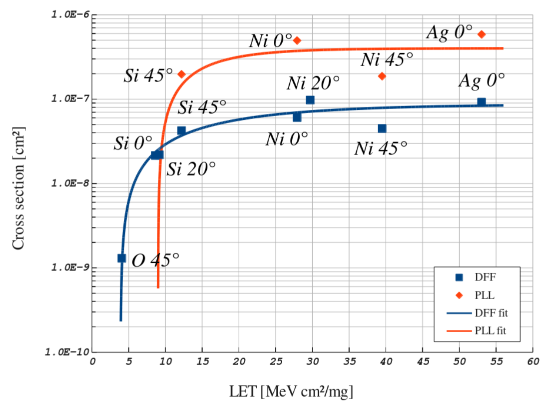


Figure: Flux 10^9 protons cm^{-2} s^{-1}



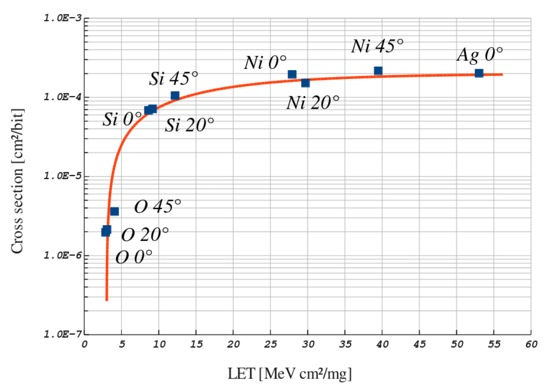
Test with ions : PLL and DFF



- $LET_{TH} = 3.9$ MeV cm^2/mg for a DFF
- *Note : cross section per bit*
- $LET_{TH} = 9$ MeV cm^2/mg for the PLL

Estimated PLL loss of lock MTBF in layer 0 (108 DTUs) : 149h 33m
Only 1 (out of 37) GTX loss of lock

Test with ions : BER cross section



- $\mathrm{LET}_{TH} = 3$ MeV $\mathrm{cm}^2/\mathrm{mg}$
- *Note : cross section per bit*

Estimated BER per link : 3.53×10^{-14}
Estimated transmission MTBF in layer 0 (108 DTUs) : 42.8 s