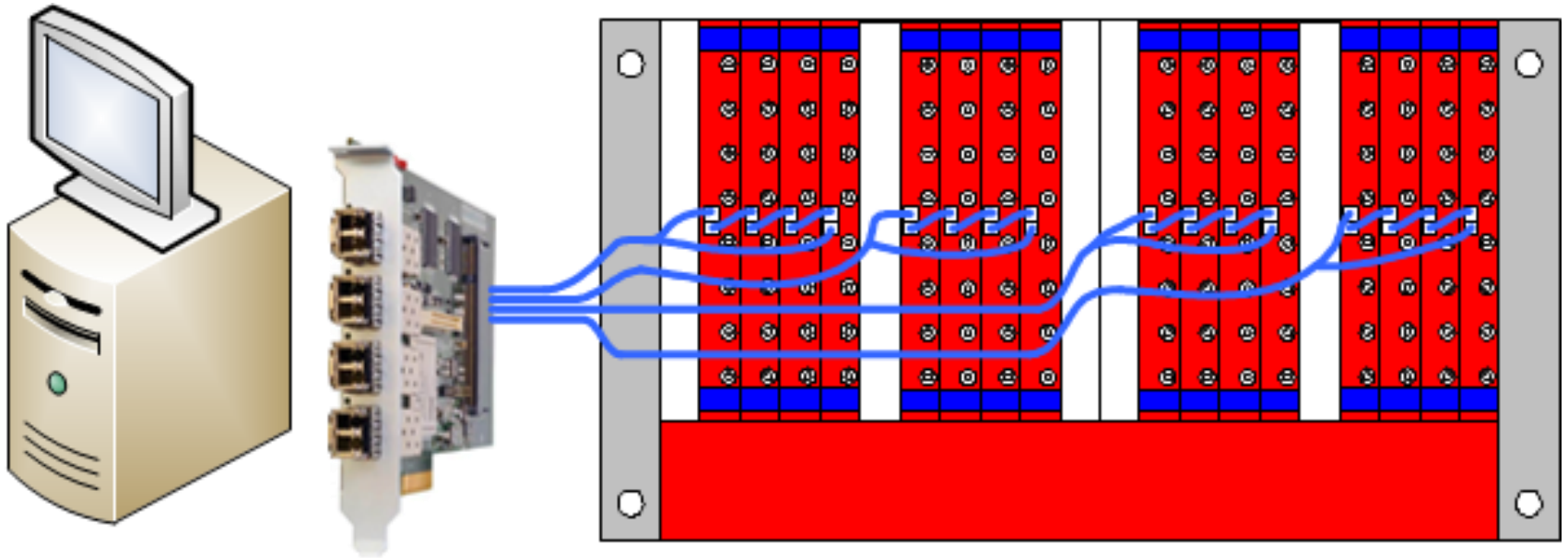
CAEN Electronic Instrumentation

Tools for Discovery

40 YEARS OF INNOVATION 1979-2019



CONET: daisy chainable Optical Network

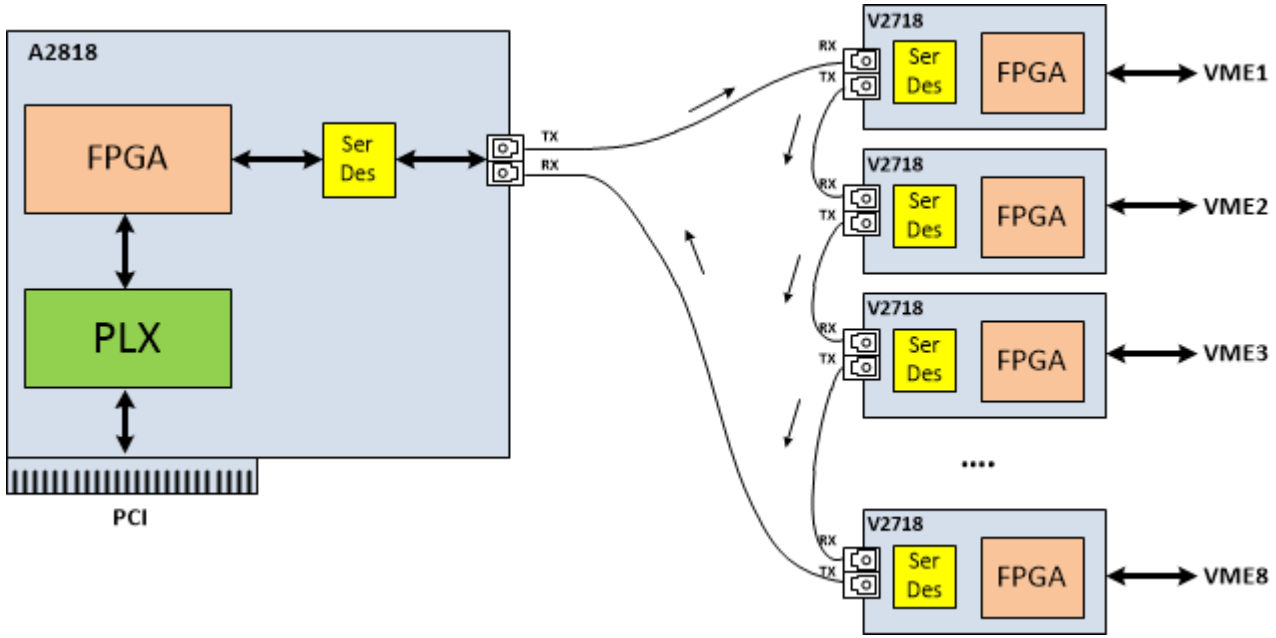
Carlo Tintori

CONET facts

- **CONET** stands for **C**hainable **O**ptical **NET**work
- PHY: 1.25 Gbit serial link over optical fiber
- Bi-directional: each node has TX and RX
- 1-Master, N-Slave Ring Architecture
- CAEN proprietary protocol
- ~90 MB/s payload bandwidth (CONET2)
- Low and predictable latency
- Optical Fiber: multimode 62.5/125μm, LC connectors
- Distance: tested up to 300m (theoretical 10 km)
- About 4000 links sold world wide (mainly for physics applications)

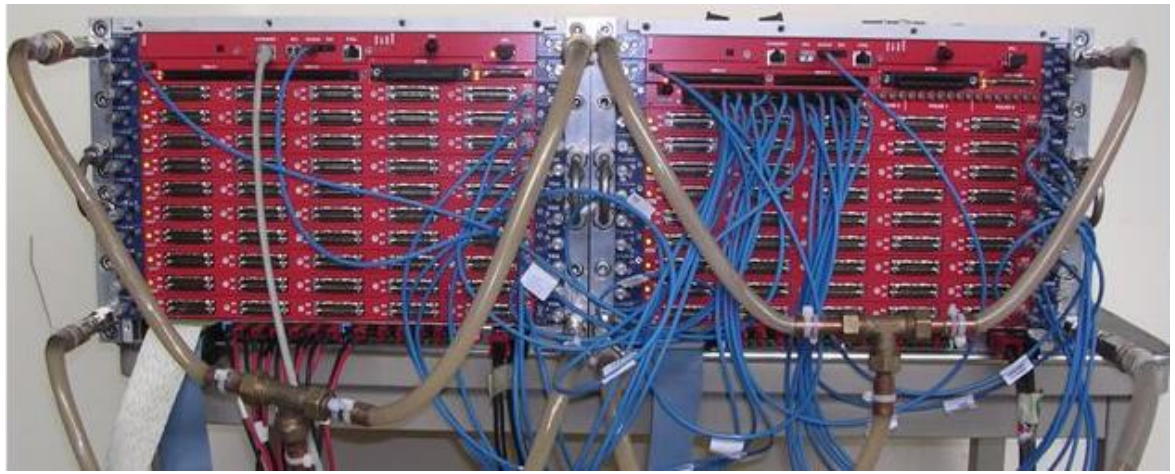
History and Motivations

- 2004
  - 1st release of CONET implemented in the VME bridge V2718 (request from CMS @ CERN)
  - Link Requirements: bandwidth > 60MB/s (quite high at that time!), low latency, easy and cheap cabling, long distance, daisy chainable
  - Implemented in FPGA **Altera Cyclone I**
  - External 1-to-10 Ser-Des (HDMP-1636A): 10 bit, 62.5 MHz, DDR link to/from FPGA
  - 3b/5b encoding (simpler than 8b/10b)
  - CONET Master implemented in **A2818** (PCI card with one single link)
  - One PC controls up to 8 VME crates!



History and Motivations

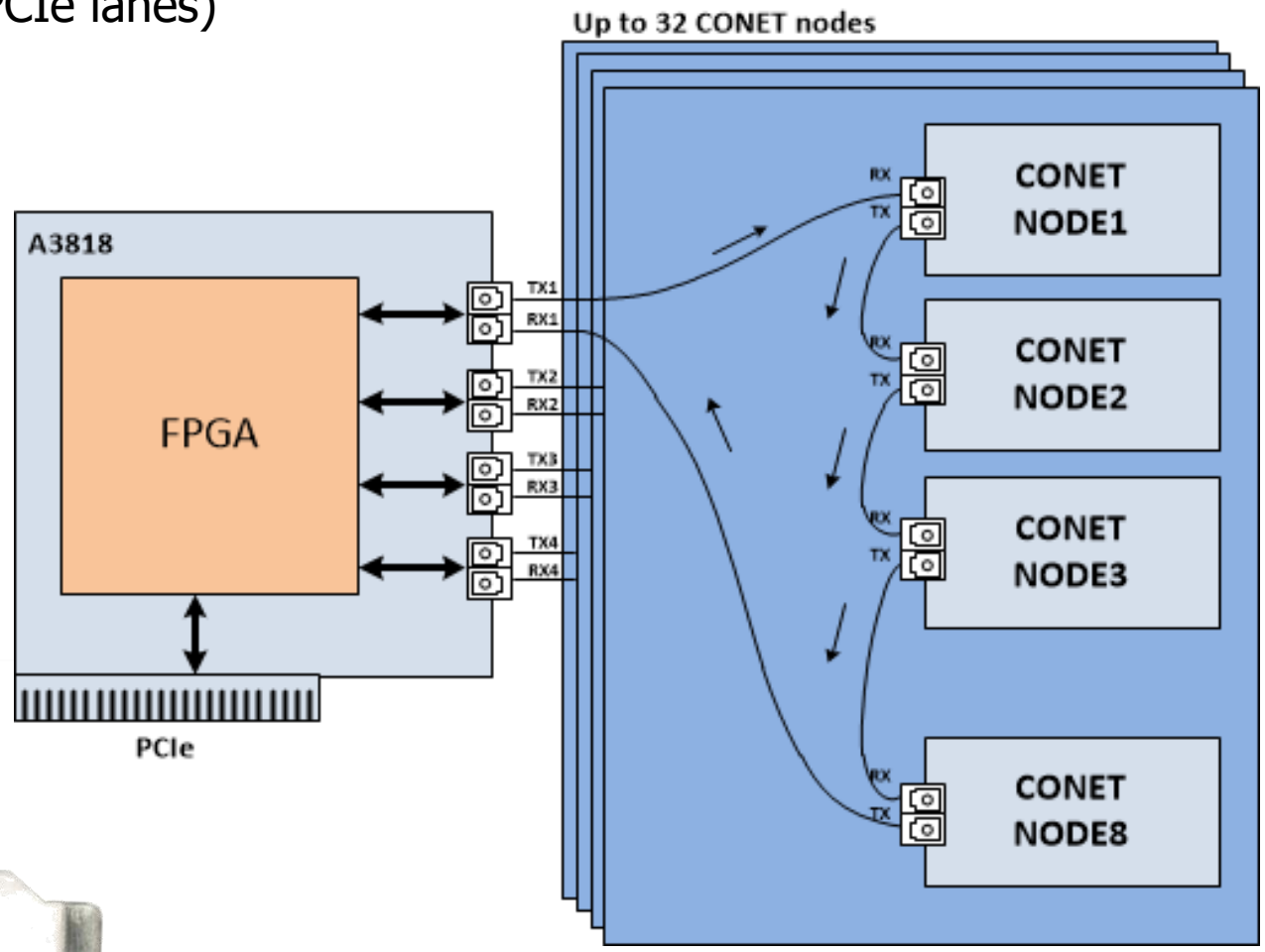
- 2005
  - CONET used in DRM (Data Readout Module) of **Alice-TOF** @ CERN
  - One A2818 with CONET implements a backup/service communication channel for the custom VME Crate (alternative to **DDL** link developed at CERN)



- 2006
  - CONET implemented in **CAEN digitizer** family (starting with V1724)
  - A new concept: **Backplane Free DAQ**!!!
  - Also for NIM and Desktop versions

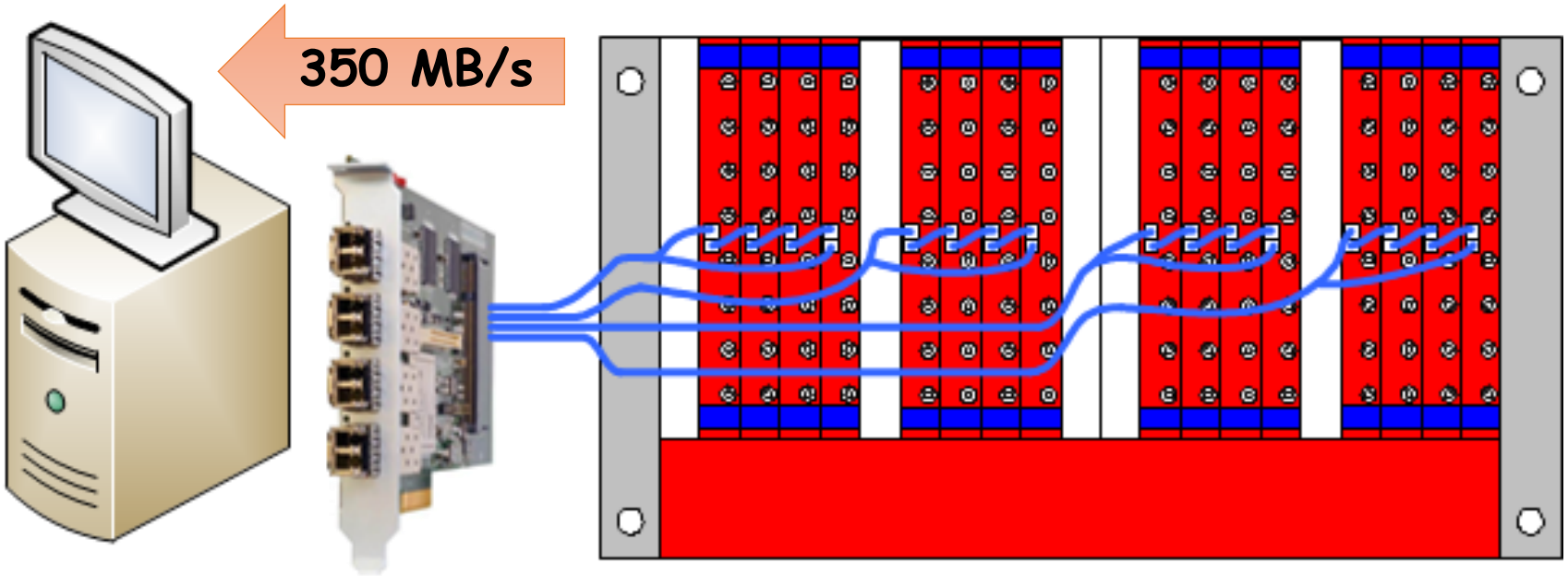
History and Motivations

- 2009
  - PCI bus becoming obsolete => A2818 cannot be used in new computers
  - A3818: PCIe card with 1, 2 or 4 CONET links (8 PCIe lanes)
  - CONET2 implemented in a **Xilinx Virtex5**
  - SerDes in FPGA (up to 3.2 GB/s)
  - SFP+ modules
  - 8b/10b decoding
  - Bandwidth increased from ~60 to ~90 MB/s
  - Up to 32 CONET nodes
  - CONET2 is not back-compatible to CONET



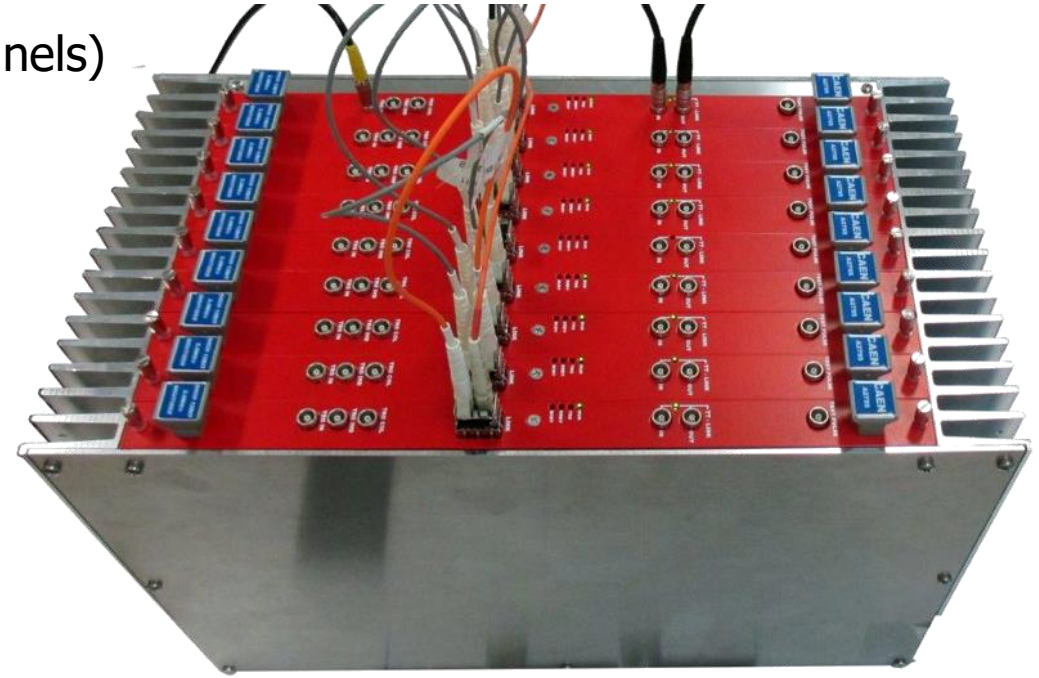
History and Motivations

- 2011
  - About 80 digitizers model V1751 (8 channels, 1 GS/s, 10 bit) installed at Kamioka for XMASS
  - Readout with A3818 (4 links)
  - Four V1751 per link => one A3818 reads a VME crate with 16 digitizers (128 channels)
  - Bandwidth Test: **350 MB/s** from one VME crate to the Host PC running Linux



History and Motivations

- 2014
  - CONET used in A2795: 64 channel TPC readout module for **ICARUS**
  - Custom crate mounted on flage with 9 boards (576 channels)
  - 54000 readout channels
  - 1 CONET link reads 8 A2795 (= 512 channels)
  - ~25 A3818s (4 links), each reading 2048 channels
  - CONET implemented in **Altera Cyclone V**
  - SerDes in FPGA



- 2015
  - CONET used in DRM2: new Data Readout Module for **Alice-TOF**
  - Implemented in **MicroSemi IGLOO2** FPGA with SerDes
  - Rad-tolerant

History and Motivations

- Today - Tomorrow
  - CAEN is developing a **new family of Waveform Digitizers**
  - CONET will be supported, together with standard protocols such as Ethernet 1/10 Gb and USB 3.0
  - Being implemented in **Xilinx ZYNC UltraScale+**
  - Possibility to increase the bandwidth (CONET10, up to 10 GB/s)

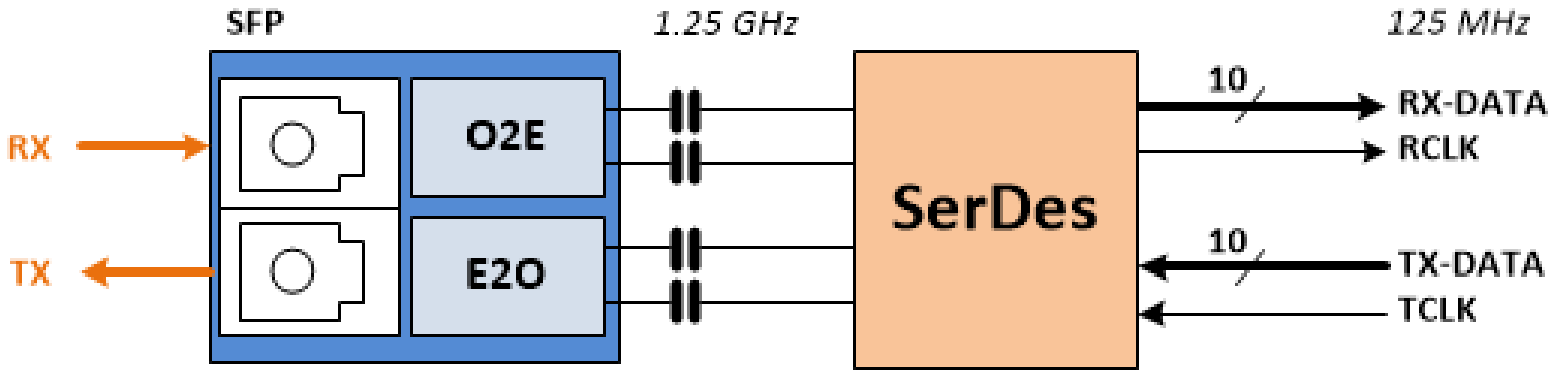
  - The VME bridge V2718 (the board that used CONET for the 1st time) is obsolete (FPGA too old)
  - CAEN is redesigning a **new V2718**, still supporting CONET
  - Being implemented in **Xilinx Artix**

  - Some compatibility issues of A3818 and PCIe with new computers
  - Plans for a stand-alone **bridge between CONET and USB 3.0 and/or Ethernet**

  - Backward compatibility and long term support are important values for CAEN!

Physical layer

- **PHY**: 1.25 Gbit/s Serial Link. Clock and Data transmitted on the same wire
- Optical Transceivers in SFP form factor: TX + RX
- The **SerDes** circuit (either external chip or internal to the FPGA) performs the clock recovery and transforms the serial data into 10 bit words
- A special symbol called "comma" is used to synchronize the data frames (1st bit of the word)

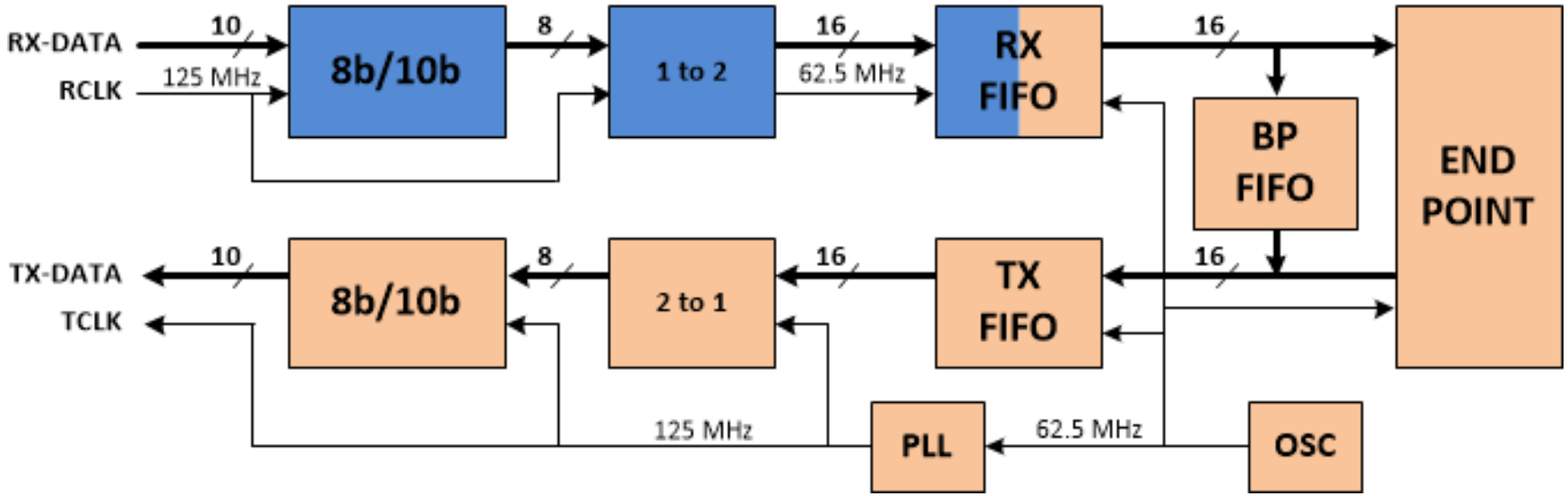


8b/10b encoding

- **DC balancing**: same number of 0s and 1s for a given length of data stream
- Required to pass the AC coupling (DC doesn't pass through) and to ensure enough state changes for the clock recovery
- The total number of 10 bit combinations with parity of 0s and 1s are not enough to encode all possible 256 characters of one byte
- Accept few symbols with +/-1 disparity
- +1 disparity is then compensated by a -1 disparity
- 8b/10b encodes the **256 Characters** of 1 byte and 12 **Control Symbols**
- The Control Symbols are used to reset the link, to send the "comma" (synchronization) and for other functions defined by the specific protocol

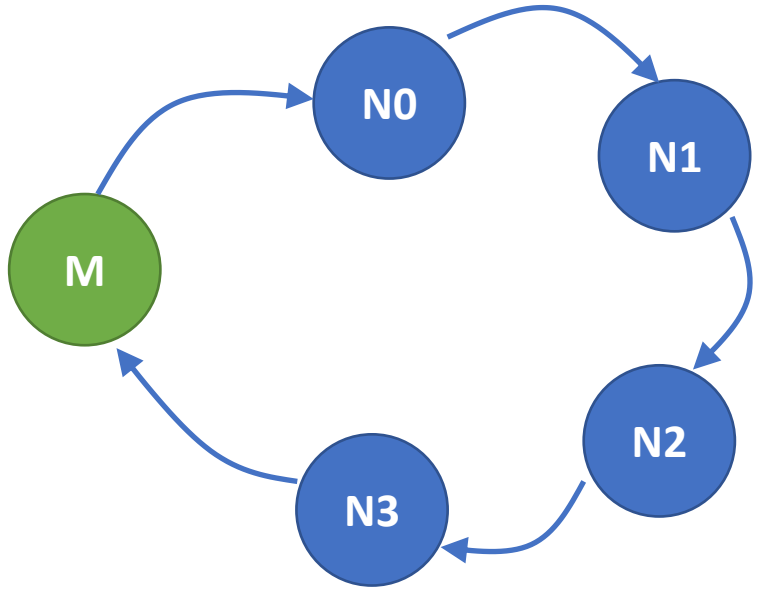
Low level CONET protocol

- Data transfer over CONET is organized in 16 bit data packets
- Incoming packets are written into the RX FIFO (16 bit @ 62.5 MHz) in the RCLK domain
- RX FIFO implements the clock domain crossing (from recovered RCLK to local TCLK)
- After the address decoding, the incoming data packets can be sent to the end point or re-injected to the CONET link passing through the BP FIFO (ByPass)
- Packets produced locally by the CONET node can be sent through the TX FIFO when the BP FIFO is empty



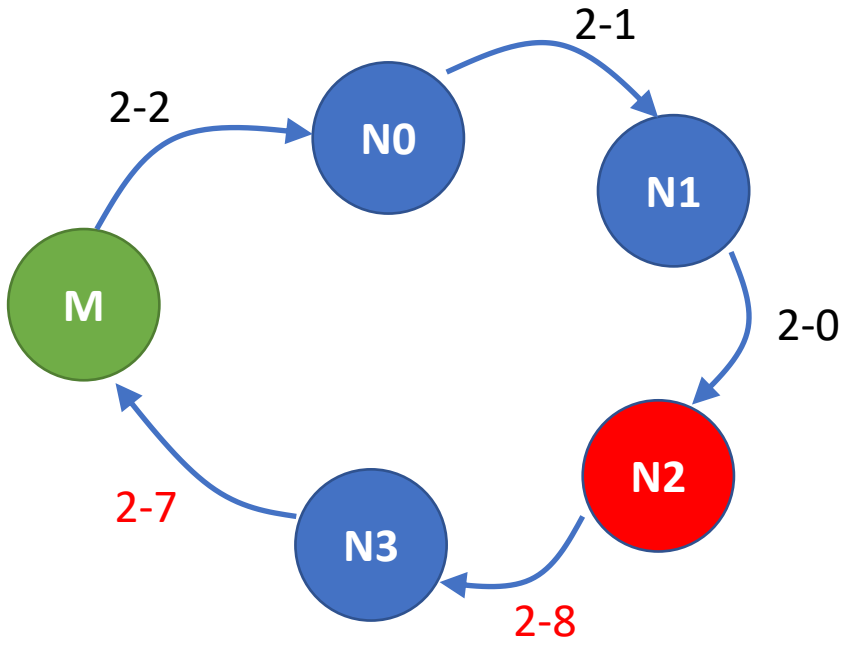
Packets circulation

- The CONET network is made of one Master and N Slaves (up to 8), connected in a ring
- When IDLE, the Master circulates a TOKEN between the nodes
- The Master initiates a transaction by removing the TOKEN and sending a "request packet" to a specific node
- The addressed node reads the "request packet" and prepares a "response packet"; in the meanwhile, it re-injects a TOKEN to let other transactions to take place
- When the "response packet" is ready, the addressed node takes the 1st TOKEN and transmits its data packet with a tag that indicates the node number
- The master receives the "response packet" and injects a new TOKEN
- A node must propagate a data packet if it not addressed
- The master never propagates a data packet



Node addressing

- The node address is given by the position (1st slave in the ring is at address 0)
- The master sends a data packet with 2 equal indexes (e.g. 2 - 2)
- Each node checks the right index: if zero, then it is the addressed node and the left index gives the position (used for the response packet). If greater than zero, the node decreases the right index and propagates.
- The response packet contain the node index on the left and the maximum node number (8) on the right, so that the packet passes through the following slaves up to the master that reads it.
- Example: Master sends **2-2**; N0 propagates **2-1**; N1 propagates **2-0**; N2 finds right index=0, reads the data packet and memorizes the left index = 2. When ready, N2 sends the response packet with **2-8**.



Packet format

- The “request packet” generated by the master can contain the following information:
  - Node Address (destination)
  - Opcode that defines the type of operation
  - Local Address (e.g. VME Address or Internal Register Address)
  - Some Parameters (e.g. Data Width, AM for the VME bus…)
  - Number of beats (for block transfers)
  - Array of data to write (only for Write Accesses)
- The “response packet” generated by a slave can contain the following information:
  - Node Index
  - Array of data read from the local node (only for Read Accesses)
  - Status Word (success, fail, etc…)
- The maximum size of a packet is 258 bytes (header+256 bytes payload). Larger block transfer must be split into a series of consecutive packets of 258 bytes.
- The size of the response packet is not known a priori. The CONET protocol provides a mechanism to close a transaction prematurely (end markers)

Allowed transactions

- **Single Write/Read** to/from the device (e.g. single read cycle on the VME bus or Read a register of the digitizer)
- **Multi-Write/Read** to/from the device: packing of N read/write accesses in a single request packet and response packet (optimizes the bandwidth)
- CONET internal register Read/Write (**service access**, no VME/digitizer involved)
- **Block Read** (e.g. BLT/MBLT Read from the VME bus or get a block of data from the memory of the digitizer)
- **Block Write** (e.g. BLT/MBLT Write to the VME bus; not used in digitizers)
- **IACK cycle** (interrupt acknowledge on the VME bus)
- **Interrupt Request**: this is the only case where a CONET slave is allowed to send a packet without any request from the master. The IRQ packet contains the status of the IRQ lines (e.g. IRQ[7:1] on the VME or Data Ready from the digitizer memory). When the Master receives the IRQ status, it generate an interrupt on the PCI/PCIe bus of the PC

Ongoing and future developments

- Implementation of CONET2 in the new digitizer line
- Development of CONET10 (10 Gbit/s => higher bandwidth)
- CONET to USB 3.0 or Ethernet bridge (Stand Alone module)
- Keep backward compatibility with old installations (e.g. new VME bridges)
- A new version of CONET might be developed to implement a readout link for a new line of Front End modules. Besides the data readout, this link should be able to propagate the clock (synchronization of several nodes) and send signals such as global trigger, acquisition start/stop, time stamp reset, etc…

Thank You!