CGEM-IT ELECTRONICS

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LNF-INFN

CGEM-IT SPATIAL RESOLUTION GOAL ≃ 100 μm

BINARY READOUT

- Single bit info per strip
- Resolution ~ pitch/√12
- Strip pitch to match σ_S requirement: 300 μm (~ 25000 chs)
- Sensitive to S/N ratio (single threshold)

ANALOG READOUT

- Charge centroid measurement
- Less sensitive to S/N ratio (threshold can be set both on single strip and, on total collected charge)
- Requirement on strip pitch can be relaxed: 650 μm (~ 10000 chs)
- On-detector readout electronics requires a digitization sections
  - At the moment there is only the APV25 hybrid available for analog readout of micro-pattern detector, but the buffer size do not match the experiment latency → A new ASIC must be developed

FRONT-END NUMBERS

GOALS

- Spatial resolution: ~ 100 μm
- Time resolution ~ 5 ns
- Dead time: < 1 μs (shaping time + analog-to-digital conversion to limit pile-up probability to a few %)

CHANNELS

- ~ 10 000 channels → ~ 160 ASICs → ~ 80 boards (two 64 chs ASICs/board)

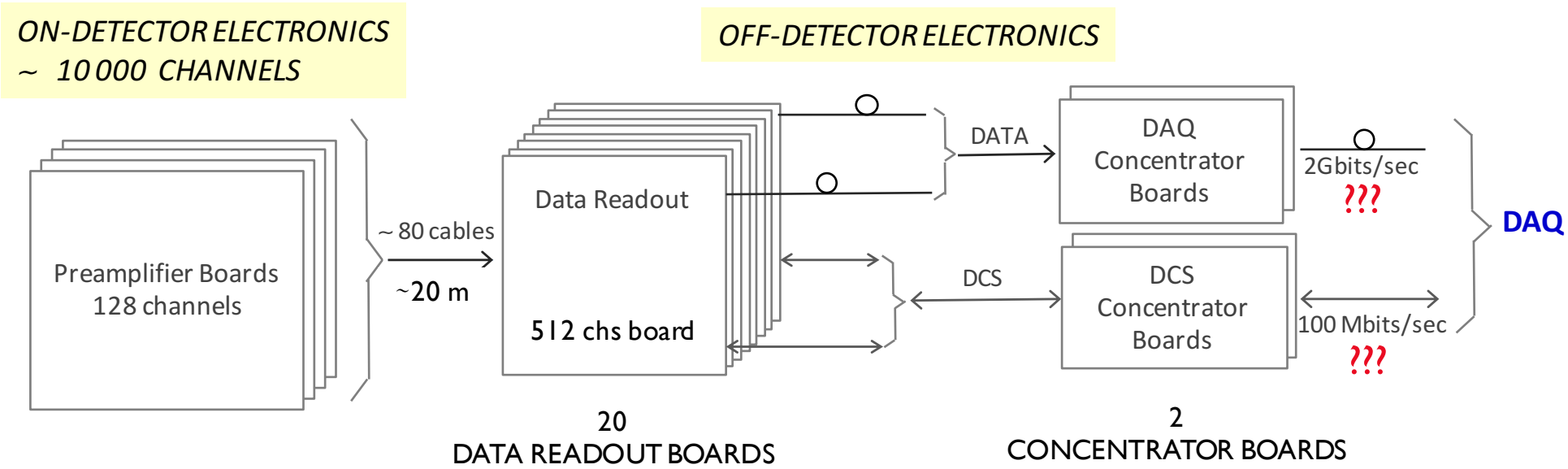
ASIC REQUIREMENTS

- Input charge range: 1– 60 fC
- Input capacitance: 100 – 150 pF
- Rate per channel (4 safety factor included): 60 kHz
- Peaking time: 5/100 ns

TRIGGER LATENCY

- Trigger latency: 6.4 μs (nominal)

FEE ARCHITECTURE



ON-DETECTOR ELECTRONICS

- Preamplifier boards located on the detector to preserve S/N ratio

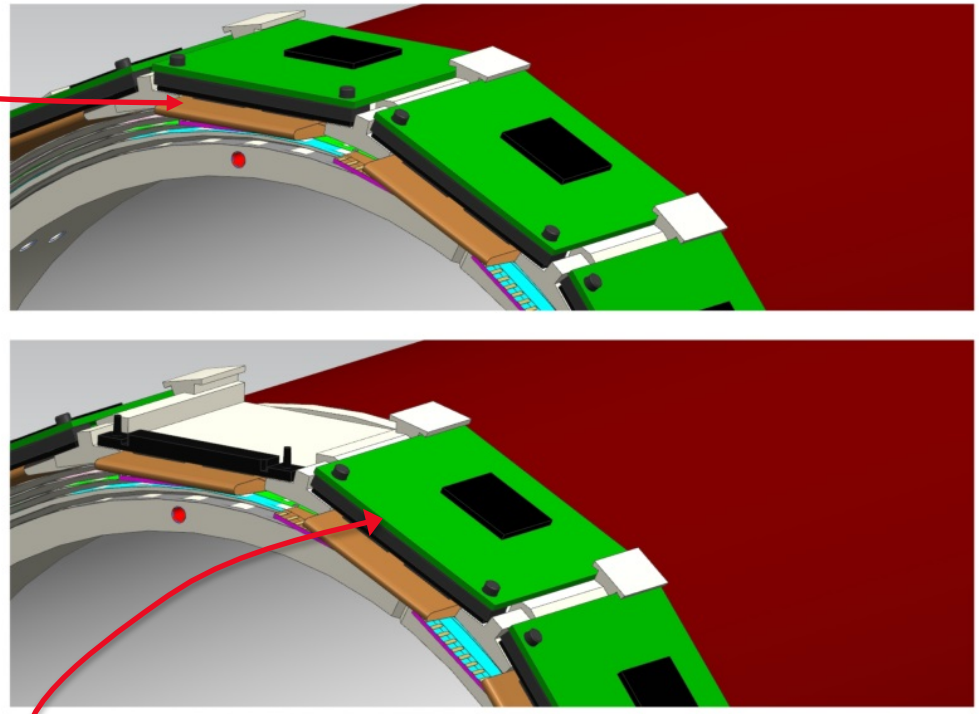
OFF-DETECTOR ELECTRONICS

- Readout Boards and Concentrator Board on the experiment platforms (~20 m cables)

PREAMPLIFIER-TANSITION BOARDS

TRANSITION BOARDS:

- Provide interconnections to the anode strips and anode GND
- Provide support and anchoring for preamplifier board
- Hosts asic input protection network



PREAMPLIFIER BOARDS:

- host two 64 chs asic and input/output connectors

ASIC DEVELOPMENT

New ASIC under development at INFN-Torino in collaboration with IHEP, wich provides two PhD Students (2x3 years, C.Leng and J.Chai) and one Expert (2 years, H.S.Li) for ASIC design and tests, with two technical advisors (A. Rivetti and M. Rolo)

The ASIC design started from two designs:

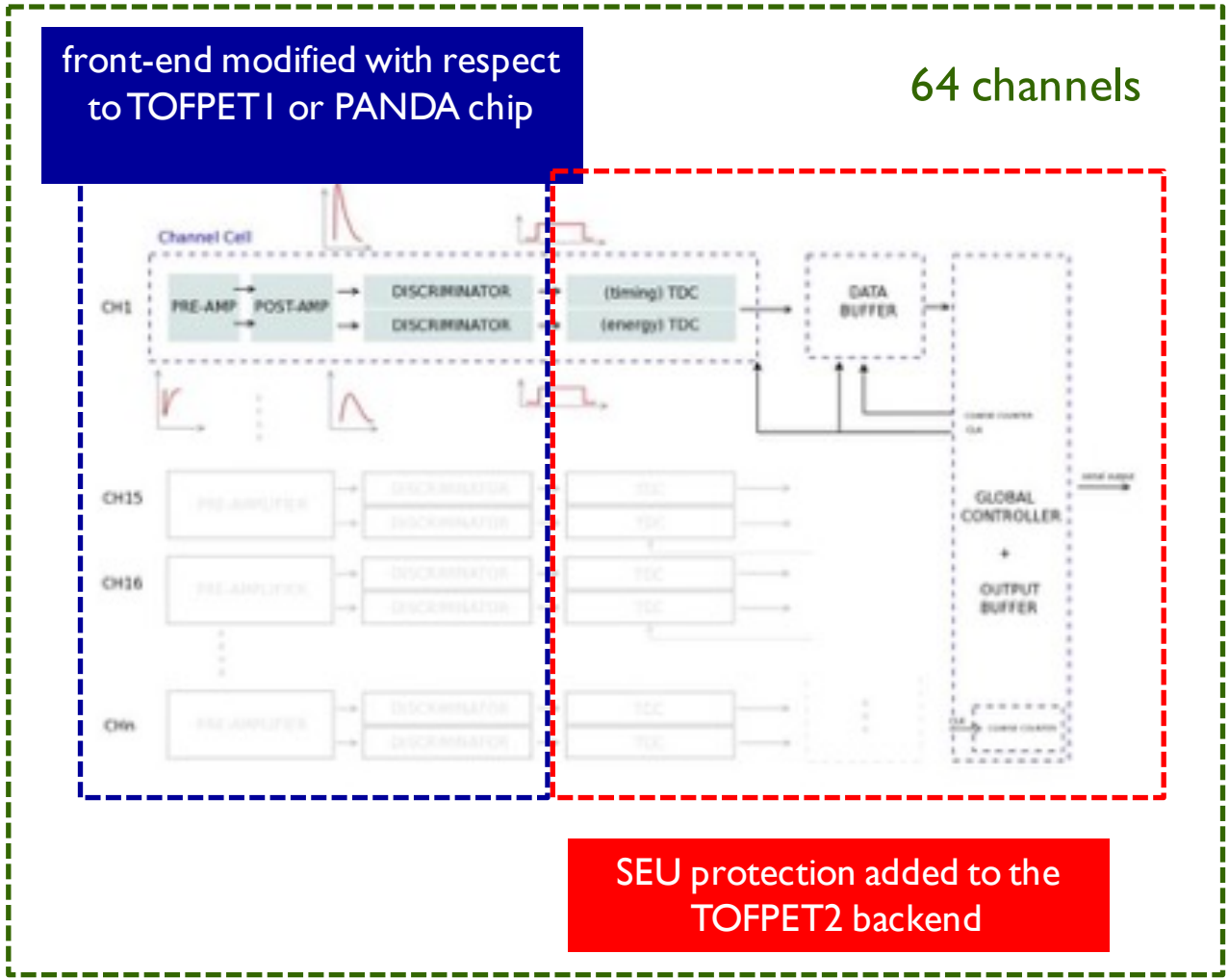
- TOFPET-1:
  - Used for medical applications
  - IBM 130nm technology
  - Preamplifier match SiPM signals (> 100 fC)
  - No SEU protection
- PASTA:
  - Developed for PANDA experiment
  - UMC 110nm technology (exportable in China, limited power consumption, reduced cost wrt IBM, to be tested for Radiation Tolerance)
  - Preamplifier match SiPM Si microstrip signals (some fC)
  - SEU protection

Both ASICs:

- Time and charge measurements by means of two independent TDCs
- Time over Threshold (ToT) for charge measurement

Now TOFPET2 BackEnd (for PET application) will be used instead of TOFPET1/PASTA

BES ASIC



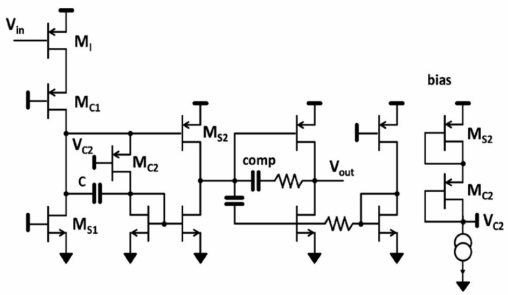
- UMC 110nm technology Preamplifier match
- ADC charge measurement
- SEU implementation

ASIC STATUS

DESIGNERS:
H.S. Li, C.Y. Leng, J.Y. Chai (IHEP)

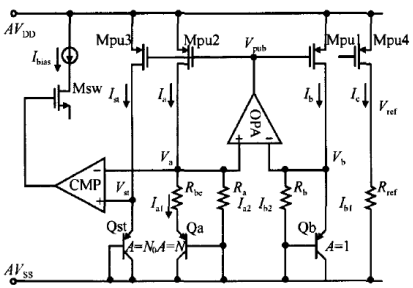
TECHNICAL ADVISOR:
A. Rivetti, M. Rolo (INFN)

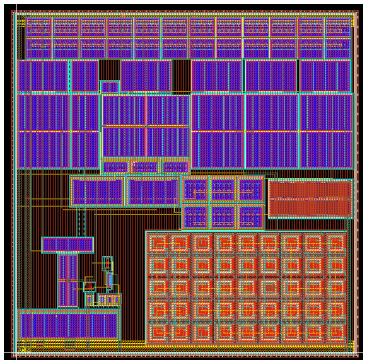
PREAMPLIFIER



UNDER STUDY

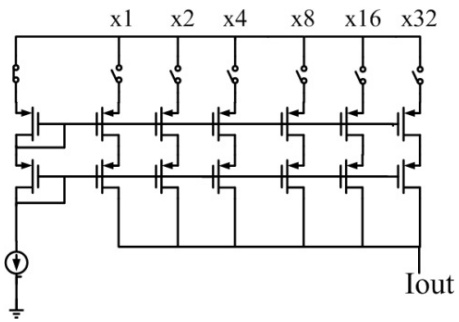
BANDGAP

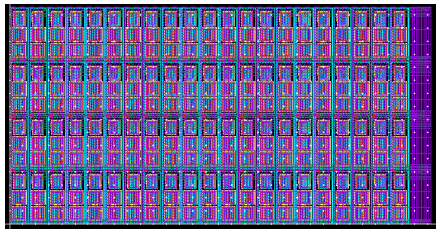




COMPLETED

6BITS DAC
for BIAS and thres. Voltage

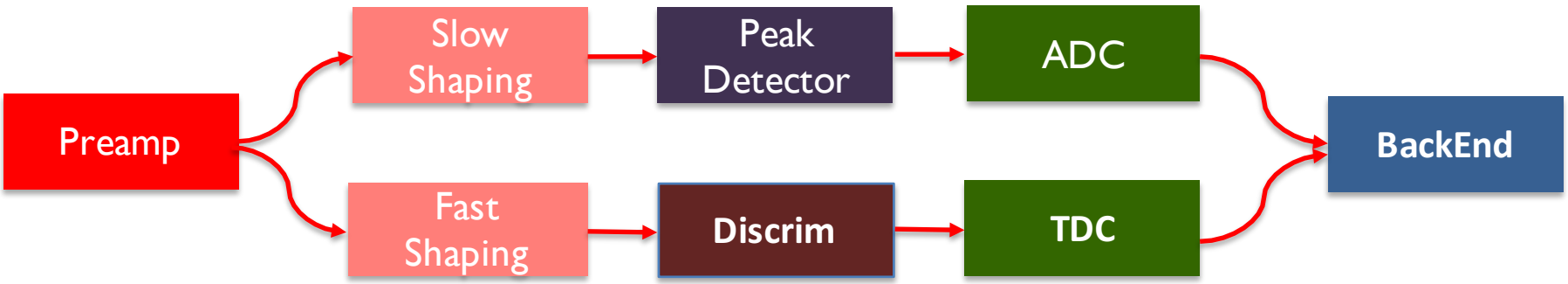




COMPLETED

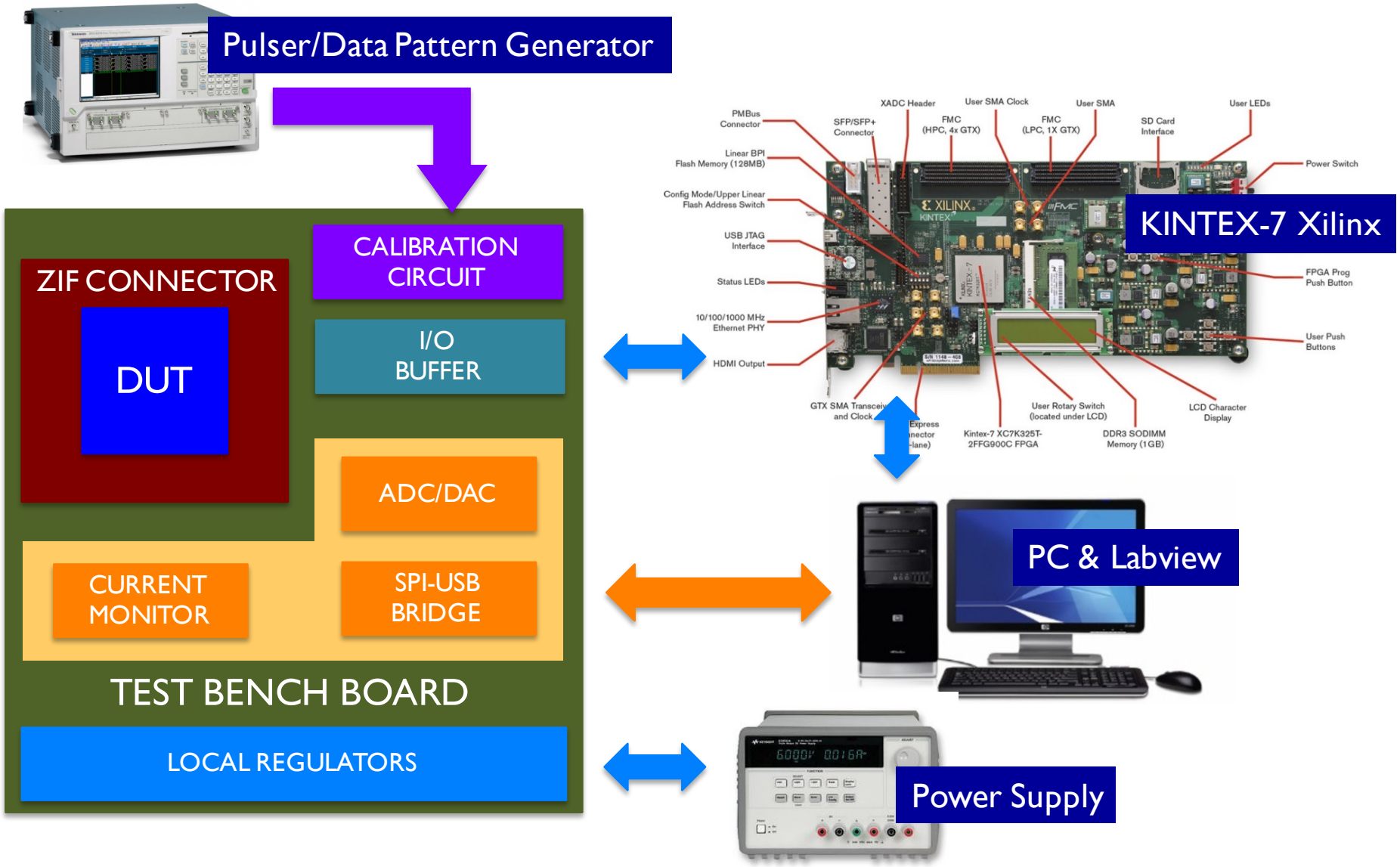
ASIC FAST-SLOW CHAIN

DUAL PATH CHAIN



- Slow channel peaking time: 100ns
- Fast channel peaking time: 5 ns

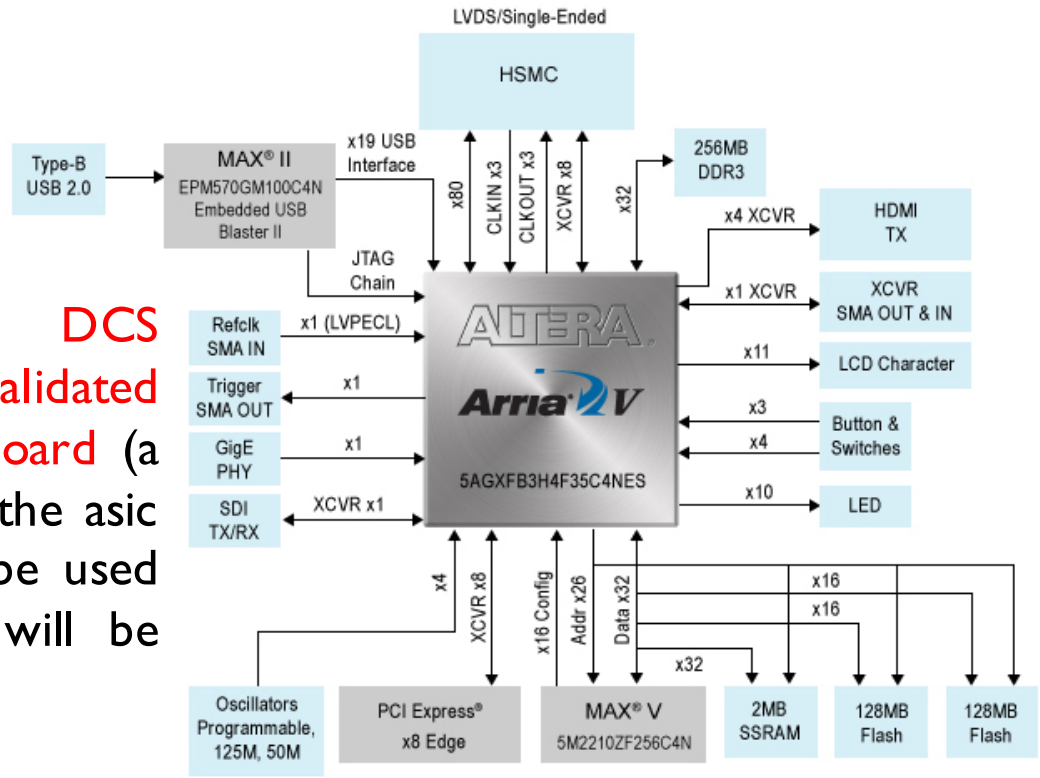
ASIC TEST BENCH



READOUT BOARDS DEVELOPMENT (I)

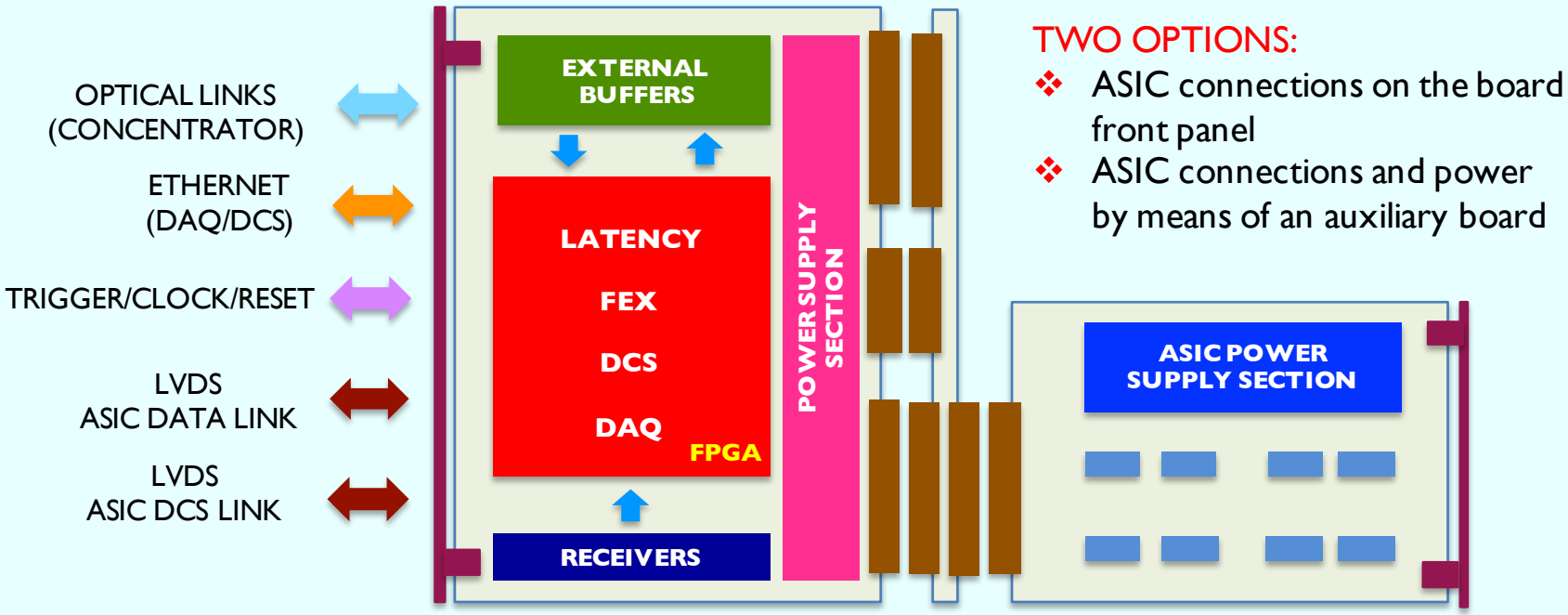
Readout Boards are used to download ASIC data, set ASIC working conditions, manage experiment signals (clock, reset, trigger) and send data to Concentrator or to DAQ via the Ethernet port.

ASIC readout protocol and DCS sensing/setting will be developed and validated by means of an ALTERA evaluation board (a board running VHDL code simulating the asic back-end and DCS I/O interface will be used as long as the first asic prototype will be available)



READOUT BOARDS DEVELOPMENT (II)

- As soon as the designers will verify that the FPGA resources match the project requirements (with some contingency for future upgrades) the board schematics will be defined and sent to the company for board layout.
- After board layout check three PCB will be produced and assembled
- A full chain test will be carried out using one of the Readout Board/ASIC prototypes by means of a dedicated test bench and/or real detector signals (planar or cylindrical GEM)



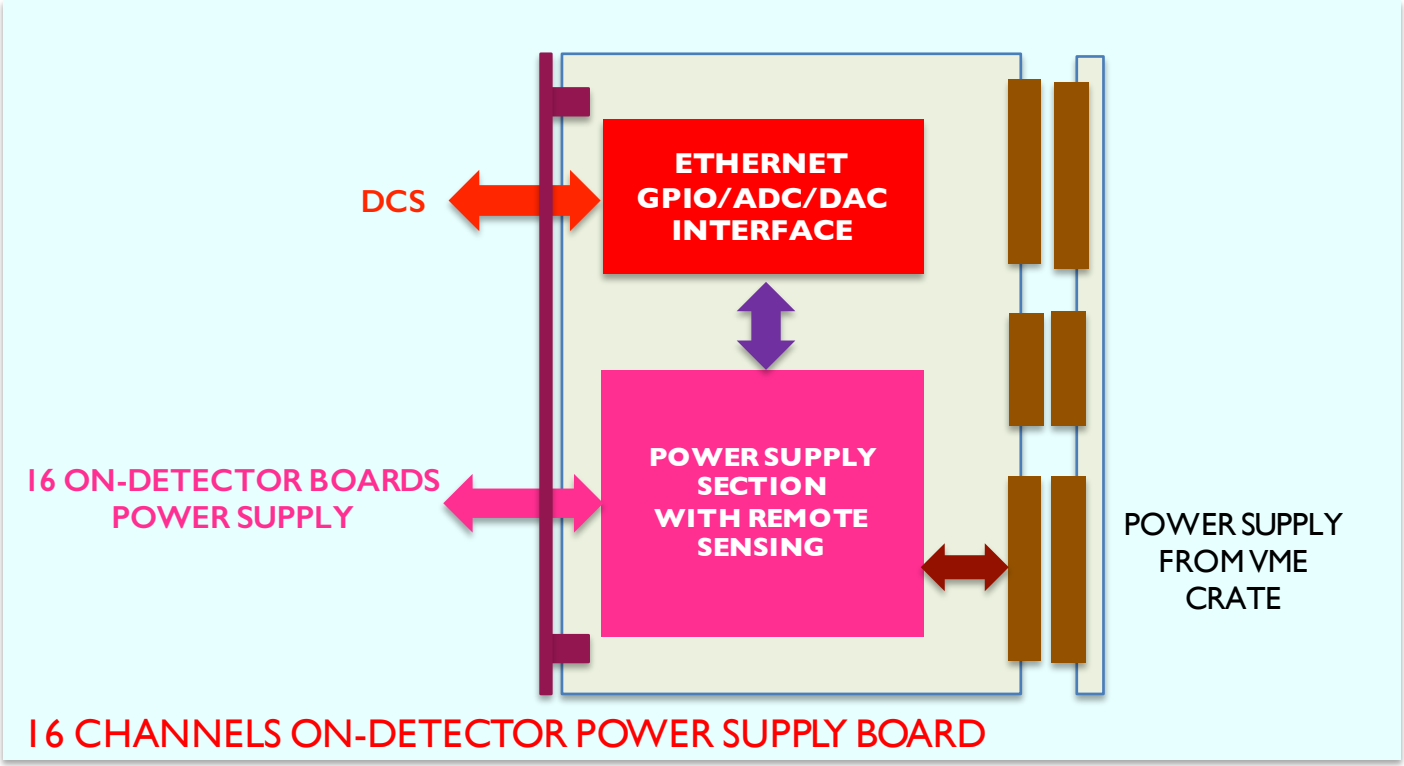
TWO OPTIONS:

- ASIC connections on the board front panel
- ASIC connections and power by means of an auxiliary board

FOUR OR EIGHT INPUTS READOUT BOARD

LOW VOLTAGE POWER SUPPLY (LVPS)

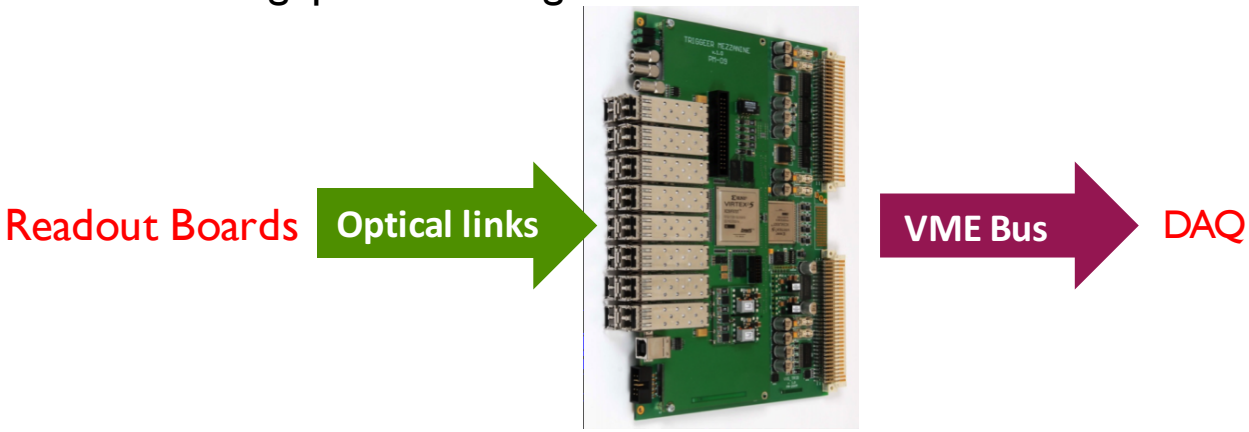
- LVPS system foresees few (main) power supplies, a fuse/protection circuit, a current monitor and on/off circuit for each On-Detector board.
- Circuits could be assembled in an auxiliary board or in an independent board hosted in the VME crate (the main power supply could be the VME power supply itself)
- Channel monitor e/o single On-Detector on/off board circuits could be managed through Ethernet links.



CONCENTRATOR

ATLB VM64x Readout Module based on Xilinx Vitex-5 FPGA (65 nm technology) UPPSALA

- Evaluate trigger decision
- Event formatting
- Data stored in 16 FIFO (32 kB capacity)
- VME data readout
- 1.3 Gb/s data throughput assuming 4 kHz L1 rate

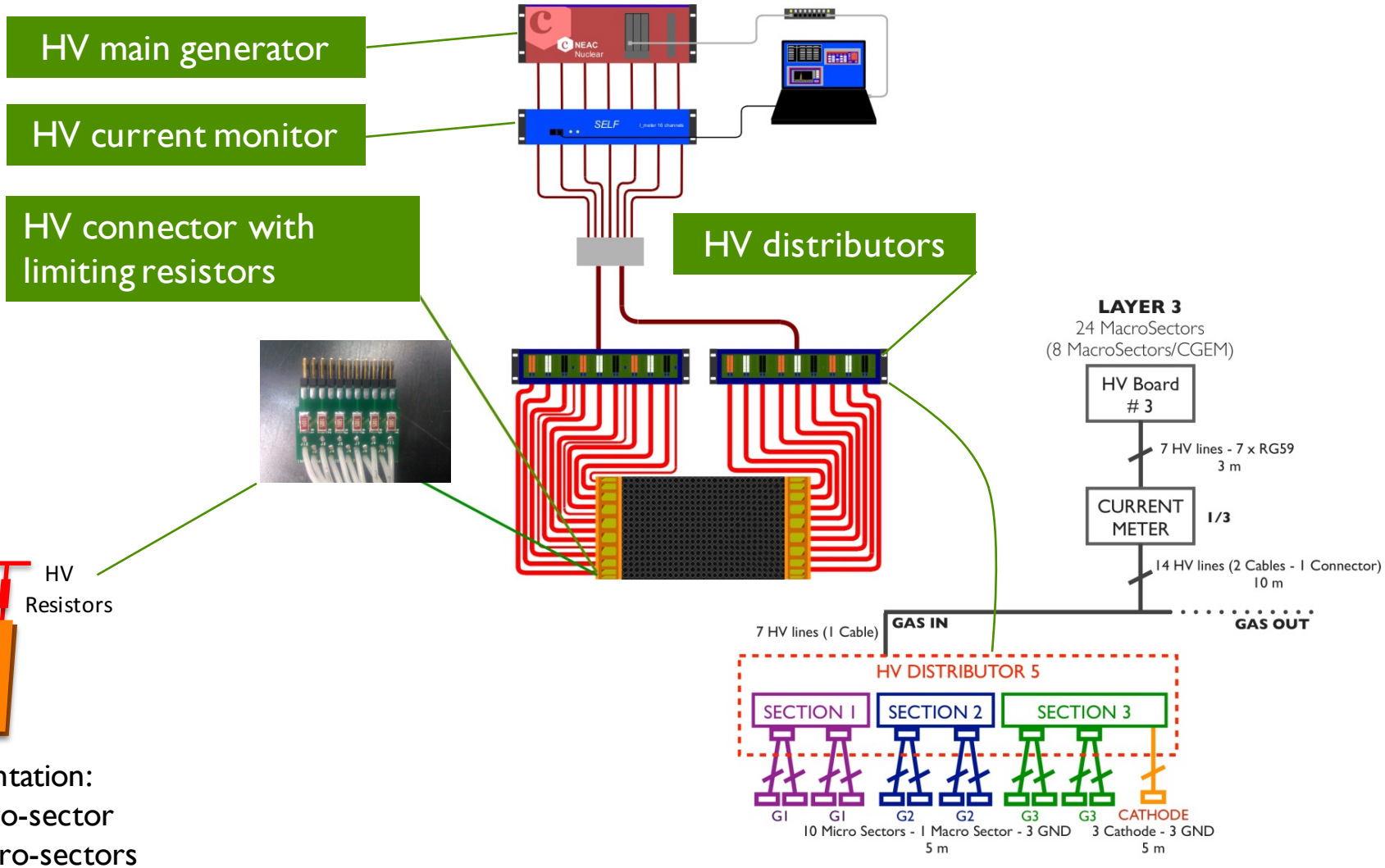


New development using Xilinx Kintex-7/Zynq has been started

- Optical link up to 12.5 Gb/s
- Output data communication over 1 Gb/s ethernet

HV DISTRIBUTION SYSTEM (I)

HV full System based on KLOE-2 design by INFN-LNF to be developed at Mainz and HIM



HV segmentation:

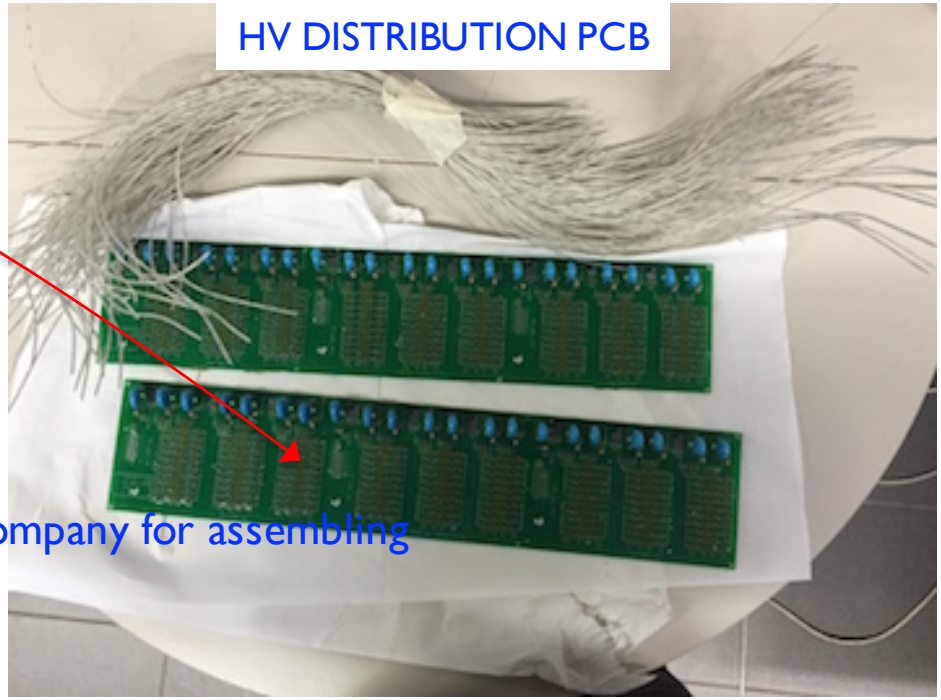
- 1 macro-sector
- 10 micro-sectors

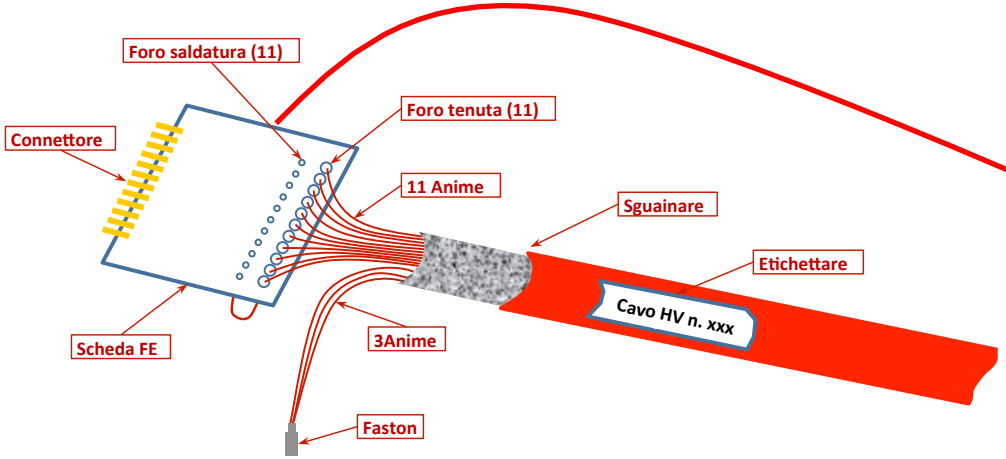
HV DISTRIBUTION SYSTEM (II)

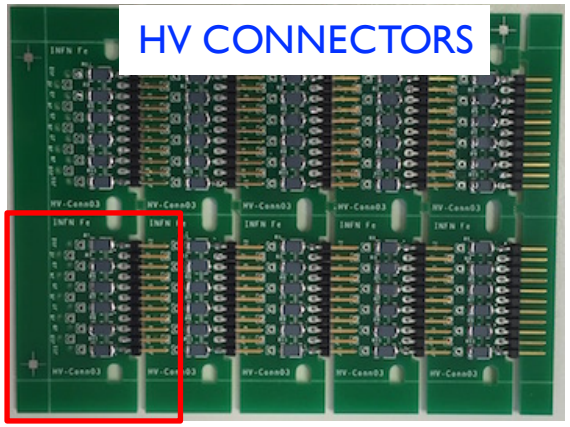
- Main Generator → OK
- Current Monitor → OK

- HV Distributors →
  - Mechanics delivery time: November
  - Board assembling and passivation: OK
  - Two full box assembling: December

- HV Cables →
  - HV cables and connectors: sent to the company for assembling
  - HV connectors (GEM side): assembled
  - Two full box assembling: December







SUMMARY(I)

ASIC

- New chip development based on TOFPET and PASTA asic.
- Preamplifier/Shaper chain has to be modified to cope with high input capacitance (up to 150 pF) and low level input signals (< 5 fC)
- Backend based on TOFPET2 (use ADC instead of ToT)

➡ FOUNDRY SUBMISSION: early Spring 2016

OFF-DETECTOR

- The Readout and Concentrator boards development has already started, but … We need to know DAQ specs to design the ON-LINE and DCS interface

  - CLK signal: LVPECL (what connector ?)
  - CLK frequency: 41.65MHz
  - TRIGGER latency: 6.5μs (or ≃ 8μs or what ?)
  - TRIGGER signal (L1): LVPECL (what connector ?)
  - TRIGGER signal width: 8 clocks

SUMMARY(II)

OFF-DETECTOR DAQ

- Initialization procedure: ???
- Readout module synchronization: ???
- On-line data format ???

HV

- A complete HV chain (Main Power Supply - Current Monitor - HV Distributors – Cables) to supply Layer 2 prototype will be available within December 2015

LAYER 2 CGEM PROTOTYPE INSTRUMENTATION

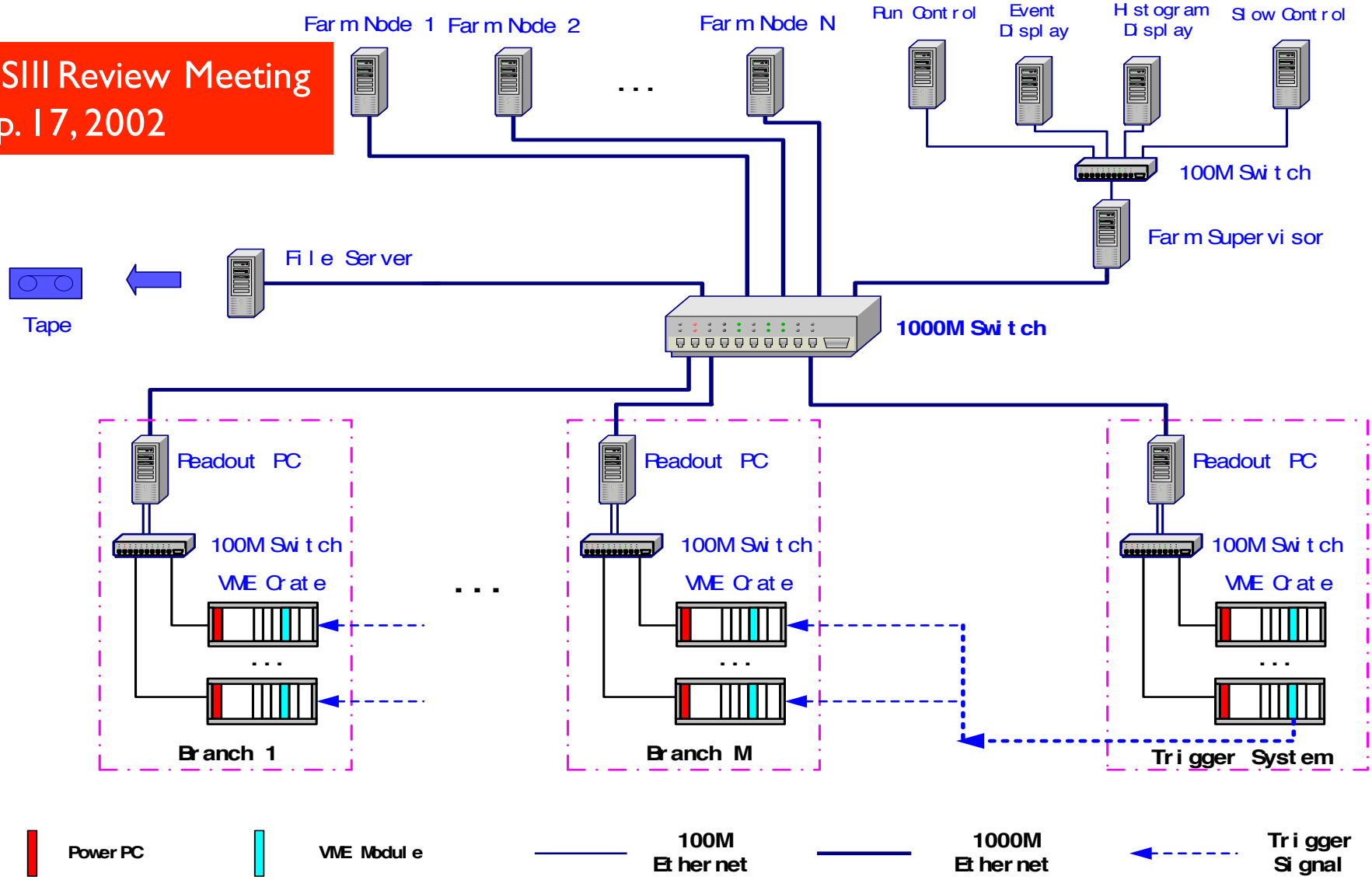
- High Voltage Distribution: December 2015
- Readout will be implemented by means of APV25 hybrid boards + Transition Boards
  - Transition Boards (anode connector → APV25 hybrid): Layout OK (Fe-Roberto)
  - Ground Connection Boards: Layout OK (Fe-Roberto)

➡ Both boards could be available within December 2015

SPARES

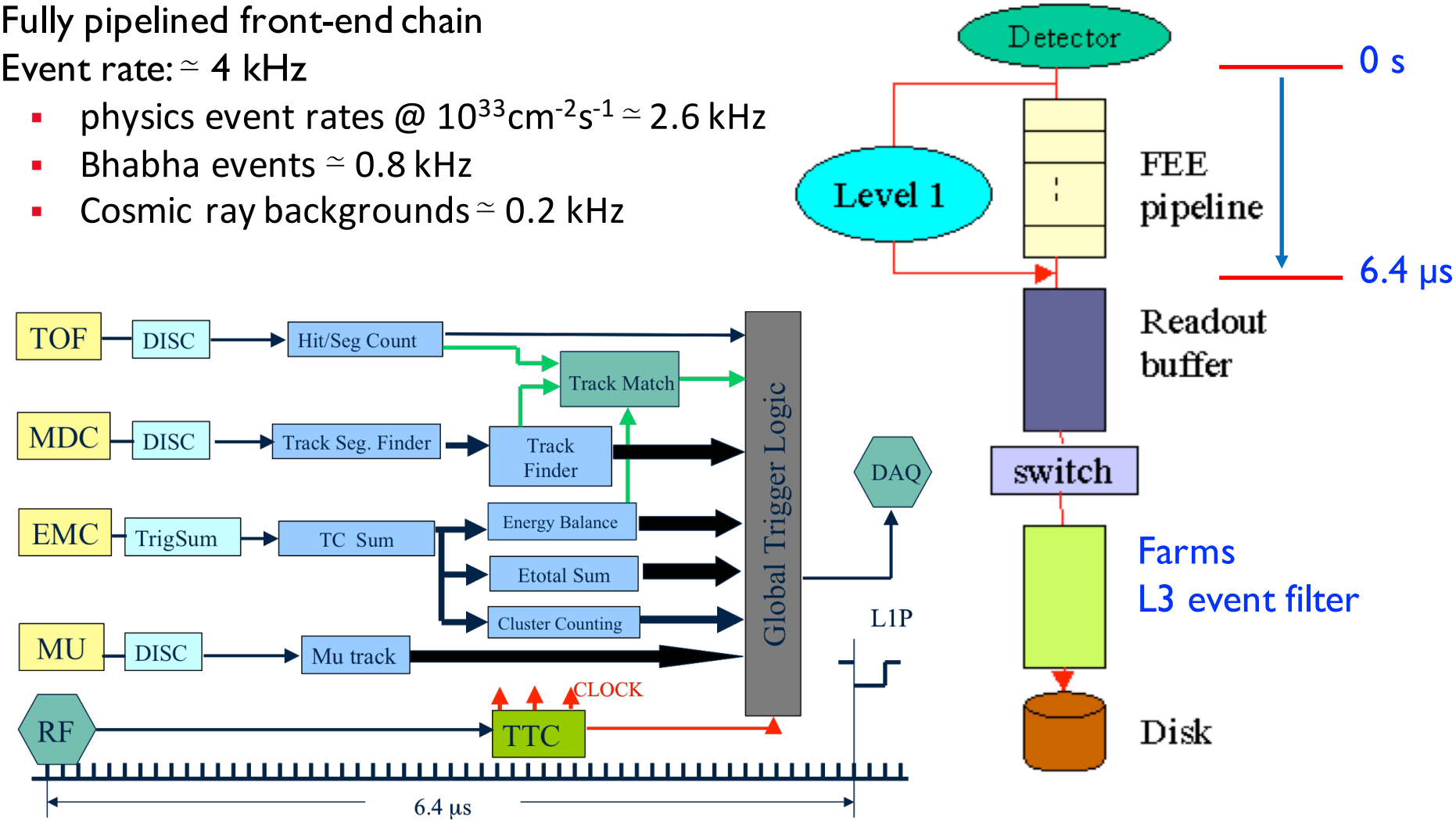
BESIII - READOUT ARCHITECTURE

BESIII Review Meeting
Sep. 17, 2002



BESIII - TRIGGER

- Fully pipelined front-end chain
- Event rate: ≃ 4 kHz
  - physics event rates @ $10^{33}cm^{-2}s^{-1}$ ≃ 2.6 kHz
  - Bhabha events ≃ 0.8 kHz
  - Cosmic ray backgrounds ≃ 0.2 kHz



BESIII - FAST CONTROL FIBER LINKS

- Fast control fiber links are used to transmit L1 signals to readout electronics modules

- TRIGGER SYSTEM → READOUT ELECTRONICS
  - RST: initialization signal (RocketIO/optical transceivers)
  - L1: increase L1 counter. L1 Counter number is used as event number counter for the data in the readout buffer
  - CHK: 500 ns after the 256th L1 signal is issued for checking and resetting the event number counter.

- READOUT ELECTRONICS → TRIGGER SYSTEM
  - RERR: the signal is issued if an error is found in the readout electronics (for example in case of mismatch when CHK is delivered)
  - FULL: the signal is issued when data in the buffers reaches the 80% of the buffers size to hold L1 generation
  - EMPT: the signal is issued when data in the buffers reaches the 10% of the buffer sizes to restart L1 signal generation.