Front End Electronics for the SuperB IFR prototype and detector development

Istituto Nazionale di Fisica Nucleare

Sezione di Ferrara

- Roberto Malaguti (malaguti@fe.infn.it)

Front End Electronics for the SuperB IFR prototype and detector development

Summary

- Front end electronics R&D and test results
- Outline of readout electronics for the SuperB IFR prototype
- Outline of readout electronics for the SuperB IFR detector : TIMING mode readout
- Outline of readout electronics for the SuperB IFR detector : BINARY mode readout
- Outline of readout electronics for the SuperB IFR detector : summarizing

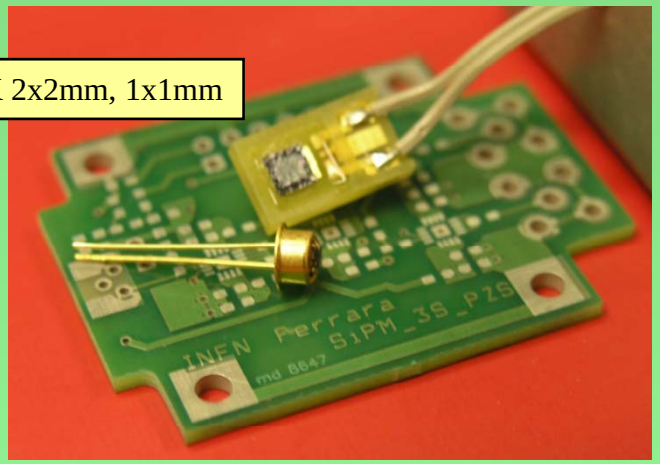
Solid State Photon Counter

SiPM & MPPC detetors

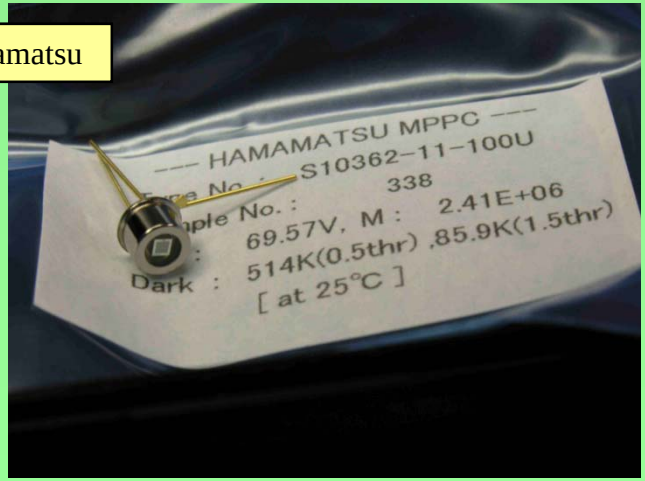
PRO:
- Low working voltage (30 ~ 70V) compared to Photomultiplier or Hybrid Photodiode.
- Good time resolution.
- High gain.
- Insensitivity to magnetic field.
- Low dimension.
- Low price.

CON:
-High dark noise

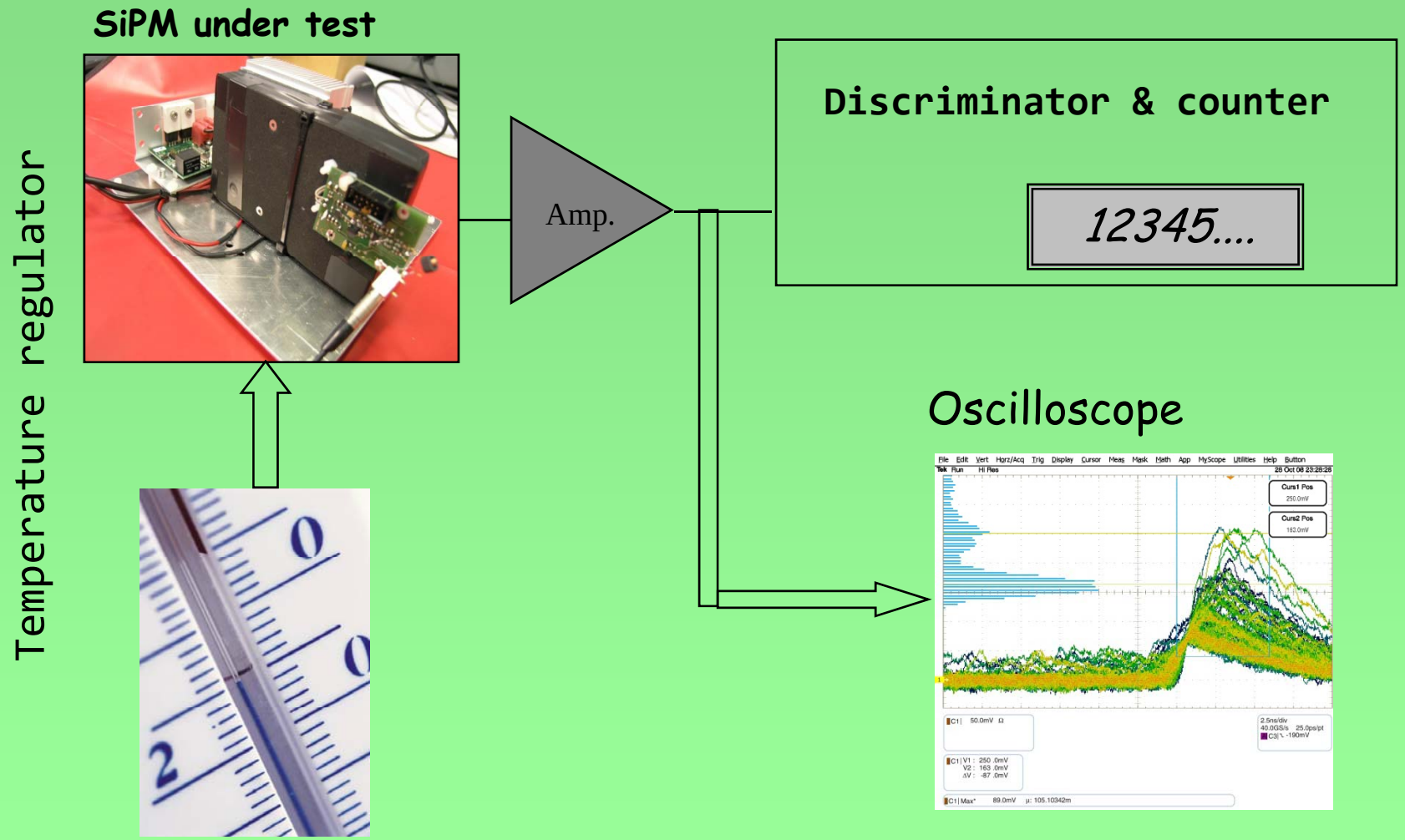
SiPM FBK 2x2mm, 1x1mm



MPPC Hamamatsu



Dark count vs. temperature

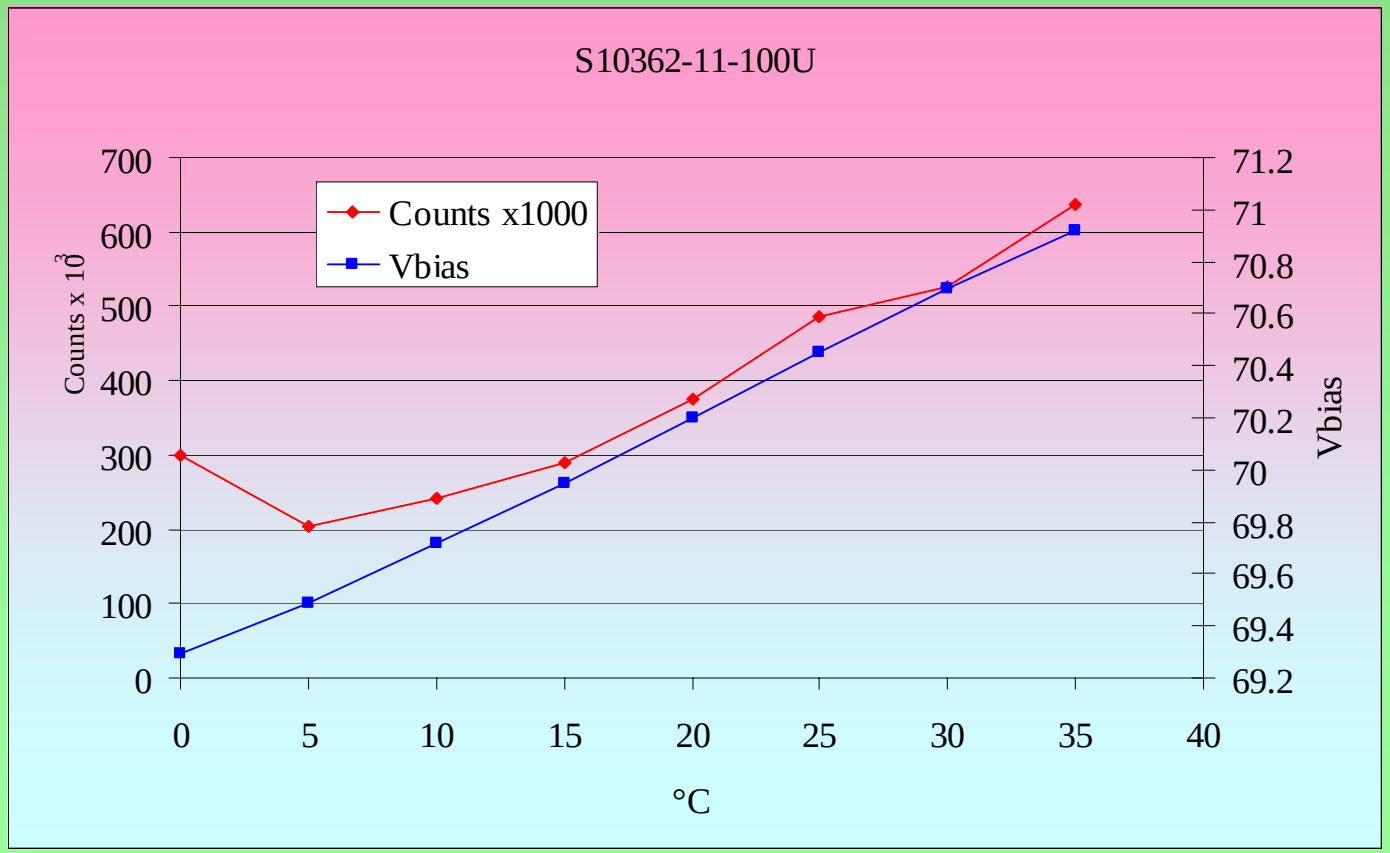


Dark count vs. temperature

MPPC Hamamatsu mod. S10362-11-100U .

The Bias voltage was regulated to keep the MPPC gain constant when varying the temperature.
Count threshold was set at 0.5 photoelectrons.
The counts halve when the temperature goes from 25° to 10°

Temp °C	Counts x10^3
0	300
5	205
10	241
15	290
20	374
25	486
30	526
35	637

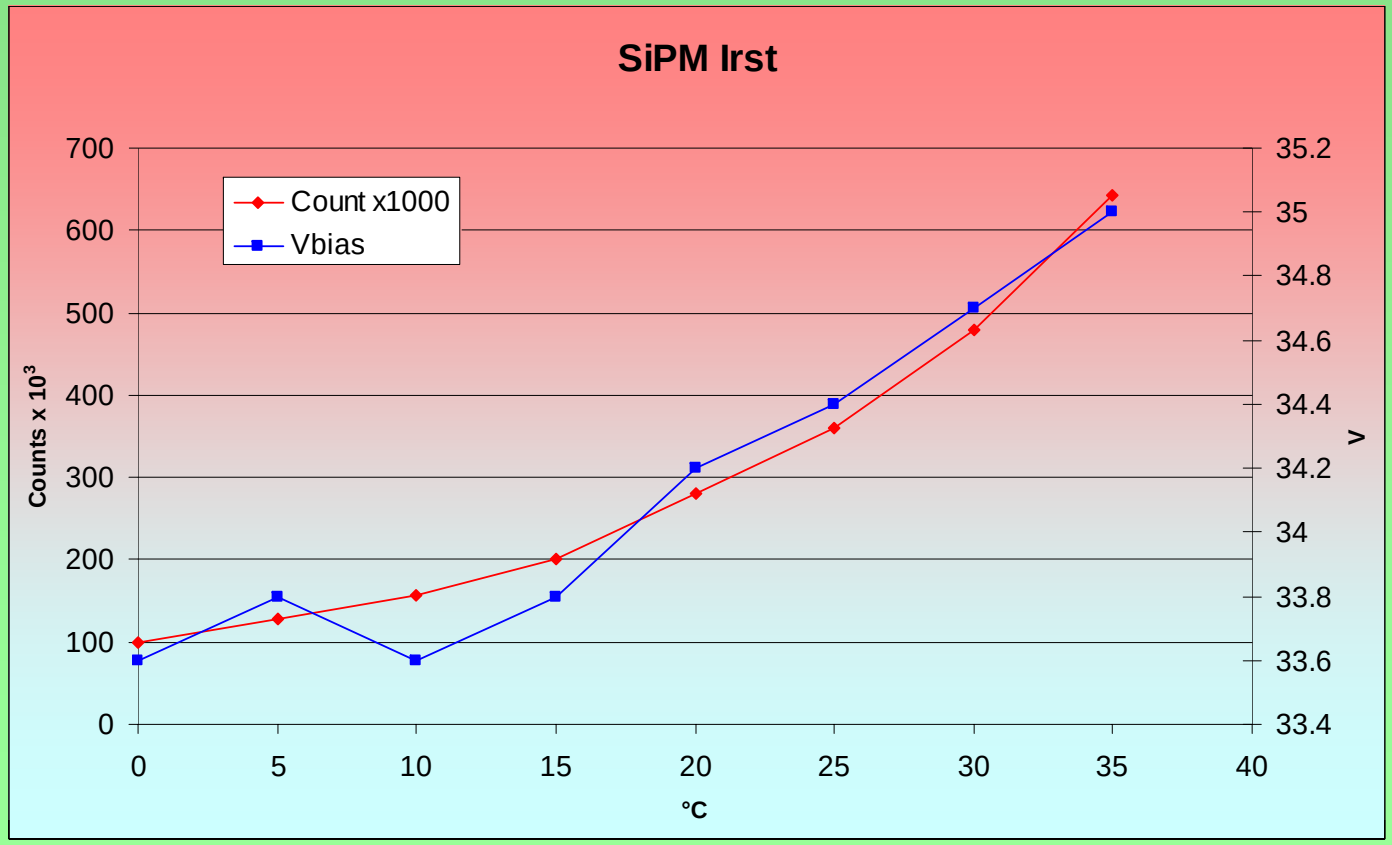


Dark count vs. temperature

SiPM FBK (Fondazione Bruno Kessler) sensor area 1x1mm^2 cell size 40x40um^2.

The Bias voltage was regulated to keep the SiPM gain constant when varying the temperature.
Count threshold was set at 0.5 photoelectrons.
The counts halve when the temperature goes from 25° to 10°

Temp °C	Counts x10^3
0	99
5	128
10	157
15	200
20	281
25	360
30	480
35	642



Front End Electronics for SiPM: prototype development and design outline

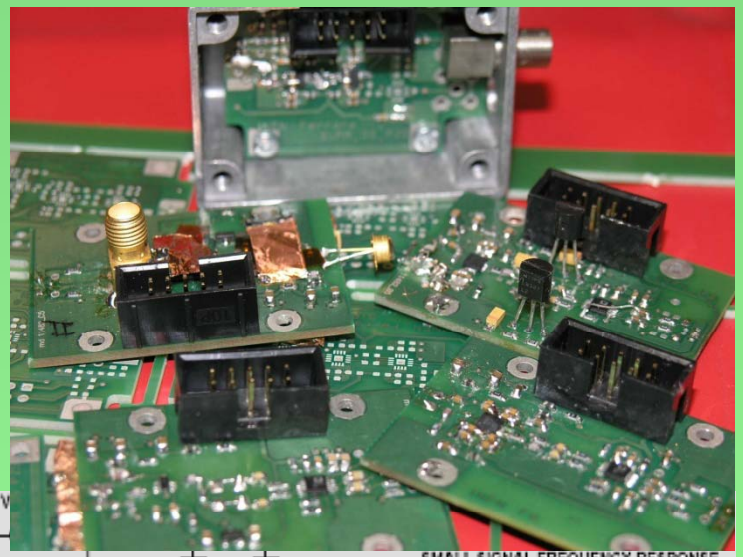
Four different front-end configuration were tested:

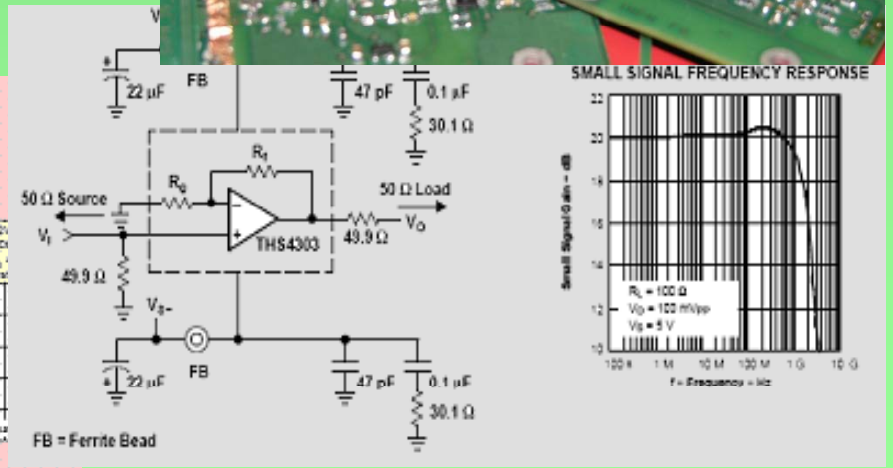
1) THS4303 as inverting amplifier

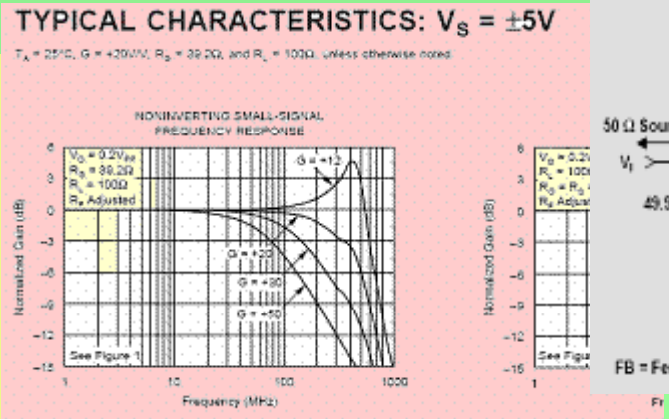
2) THS4303 as NON inverting amplifier

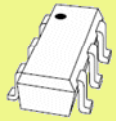
3) MMIC BGA2748

4) AD8009 as inverting amplifier









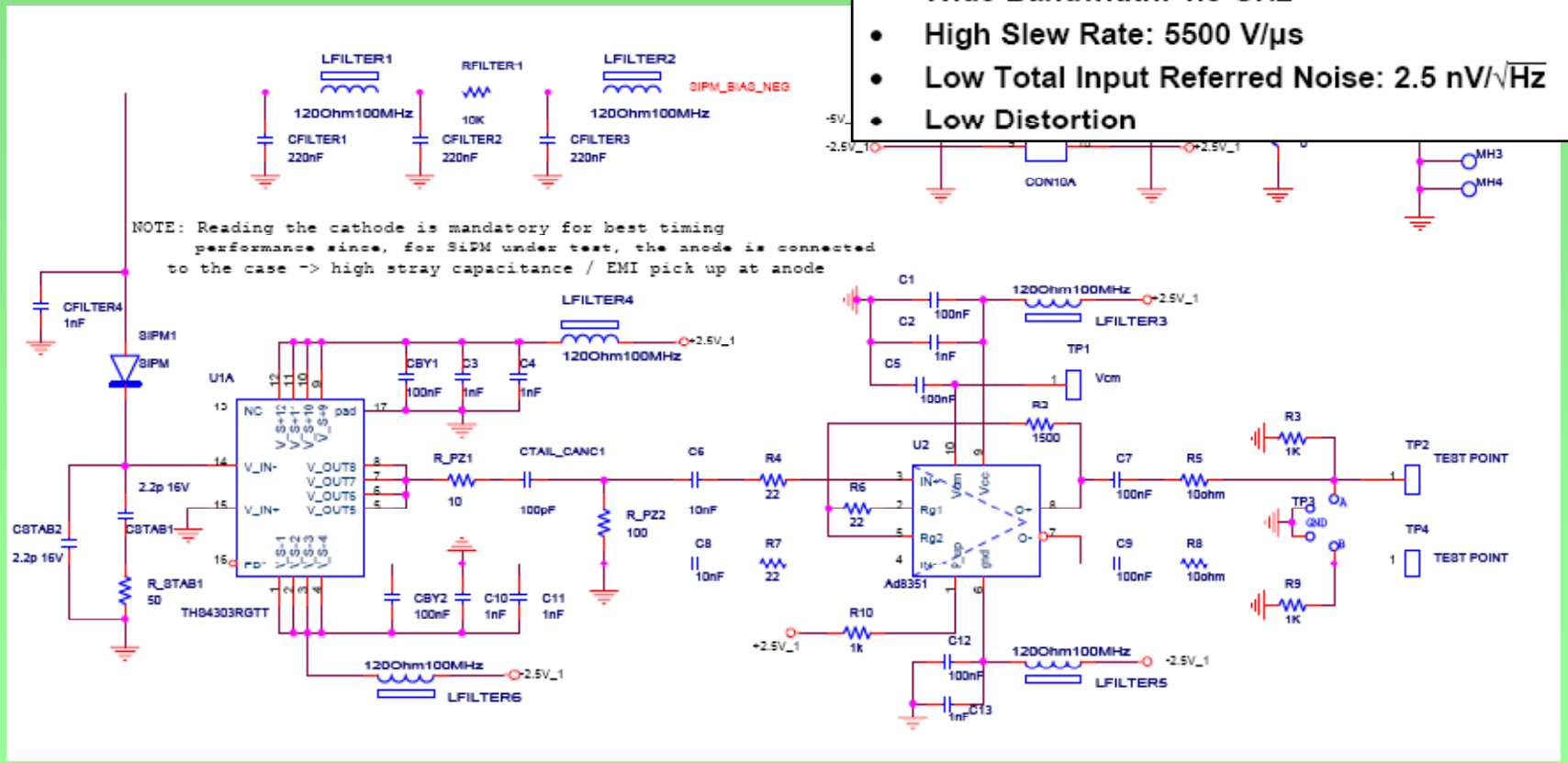
BGA2748
MMIC wideband amplifier

Front End Electronics for SiPM: prototype development and design outline

1) Texas Instruments THS4303 as inverting amplifier

FEATURES

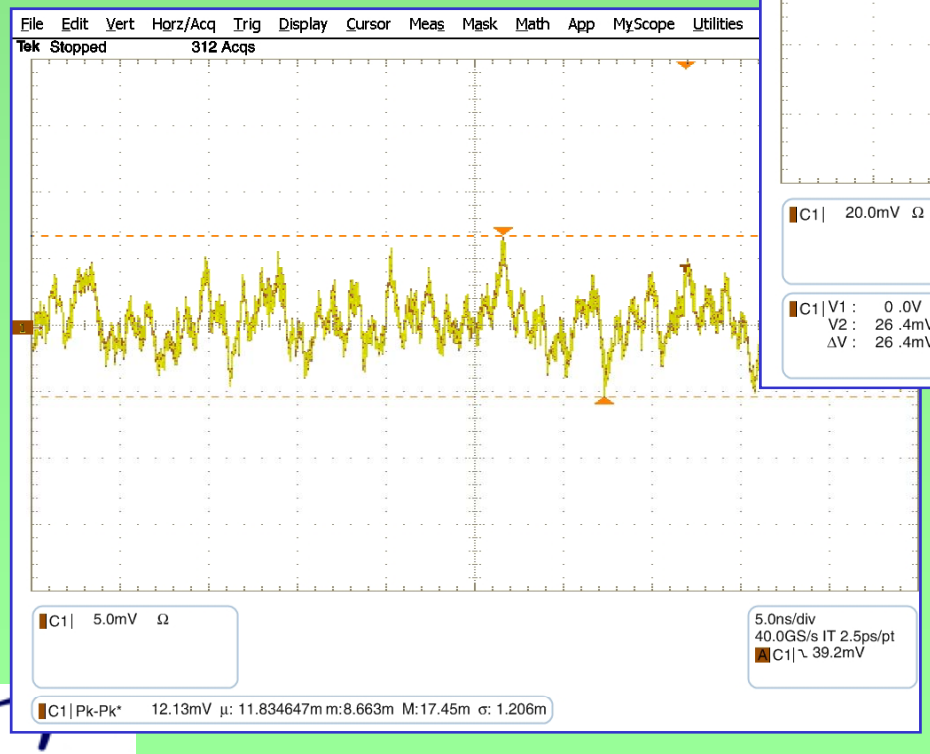
- Fixed Closed-Loop Gain Amplifier – 10 V/V (20 dB)
- Wide Bandwidth: 1.8 GHz
- High Slew Rate: 5500 V/µs
- Low Total Input Referred Noise: 2.5 nV/√Hz
- Low Distortion

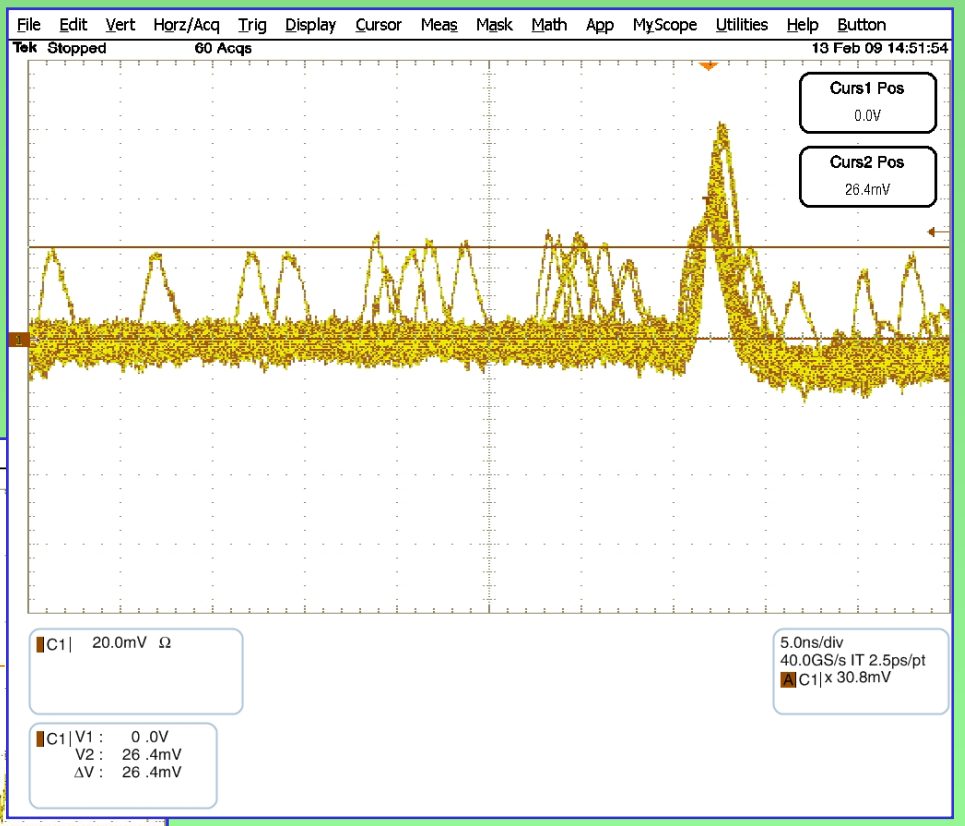


Front End Electronics for SiPM: prototype development and design outline

1) THS4303 as inverting amplifier

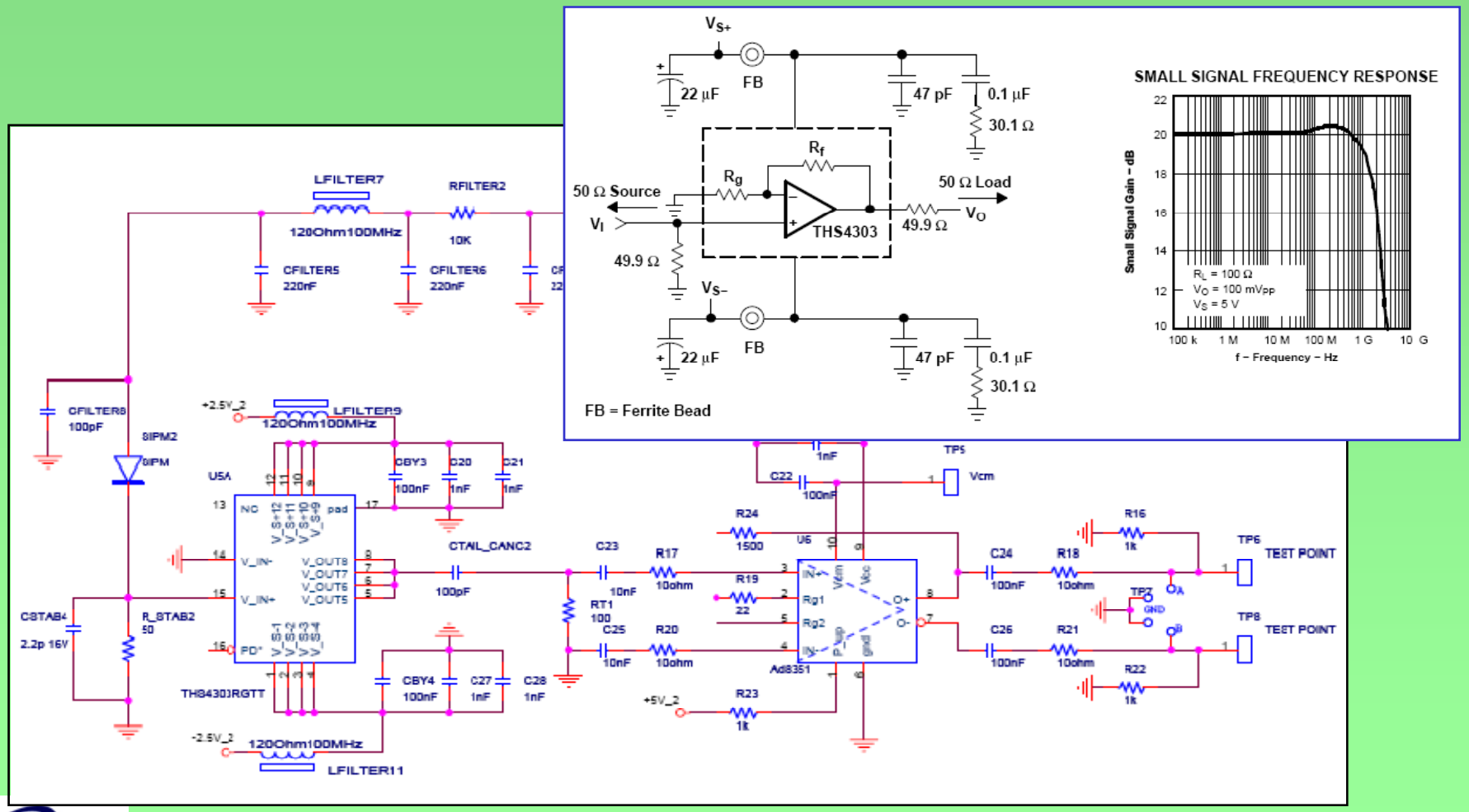
- Noise = 12mV Pk-Pk
- Single Photo-electron = 26mV
- Signal/noise ratio = 2.16





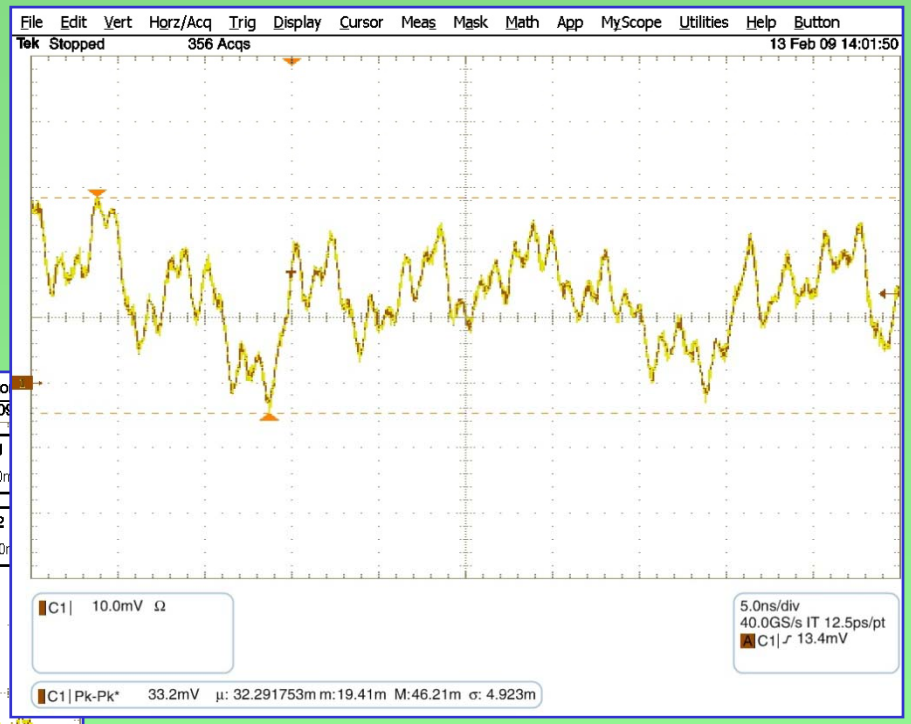
Front End Electronics for SiPM: prototype development and design outline

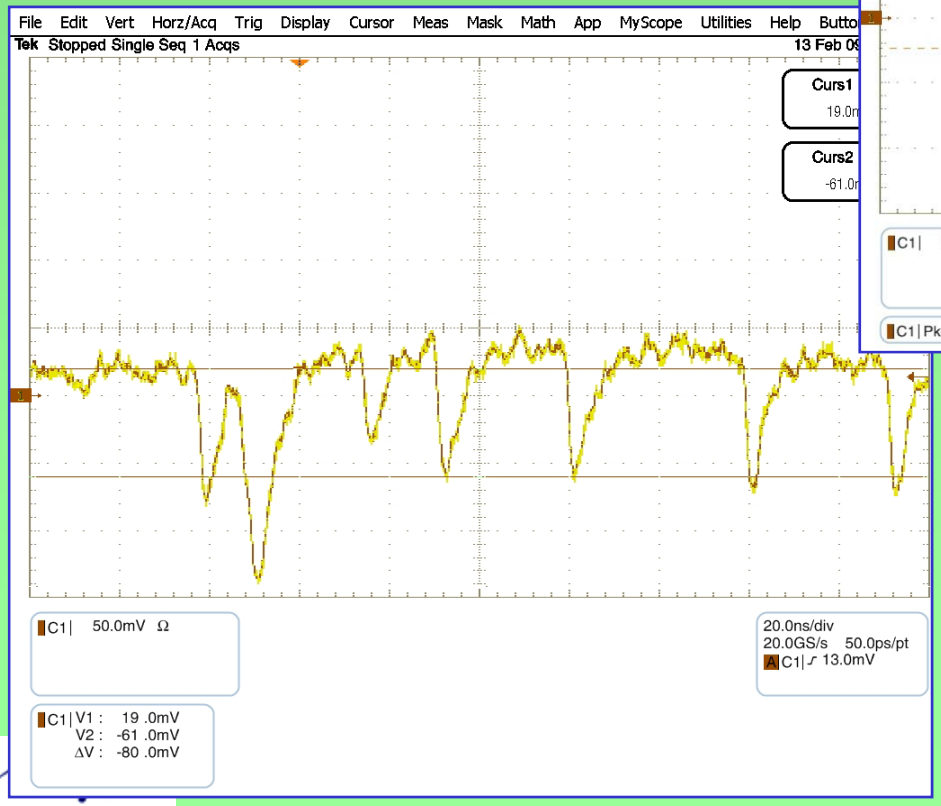
2) Texas Instruments **THS4303 Non inverting amplifier**



Front End Electronics for SiPM: prototype development and design outline

2) **THS4303 Non inverting amplifier**
- Noise = 32.3mV Pk-Pk
- Single P.e. level = 80mV
- S/N ratio = 2.47





- the signals shown were picked up after a differential to single-end stage and so they are little bigger and a little slower than the signals for the THS4303 inverting configuration

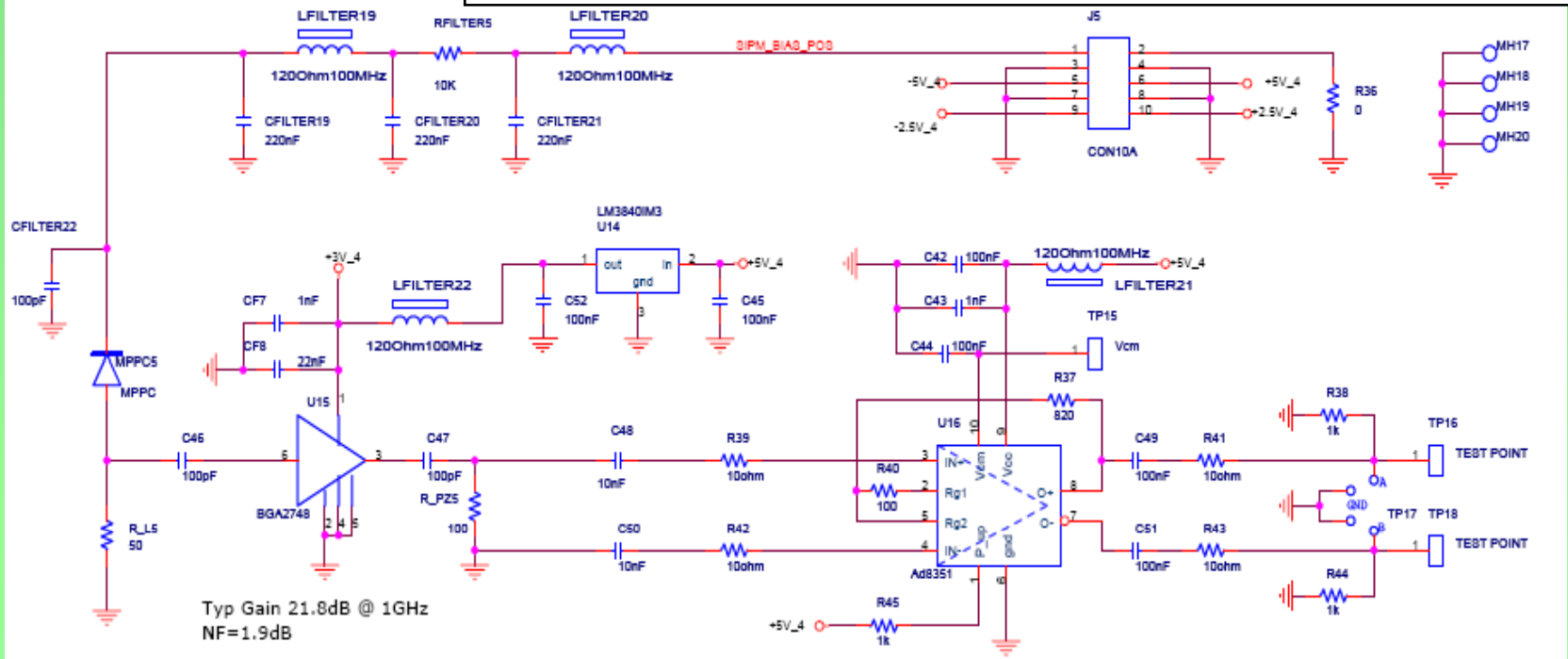
Front End Electronics for SiPM: prototype development and design outline

3) **MMIC BGA2748**

NXP Silicon Monolithic Microwave Integrated Circuit (MMIC)

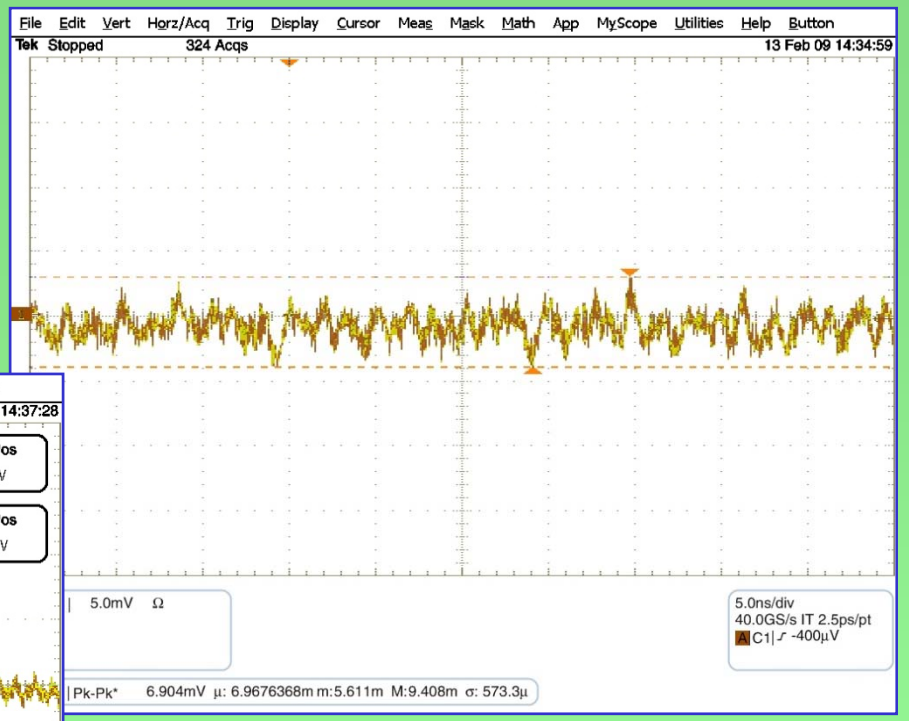
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_S	DC supply voltage		3	4	V
I_S	DC supply current		5.7	–	mA
$\|s_{21}\|^2$	insertion power gain	f = 1 GHz	21.8	–	dB
NF	noise figure	f = 1 GHz	1.9	–	dB
$P_{L(sat)}$	saturated load power	f = 1 GHz	–2.3	–	dBm



Front End Electronics for SiPM: prototype development and design outline

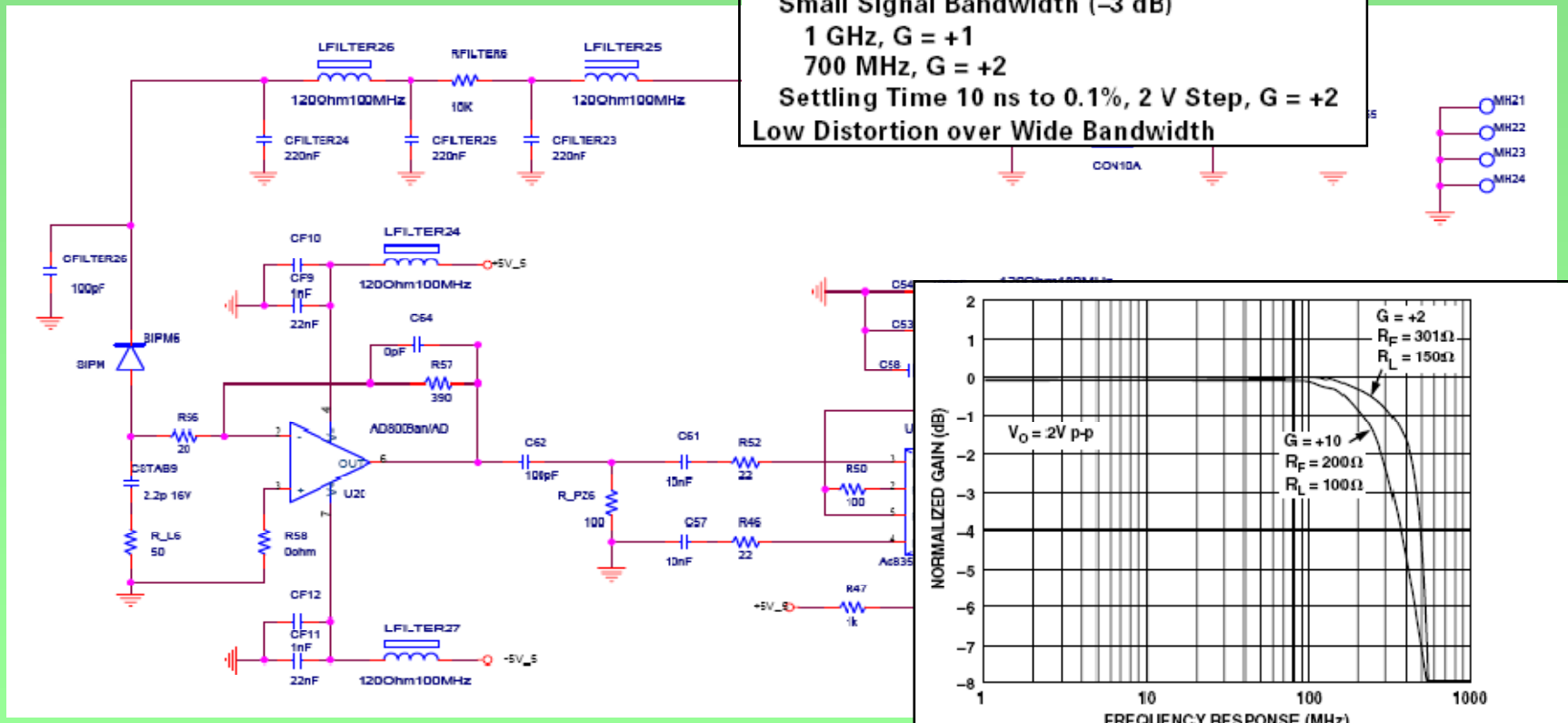
3) BGA2748 **MMIC wide band amplifier**
- Noise = 6.9mV Pk-Pk
- Single P.e. level = 17mV
- S/N ratio = 2.46



Front End Electronics for SiPM: prototype development and design outline

4) Analog Device AD8009 Inverting amplifier

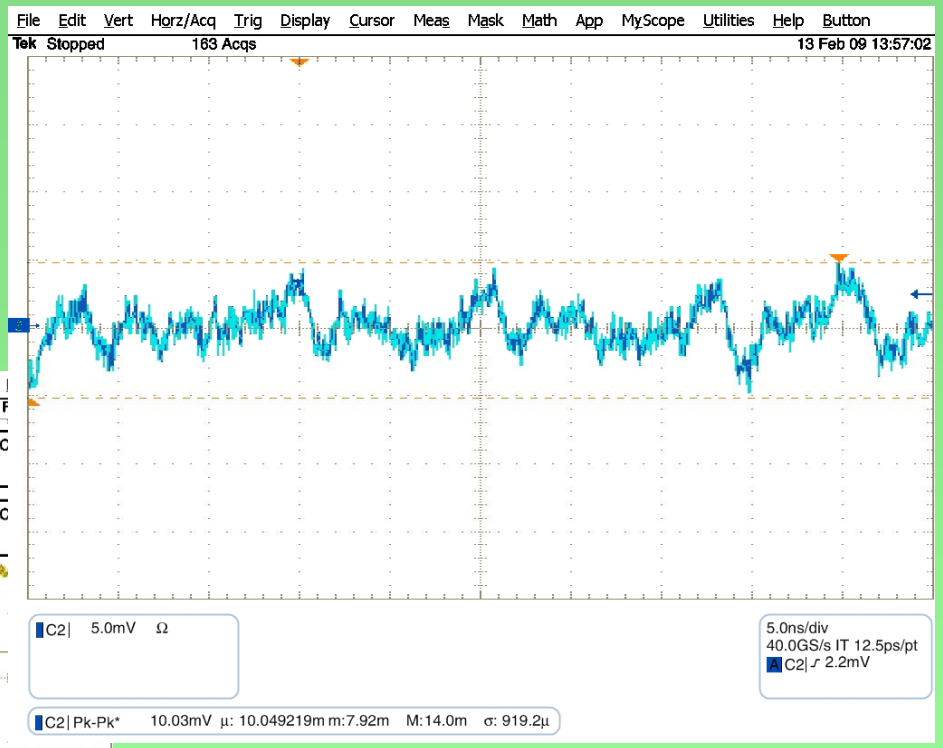
FEATURES
Ultrahigh Speed
5,500 V/µs Slew Rate, 4 V Step, G = +2
545 ps Rise Time, 2 V Step, G = +2
Large Signal Bandwidth
440 MHz, G = +2
320 MHz, G = +10
Small Signal Bandwidth (–3 dB)
1 GHz, G = +1
700 MHz, G = +2
Settling Time 10 ns to 0.1%, 2 V Step, G = +2
Low Distortion over Wide Bandwidth

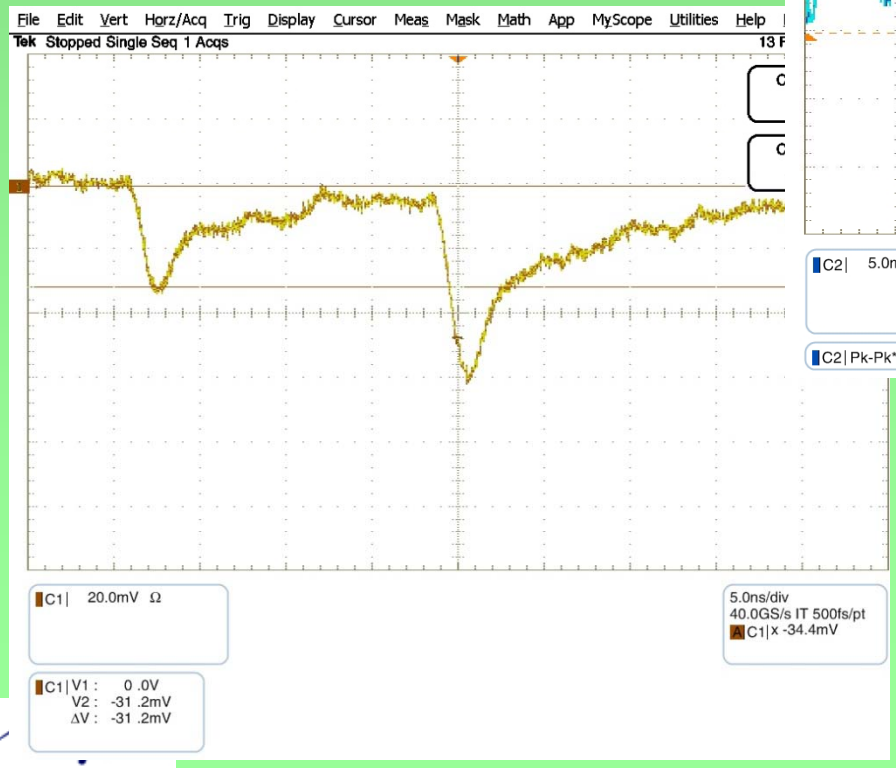


re 1. Large Signal Frequency Response; G = +2 and +10

Front End Electronics for SiPM: prototype development and design outline

4) AD8009 **Inverting amplifier**
- Noise = 10mV Pk-Pk
- Single P.e signal = -31mV
- S/N ratio = 3.1





Summary table

Type	Noise	Single P.e.	S/N ratio	Note
THS4303 inv	12mVpp	26mV	2.16	Sometime instable..
THS4303 non inv	32.3mVpp	80mV	2.47	Good signals amplitude
MMIC	6.9mVpp	17mV	2.46	Faster
AD8009	10mVpp	31mV	3.1	Slower

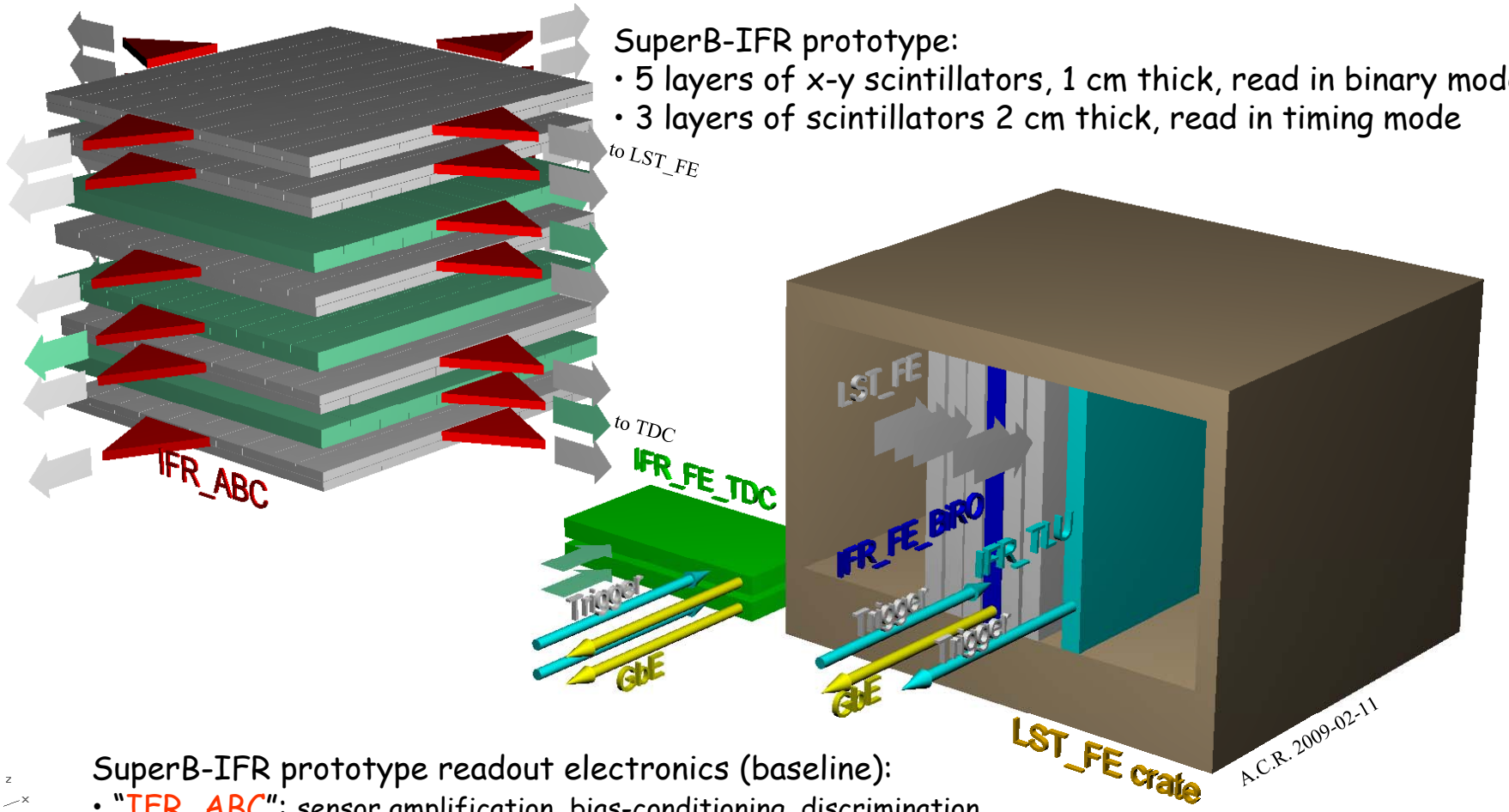
Front End Electronics for the SuperB IFR prototype and detector development

Summary

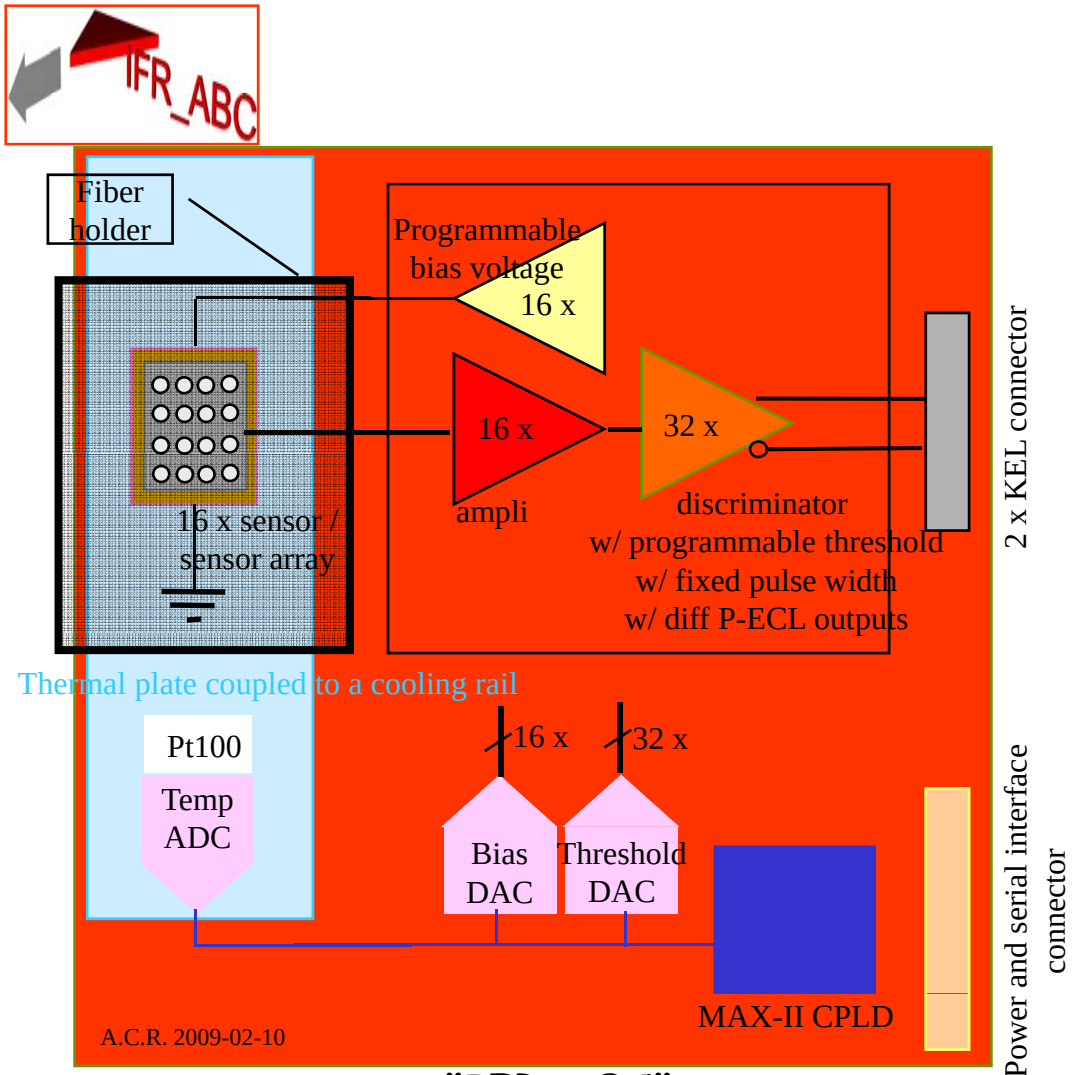
- Front end electronics R&D and test results
- **Outline of readout electronics for the SuperB IFR prototype**
- Outline of readout electronics for the SuperB IFR detector : TIMING mode readout
- Outline of readout electronics for the SuperB IFR detector : BINARY mode readout
- Outline of readout electronics for the SuperB IFR detector : summarizing

Proposal of readout electronics for the SuperB IFR prototype

SuperB-IFR prototype:
- 5 layers of x-y scintillators, 1 cm thick, read in binary mode
- 3 layers of scintillators 2 cm thick, read in timing mode



SuperB-IFR prototype readout electronics (baseline):
- "IFR_ABC": sensor amplification, bias-conditioning, discrimination
- "LST-FE": front end card used in BaBar IFR equipped with PECL receiver daughter cards. It samples status of inputs @ 80MHz and stores it, pending the trigger request
- "IFR_FE_BiRO": collects data from LST-FE upon trigger request and sends it to DAQ PC (via GbE)
- "IFR_FE_TDC": a multi-hit TDC design based on commercially available TDC chips with trigger interface and GbE output link to the DAQ PC
- "IFR_TLU": a module (Trigger Logic Unit) to generate a fixed latency trigger based on primitives from the IFR prototype itself or from external sources



Outline of the **"IFR_ABC"** card

(sensor amplification, bias-conditioning, discrimination)

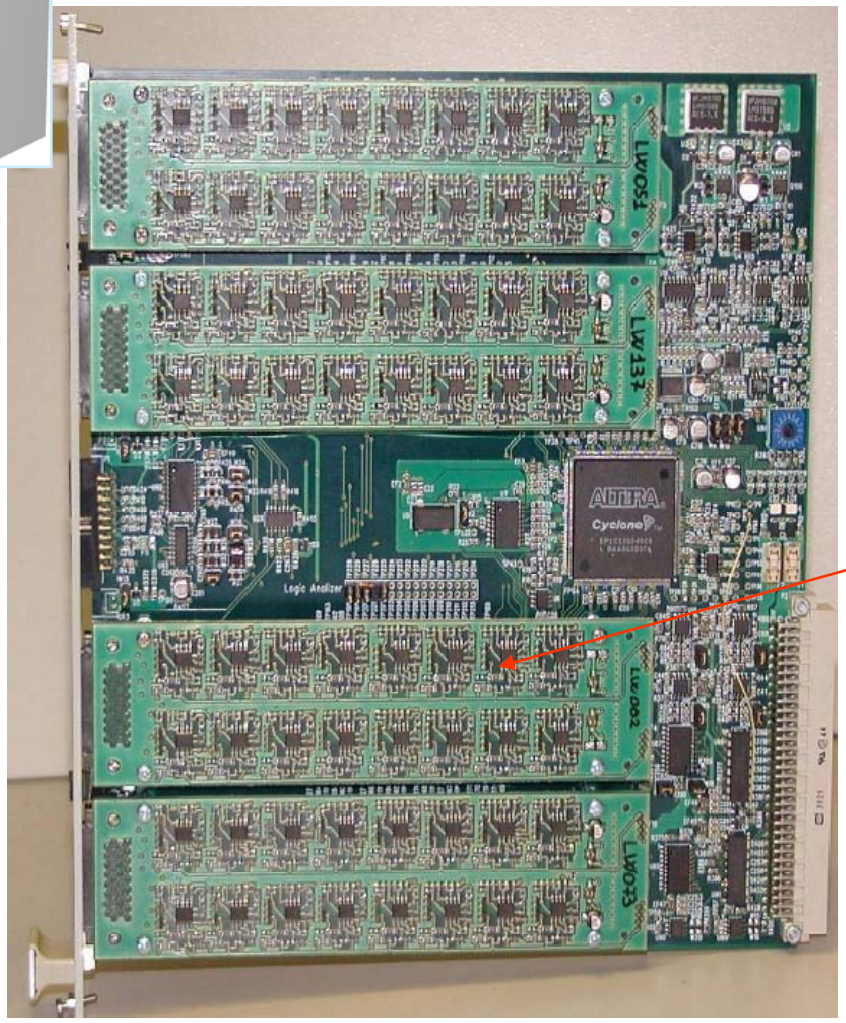
"IFR_ABC" card features:

- ampli: two stage w/discrete components: THS4303 (2.6$ea) + AD8009(1.8$ea).
- discri: ADCMP562BRQ (dual, 2.7$ea)

For the SuperB IFR prototype it is foreseen to use two comparators at different thresholds (2.5 pe and 1.5 pe for instance) for each sensor

- DAC: MAX5592 (10bit, octal, 5.24$ea)
- CPLD: ALTERA EPM1270GT144C5N (22$ ea)
- signal connector compatible with BaBar IFR signal cables (re-usable): KEL 8831E-034-170LD (3€ea for the PCB-mount+ 6.5€ea for the cable mount)

Total needed for prototype readout : 26



"LST_FE" card features:

• designed for the LST based IFR at BaBar. It sampled and stored the 64 inputs (16 x daughter card) for the BaBar trigger latency. The LST_FE already provides 4 Fast-OR output signals, one per daughter card, which can be used for stand-alone triggering of the SuperB-IFR prototype (one daughter card = one side of one plane of thin scintillators)

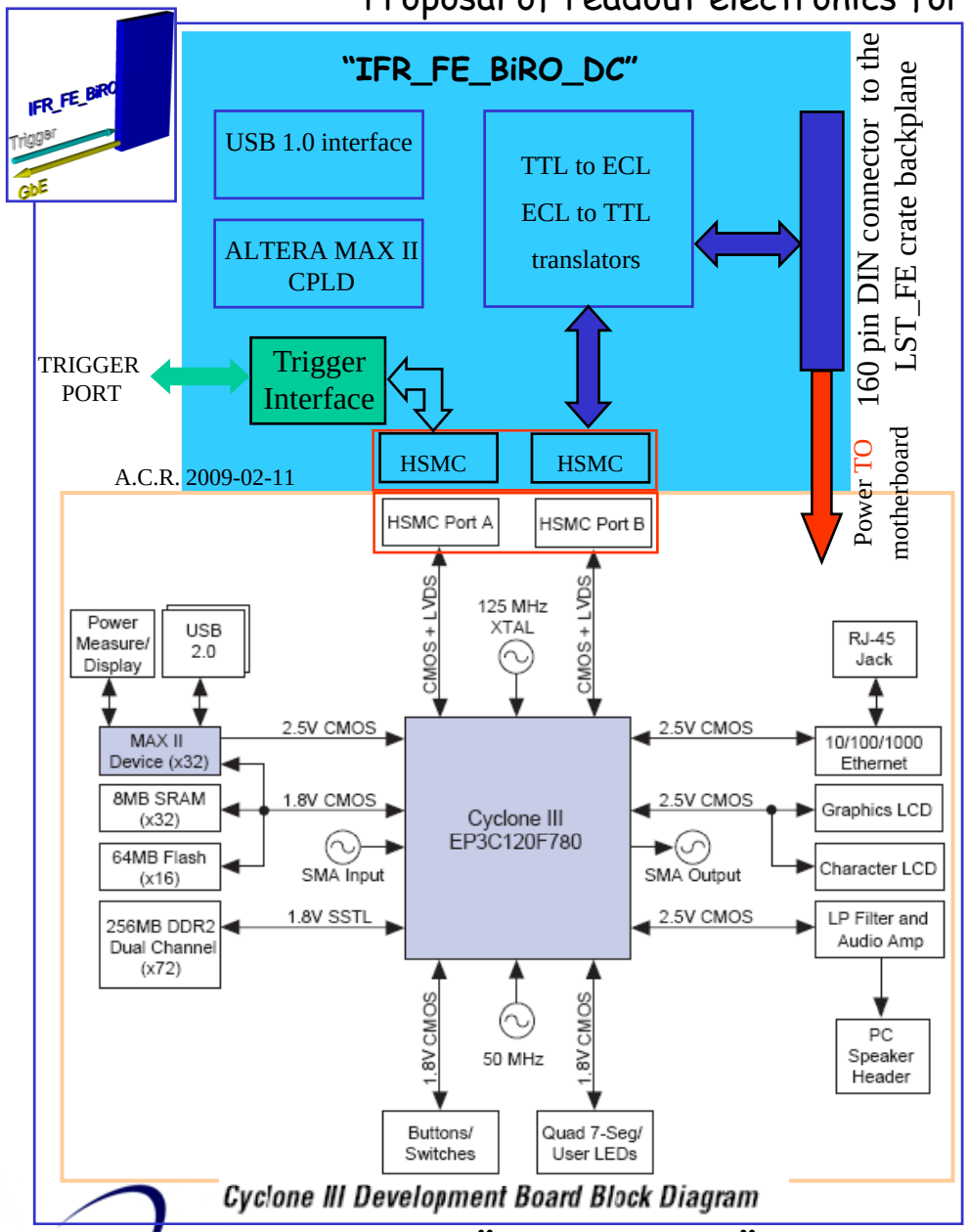
• to be used for the SuperB IFR prototype readout it needs replacement of present daughter cards with new daughter cards **"LST_FE_pECL_Rx"** which would:

a) translate the PECL differential inputs into TTL using, for instance, MC100LVELT23D dual PECL/LVTTL translators (2.3 €ea)

b) provide signal connectors compatible with BaBar IFR signal cables: KEL 8831E-034-170LD (3€ea for the PCB-mount+ 6.5€ea for the cable mount)

Total needed for prototype readout in binary mode: 20

Proposal of readout electronics for the SuperB IFR prototype



Outline of the "IFR_FE_BiRO" card

"IFR_FE_BiRO" card features:

• motherboard: it is based on an ALTERA development board for the Cyclone III FPGA (**DK-DEV-3C120N, cost 1000 €**). The Cyclone III FPGA on board has enough memory resources to buffer the data collected from the LST_FE boards. Data requested by a trigger is sent over the GbE link featured by the development board.

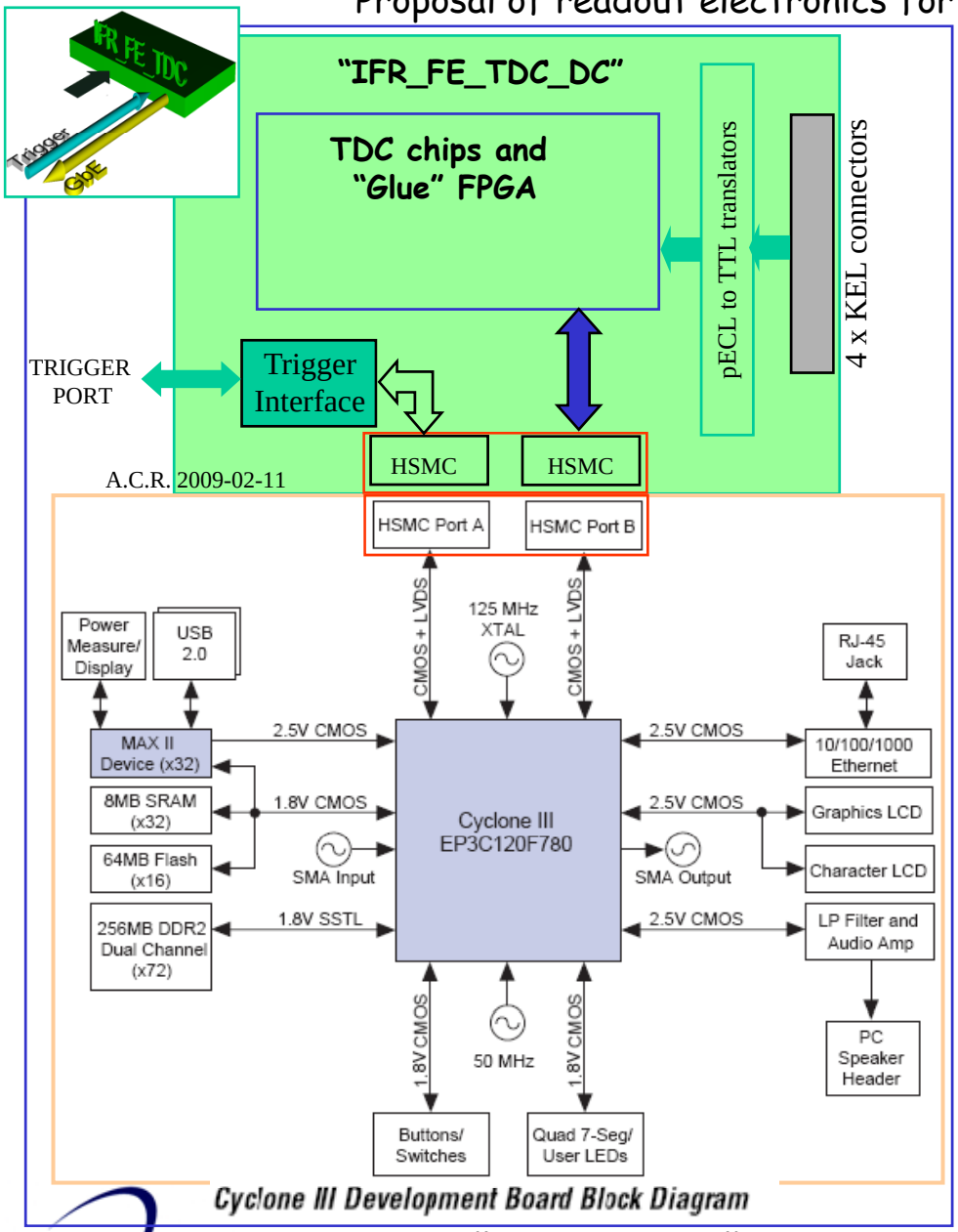
• daughter card (**"IFR_FE_BiRO_DC"**): it provides mostly level translators and connections to:

- the LST_FE crate backplane
- the Trigger Logic Unit
- the motherboard through the HSMC connectors (SAMTEC ASP-122952-01)

Total needed for prototype readout: 2 (one for the "IFR_FE_BiRO", one for the "IFR_TLU")

The LST_FE and the IFR_FE_BiRO cards are hosted in one of the LST_FE crates recovered from BaBar (**designed by INFN Genova for the LST based IFR readout**).

Proposal of readout electronics for the SuperB IFR prototype



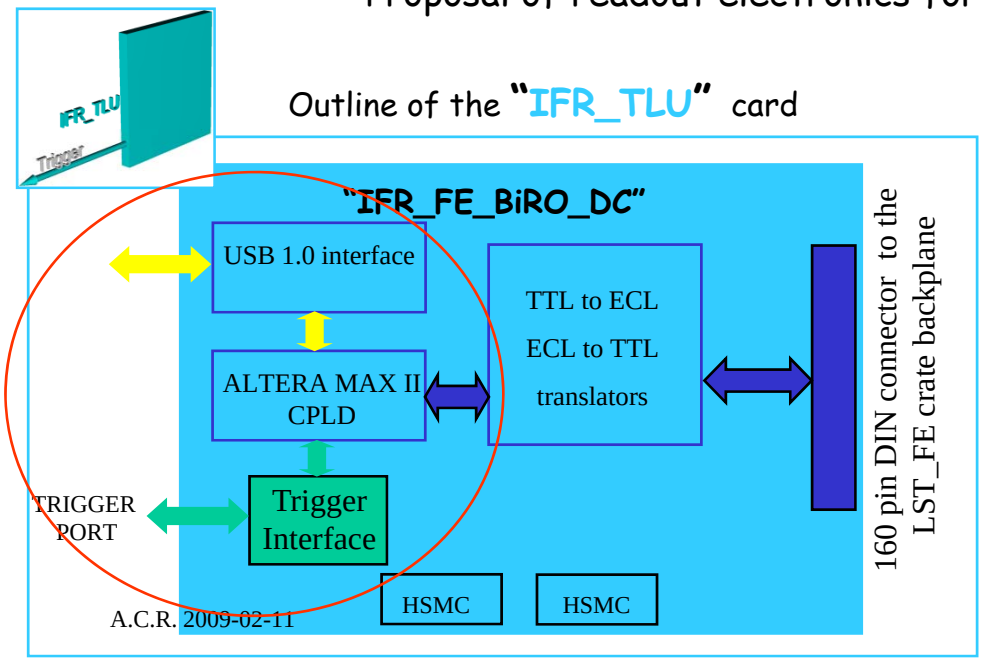
Outline of the "IFR_FE_TDC" card

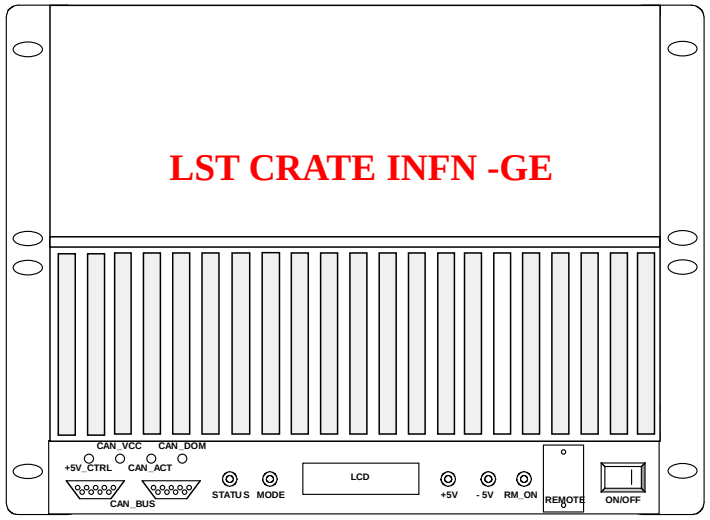
"IFR_FE_TDC" card features:

• motherboard: it is based on an ALTERA development board for the Cyclone III FPGA (**DK-DEV-3C120N, cost 1000 €**). The Cyclone III FPGA on board continuously collects data from the **"IFR_FE_TDC_DC"** daughter card and stores it in a circular buffer pending a trigger request. Data requested by a trigger is sent over the on-board GbE link.

• daughter card (**"IFR_FE_TDC_DC"**): it features commercially available TDCs (8 x ACAM TDC-GPX as a baseline) to handle at least 64 channels per board. An on-board FPGA configures the TDC chips, provides the primary buffers into which data is stored pending the trigger request and performs transfer of "trigger matched data" through a FIFO-buffered output port towards the motherboard.

Total needed for prototype readout : 4 (assuming timing measurement with double threshold)





Layout of the BaBar LST crate

"IFR_TLU" card features:

• **it is simply the "IFR_FE_BiRO_DC"** (plugged in a specific location of the LST_FE backplane) in which the section based on the ALTERA MAX-II CPLD is activated.

The CPLD performs programmable (via USB 1.0) combinatorial functions on the "Fast-OR" signals coming from the "LST_FE" cards to generate the trigger requests to the DAQ.

the "IFR_TLU" provides level translators and connections to:

- the LST_FE crate backplane
- the Trigger Logic Unit I/o port (which includes an Open Collector "Busy" Line driven by the FE cards)
- additional inputs for external trigger sources

Front End Electronics for the SuperB IFR prototype and detector development

Summary

- Front end electronics R&D and test results
- Outline of readout electronics for the SuperB IFR prototype
- **Outline of readout electronics for the SuperB IFR detector : TIMING mode readout**
- Outline of readout electronics for the SuperB IFR detector : BINARY mode readout
- Outline of readout electronics for the SuperB IFR detector : summarizing

Proposal of readout electronics for the SuperB IFR detector : TIMING mode readout

SuperB-IFR numerology:

- Barrel: N_Barrel = 3600
- EndCaps: N_EndCap = 2400 + 2400

(quoting G. Cibinetto)

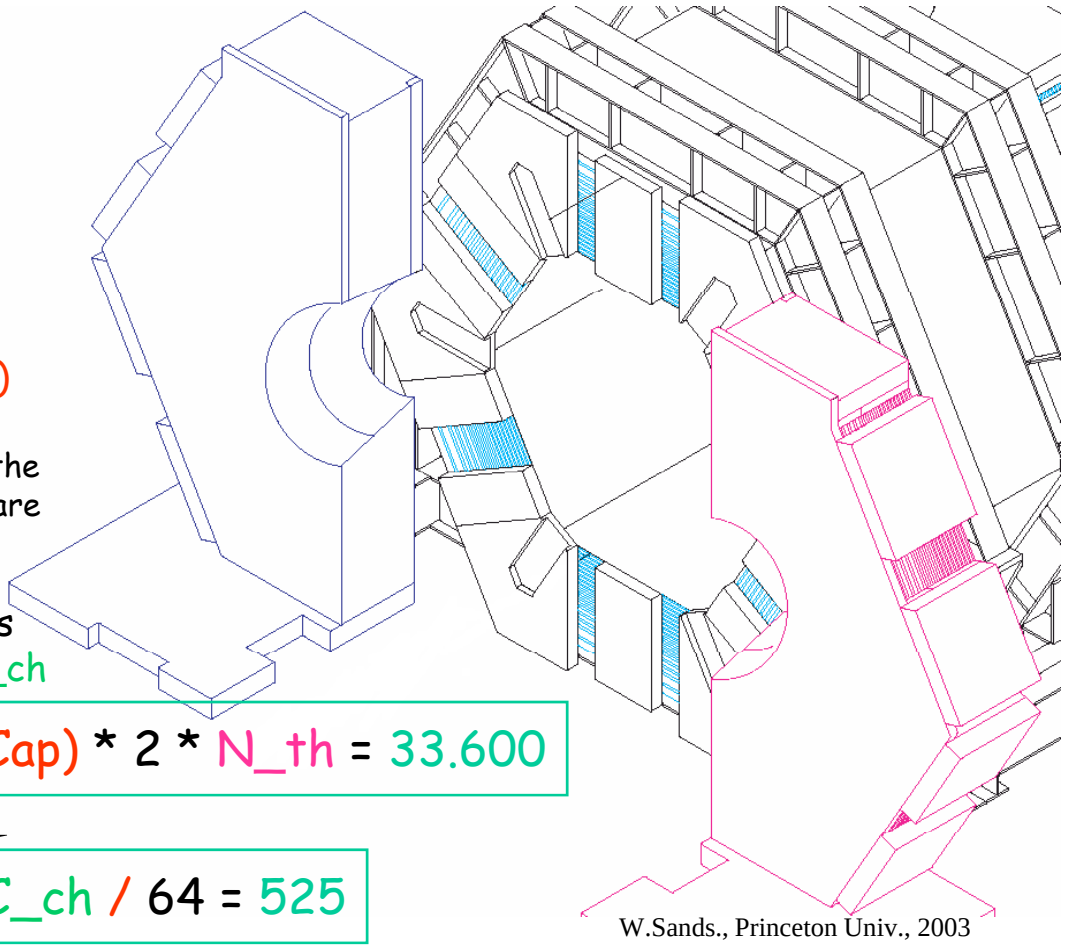
Assuming:

- readout in TIMING mode with N_th (=2) thresholds:

both the high threshold (2.5 p.e. for instance) and the low threshold (1.5 p.e. for instance) crossing times are acquired by the F.E., the second threshold crossing validating the first for better noise rejection.

-> each scintillator is readout at both ends

-> total number of TDC channels: N_TDC_ch



W.Sands., Princeton Univ., 2003

$$N\_TDC\_ch = (N\_Barrel + N\_EndCap) * 2 * N\_th = 33.600$$

$$N\_TDC\_board = N\_TDC\_ch / 64 = 525$$

Hopefully the tests on the prototype will show that it will be possible to keep:

N_th = 1

but in the meantime it is better to consider the worst option

!!! Multihit TDC ASICs currently available assume a reference clock of 40MHz meanwhile the latest document edited by D.Breton and U. Marconi assumes a 56.25MHz clock: it is an issue !!!

Proposal of readout electronics for the SuperB IFR detector : TIMING mode readout

SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, in the hottest region, arising from:

- particle rate : O(100Hz) / cm^2 (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm² SiPM by FBK**:

(quoting R.Malaguti, L.Milano test results in Ferrara)

@ 0.5pe threshold

- @ 25°C, 34.4V: ≈ 360kHz
- @ 5°C, 33.8V: ≈ 128kHz

@ 2.5pe threshold

- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm² is also being considered)

!!! We need to have, on each processing channel, one comparator with a low threshold (0.5pe? 1.5pe? Only prototype test will tell) → it's TDC input will see the highest rate.

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≤ 1MHz per TDC input !!!

Proposal of readout electronics for the SuperB IFR detector : TIMING mode readout

SuperB-IFR numerology:

A "Hit" rate of 1MHz per channel is compatible with the input and output rate of the TDC_GPX or the CERN HPTDC

BUT:

if we don't do L1 trigger matching on board

if we do L1 trigger matching on board

NEXT PAGE

Assuming that:

- "Hits" are packed into **FRAMES collecting all hits recorded in a time-slice of, say, 6.4us**
- Each FRAME contains:
  - Header = Board ID + Frame ID (allows to reconstruct ABSOLUTE timing for hit records) : 12 Byte
  - Channel ID + hit timing information RELATIVE to beginning of frame : 4 Byte per Hit
  - Trailer = WordCount + CRC : 4 Byte
- On each TDC half of the channels has a 1MHz input rate and half has a 500KHz input rate

  → we can expect, for a 64 channel TDC card, an **average** frame size of:

  <Frame size> = 12 + (6.4 hit * 32 + 3.2 hit * 32) * 4 + 4 ≈ 12 + 320 * 4 + 4 ≈ **1.3kB**

A.C.R. 2009-02-13

Each 64 channel TDC card would produce a sustained stream of (on average) :

<Bandwidth per 64ch TDC> = 1.3kB / 6.4us ≈ **200MB/s**

→ it would need a 5Gbps link to the downstream buffers !!!

A.C.R. 2009-02-13

Proposal of readout electronics for the SuperB IFR detector : TIMING mode readout

SuperB-IFR numerology:

From previous slide

if we do L1 trigger matching on board

Assumptions on L1 trigger rate and window:

- L1 trigger at fixed latency with respect to the event (our preferred option): latency in the order of 10us
- L1 trigger rate : 150KHz (*)
- L1 trigger window : 1us (*)

(*) (quoting "Electronics, trigger and DAQ for SuperB.", D. Breton, U.Marconi, Feb. 11 2009)

NOTE: **if a fixed latency trigger is adopted** it might be convenient to use the HPTDC ASICs which have internal trigger matching resources instead of the TDC-GPX which would require intense parallel processing to provide primary storage and perform trigger matching off-chip.

To roughly estimate of the "trigger matched" output bandwidth from a 64 channel TDC card one could assume a reduction factor of: (1/150KHz) / 1us = 6.(6)

Each 64 channel TDC card would produce a "TRIGGER MATCHED" sustained stream of (on average) :

<Bandwidth per 64ch TDC> = 200MB/s / 6.(6) ≈ 30MB/s

(it would be less if we could implement:

- D.Breton's scheme to handle the "overlap" of trigger requested data
- the BhaBha veto)

→ **a 1Gbps link to the downstream buffer would be adequate**

A.C.R. 2009-02-13

Front End Electronics for the SuperB IFR prototype and detector development

Summary

- Front end electronics R&D and test results
- Outline of readout electronics for the SuperB IFR prototype
- Outline of readout electronics for the SuperB IFR detector : TIMING mode readout
- **Outline of readout electronics for the SuperB IFR detector : BINARY mode readout**
- Outline of readout electronics for the SuperB IFR detector : summarizing

Proposal of readout electronics for the SuperB IFR detector : BINARY mode readout

SuperB-IFR numerology:

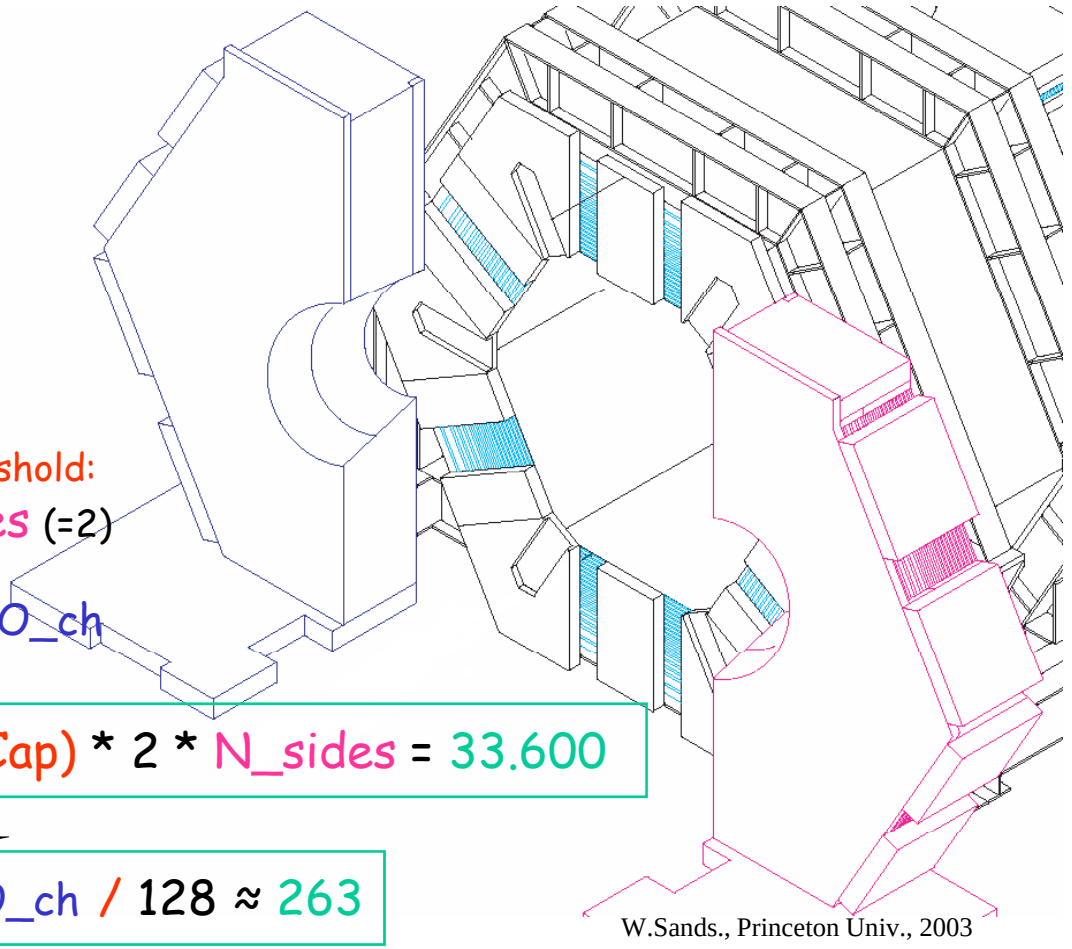
- Barrel: N_Barrel = 3600
- EndCaps: N_EndCap = 2400 + 2400

(quoting G. Cibinetto)

Assuming:

- the number of (thin) scintillators doubles (for X-Y readout; it's a coarse estimate)
- readout in BINARY mode with single threshold:
- each scintillator is readout from N_sides (=2) ends

-> total number of BiRO channels: N_BiRO_ch



W.Sands., Princeton Univ., 2003

$$N\_BiRO\_ch = (N\_Barrel + N\_EndCap) * 2 * N\_sides = 33.600$$

$$N\_BiRO\_Board = N\_BiRO\_ch / 128 \approx 263$$

It is possible that construction / dead space constraints will result in :

N_sides = 1

at least for part of the scintillators but let's now consider the full number

Proposal of readout electronics for the SuperB IFR detector : BINARY mode readout

SuperB-IFR numerology:

"Physics" rate : **500kHz**/channel, in the hottest region, arising from:

- particle rate : O(100Hz) / cm^2 (including background)
- dimensions of a detector element : < 400cm x 4cm (thickness 20mm)

(quoting R.Calabrese, W.Baldini, G.Cibinetto)

"Dark count" rate : **for a 1mm^2 SiPM by FBK**:

(quoting R.Malaguti, L.Milano test results in Ferrara)

@ 0.5pe threshold

- @ 25°C, 34.4V: ≈ 360kHz
- @ 5°C, 33.8V: ≈ 128kHz

@ 2.5pe threshold

- @ 25°C, 35V: ≈ 20kHz
- @ 5°C, 34V: ≈ 6.3kHz

!!! The "dark count" rate scales with the sensor's area and we don't know yet which would be the final area of the sensor of choice (a 4mm^2 is also being considered)

!!! We need to have, on each processing channel, just one comparator with a 2.5pe threshold

→ The dark count rate @ 2.5pe threshold is just a fraction of the physics rate

Let's consider a "Hit" rate of:

Hit_rate = physics_rate + dark count_rate ≈ 600kHz per BiRO input

Proposal of readout electronics for the SuperB IFR detector : BINARY mode readout

SuperB-IFR numerology:

A Hit_rate of 600kHz per channel will be processed by an FPGA which will sample the input pulses and provide temporary storage for the samples

LET's ASSUME:

- 20ns minimum pulse width from the Front End discriminators → dead time of 1.2% for a 600kHz rate
- FPGA sampling clock of 56.25MHz

A.C.R. 2009-02-13

if we don't do L1 trigger matching on board ← SO: → if we do L1 trigger matching on board

NEXT PAGE

Assuming that:

- "Hits" are packed into **FRAMES collecting, say, 256 samples of all 128 inputs corresponding to a time-slice of ≈** 4.55us
- Each FRAME contains:
  - Header = Board ID + Frame ID (allows to reconstruct ABSOLUTE timing for hit records) : 12 Byte
  - Channel ID + Sample ID for which the "Hit" was found : 2 Byte per Hit

  (**this implies that the FPGA performs ZERO SUPPRESSION: only address of active channels for each sample are recorded: to be tested**)
  - Trailer = WordCount + CRC : 4 Byte
- We can expect, for a 128 channel BiRO Front End Card, an **average** frame size of:

  <Frame size> = 12 + <2.73> hit * 128 * 2 + 4 ≈ 12 + 350 * 2 + 4 ≈ **0.72kB**

A.C.R. 2009-02-13

128 channel BiRO Front End Card would produce a sustained stream of (on average) :

<Bandwidth per 128ch FE_BiRO> = 0.72kB / 4.55us ≈ **160MB/s**

→ it would need a 5Gbps link to the downstream buffers !!!

A.C.R. 2009-02-13

Proposal of readout electronics for the SuperB IFR detector : BINARY mode readout

SuperB-IFR numerology:

From previous slide

if we do L1 trigger matching on board

Assumptions on L1 trigger rate and window:

- L1 trigger at fixed latency with respect to the event (our preferred option): latency in the order of 10us
- L1 trigger rate : 150kHz (*)
- L1 trigger window : 1us (*)

(*) (quoting "Electronics, trigger and DAQ for SuperB.", D. Breton, U.Marconi, Feb. 11 2009)

To roughly estimate of the "trigger matched" output bandwidth from a 128 channel FE_BiRO one could assume a reduction factor of: (1/150KHz) / 1us = 6.(6)

Each 128 channel FE_BiRO card would produce a "TRIGGER MATCHED" sustained stream of (on average) :

<Bandwidth per 128ch FE_Biro> = **160MB/s** / 6.(6) ≈ **24MB/s**

(it would be less if we could implement:

- D.Breton's scheme to handle the "overlap" of trigger requested data
- the BhaBha veto)

→ **a 1Gbps link to the downstream buffer would be adequate**

A.C.R. 2009-02-13

Front End Electronics for the SuperB IFR prototype and detector development

Summary

- Front end electronics R&D and test results
- Outline of readout electronics for the SuperB IFR prototype
- Outline of readout electronics for the SuperB IFR detector : TIMING mode readout
- Outline of readout electronics for the SuperB IFR detector : BINARY mode readout
- **Outline of readout electronics for the SuperB IFR detector : summarizing**

Proposal of readout electronics for the SuperB IFR detector : summarizing

TIMING mode readout

number of TDC_board ≈ 525

Channel per board = 64

Bandwidth per board

raw 200MB/s

trigger matched 30MB/s

BINARY mode readout

number of BiRO_Board ≈ 263

Channel per board = 128

Bandwidth per board

raw 160MB/s

trigger matched 24MB/s

ensured that the on-board FPGA can performs the on-line Zero Suppression mentioned above, the binary mode readout FEE should be less expensive than the timing mode readout of a factor ≈ 4

but

- input deadtime ≈ 1.2%
- detector construction more complex and with more dead areas due to fiber routing