SVT organization for TDR

1.Major decisions needed and R&D required to make them.

- Layer 0 technology:
  - Hybrid Pixel: Want to demonstrate that reduction in the front-end pitch to 50x50 μm2 and in the total material budget is possible to meet Layer0 requirements. Working on a plan to test this option with beam Sep. 2010.
  - CMOS MAPS: Plan to build a multichip CMOS MAPS prototype module with specs close to the SuperB Layer0 requirements → Testbeam in 2010.
  - All the module components could be the same for a Layer0 module based on MAPS/Hybrid Pixels
  - Striplets: evaluate real limit of FSSR2 speed with high background.

2. Manpower in place and still required

- Still Working on a better estimate of manpower for TDR
  - Old estimate: Phy~6 FTE(~4 avail.), Mech Eng.~ 4 FTE (< 2 avail.), Electr. Eng. ~ 6 FTE (<4 avail.)
- Layer0 activities somehow covered
- External layer design: interest from some groups but lack of manpower and activities not yet started (no real commitments yet).
- Mechanics: long list of activities but < 2 FTE involved

SVT organization for TDR

3. Milestones (very preliminary)

- May '09: finalize readout architecture for MAPS & Hybrid pixel front-end chips
- Sept-Nov '09 chips submission
- Sept '09 high resistivity pixel sensor production
- Jan - July 2010: lab test (sensor/front-end chip/MAPS) → bump bonding hybrid pixel / MAPS module assembly → lab test
- Sep 2010: testbeam

				start	end	d
1.1	Hybrid pixels					
1.1.1	front-end chip					
	optimization readout arch			1-Feb	Apr-09	
	design analog cell			1-Apr	May-09	
	VHDL			1-May	Jun-09	
	layout			1-May	Sep-09	
	production			Sep-09	Jan-10	
	test			Feb-10	Mar-10	
1.1.2	sensor					
	design			Jul-09	Aug-09	
	production			Sep-09	Dec-09	
	test			Jan-10	Feb-10	
1.1.3	chip+sensor					
	interconnection			Mar-10	Apr-10	
	test			May-10	Jul-10	
1.1.4	testbeam			Sep-10		

4. Status of WBS planning

- Major activities defined
- Need to fill in manpower
- Iteration with Institutions

WBS	Item	Required Man-months (2 yea			
		Phy	Eng	Tecn	Comp
1	SVT (TDR)				
1.1	**Design optimization**				
1.1.1	detetctor geometry optimization				
1.1.1.1	FastSim implementation				
1.1.1.2	Physic Study				
1.1.2	background studies				
1.1.2.1	Geometry implementation				
1.1.2.2	SVT rate				
1.2	**Mechanics**				
1.2.1	L0				
1.2.1.1	Module support and cooling design/simulation/test				
1.2.1.2	Full layer0 design				
1.2.2	L1-L5				
1.2.2.1	Module support and cooling design				
1.2.2.2	Full L1-L5 support design				
1.2.3	Beam Pipe design				
1.2.4	Mech integration (fast dismounting design)				
1.2.5	Mechanical System Engineer				
1.3	**Electronics & Sensor**				
1.3.1	Hybrid Pixels				
1.3.1.1	Sensor design/test				
1.3.1.2	FE analog optimization				
1.3.1.3	FE chip layout				
1.3.1.4	FE chip testboard design/construction/chip mounting				
1.3.1.5	FE chip test				
1.3.1.6	FE chip + sensor bump bonded test				
1.3.2	MAPS				
1.3.2.1	FE analog-sensor optimization				
1.3.2.2	MAPS readout architecture (VHDL				
1.3.2.3	MAPS chip layout				
1.3.2.4	MAPS chip testboard design/construction/chip mounting				
1.3.2.5	MAPS chip test				
1.3.3	Pixel Module design electronics				
1.3.3.1	Pixel bus				
1.3.3.2	HDI				
1.3.4	Prototype MAPS module				
1.3.4.1	Pixel bus test				
1.3.4.2	HDI				
1.3.4.3	Module Integration				
1.3.4.3	Module lab test				
1.3.5	Radiation damage MAPS chip				
1.3.6	Striplets				
1.3.6.1	FSSR2 speed evaluation				
1.3.6.2	multilayer interconnection				
1.3.7	L1-L5				
1.3.7.1	Sensors				
1.3.7.2	FE chips evaluation				
1.3.7.3	HDI				
1.3.7.4	Prototype module production ???				
1.3.6	DAQ+trigger				
1.3.7	Power Distribution				
1.3.8	Electrical System Engineer				
1.4	**Detetctor Monitoring & Interlocks**				
1.5	**Testbeam**				

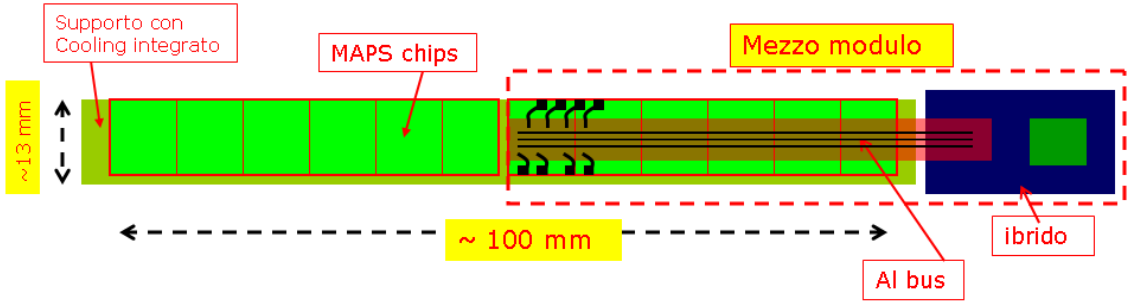
SVT Activities for TDR (I)

Activities now more focused on TDR preparation (end of 2010)

Some R&D still needed for Layer 0:

- Plan to build a multichip CMOS MAPS prototype module with specs close to the SuperB Layer0 requirements → Testbeam in 2010.
  - All the module components could be the same for a Layer0 module based on Hybrid Pixels.

Activity funded by INFN. Institutions: Bologna, Milano, Pavia/Bergamo, Pisa, Roma III, Torino, Trieste.



- Hybrid Pixel: more emphasis now on this option: it could become the baseline Layer0 option for the TDR in case MAPS are not considered mature enough by that time.
  - Need to demonstrate by 2010 that reduction in the front-end pitch to 50x50 μm^2 and in the total material budget is possible to meet Layer0 requirements.
- Striplets: continue to evaluate the use of FSSR2 readout chip and light interconnections from sensor to front-end

SVT Activities for TDR (II)

Background Simulation:

- This set the scale for requirements on Layer0 and the inner SVT Layers.

External Layers Design

- Technology is not an issue
- Need to optimize the geometry with Fast Simulation (D. Brown's talk)
- Need to evaluate the best front-end chip for strip modules among the ones "on the market" (FSSR2…)

Off Detector electronics and DAQ Development

- (M. Citterio, M. Villa's talk)

Mechanics:

- Beam-pipe design
- Light support and cooling for Layer0 modules (F.Bosi's talk)
- Module design for the external Layers
- Design the full SVT support structure (want to have the Layer0 easily accessible for replacement). Important interplay with IR design.

- A significant amount of work is needed for the TDR and not all listed activities are well covered.