Electronics/DAQ/trigger

- We wrote a first version of the document describing the base of the architecture we want to set up for SuperB, and it will be the template used for the TDR.
  - We already started to enrich and refine it!

- During this workshop, we started drawing a draft of the general architecture of the electronics/DAQ/trigger system:
  - We are looking for the best solution for the clock distribution, taking radiation into account => we will work on developing our own solution for the links
    - It has to be simple and safe
    - Requirements for control and readout links are different
    - We found commercial chips that could fit the different functions
  - We refined the DAQ-linked part of the FEE with the mezzanine option in mind
  - We started to think of a flexible but common and standard solution for the pre-processing board
    - Each sub-detector would be able to put its own firmware inside the board's FPGA for performing noise filtering, feature extraction, data compression, etc.
  - We wish to build the HLT by means of PC clusters performing both the event building and the event selection

Organisation for TDR

- Clock and control distribution needs R&D!
  - Manpower in place should be able to make it for FEE/DAQ for the first TDR phase

- But the L1 is still uncovered
  - We will start looking for collaborators taking care of this issue, especially the L1 processors
  - Particular attention has to be given to the transmission of calorimeter data towards the L1 calorimeter processor because on BABAR calorimeter electronics was untriggered
  - We consider the front-end part of the L1 trigger (building up the primitives) in charge of the sub-detector teams

- We will soon summarize the brainstorming done here in an upgraded version of our document.
  - We will set up an electronics mailing list
  - We aim at getting feedback from you
  - We have already foreseen to have an external review about this proposal

- We will go on with regular technical meetings to cover all the items.