

FDIRC tests in the SLAC cosmic ray telescope

J. Va'vra, SLAC

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FDIRC

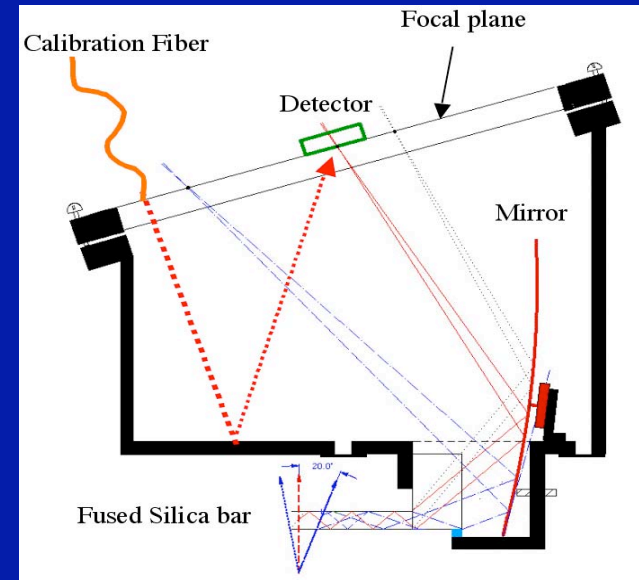
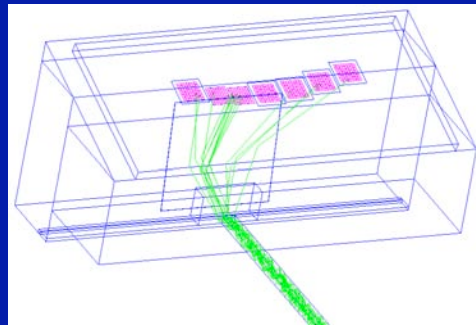
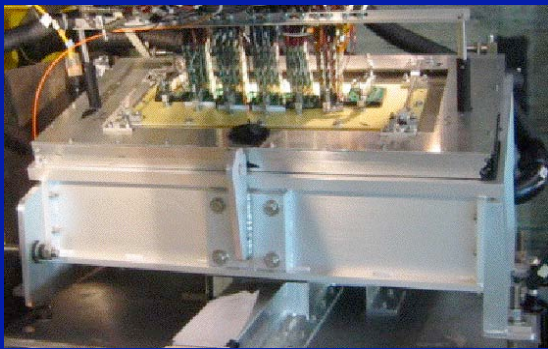
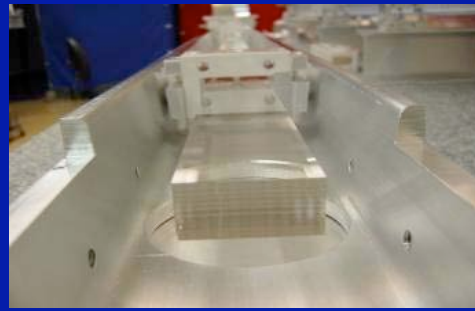
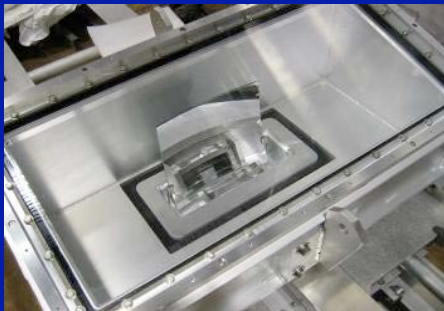
- **Successfully tested in the SLAC test beam:**

- J. Benitez, I. Bedajane, D.W.G.S. Leith, G. Mazaheri, B.N. Ratcliff, K. Suzuki, J. Schwiening, J. Uher, and J. Va'vra, "Development of a Focusing DIRC," IEEE Nucl. Sci., Vol. 3, pp. 1550-1556, Conference Record, October 2006, and SLAC-PUB-12236.
- J. Va'vra, J. Benitez, D.W.G.S. Leith, G. Mazaheri, B. Ratcliff, J. Schwiening, and K. Suzuki, "The Focusing DIRC – the first RICH detector to correct the chromatic error by timing, and the development of a new TOF detector concept," Presented at Vienna conference on Instrumentation, February 19, 2007, Vienna, Austria, September 2007, SLAC-PUB-12803.
- J. Benitez, D.W.G.S. Leith, G. Mazaheri, B.N. Ratcliff, J. Schwiening, J. Va'vra, L. Ruckman, G. Varner, "Status of fast focusing DIRC (fDIRC)," Nucl. Inst. & Meth., A595(2008)104-107.
- J. Va'vra, "Simulation of the Focusing DIRC Optics with Mathematica," Presented at IEEE in Dresden in 2008, SLAC-PUB-13464. October, 2008; IEEE conference records.

- **FDIRC main points:**

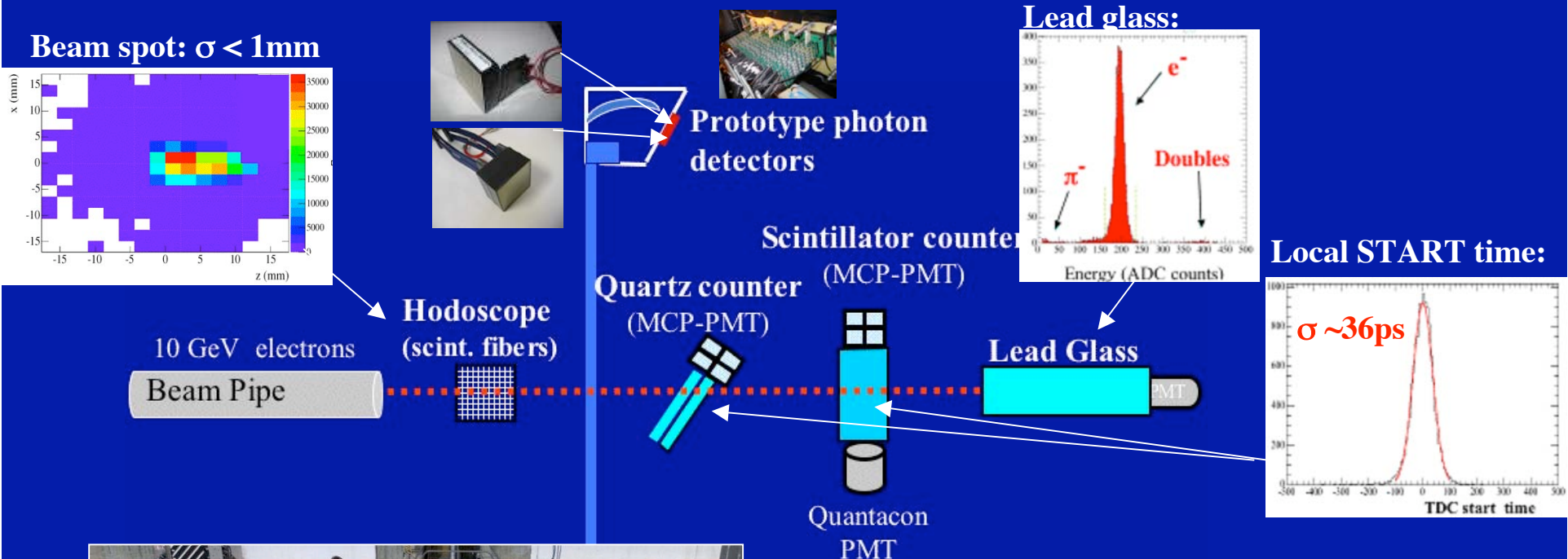
- Its "pixel imaging quality" is the same as that of BaBar DIRC - the same σ_θ
- However, it is ~10x faster than BaBar DIRC =>
 - => can correct chromatic error by timing,
 - => less sensitive to background.
- Its "detector canvas" size is ~2x smaller than a non-focusing DIRC with similar detector concept.

Focusing DIRC Prototype Optics

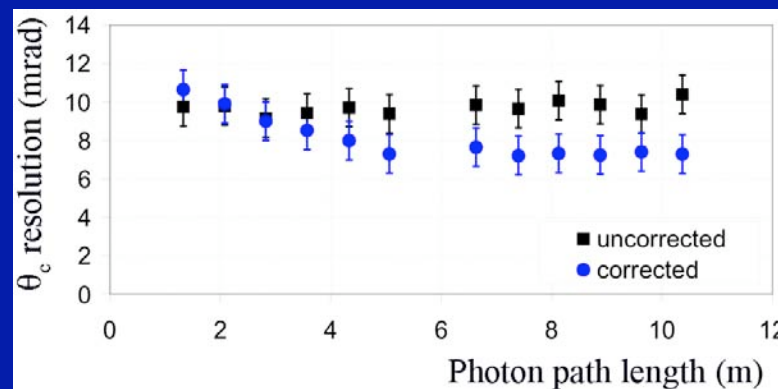


- **Radiator:**
 - 1.7 cm thick, 3.5 cm wide, 3.7 m long fused silica bar (spares from BABAR DIRC).
- **Optical expansion region:**
 - filled with a mineral oil to match the fused silica refraction index (KamLand oil).
 - include optical fiber for the electronics calibration (PiLas laser diode).
- **Focusing optics:**
 - a spherical mirror with 49 cm focal length focuses photons onto a detector plane.

Focusing DIRC Prototype beam test (T-492)



Effect of the chromatic correction by timing:



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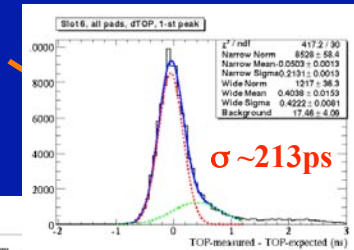
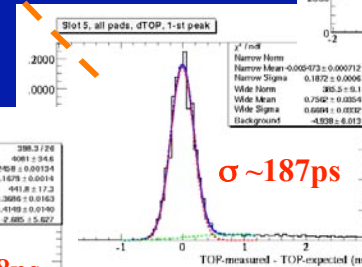
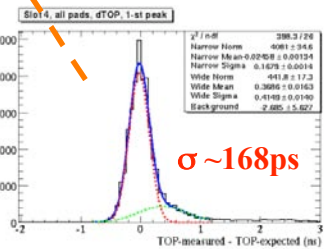
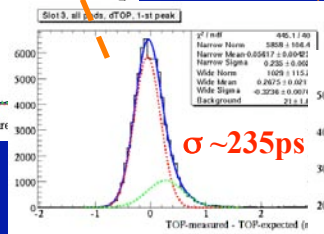
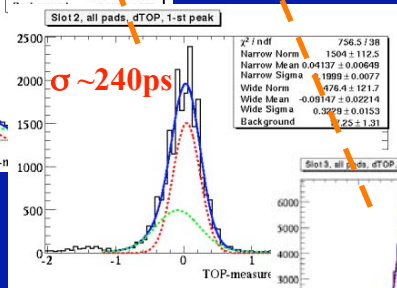
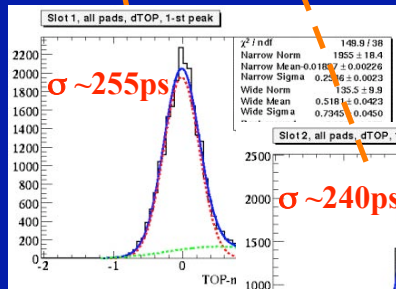
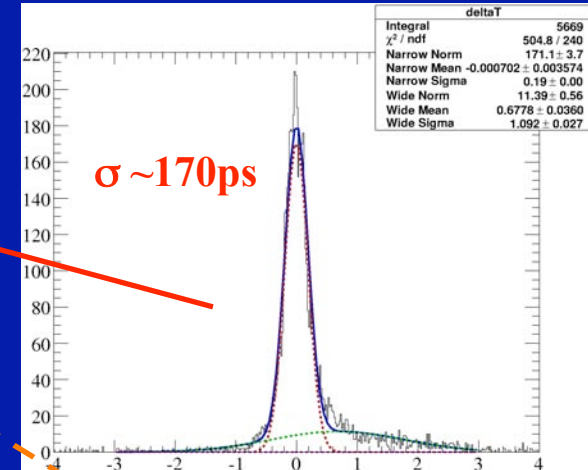
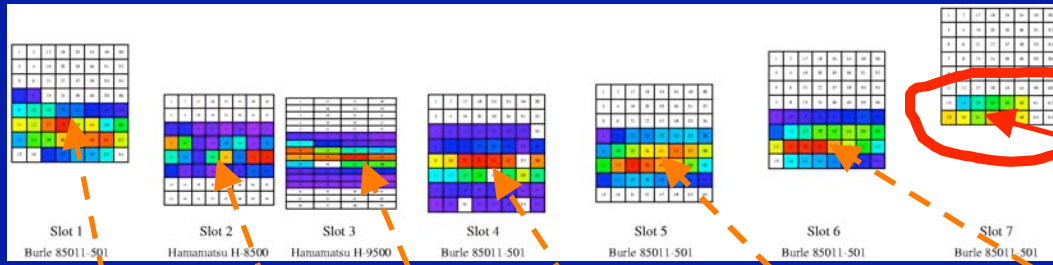
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Photon path length (m) 4

Beam test results at SLAC:

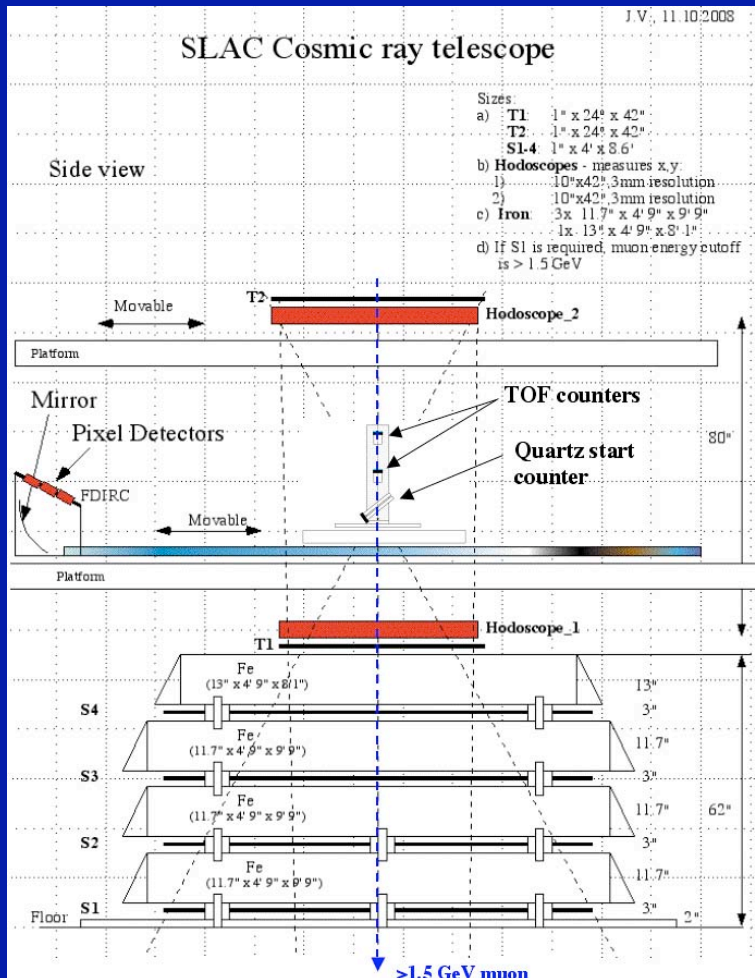
(Compare the CFD/Philips TDC timing (slots 1-6) with a new waveform digitizing method using BLAB1 chip - slot 7)

New BLAB-based Readout (slot 7, pad 15):



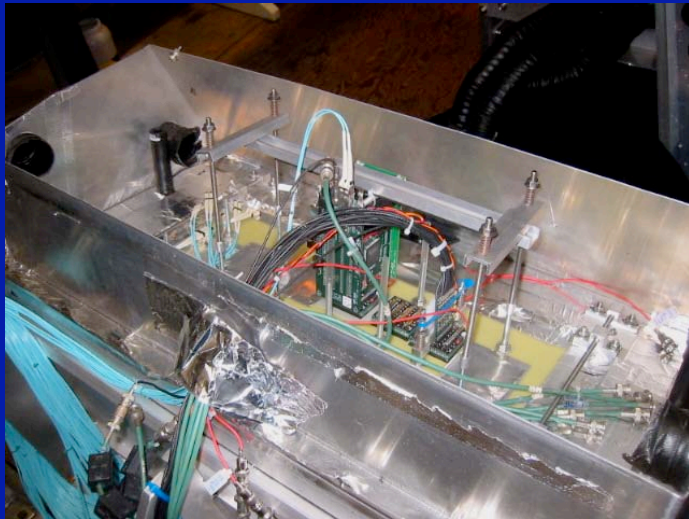
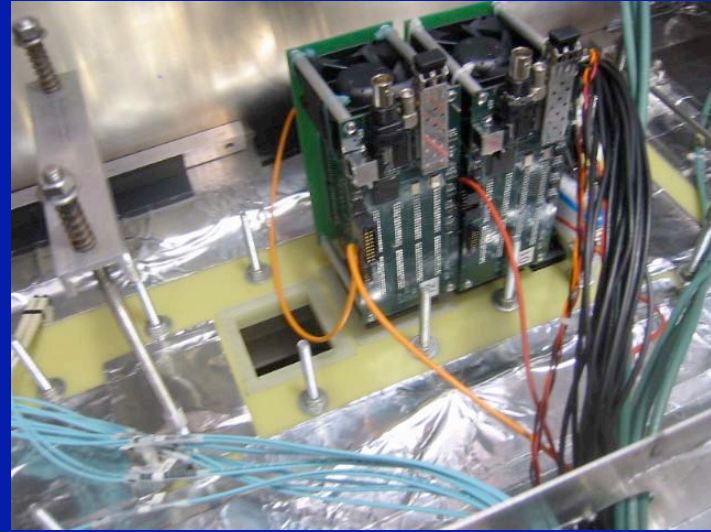
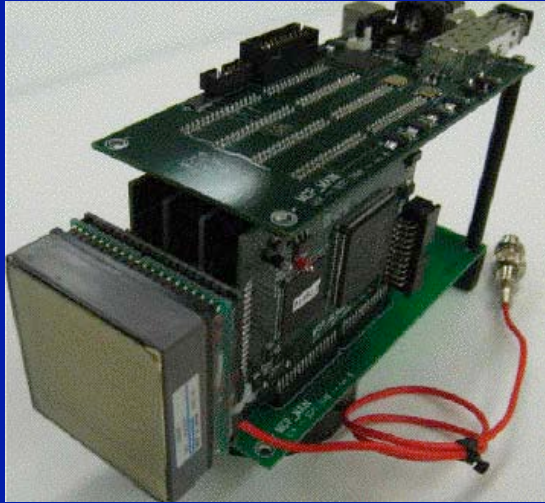
Based on promising results we decided to upgrade all channels to new BLAB2 electronics

SLAC cosmic ray telescope - our "test beam" for the next 1-2 years



- **~ 4 feet of iron (an old TPC magnet) \Rightarrow ~ 1.6 GeV muon energy cutoff**
- **Tracking resolution: ~1 mrad.**
- **Status: taking data with the 1-st Hawaii electronics package; 6 more in March.**

Test setup in the cosmic ray telescope



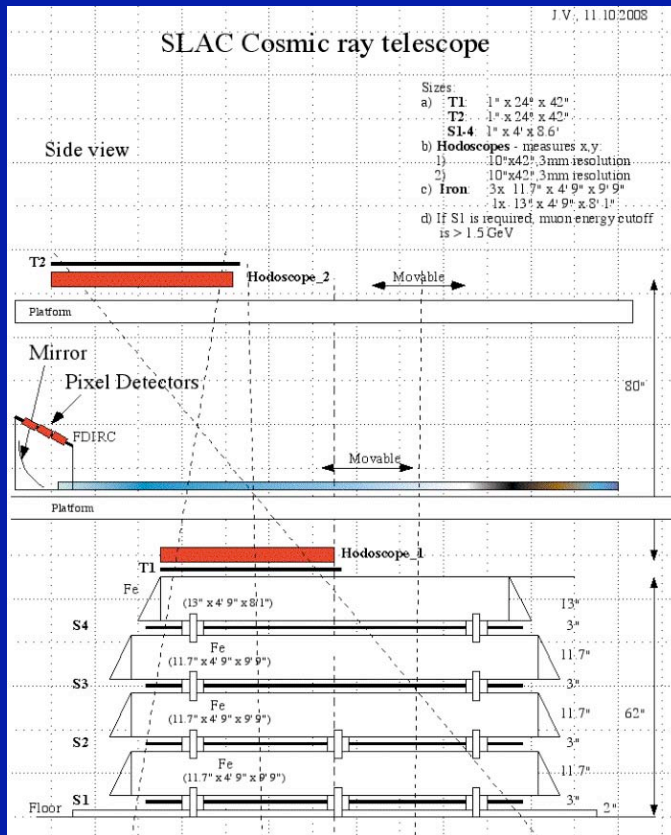
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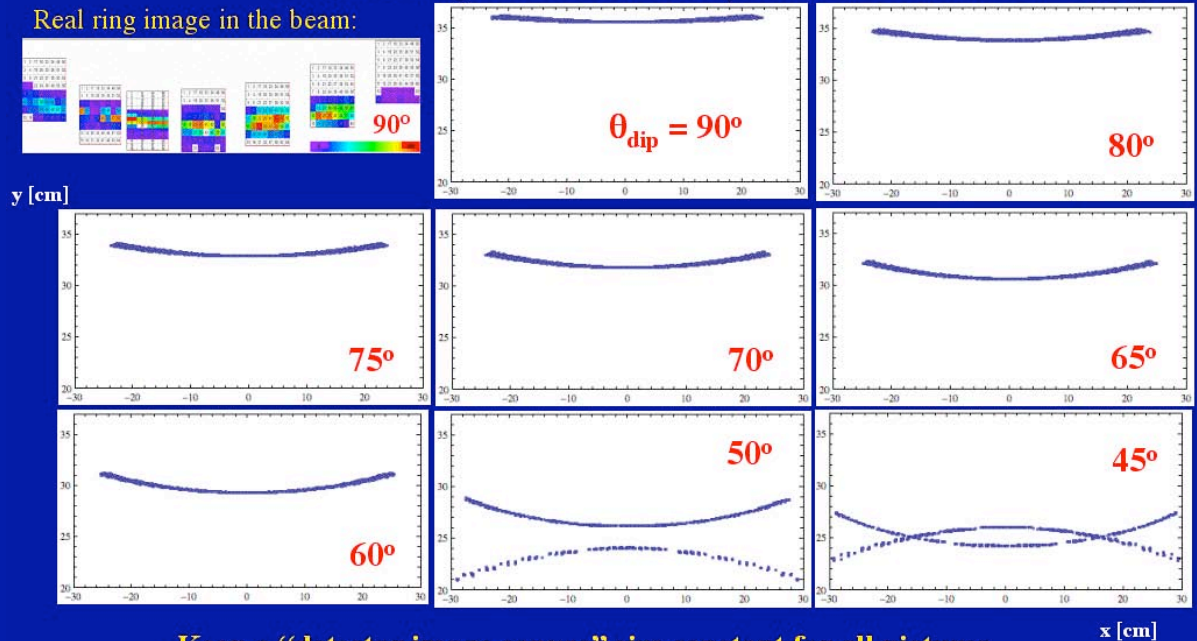
Images in the SLAC cosmic ray telescope

Side view:



Ring image simulation for FDIRC prototype with:
no wedge, spherical mirror, flat detector plane (vary θ_{dip})

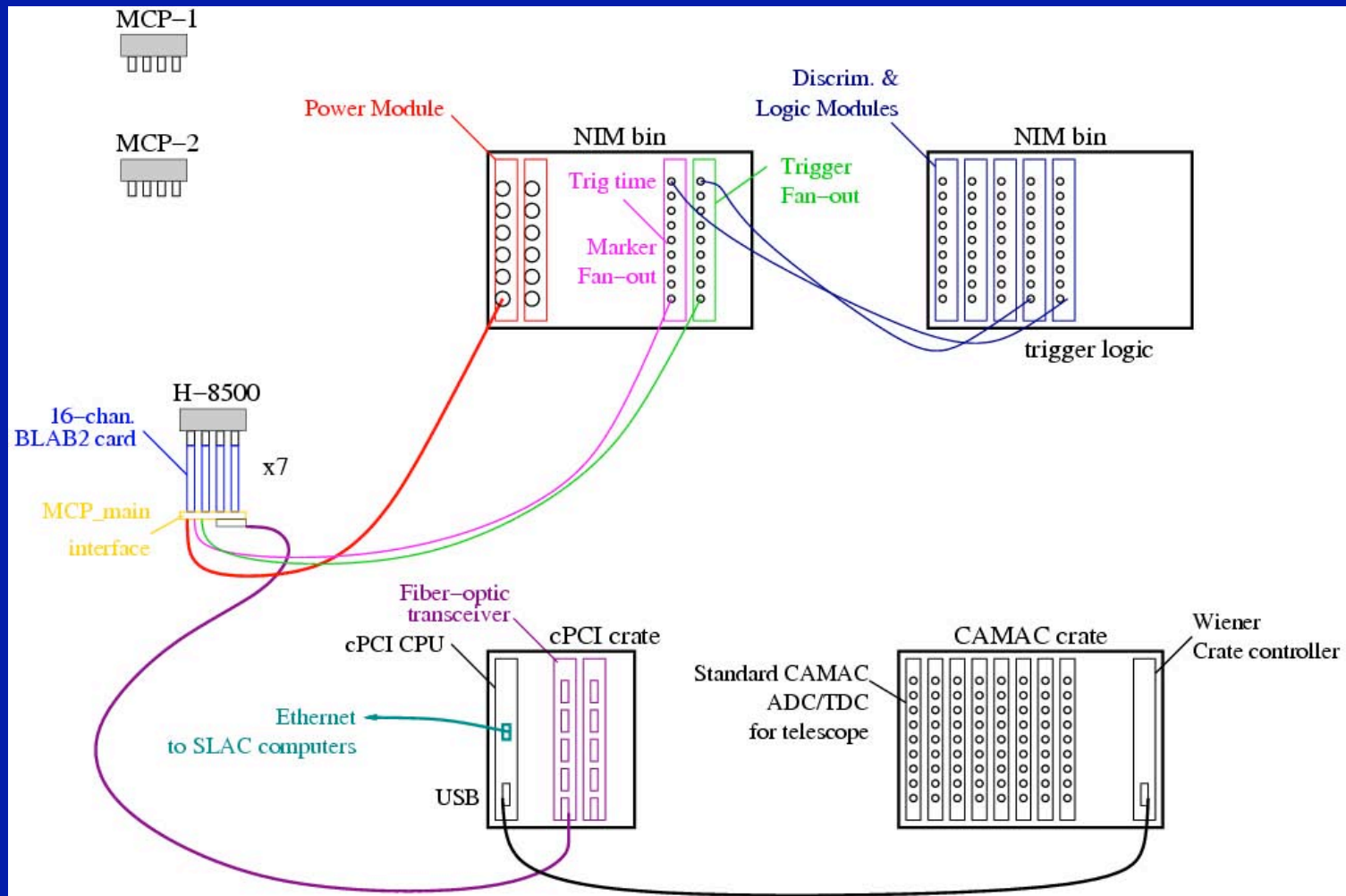
Calculated images in the flat detector plane located in the mirror's focus:



- Keep a "detector image canvas" size constant for all pictures

- Will start with a nominal position: $\theta_{dip} \sim 90^\circ$ & position # 3.
- Need to shift the detector plane to reach smaller dip angles (~ 1.8 cm/ 10° dip angle).
- With some modification we could reach, perhaps, $\theta_{dip} \sim 75^\circ$.

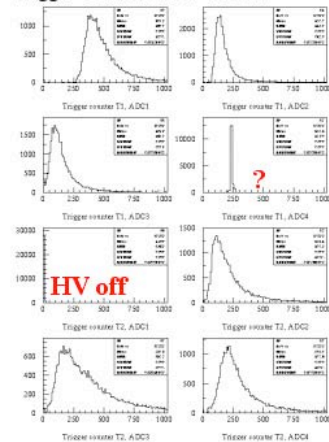
New readout configuration



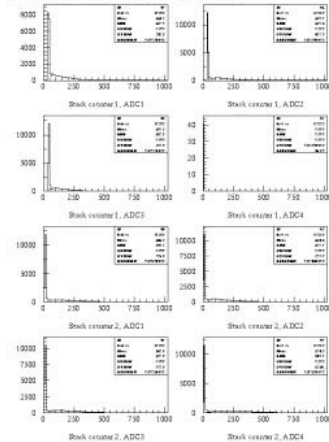
Cosmic ray telescope counters:

2) Linear scale now:

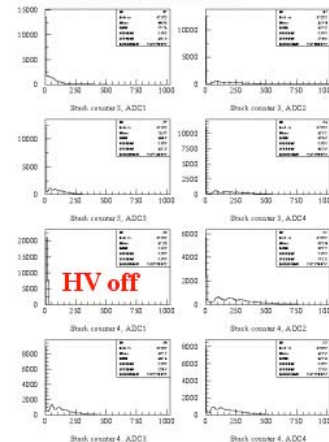
Trigger counters 1&2 ADCs:



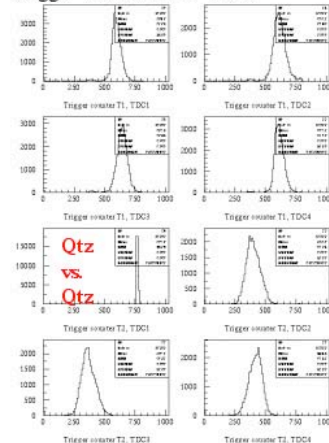
Stack counter 1&2 ADCs:



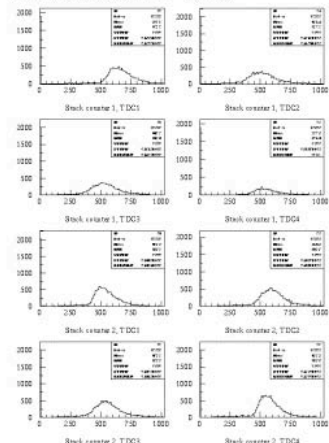
Stack counter 3&4 ADCs:



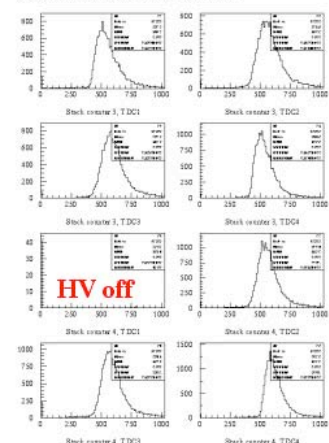
Trigger counters 1&2 TDCs:



Stack counter 1&2 TDCs:



Stack counter 3&4 TDCs:



- As one goes to lower stack counter number of TDC zeroes increases, as one would expect.

Trigger rates:

- $T1 * T2 \sim 5-6 \text{ Hz}$
- $T1 * T2 * S1 \sim 1-2 \text{ Hz}$
- $T1 * T2 * \text{Quartz_counter} \sim 5-6 \text{ k/day}$
- $T1 * T2 * S1 * \text{Quartz_counter} \sim 2-3 \text{ k/day}$

Note:

We use $T1 * T2 * \text{Quartz_counter}$ trigger

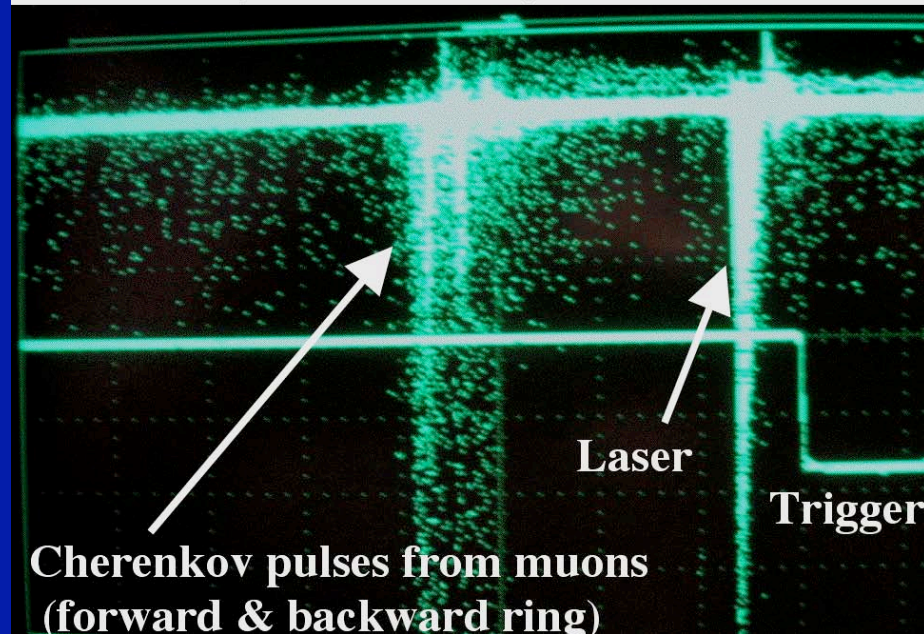
Status:

- Taking data
- CAMAC running
- BLABs need timing calibration

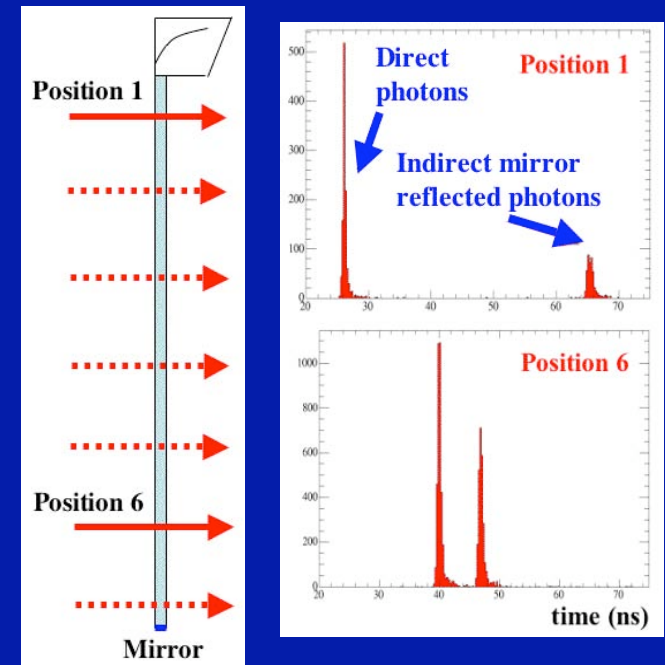
Monitoring of FDIRC in the telescope

On-line monitor:

100ns/div, 100mV/div, 500mV/div



Cherenkov photons in time domain



- See forward and backward part of the Cherenkov ring in time domain, the PiLas laser monitoring pulses and the BLAB2 trigger

The new Hawaii electronics

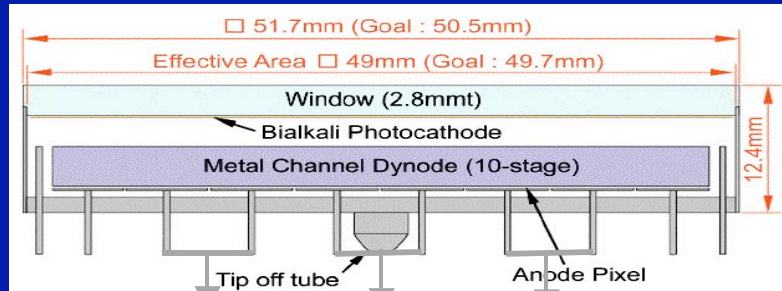


FDIRC electronics chain

Gary Varner, Larry Ruckman, Kurtis Nishima, and Andrew Wong, Nucl.Instrum.Meth. A591,534-545,2008

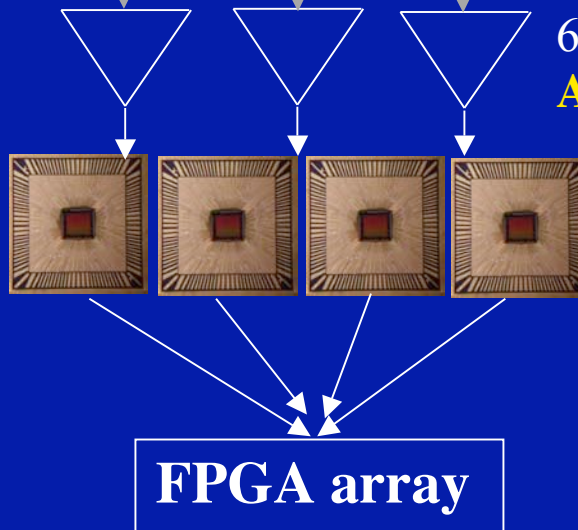
H-8500

MaPMT:



64 pixels, 8x8

**BLAB2
ASIC:**



64 Amplifiers/MaPMT,
Amp. gain ~ 40x

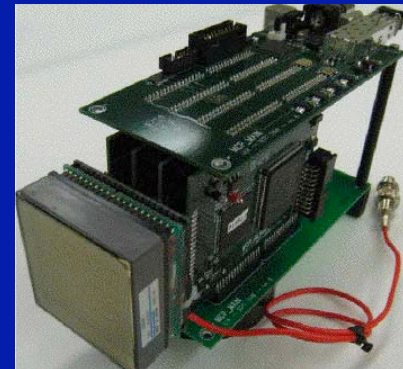
Waveform sampling electronics:

4 BLAB2 chips / MaPMT

Waveform sampling rate: ~ 2.5 GSa/s

Timing resolution goal: $\sigma_{\text{final}} \sim 150-170$ ps

Initial geometry:



Status:

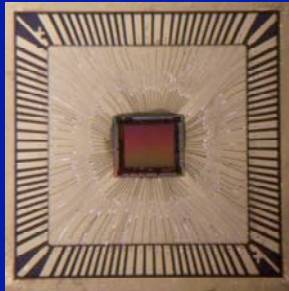
- One H-8500 is running in the telescope.
- Will have six more ready in March.

2/12/09

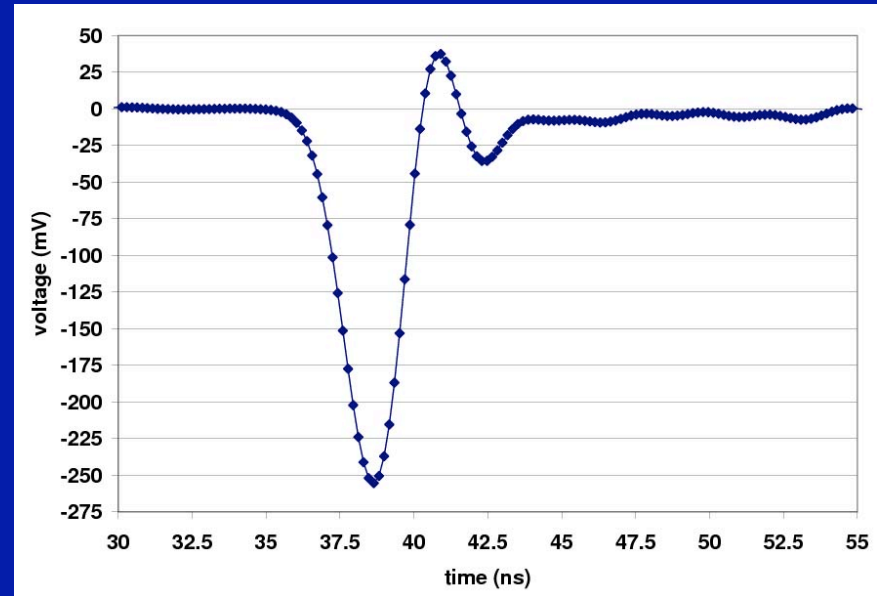
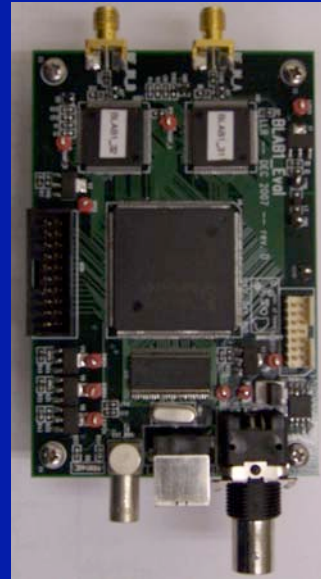
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telescope

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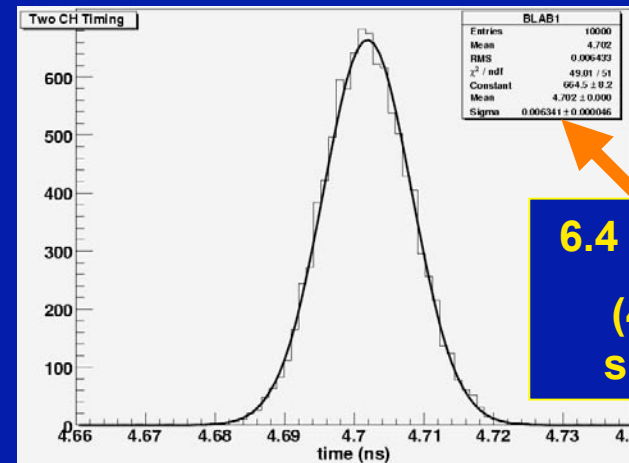
BLAB ASIC further studies



BLAB1 chip
Nucl.Instrum.Meth.
A591,534-545,2008,
and arXiv:0805.2225



- Comparable timing performance to best CFD + HPTDC methods
- MUCH lower power, no need for huge cable plant!
- Using full samples significantly reduces the impact of noise
- Photodetector limited



6.4 ps RMS
(4.5ps single)

Summary of BLAB2 ASIC parameters

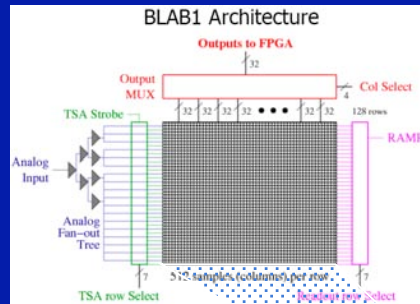
G. Varner

Parameter	Value
Samples	6 rows & 1024 samples
Triggering mode	Trigger on individual pixel
Analog BW of the present BLAB2 chip	~ 0.85 GHz
BLAB2 chip input impedance	30-80 Ω (adjustable)
Number of MaPMT pixels / BLAB2 ASIC	16
Number of BLAB2 ASICS / MaPMT (final vs. prototype)	2 - 4
Dynamic range	1mV / 1V
Cross-talk	< 0.1%
BLAB2 waveform sampling speed	1 - 10 GSa/sec
On chip ADC	1 GHz Wilkinson
Number of Wilkinson conversions in parallel	32
ADC resolution	10 bits
ADC conversion time for 10 bits	1 μ s
Number of words / event	32 - 512
Read time for 16 channels (1 BLAB2 chip) / event	16 μ s
Sustained readout speed	50 kHz
12 μ s latency accomplished by	Self-trigger & analog or digital storage
Cost per channel	< \$10 in volume

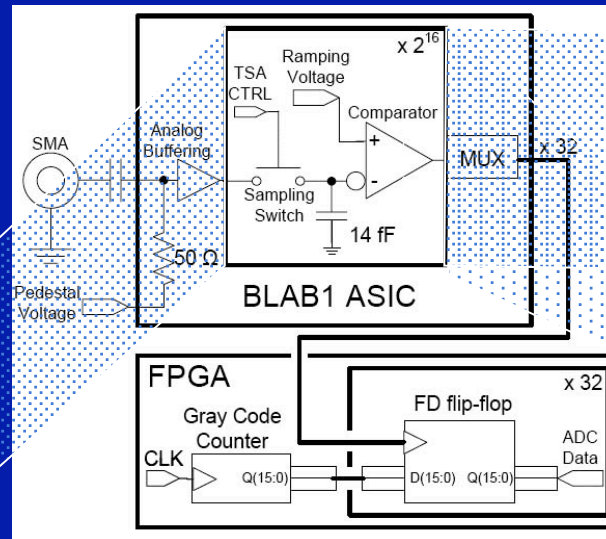
Details

Waveform sampling principle: Switched Capacitor Array

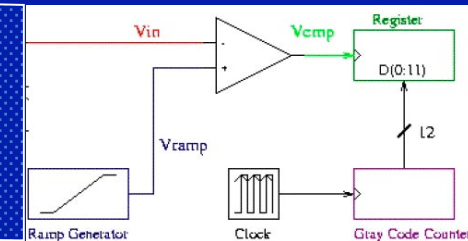
G. Varner, Larry Ruckmann and A. Wong, arXiv:0802.2278v1 [physics.ins-det], submitted to NIM, 2008



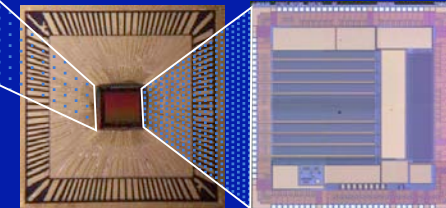
Capacitor array:



Wilkinson ADC:



BLAB2 ASIC:



Principle of waveform sampling in BLAB chip:

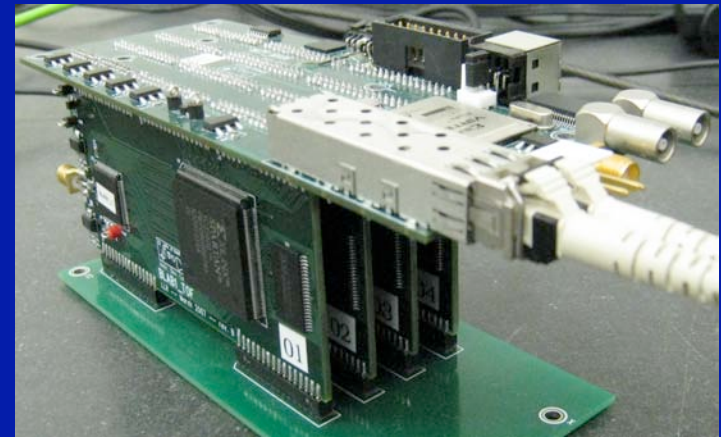
- Fast signal waveform is terminated in 50 Ω on the chip
- **BLAB2 ASIC:** 17ch & 6 rows & 1024 samples (102k storage cells)
- Each row can be independently addressed to initiate a storage cycle
- When analog switch is closed the instantaneous signal is stored on a 14 fF capacitor
- ADC conversion is done via the **Wilkinson method:**
Comparators done inside BLAB chip & high speed encoding done in FPGA
32 samples are converted in parallel
- 10-bits corresponds to a conversion time of 1 μ s in the current scheme.
- **Up to 10 GSa/s** (100ps sampling interval \Leftrightarrow \sim 5 samples on the leading edge); the present limit: 2.5GSa/s.
- **12 μ s latency:** (a) TOF: self-trigger and digital temporary storage
(b) FDIRC: analog storage

Highly Integrated Readout

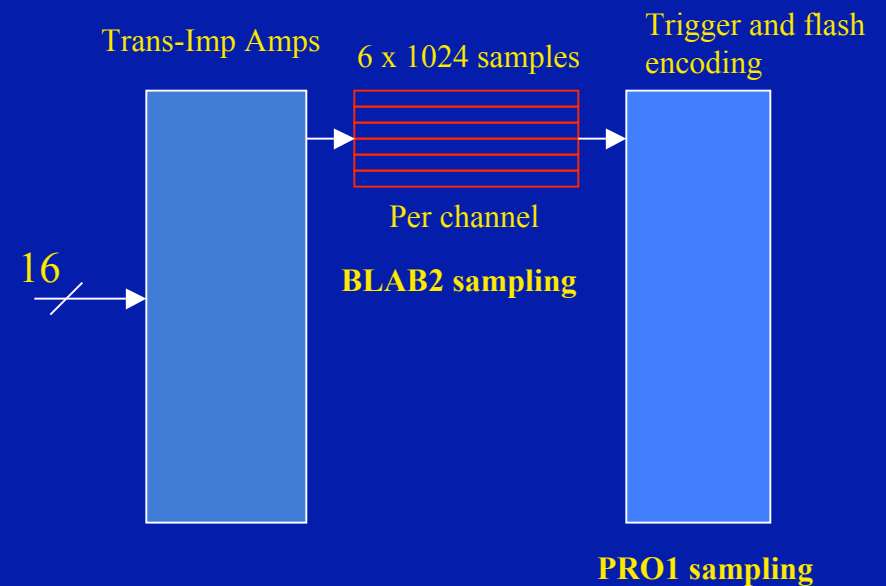
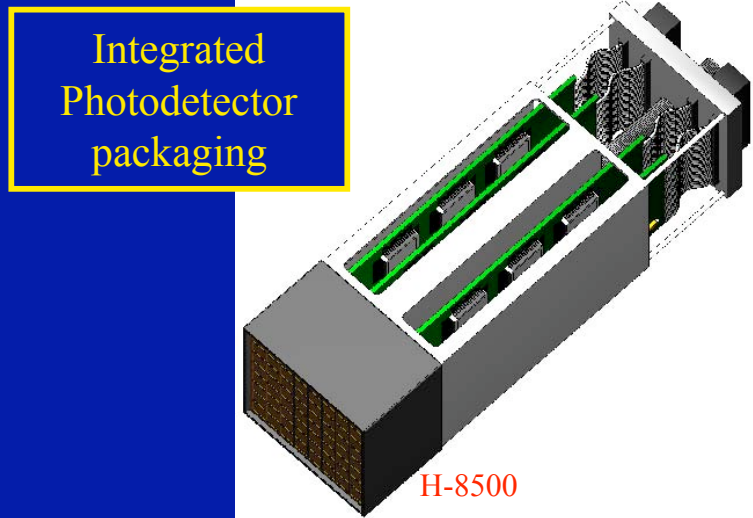
- **Buffered LABRADOR**

TABLE II: *BLAB2 ASIC Specifications.*

Item	Value
Photodetector Input Channels	16
Linear sampling arrays/channel	2 \rightarrow 6
Storage cells/linear array	512 \rightarrow 1024
Sampling speed (Giga-samples/s)	2.0 - 10.0
Outputs (Wilkinson)	32

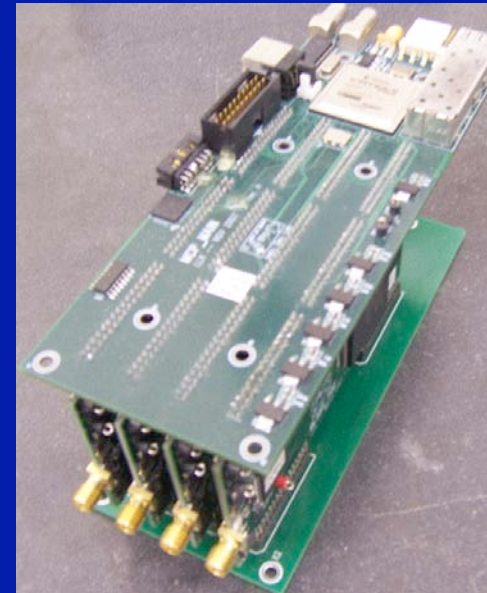
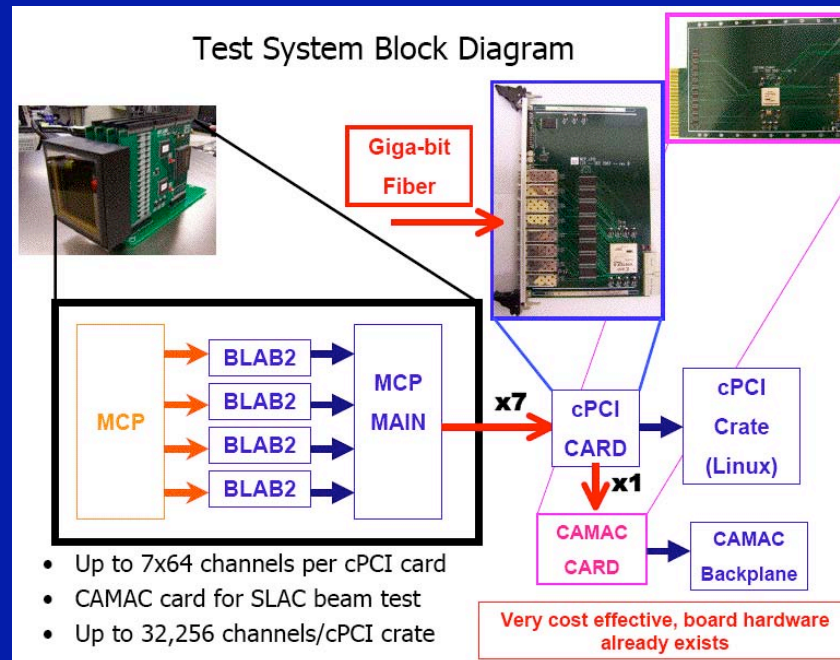


BLAB2 ASIC



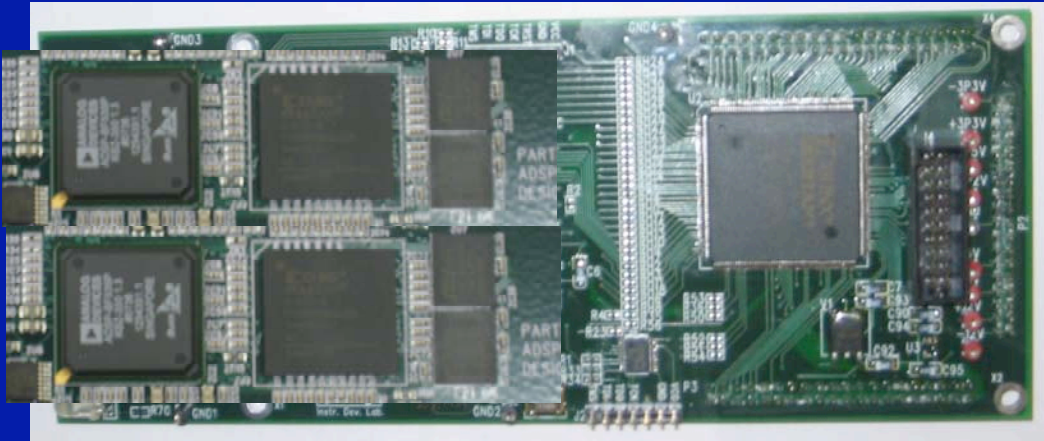
BLAB2 electronics for the next beam or cosmic ray tests at SLAC

Gary Varner & Larry Ruckman

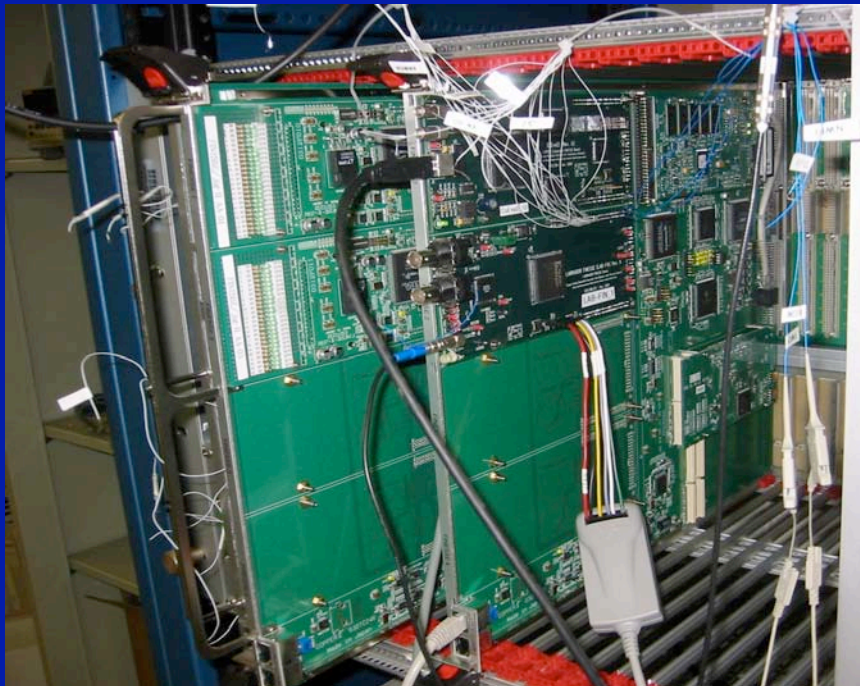


- Prototype boards with BLAB1 chip now exists; BLAB2 chip is almost ready and will be submitted to a foundry on June 2.
- To instrument all 64 pixels one needs 4 BLAB chips. That is what we want to have in the prototype in the fall. However, the final DIRC will very likely use 2 chips per MaPMT (2 pads ganged together, 32 pixels/MaPMT).
- Worry about a miniaturization later.

Readout Requirements



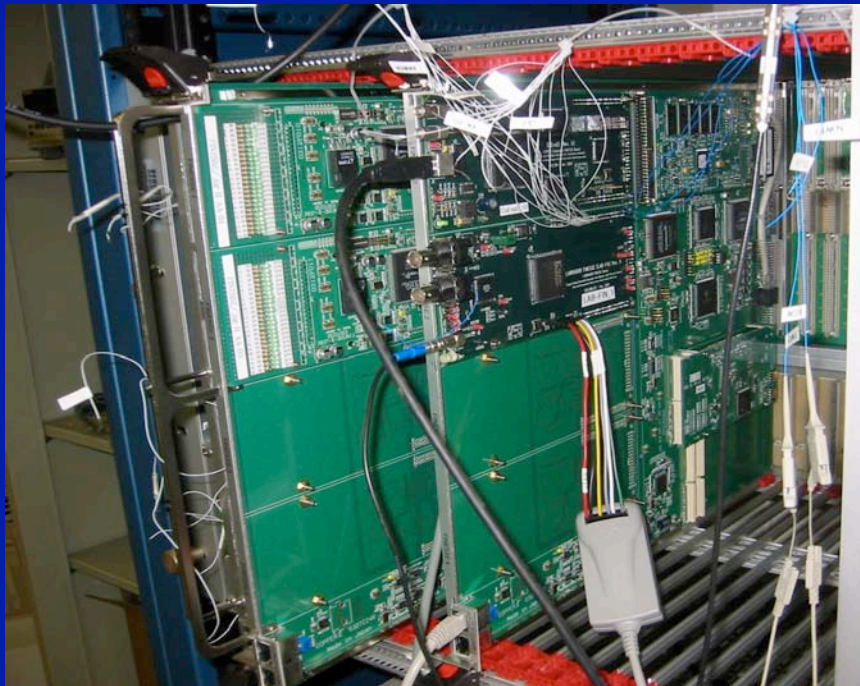
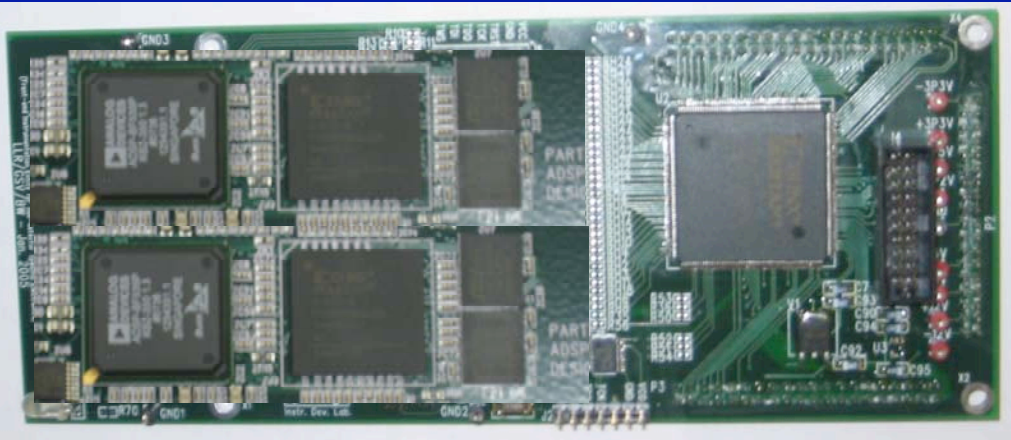
4x fiber pairs/FINESSE
(= 1 iTOP) module
2x dual Shark DSP/FINESSE



4 FINESSE/COPPER (2k chan)
8 COPPER Total
16k total system channels
Even less if use GaAs (4-channel PMTs)

8x COPPER-sized cards for trigger
collection/Trigger fan-out

Data volume estimate



Assume:
100kHz charged track hits on each bar
~32 p.e./track (1% of 100ns windows)
30kHz trigger rate
Each PMT pair sees $\langle 8 \rangle$ hits
240k hits/s
Each hit = 64samples * 8bits = 512bits
→ ~125Mbits/s
(link is 1.2Gb/s ~ x10 margin)

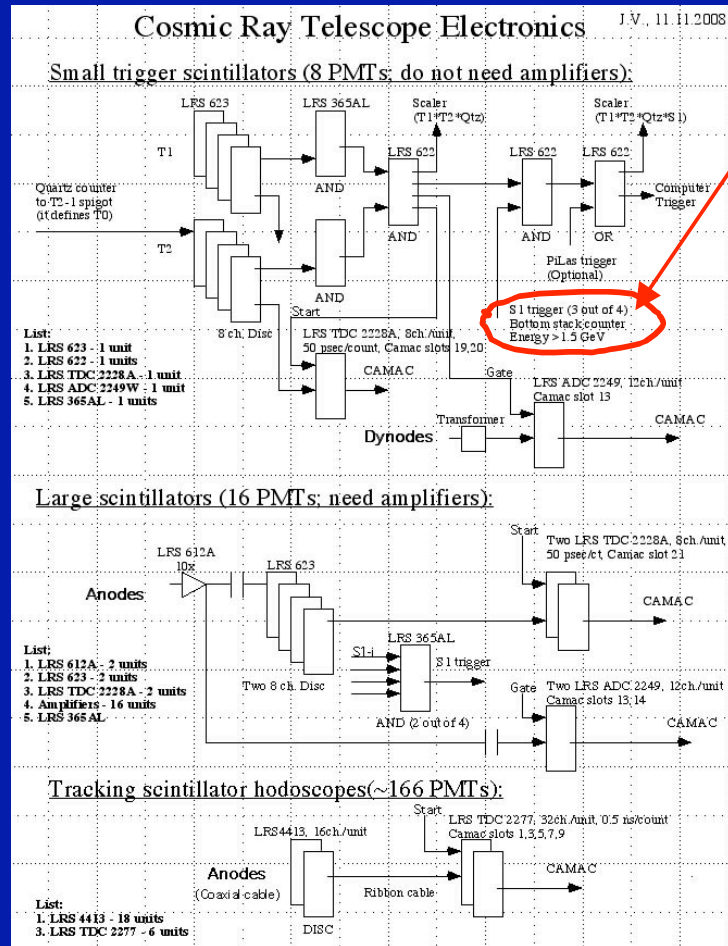
BlackFin DSP

- Pedestal subtract
- Feature extract → T, Q
(tentatively allow up to 4x hits in 100ns)
- Time = 2Bytes, Q = 2Bytes

8 hit chan * 1 hit typ * 4By = 32By/link
256 By/iTOP counter
1kB/event/COPPER

8kByte/event iTOP

SLAC cosmic ray telescope



Energy

Trigger rates:

- $T1*T2 \sim 5-6 \text{ Hz}$
- $T1*T2*S1 \sim 1-2 \text{ Hz}$
- $T1*T2* \text{ Quartz_counter} \sim 5-6 \text{ k/day}$
- $T1*T2*S1*\text{Quartz_counter} \sim 2-3 \text{ k/day}$

New DAQ:

- μ PCI ceate: μ PCI CPU - master, fiber optics transievers talk to boards on H-8500 MaPMTs
- Communicate with the rest of CAMAC via the CC-USB controllers
- The new DAQ system created by Gary Varner & Kurtis Nishima

- Status: cosmic ray telescope is running, together with the PiLas laser diode.