Feedback System Design

Alessandro Drago

SuperB Workshop

LAL, Orsay

15-18 February 2009

Main Topics

- SuperB parameters for feedback design
- Design general consideration
- R & D main list
- Scalability
- Innovation
- Conclusion

LER/HER	Unit	June 2008	Jan. 2009	$2N_b$, $I_b/\sqrt{2}$	$4\varepsilon_y$, $2N_b$
E+/E-	GeV	4/7	4/7	4/7	4/7
L	$cm^{-2}\ s^{-1}$	$1x10^{36}$	$1x10^{36}$	$1x10^{36}$	$1x10^{36}$
I^+/I^-	Amp	1.85 /1.85	2.00/2.00	2.82/2.82	4.00/4.00
N_{part}	$x10^{10}$	5.52 /5.52	5.97/5.97	4.23/4.23	5.97/5.97
N_{bun}		1250	1250	2500	2500
I_{bunch}	mA	1.48	1.6	1.13	1.6
$\theta/2$	mrad	25	30	30	30
β_x^*	mm	35/20	35/20	35/20	35/20
β_y^*	mm	0.22 /0.39	0.21 /0.37	0.21 /0.37	0.21 /0.37
ε_x	nm	2.8/1.6	2.8/1.6	2.8/1.6	2.8/1.6
ε_y	pm	7/4	7/4	7/4	28/16
σ_x	μm	9.9/5.7	9.9/5.7	9.9/5.7	9.9/5.7
σ_y	nm	39/39	38/38	38/38	76/76
σ_z	mm	5/5	5/5	5/5	5/5
ξ_x	X tune shift	0.0043/0.0025	0.0046/0.0027	0.0032/0.0019	0.0092/0.0054
ξ_y	Y tune shift	0.15 /0.15	0.128/0.128	0.090/0.090	0.064/0.064
RF stations	LER/HER	5/6	5/6	5/8	7/11
RF wall plug power	MW	16.2	18	25.5	39.3
Total wall plug power	MW				

SuperB feedback parameters

FB Sampling frequency	476	MHz
Harmonic number	2850	
Revolution period	~ 6	us
Stored bunches	~1250 (2500)	Ph-1 (Ph-2)
Bucket length	~2	ns
Ph-1 (ph-2) bunch spacing	1.26 (.63)	m
n_s HER/LER	0.0141/0.0133	
Synchrotron frequency	~2.35/2.2	kHz
Longitudinal damping time	~20	ms
$n_{x,y}$ HER/LER	0.52/.54 (???)	
Betatron frequency	86.8/90.2	kHz
Transverse damping time	40	ms
Transv. feedback expected damping time	>120 (> 20 turns)	us
Power amplifier (long.)	4x250	W
Power amplifier (trasv.)	2x500	W
Trasverse kickers (1xV, 1xH)	2-ports	Stripline type
Longitudinal kicker	4-ports	Cavity type

Considerations on H

- H, harmonic number=2850
- Still if the stored bunches will be ~1250 (PH1) & ~2500 (PH2) to let ion clearing gaps, from a feedback point of view all buckets (2850=H) have to be processed
- **H=2850 =** 2*1425 =2*5*285=**2*5*5*57** that is not exactly a wonderful number for FB's
- PEPII_H = 3492 [with revolution period 7.336us]
- 3492 = 1746*2 = 2*2*3*3*97
- DAFNE_H = 120 = 2*2*2*3*5
- Virtex-5 has 1056 dsp: 1056=2*2*2*2*2*3*11
- In conclusion, for H, highly composed numbers are better than prime numbers or poorly composed numbers

Key points for starting to write a TDR for b-b-b feedback system

- Innovation
- Costs
- Manpower for design
- Design duration (on 5 - 8 years timescale)
- Design robustness /self & beam diagnostics
- Compatibility for new upgrade
- Flexibility
- Scalability
- Maintenance & manpower necessary for maintenance

Key points for starting TDR / 2

- Consequences:
  - Design based on last version components
  - Design based on stable (popular) components
  - Recycle what doesn’t need changes
  - Unified technology choices as much as possible
  - Scale savings
  - Easy interface for not expert operators

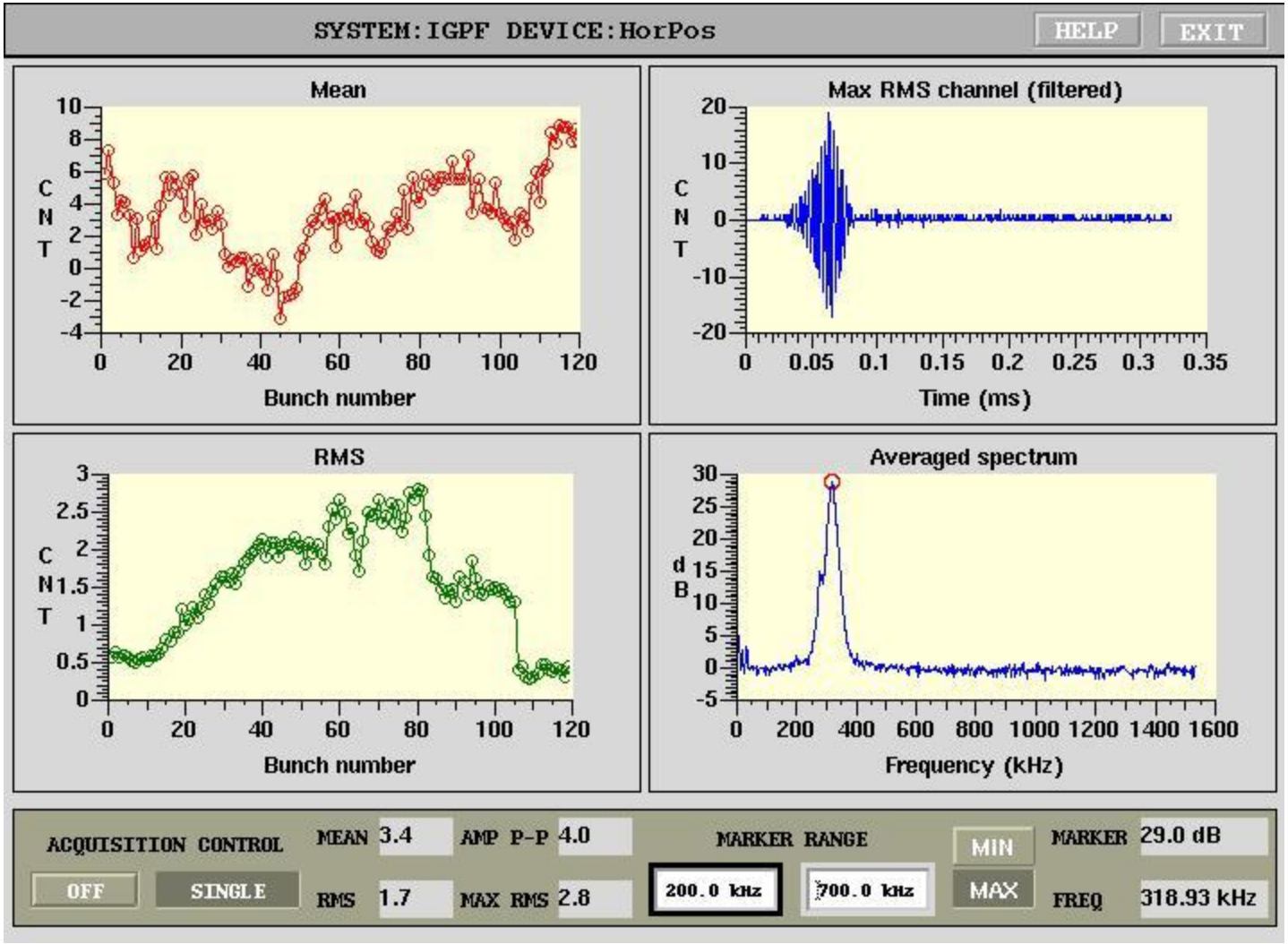
Key points for starting TDR / 3

- Consequences of second orders:
  - Every design based on old FPGA (as iGp with V-II) should migrate to last version FPGA (as Xilinx V5)
  - Unified technology choices lead to possibly use same tools, parts or designs for similar systems:
    - Transverse feedback
    - Longitudinal feedback
    - Fast IP feedback
    - Timing/injection system (pulse generator)
    - Low level RF
    - 1-D Bunch-by-bunch and turn-by-turn diagnostics, as for example transverse and longitudinal dimension/position detectors
    - 2D Bunch-by-bunch and turn-by-turn diagnostics, as for example profile monitors, etc.

Design robustness

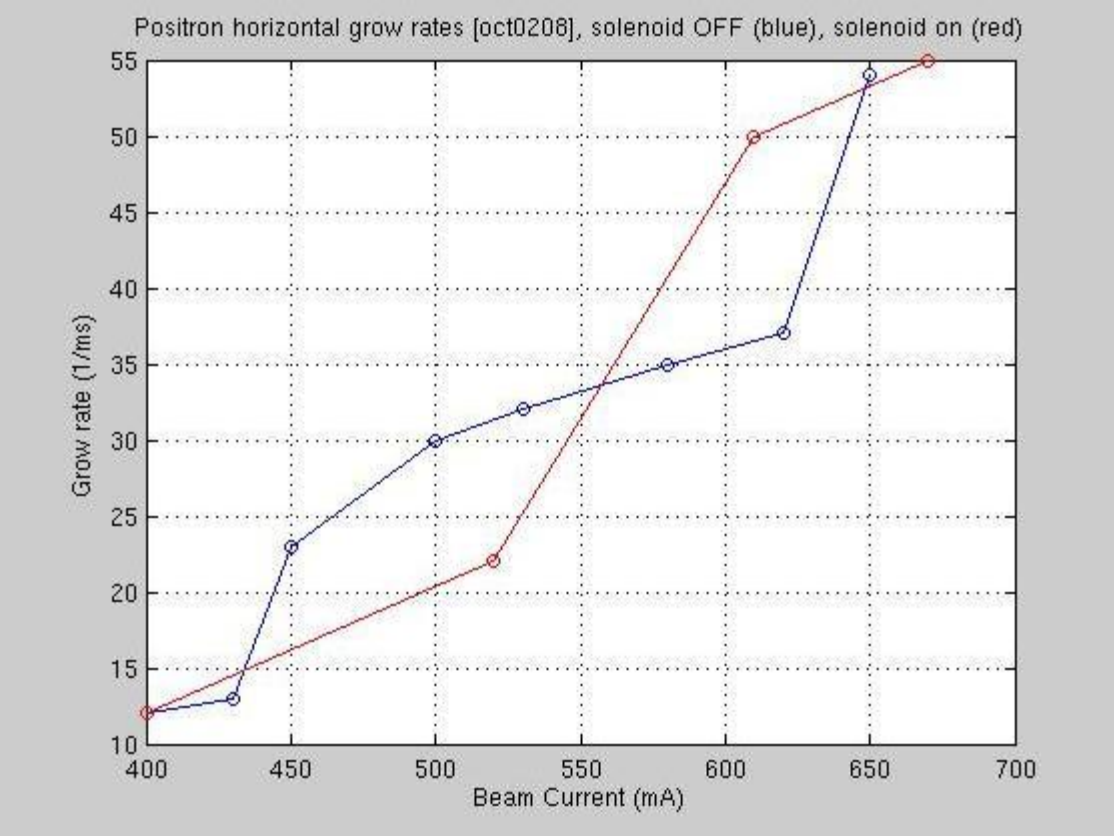
- Self diagnostics: internal efficient tools to identify quickly correct operation of every subsystem
- Easy timing procedures
- Beam diagnostics, in particular instability grow rate measurements
- Easy access for non expert operators

Positron grow-damp record made switching off the horizontal feedback, I=575mA, 105/120 bunch [October 14, 2008]



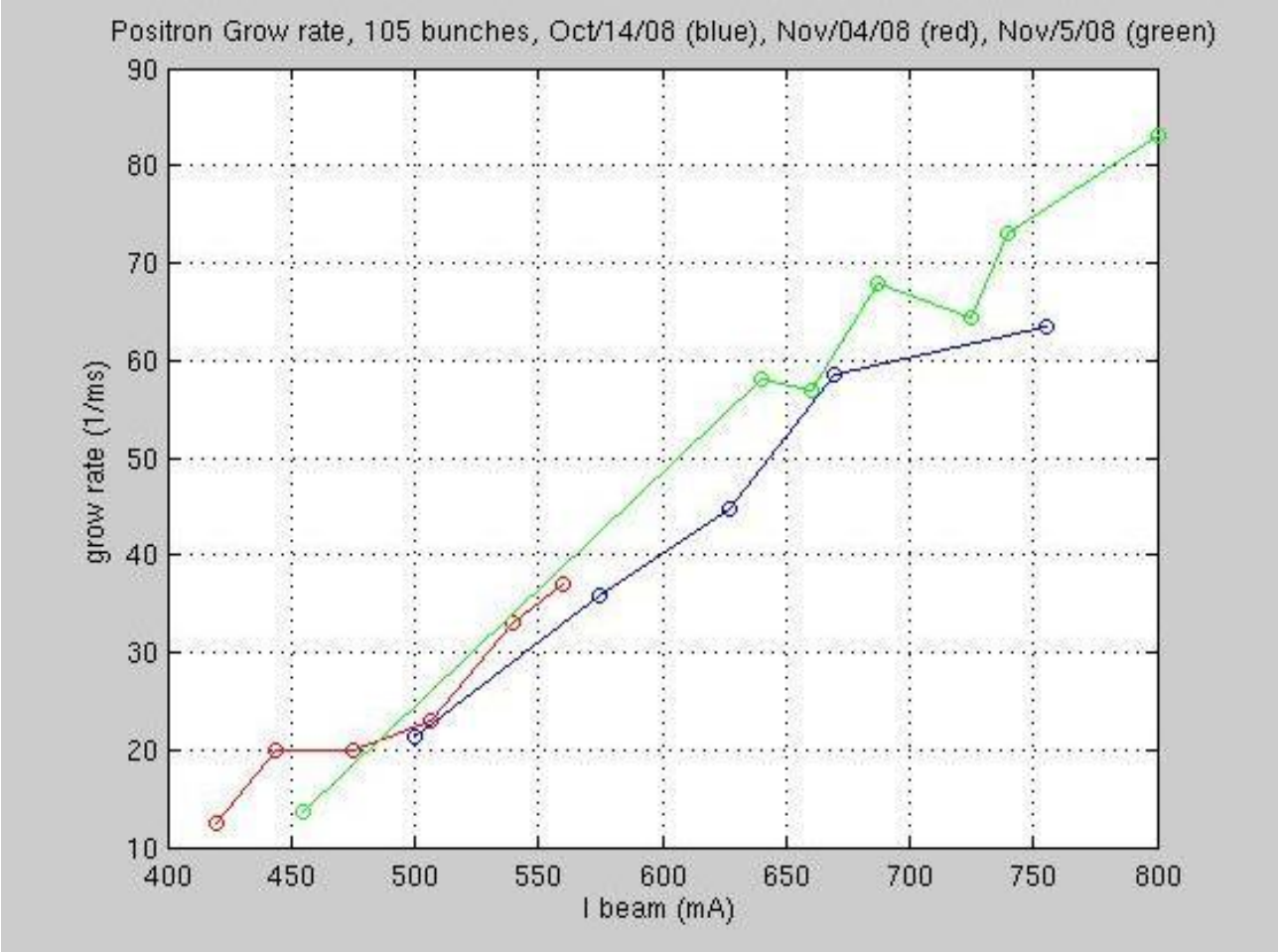
Real time waveform plot by the "iGp" feedback system

e+ instability behavior switching solenoids off (blue) & on (red)



- Switching off the solenoids installed in the positron ring the grow rates of the e+ instability does not change

e+ instability grow rates versus Δνx in PS1-PS2 and RCR

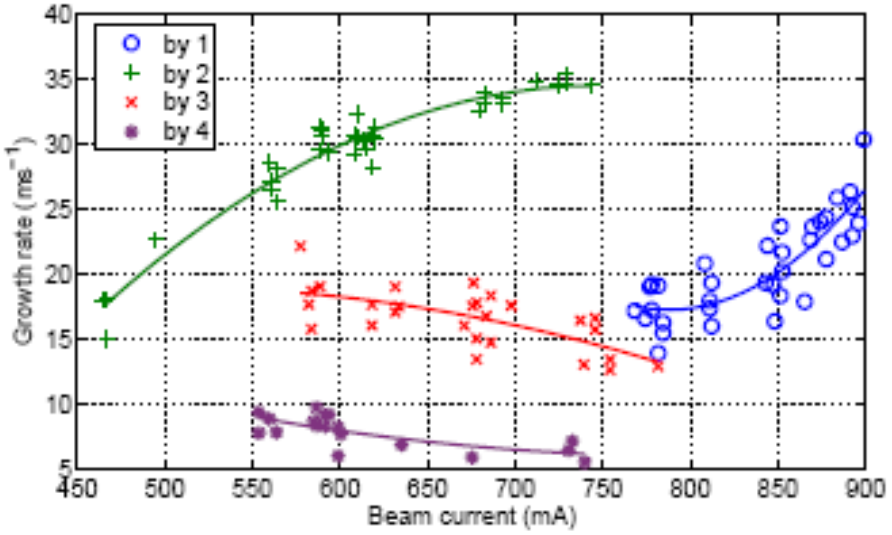


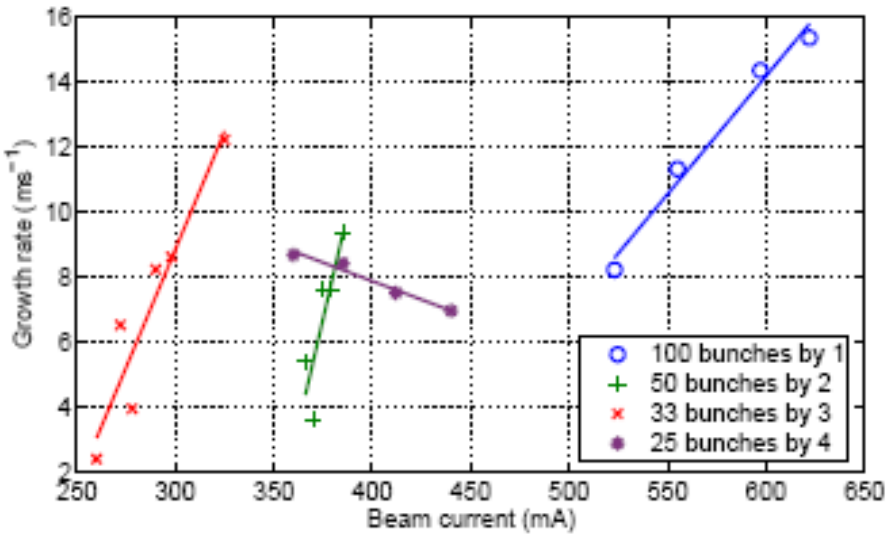
OPTICS:

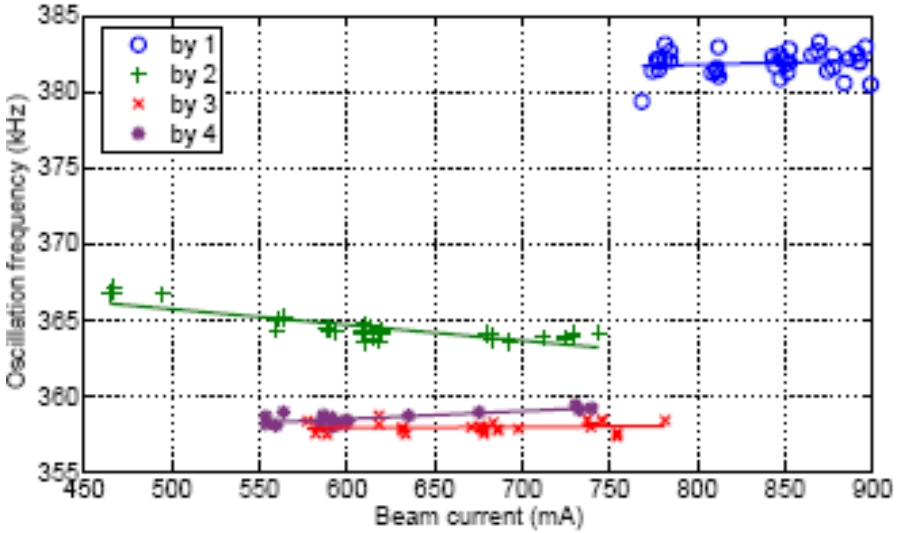
- Collision
  mode m = -1 (blue)
- Δνx = + 0.5 (PS1÷PS2)
  νx = νy
  mode m = 0 (red)
- Δνx = + 1.0 (0.5 in PS1÷PS2 0.5 in RCR)
  νx = νy
  mode m = -1 (cyan)

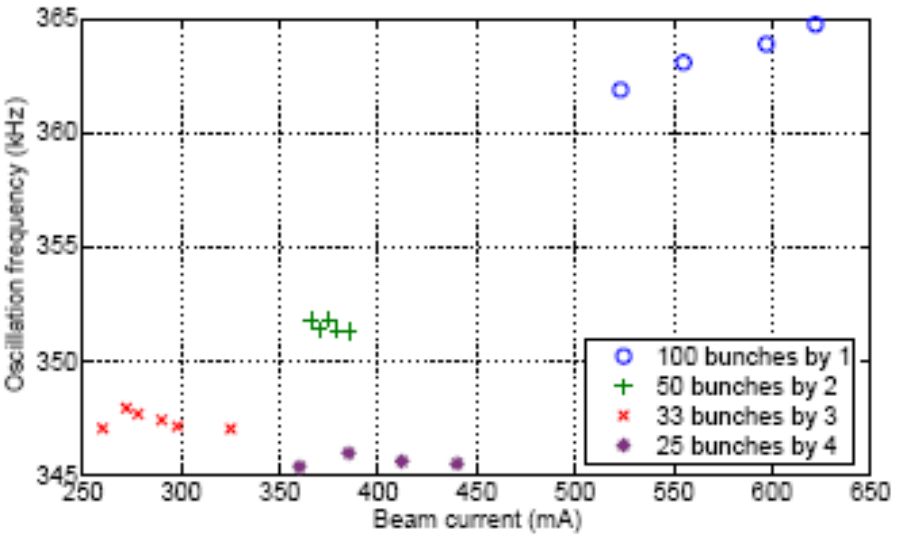
This is to study the e+ instability as a function of the relative phase advance between the WGLs

In the past years, troubles were much smaller!!!





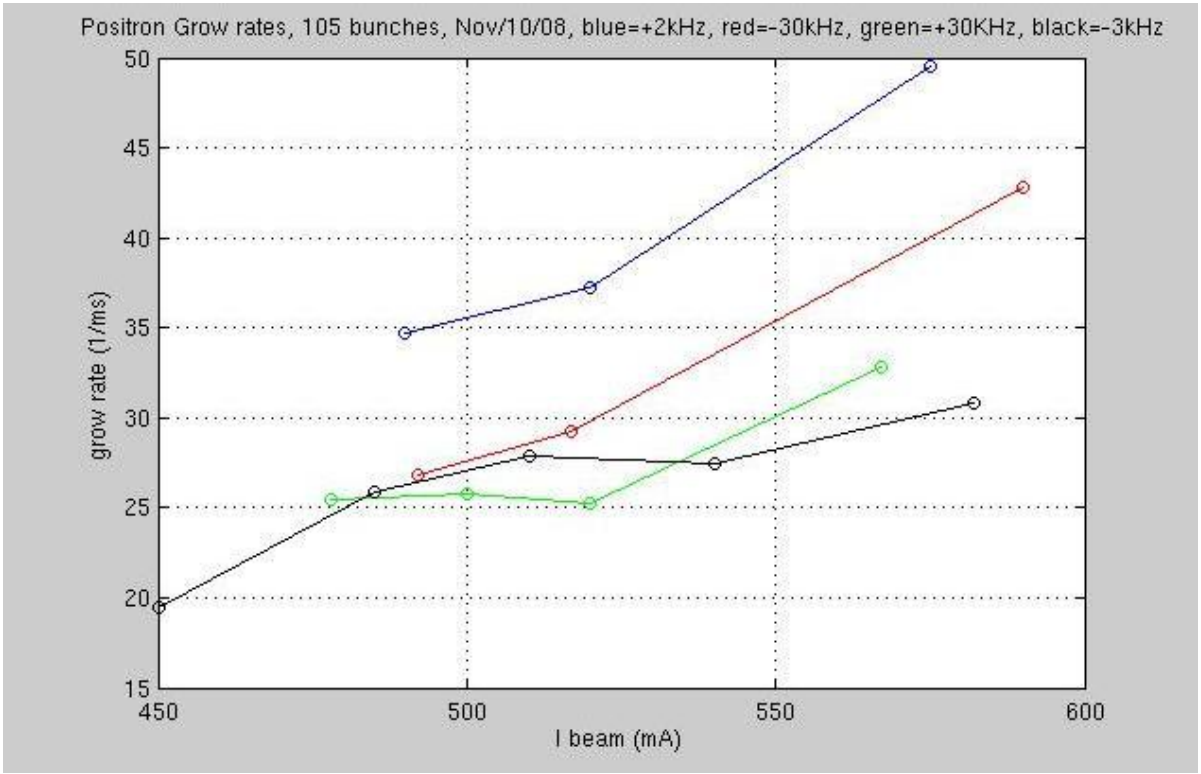




Hor. e+ grow rates, August 4, 2005

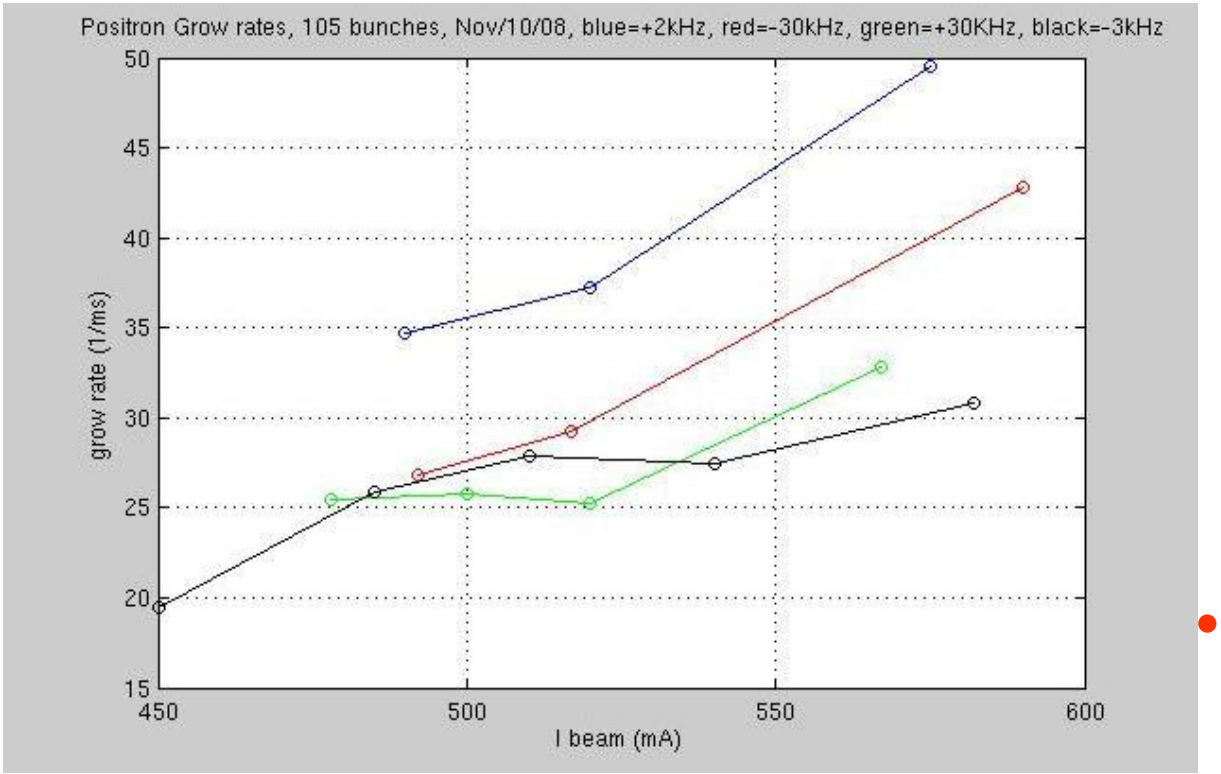
Hor. e+ grow rates, 2004

e+ instability grow rates versus orbit in the main ring dipoles



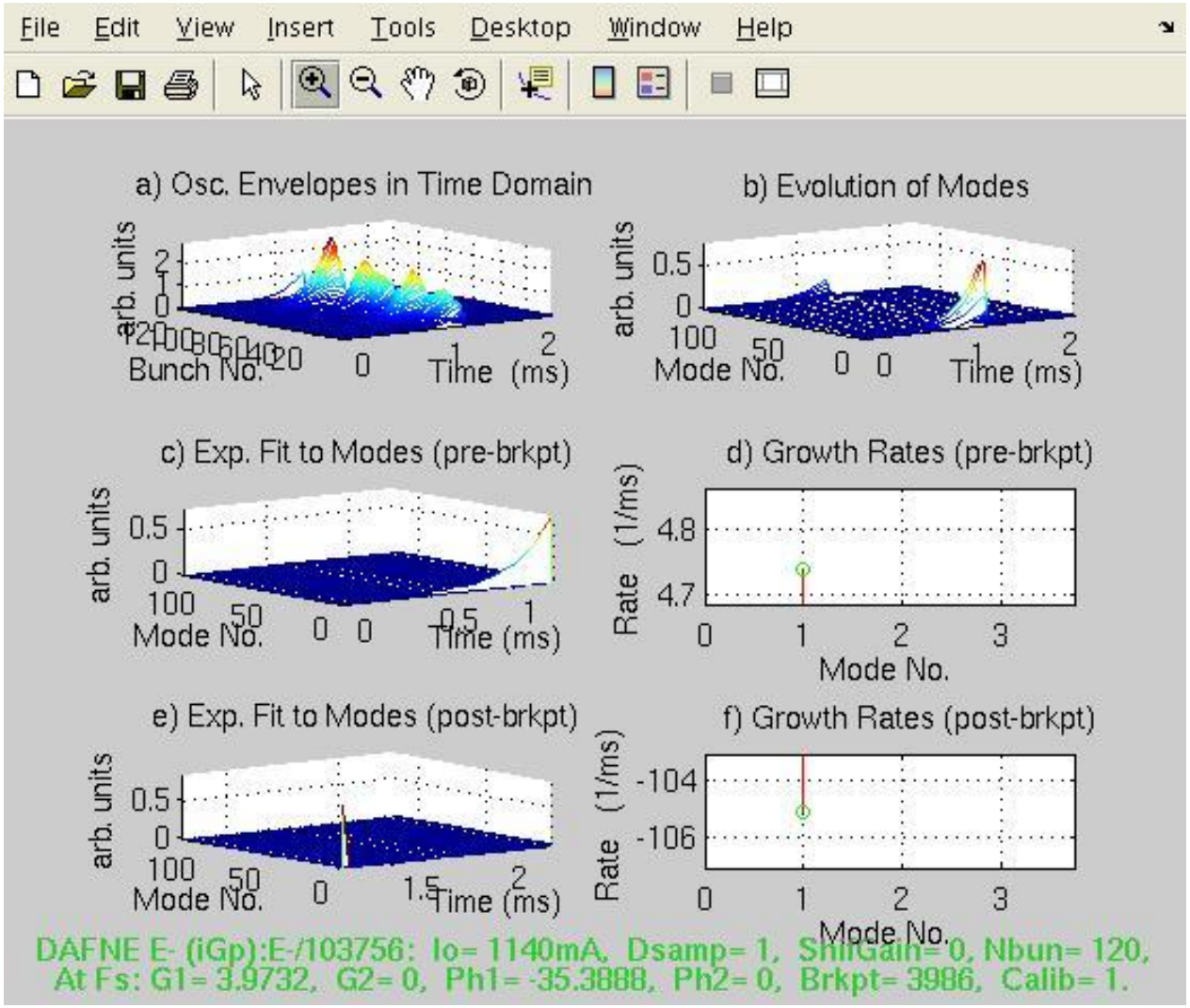
The orbit variation is performed changing the RF frequency and then compensating the beam energy

e+ instability grow rates versus orbit in the main ring dipoles



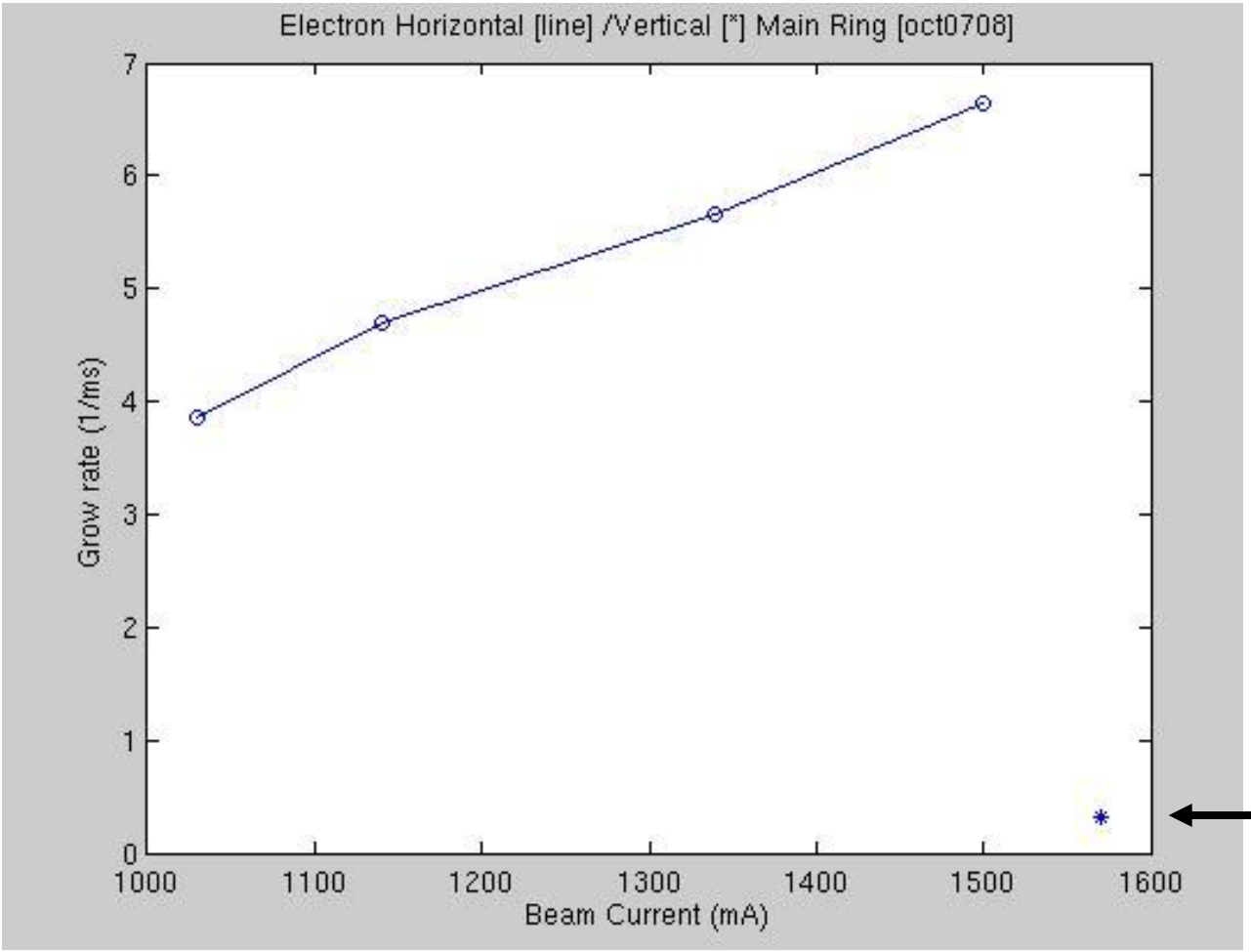
- The orbit variation shows **important differences** from the point of view of understanding the instability source
- but not to solve completely the e+ current threshold

e- beam, I=1140mA, 100/120 bunches, unstable mode=1, [October 7, 2008]



Different and **much slower** unstable mode compared with e+ beam

e- ring, Imax=1.5 A, 100/120 bunches [October 7, 2008]

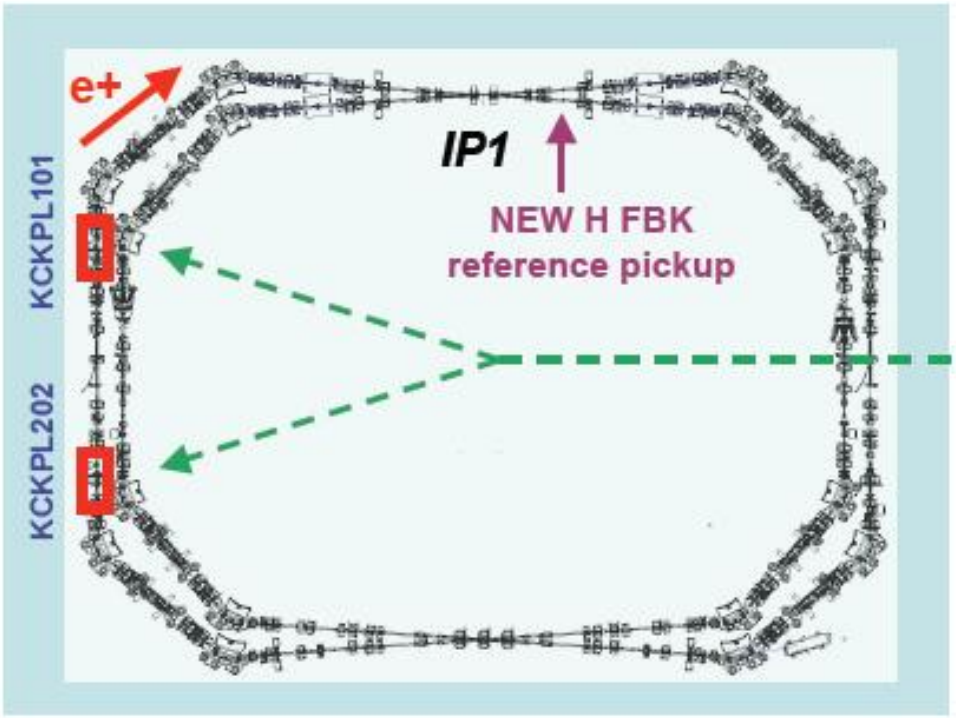


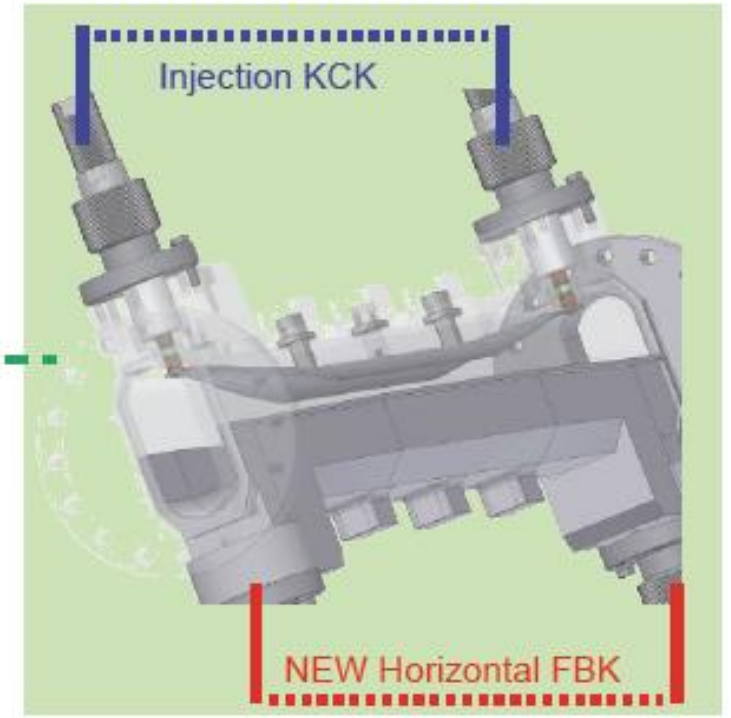
Vertical instability much slower

Scalability

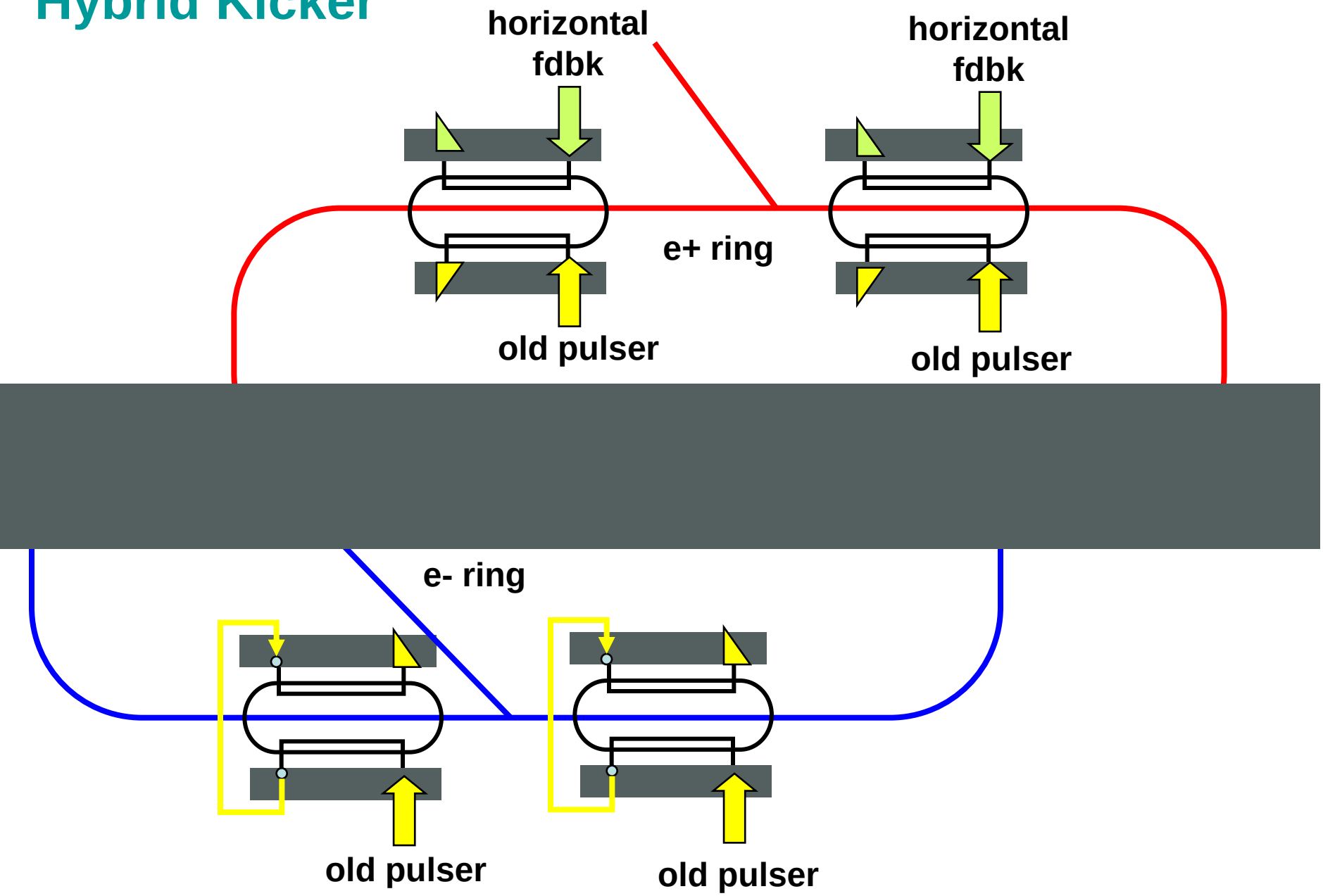
- Double feedback in the same oscillation plane to use at the best the power output
- A proved example of the scalability advantages
- Possibility to have and manage easily more than one feedback in a single oscillation plane
- Capability to damp coherent high order modes even if faster than foreseen

- **New e+ Transverse Horizontal Feedback**
- The damping times of the two feedbacks add up linearly
- Damping time measured:
- ~100 ms-1 (1 FBKs) ➔ fb damps in 30 revolution periods (~10 us)
- ~200 ms-1 (2 FBKs) ➔ fb damps in 15 revolution periods (~ 5 us)
- The power of the H FBK has been doubled

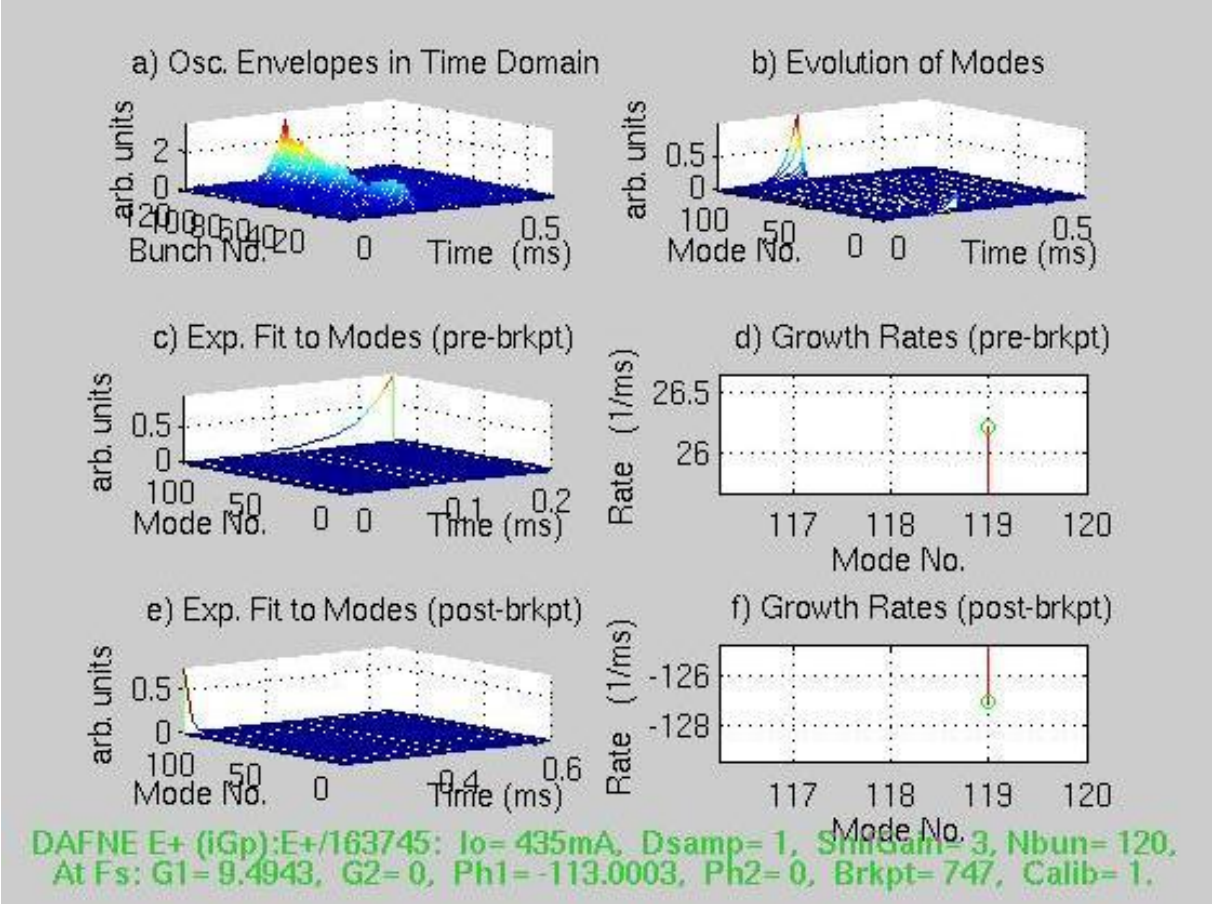




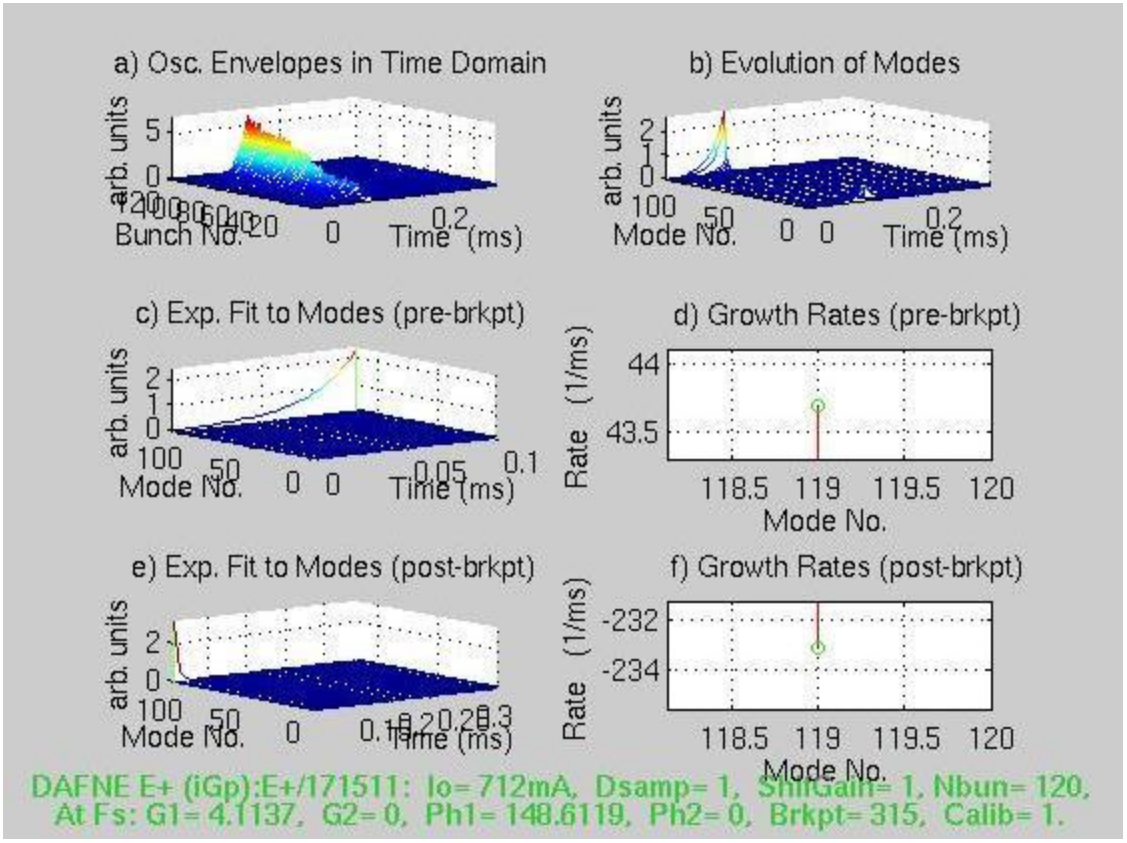
Hybrid Kicker



Single horizontal feedback: I=560mA, mode -1 [=119] , grow=34.5 (ms-1), damp=-127(ms-1)

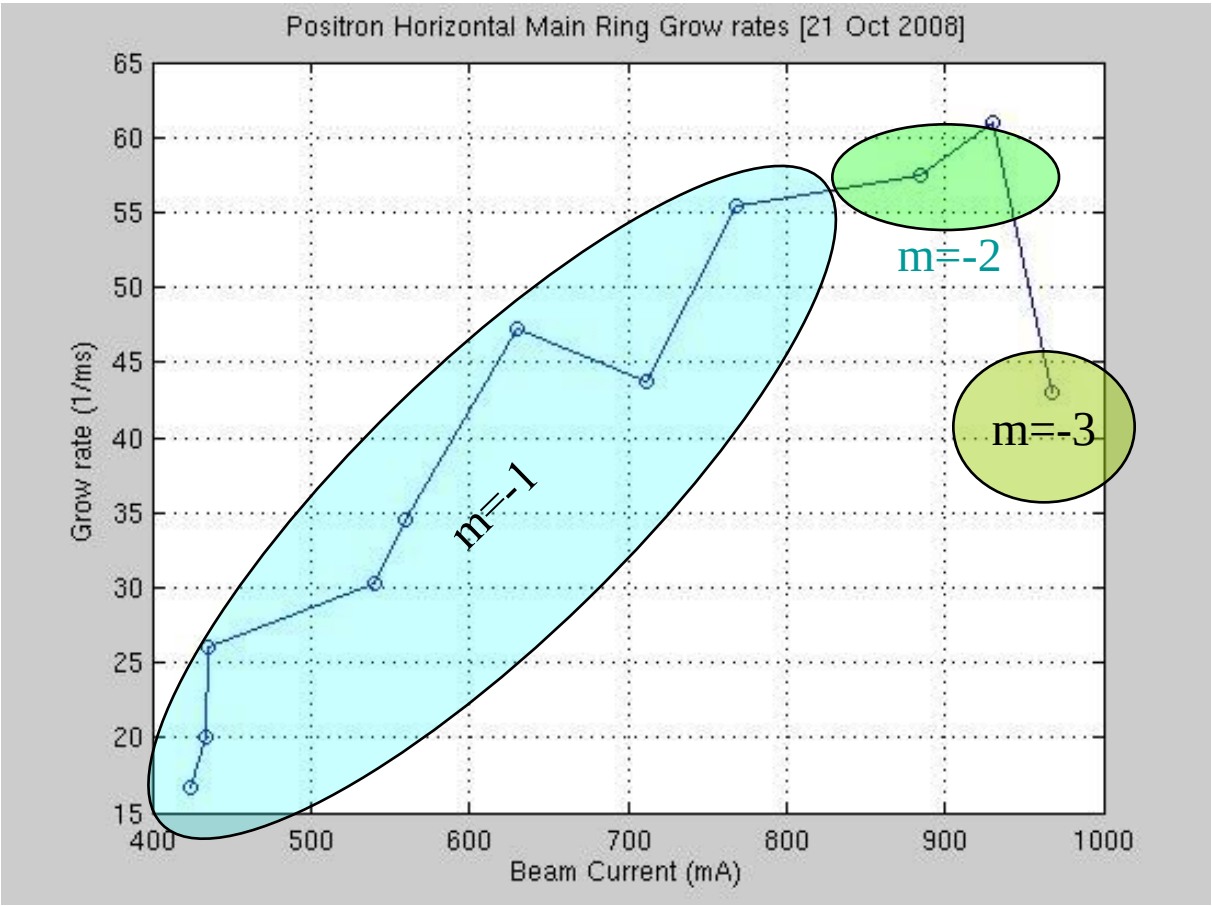


Double horizontal feedback: I=712mA, mode -1 [=119] , grow=43.7 (ms-1), damp=-233 (ms-1)



Damping time in 4.3 microsecond i.e. in ~13 revolution turns

Grow rates at higher e+ current, instability controlled by 2 feedback: the unstable mode changes becoming slower!



The beam current does not seem limited by the horizontal instability

Innovation

R&D feedback for low emittance accelerator (proposed in July 08 MiniMac)

R&D list includes:

1) very low noise analog front end @ n*RF [n=3?]
2) maintain low cross-talk between adjacent bunches under 40 dB (better 60 dB) in front end
3) dual separated timing to pilot the backend power stage
4) digital processing unit with high dynamic range (12/16 bits) > 60dB
5) “dual gain” approach to minimize residual beam motion and feedback noise on the beam [in digital processing unit]
6) integrated beam-feedback model with easy code and parameter download to digital processing unit

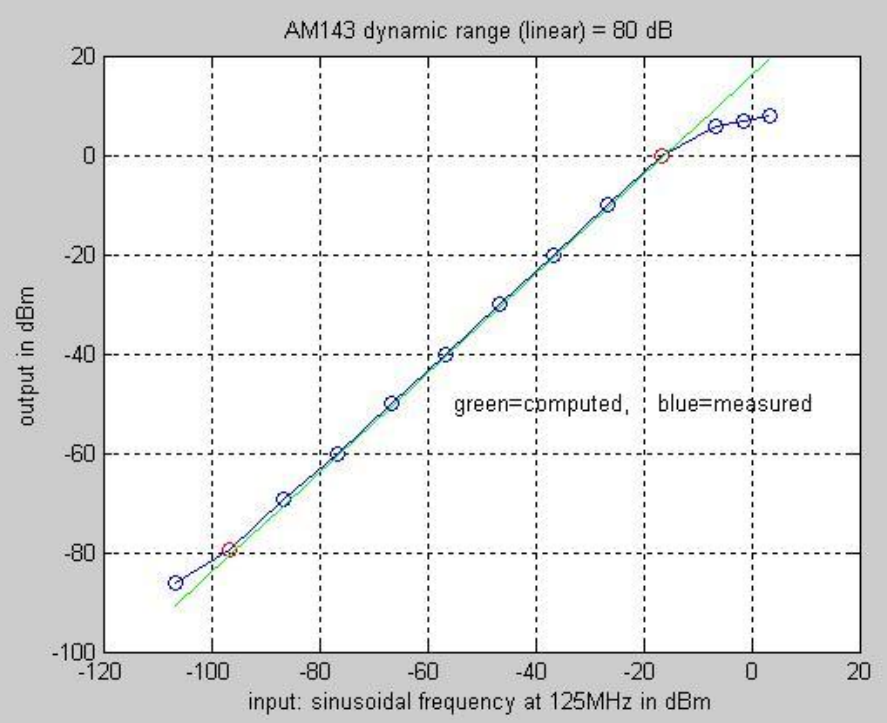
Considering a feedback upgrade for low emittance accelerators

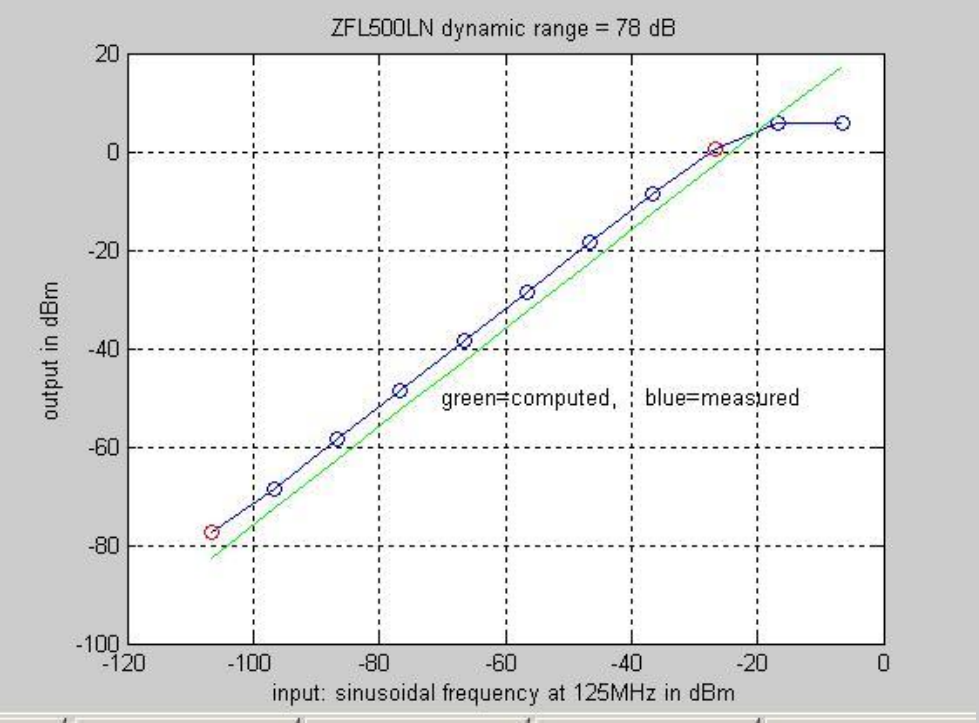
- Feedback are active system and can have strong negative impact on very low emittance beams
- The basic ideas of the upgrades consist in making the noise in the feedback loop as low as possible, and this means:
- a) Filtering at the best the external noise, i.e. coming or generated outside the feedback
- b) Reducing the internal noise, i.e. the noise coming from parts in the feedback system
- c) Reduce the crosstalk between bunch signals

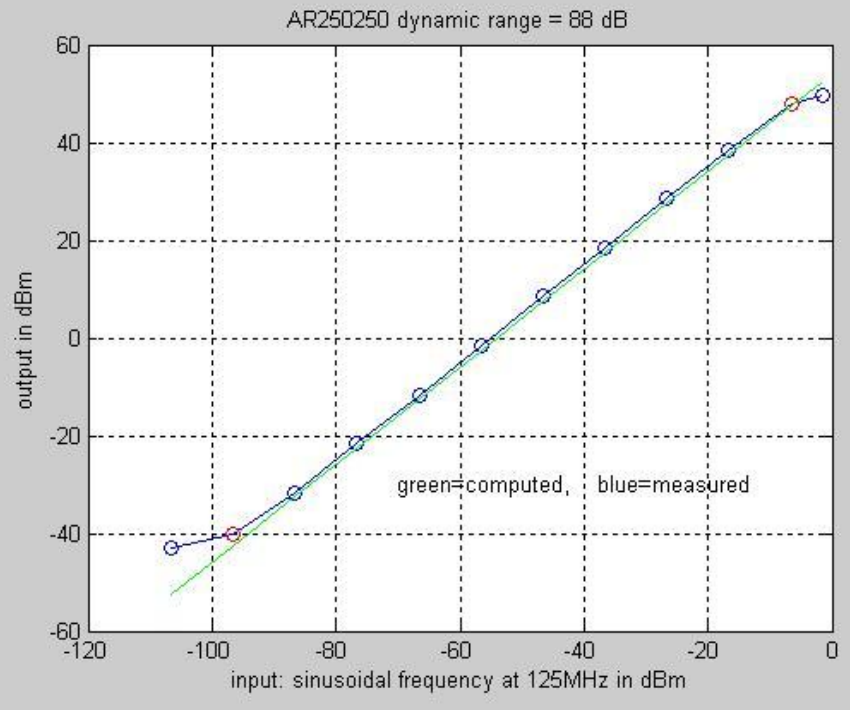
R & D areas

- Analog R&D: Front End / Back End / transverse /longitudinal
- Digital processing unit R&D
- Beam/feedback Model R&D for coefficient generation/maintenance
- other important design areas:
  - Power amplifiers R&D: not strictly necessary but the high cost of commercial power devices **could** justify a R&D
  - Longitudinal & transverse kickers
  - Beam signal pickups

The dynamic range in DAFNE feedback analog blocks is in the range
78 dB – 88 dB







ADC dynamic range versus # of bits

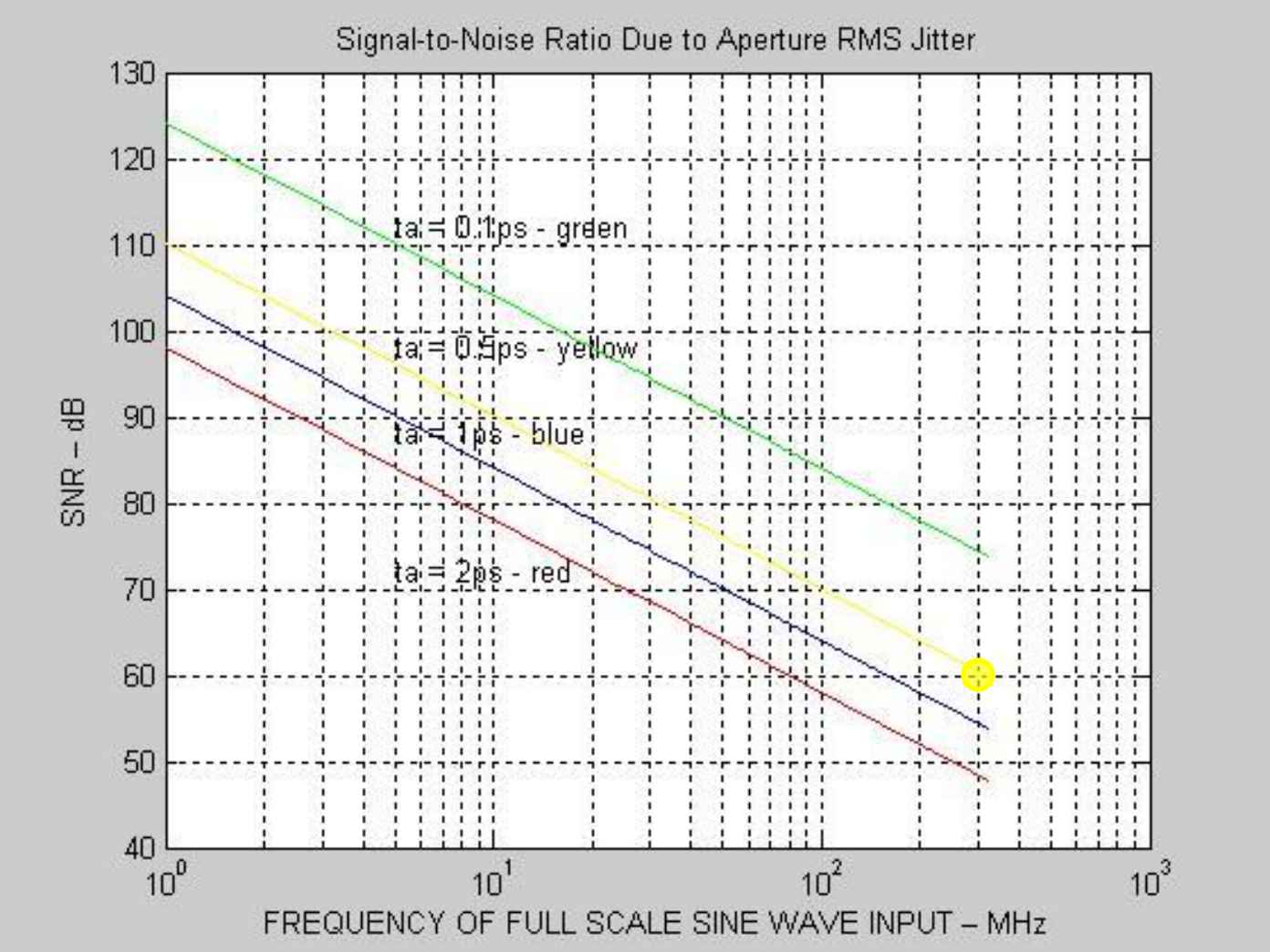
- 7.5_bit ADC_= 45.15 dB } very poor dyn.range !
- 8_bit ADC _ = 48.16 dB
- 10_bit ADC _= 60.20 dB
- 12_bit ADC _= 72.25 dB
- 14_bit ADC _= 84.29 dB [best value considering the analog blocks!]
- 15_bit ADC _= 90.31 dB
- 16_bit ADC = 96.33 dB
- 24_bit ADC = 144.49 dB

- Note: in general at least 0.5 bit (= 3dB) is not effective in the conversion

A factor liming the effectiveness of the ADC is the sampling clock jitter. I can suppose that a realistic value of the RMS jitter for the timing signal will be ~0.5 ps

This value must be included in SuperB Timing specifications

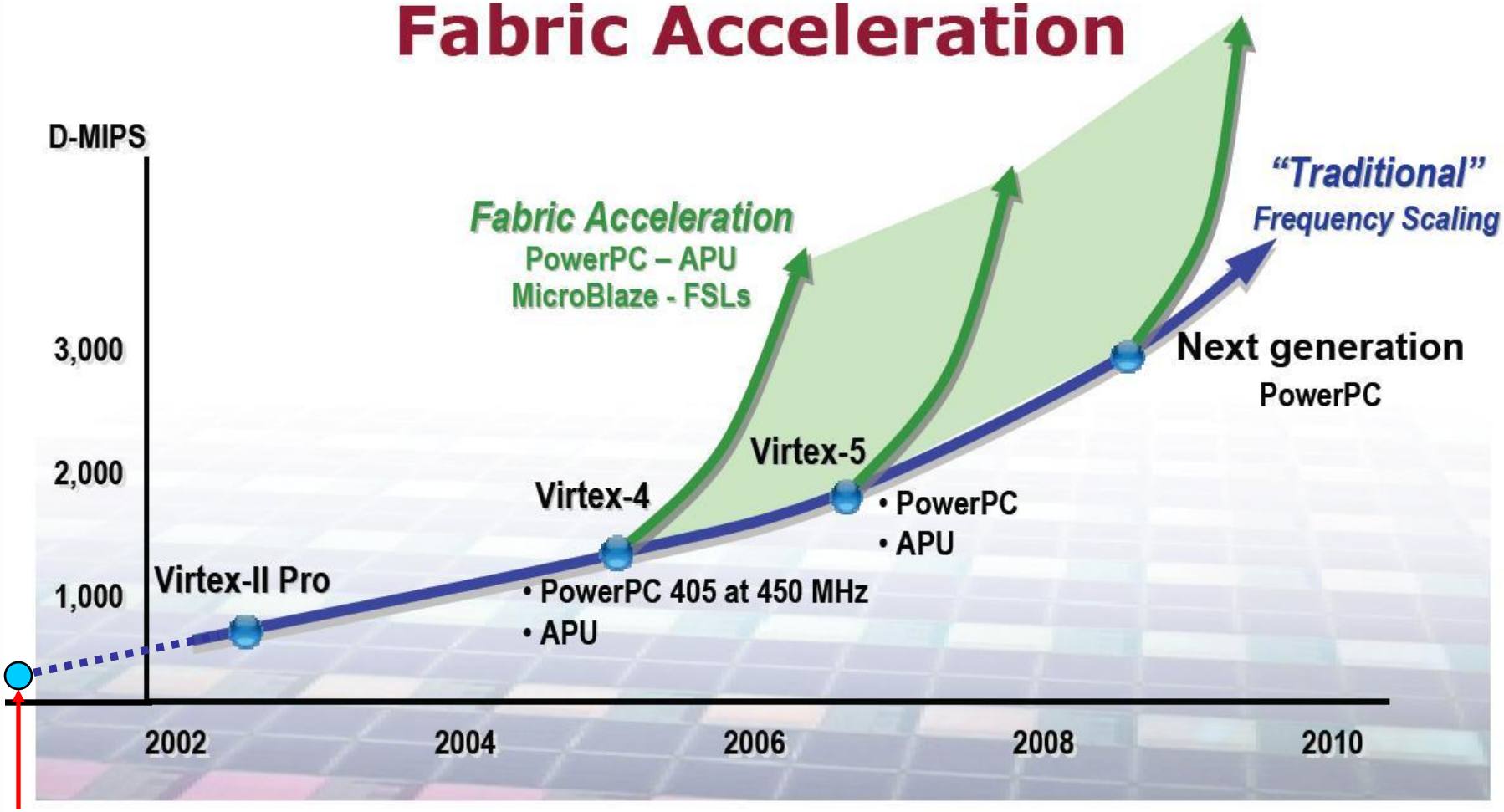
- In this case (yellow trace), the ADC dynamic range should be better than 60 dB (12bits)



FIR

- The core of a feedback digital processing unit is the FIR filter (=Finite Impulse Response filter)
- An FIR filter can have any kind of coefficients and transfer functions but the output y is always built as $y = \mathrm{sum}_i\ (c_i * x_i)$
- i = number of taps (of the filter)
- c_i = “static” but downloadable coefficients
- x_i = previuos i input values for each bunches

Processor Performance and Fabric Acceleration



VIRTEX-II
[used in iGP]

XILINX®

- Virtex-5 has 1056 DSP48 and 550MHz clock speed

Table 1: **Virtex-5 FPGA Family Members**

Device	Configurable Logic Blocks (CLBs)			DSP48E Slices[2]	Block RAM Blocks			CMTs[4]	PowerPC Processor Blocks	Endpoint Blocks for PCI Express	Ethernet MACs[5]	Max RocketIO Transceivers[6]		Total I/O Banks[8]	Max User I/O[7]
	Array (Row x Col)	Virtex-5 Slices[1]	Max Distributed RAM (Kb)		18 Kb[3]	36 Kb	Max (Kb)					GTP	GTX		
XC5VLX30	80 x 30	4,800	320	32	64	32	1,152	2	N/A	N/A	N/A	N/A	N/A	13	400
XC5VLX50	120 x 30	7,200	480	48	96	48	1,728	6	N/A	N/A	N/A	N/A	N/A	17	560
XC5VLX85	120 x 54	12,960	840	48	192	96	3,456	6	N/A	N/A	N/A	N/A	N/A	17	560
XC5VLX110	160 x 54	17,280	1,120	64	256	128	4,608	6	N/A	N/A	N/A	N/A	N/A	23	800
XC5VLX155	160 x 76	24,320	1,640	128	384	192	6,912	6	N/A	N/A	N/A	N/A	N/A	23	800
XC5VLX220	160 x 108	34,560	2,280	128	384	192	6,912	6	N/A	N/A	N/A	N/A	N/A	23	800
XC5VLX330	240 x 108	51,840	3,420	192	576	288	10,368	6	N/A	N/A	N/A	N/A	N/A	33	1,200
XC5VLX20T	60 x 26	3,120	210	24	52	26	936	1	N/A	1	2	4	N/A	7	172
XC5VLX30T	80 x 30	4,800	320	32	72	36	1,296	2	N/A	1	4	8	N/A	12	360
XC5VLX50T	120 x 30	7,200	480	48	120	60	2,160	6	N/A	1	4	12	N/A	15	480
XC5VLX85T	120 x 54	12,960	840	48	216	108	3,888	6	N/A	1	4	12	N/A	15	480
XC5VLX110T	160 x 54	17,280	1,120	64	296	148	5,328	6	N/A	1	4	16	N/A	20	680
XC5VLX155T	160 x 76	24,320	1,640	128	424	212	7,632	6	N/A	1	4	16	N/A	20	680
XC5VLX220T	160 x 108	34,560	2,280	128	424	212	7,632	6	N/A	1	4	16	N/A	20	680
XC5VLX330T	240 x 108	51,840	3,420	192	648	324	11,664	6	N/A	1	4	24	N/A	27	960
XC5VSX35T	80 x 34	5,440	520	192	168	84	3,024	2	N/A	1	4	8	N/A	12	360
XC5VSX50T	120 x 34	8,160	780	288	264	132	4,752	6	N/A	1	4	12	N/A	15	480
XC5VSX95T	160 x 46	14,720	1,520	640	488	244	8,784	6	N/A	1	4	16	N/A	19	640
XC5VSX240T	240 x 78	37,440	4,200	1,056	1,032	516	18,576	6	N/A	1	4	24	N/A	27	960
XC5VTX150T	200 x 58	23,200	1,500	80	456	228	8,208	6	N/A	1	4	N/A	40	20	680
XC5VTX240T	240 x 78	37,440	2,400	96	648	324	11,664	6	N/A	1	4	N/A	48	20	680
XC5VFX30T	80 x 38	5,120	380	64	136	68	2,448	2	1	1	4	N/A	8	12	360
XC5VFX70T	160 x 38	11,200	820	128	296	148	5,328	6	1	3	4	N/A	16	19	640
XC5VFX100T	160 x 56	16,000	1,240	256	456	228	8,208	6	2	3	4	N/A	16	20	680
XC5VFX130T	200 x 56	20,480	1,580	320	596	298	10,728	6	2	3	6	N/A	20	24	840
XC5VFX200T	240 x 68	30,720	2,280	384	912	456	16,416	6	2	4	8	N/A	24	27	960

Ready for R&D: a Xilinx board with 288 digital signal processors inside

- The last version of feedback system (the “iGp”) is built around a Virtex-II FPGA by Xilinx
- Virtex-II, aging ~10 years, has 168 multiplier blocks, as shown in the Xilinx table below
- The internal clock speed is 420MHz

Table 1: **Virtex-II Field-Programmable Gate Array Family Members**

Device	System Gates	CLB (1 CLB = 4 slices = Max 128 bits)			Multiplier Blocks	SelectRAM Blocks		DCMs	Max I/O Pads(1)
		Array Row x Col.	Slices	Maximum Distributed RAM Kbits		18 Kbit Blocks	Max RAM (Kbits)		
XC2V40	40K	8 x 8	256	8	4	4	72	4	88
XC2V80	80K	16 x 8	512	16	8	8	144	4	120
XC2V250	250K	24 x 16	1,536	48	24	24	432	8	200
XC2V500	500K	32 x 24	3,072	96	32	32	576	8	264
XC2V1000	1M	40 x 32	5,120	160	40	40	720	8	432
XC2V1500	1.5M	48 x 40	7,680	240	48	48	864	8	528
XC2V2000	2M	56 x 48	10,752	336	56	56	1,008	8	624
XC2V3000	3M	64 x 56	14,336	448	96	96	1,728	12	720
XC2V4000	4M	80 x 72	23,040	720	120	120	2,160	12	912
XC2V6000	6M	96 x 88	33,792	1,056	144	144	2,592	12	1,104
XC2V8000	8M	112 x 104	46,592	1,456	168	168	3,024	12	1,108

Conclusions

- Feedback systems needs internal and beam diagnostics tools
- The instability grow rates measured by FB show a good agreement with e-cloud model and simulations
- It is possible manage more power in the feedbacks installing as many systems as necessary
- Two separate feedback systems for the same oscillation plane work in perfect collaboration doubling the feedback damping time
- DAFNE feedback damping time is 4.3 microsecond i.e. ~13 revolution turns, this value can be used to design the SuperB feedback system