Super Nemo Absolute Time Stamper

A high resolution and large dynamic range time stamper chip

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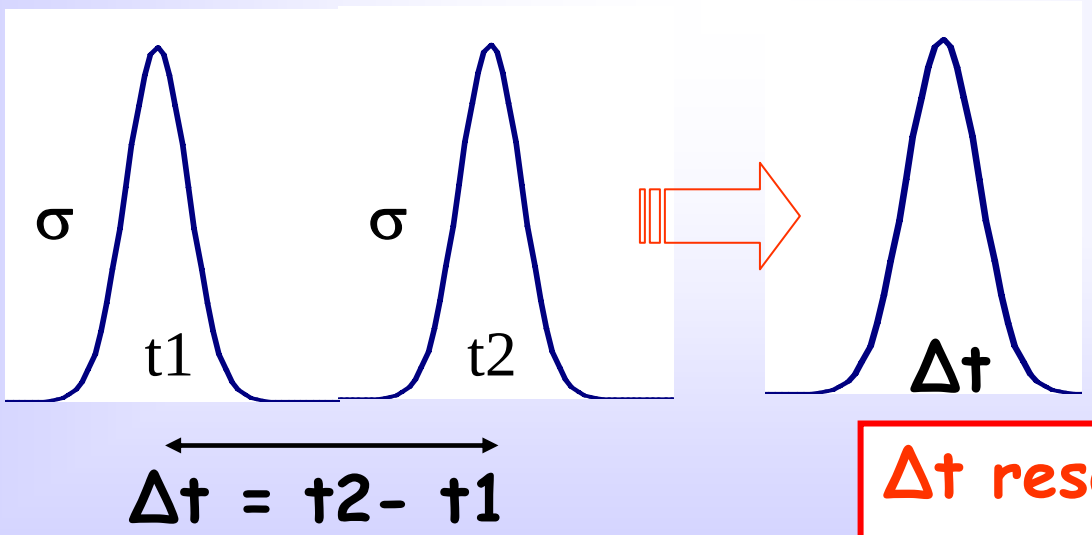
Time stamper vs TDC

- TDC : time measured between a Start & a Stop
- Time Stamper : absolute time measurement

SuperNemo experiment: 2 events will be stamped ⇒ Δt = t2- t1



$\sigma_t = \sigma \sqrt{2}$

Δt resolution degraded by a factor of √2

Requirements for SuperNemo Calorimeter Time Measurements :

- time resolution < 100ps RMS

Requirements for SNATS :

- SNATS résolution ≅ time résolution / √2
  ≅ 70ps RMS

x√12

LSB ≅ 250ps

SNATS: parameters definition

LSB < 250ps

– AMS CMOS 0.35µm: typ cell delay around 200ps
– For a minimum INL: Max number of cell in a DLL = 32

↳ Clock frequency needed: 160 MHz

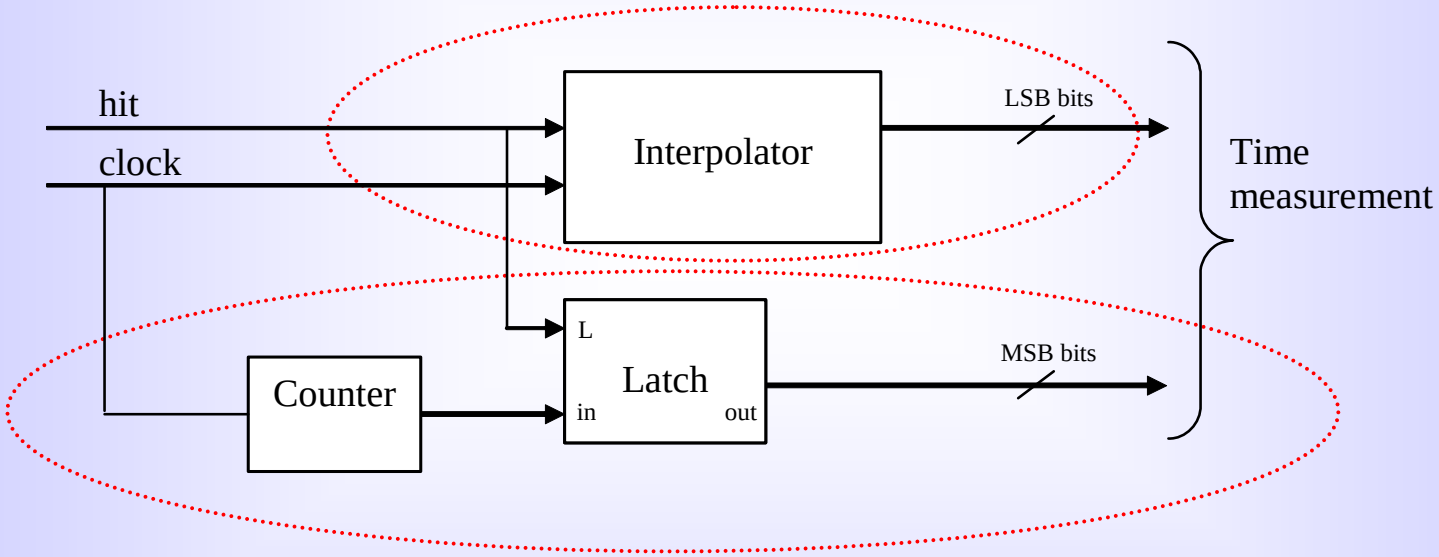
Provided by the board through commercial PLLs

SNATS Chip specifications :

- **Technology Process: AMS CMOS 0.35µm**
- **Clock Frequency: 160MHz**
- **Number of cells: 32**
- **Dynamic Range: 53 bits**
  - **48 clock counter bits**
  - **5 interpolator bits**
    - **⇘Time coverage: 20 days**
- **LSB = 250ps**
- **DNL < 10%**
- **Channels per chip = 16**

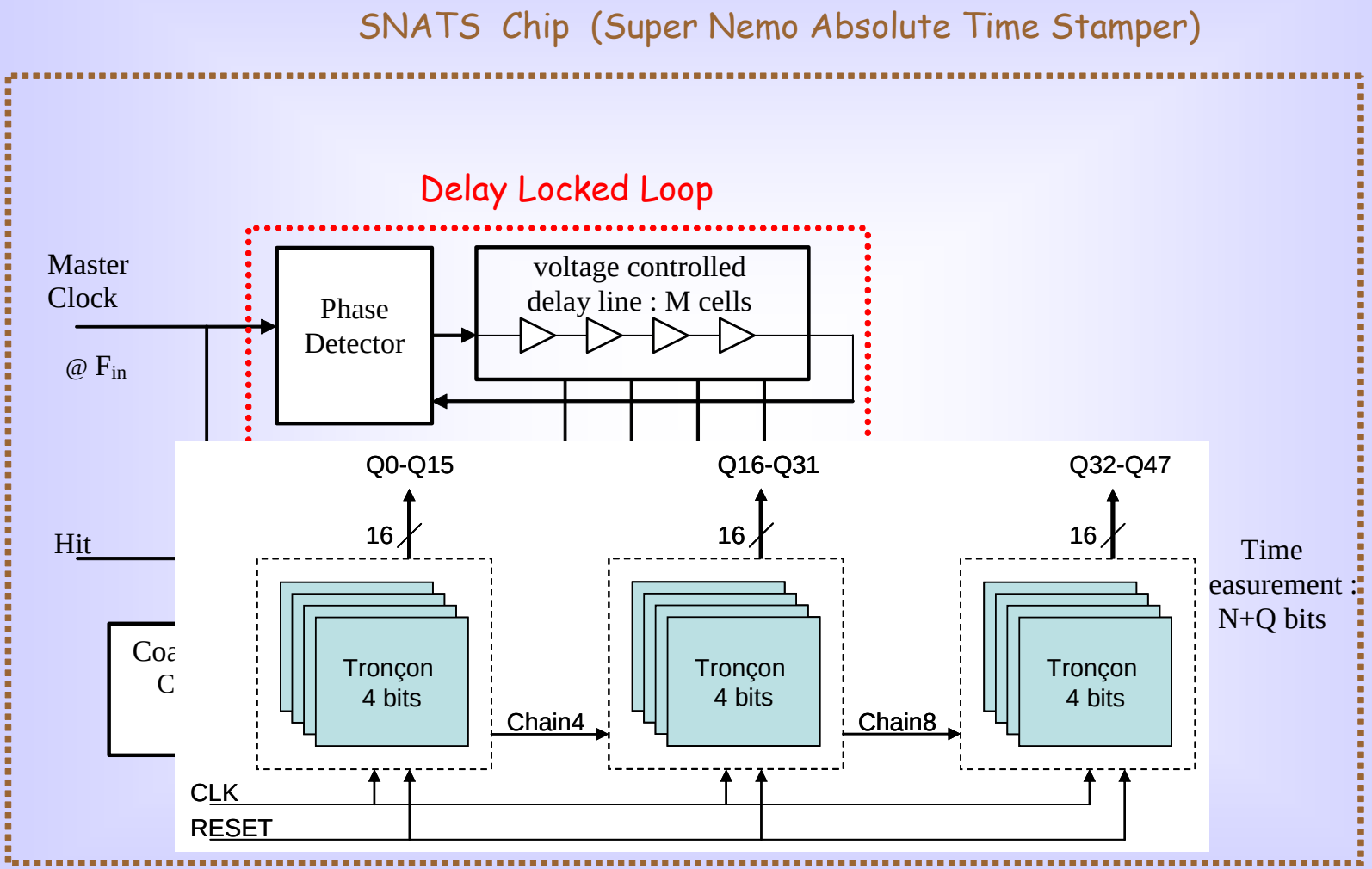
Association of a counter and an interpolator :

Fine Time Measurement → high resolution



Coarse Time Measurement → dynamic range

SNATS Chip principle :



SNATS Chip challenges :

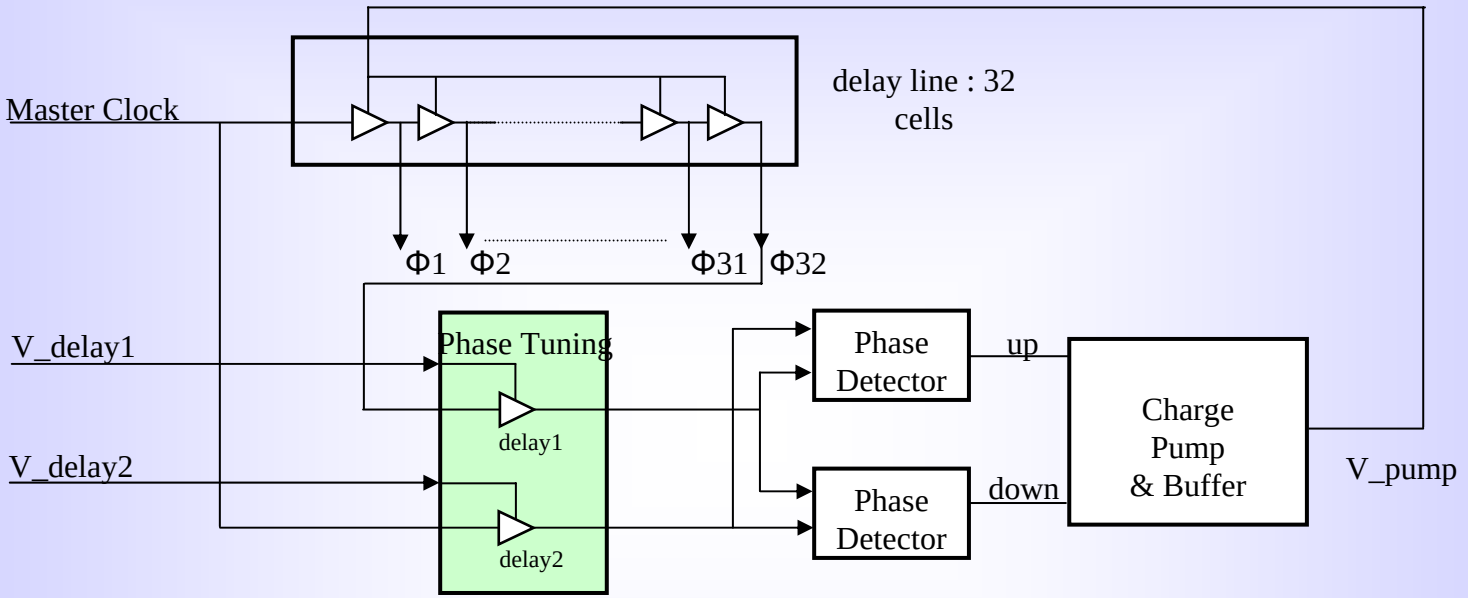
- To ensure a delay in each DLL cell lower than 200ps

  ⇒ Dealing with temperature variations
  Process & mismatch variations

- To make an easy and reliable matching between fine and coarse time

  ⇒ Improvement of architecture

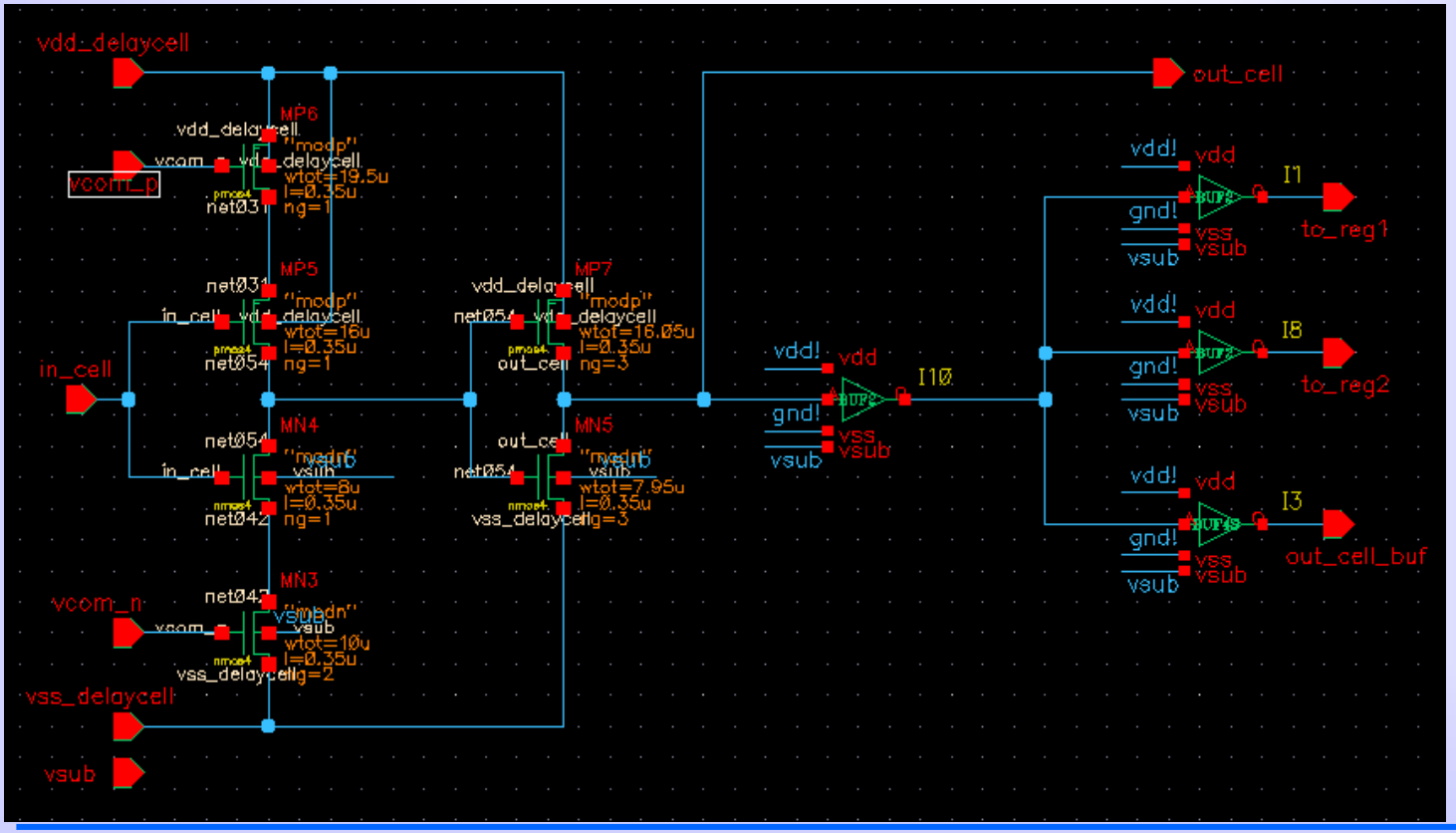
Delay Locked Loop



↳ **Phase error < 20ps**

D.L.L delay cell :

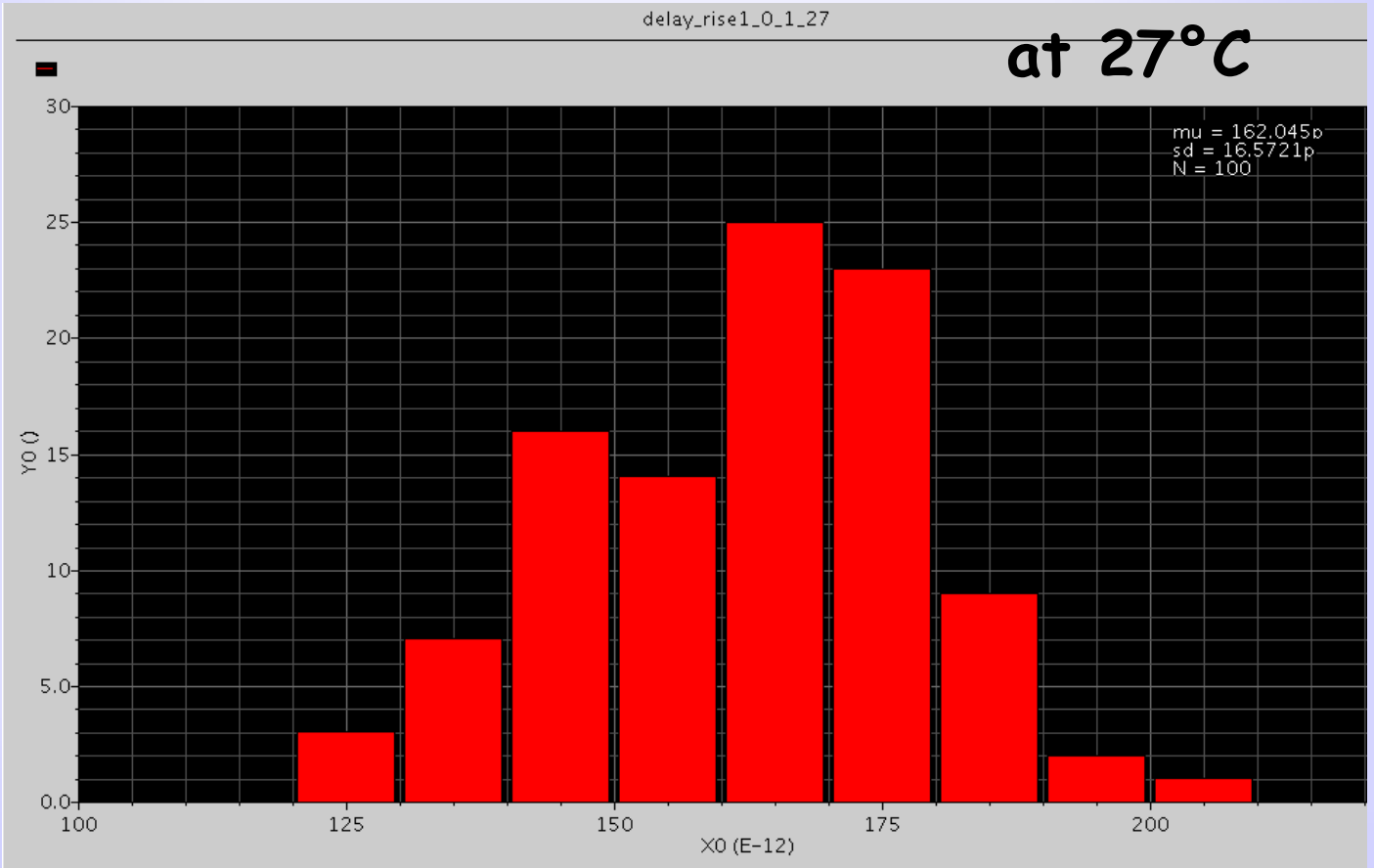
- structure optimized :
  1 starved inverter + 1 inverter followed by
  1 buffer + 3 buffers



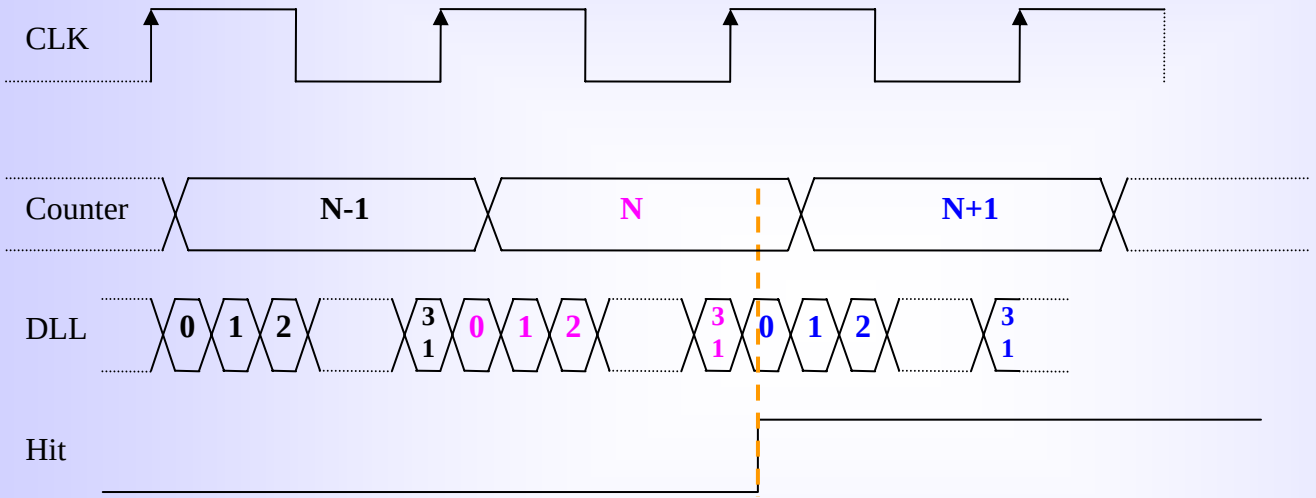
Minimum delay cell : ≈ 150ps at 27°C

≈ 166ps at 60°C

Montecarlo « Process & Mismatch »



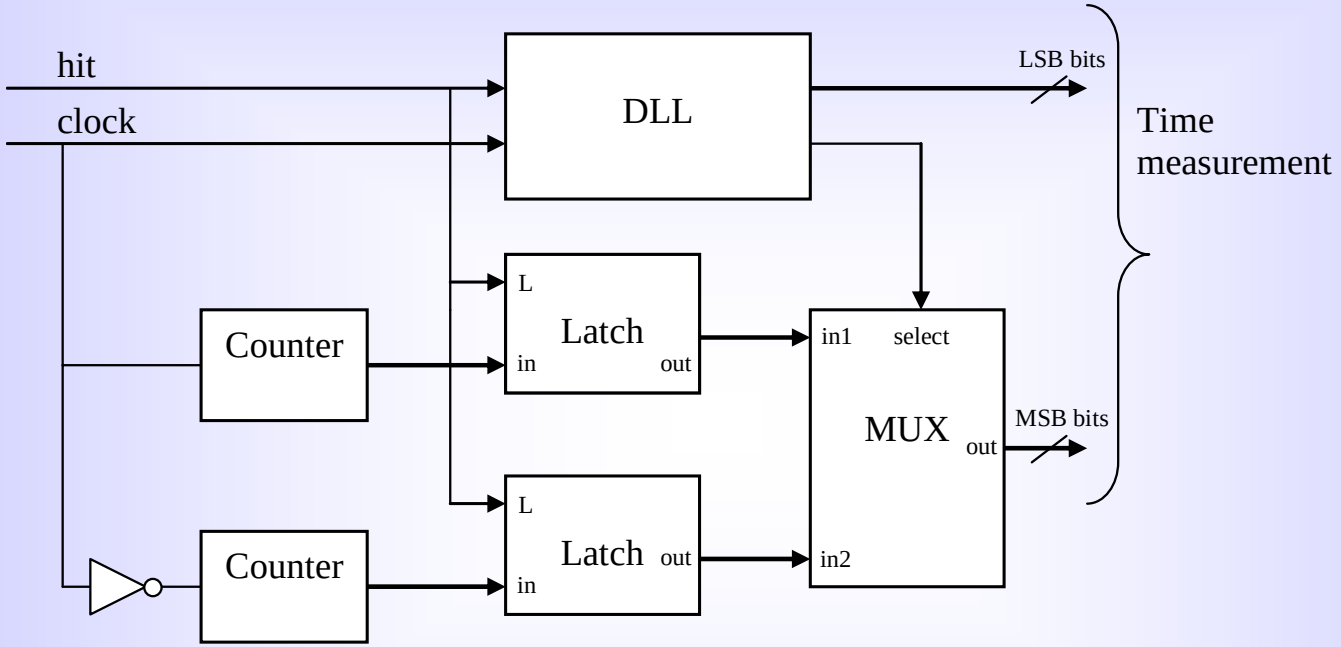
DLL and counter are synchronous but not in phase



DLL code : 0
Counter code : N instead of N+1

1 clock period error

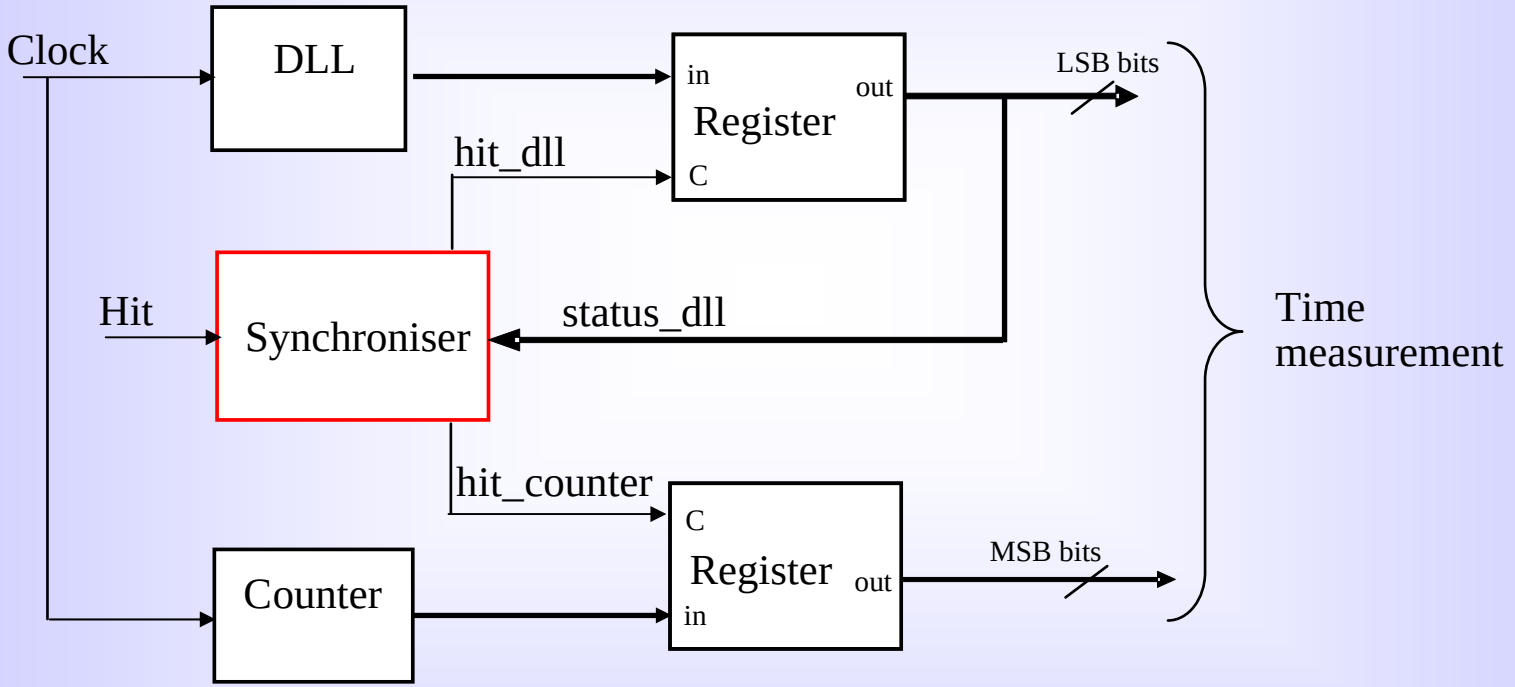
Generally: 2 chift phase counters



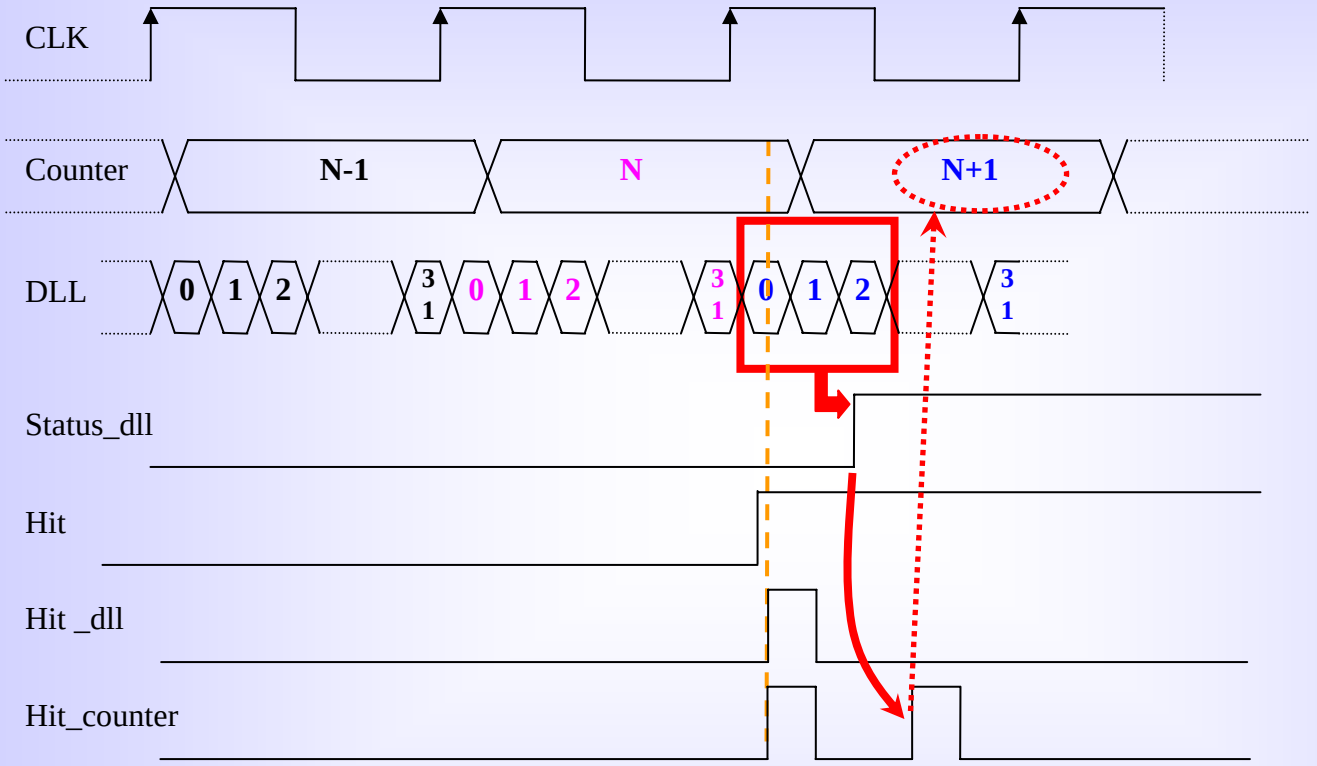
Drawbacks:

- ↗ silicon area (2 compteurs + multiplexeur)
- ↗ power consumption

Principle: production of a hit which latches the coarse time register depending on the state of latch fine time register



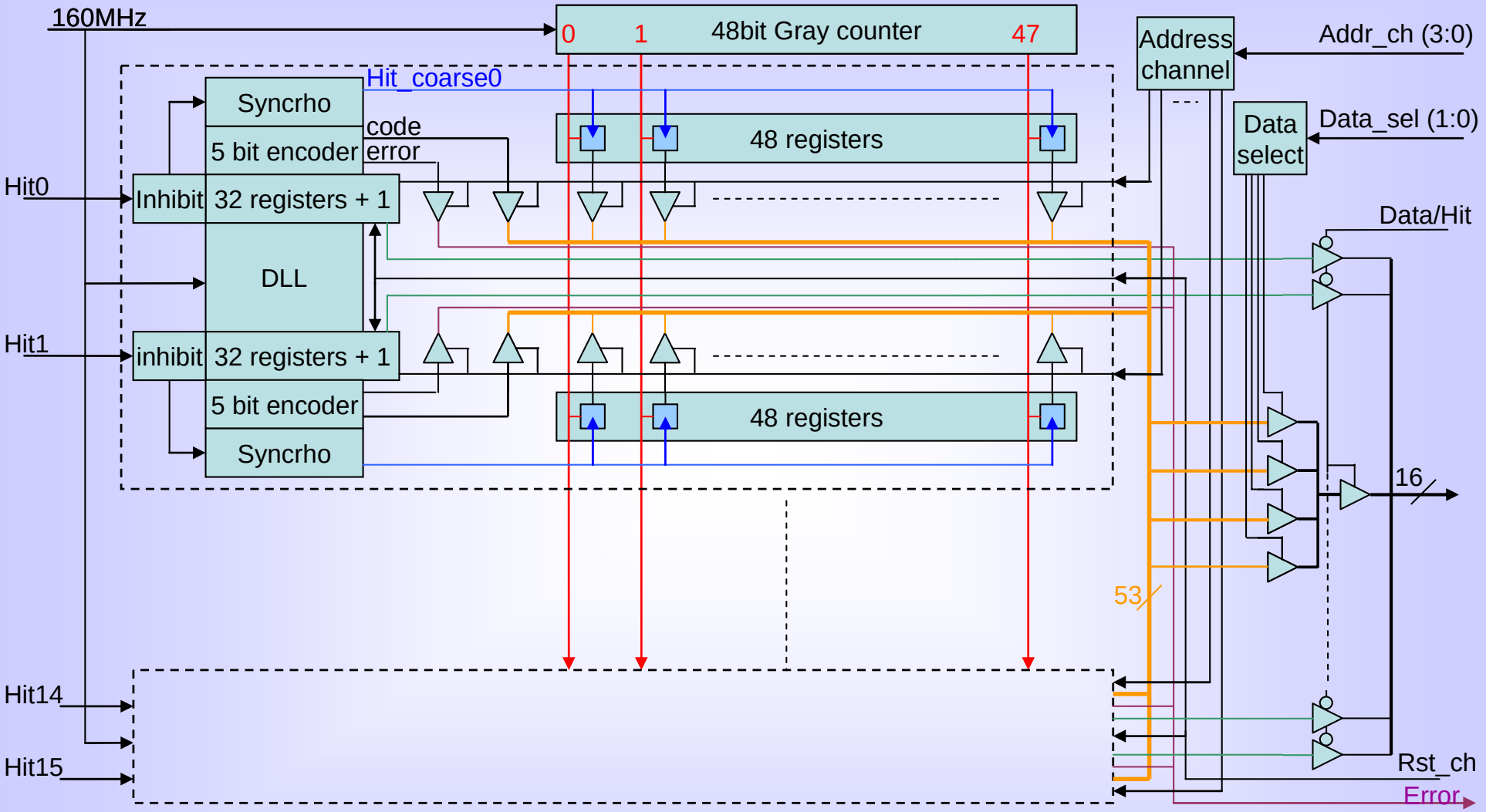
Synchronizer correction:



DLL Code : 0
Counter code : N+1

Code corrected!

SNATS Topology

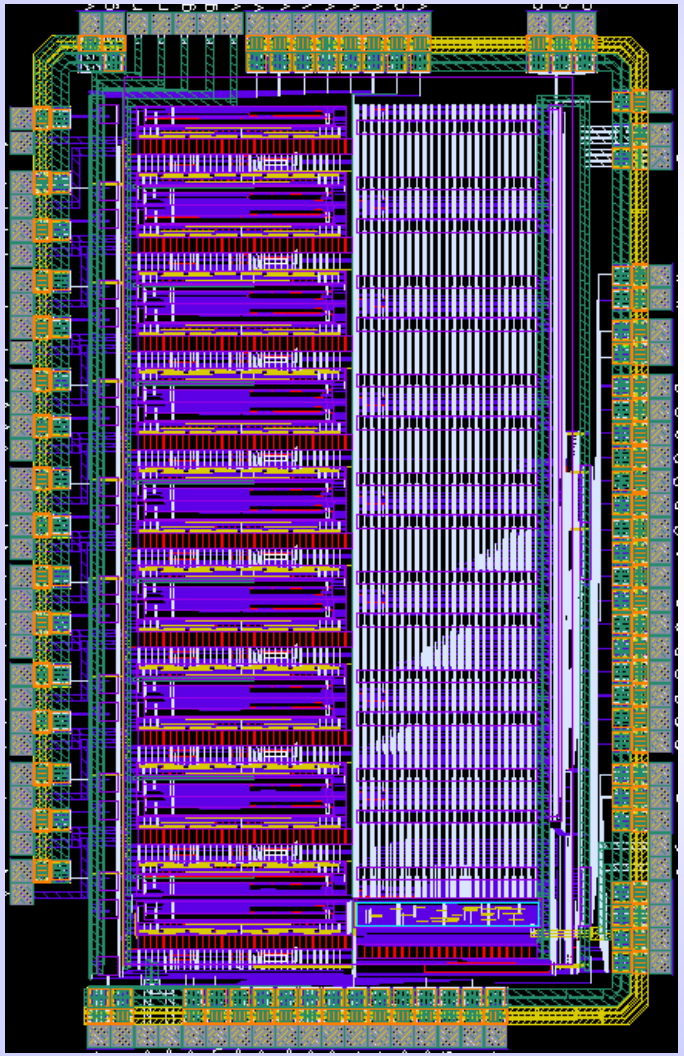


9 D.L.L's : 8 for 16 TDC channels and 1 for test

- **Master Clock: LVDS**
- **Inputs: unipolar signals from analog front end circuit with adjustable amplitude**
  - **One comparator on each input sharing a common external reference.**
- **Outputs: CMOS 3.3V level compatible with FPGAs**

SNATS : layout & package

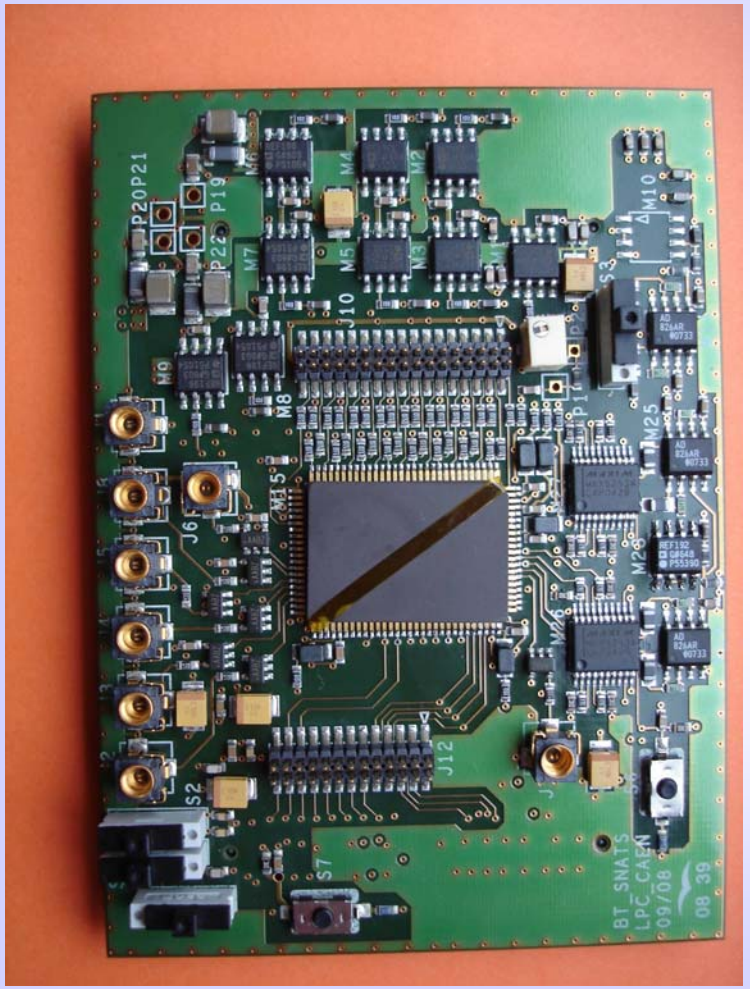
Size :4467µm X 2853µm



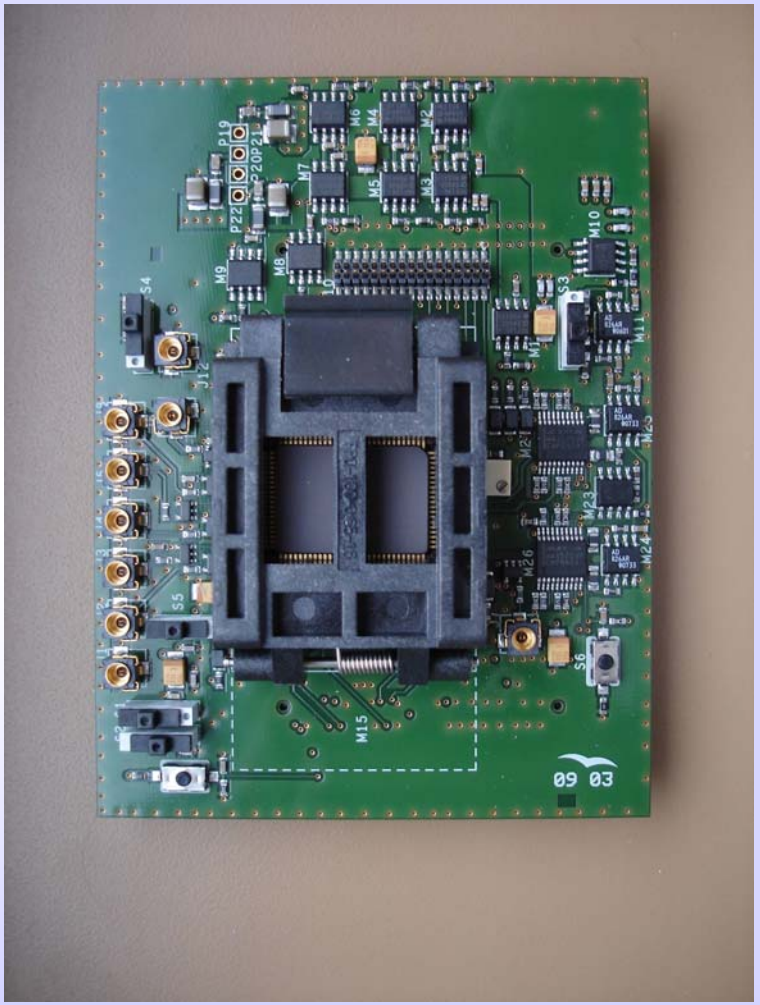
Package : CQFP100

SNATS : test boards

test-board for fine tests

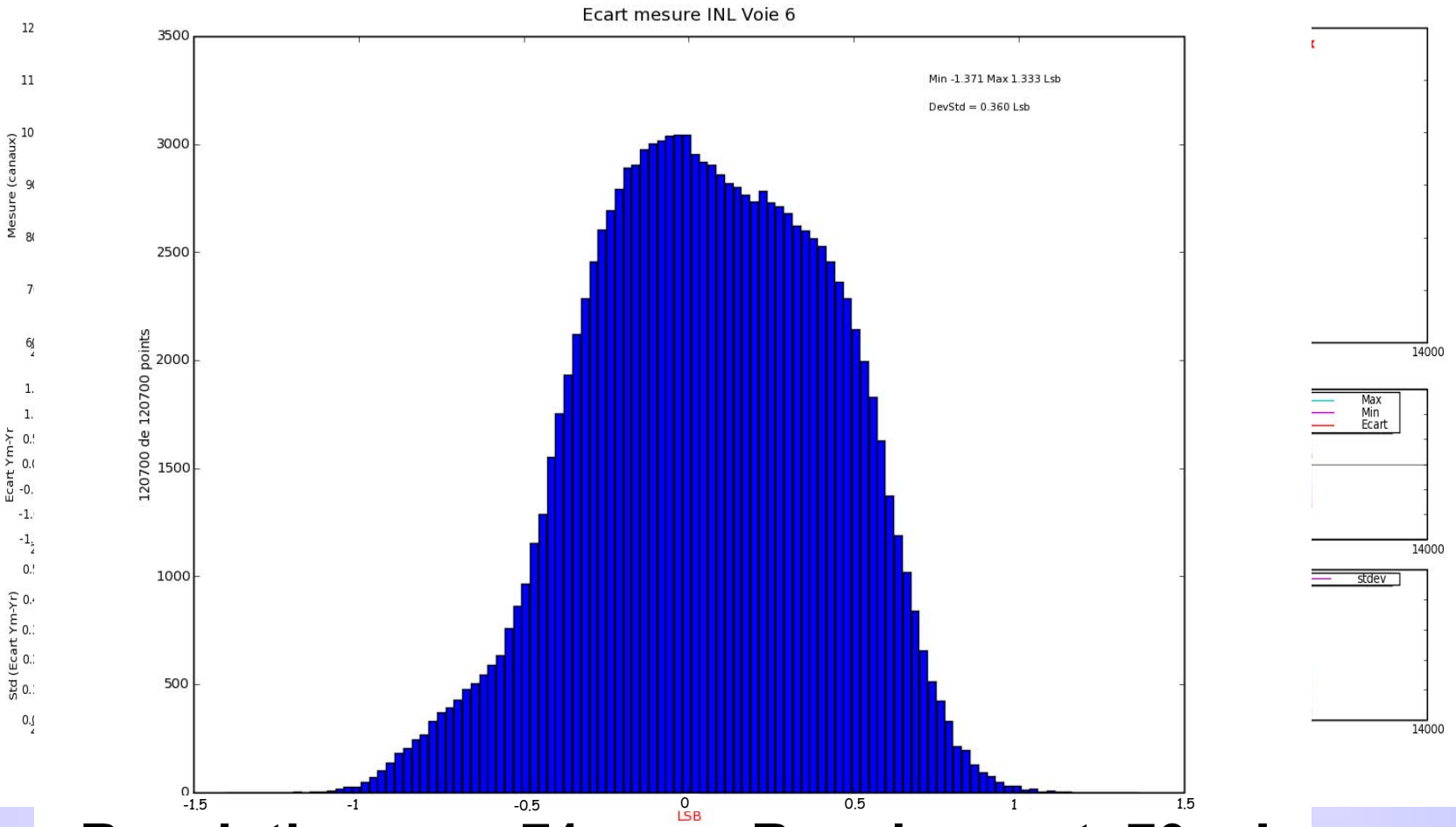


test-board for yield tests



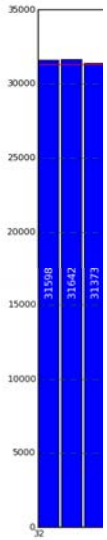
Differential Non Linearity : ± 0.2LSB

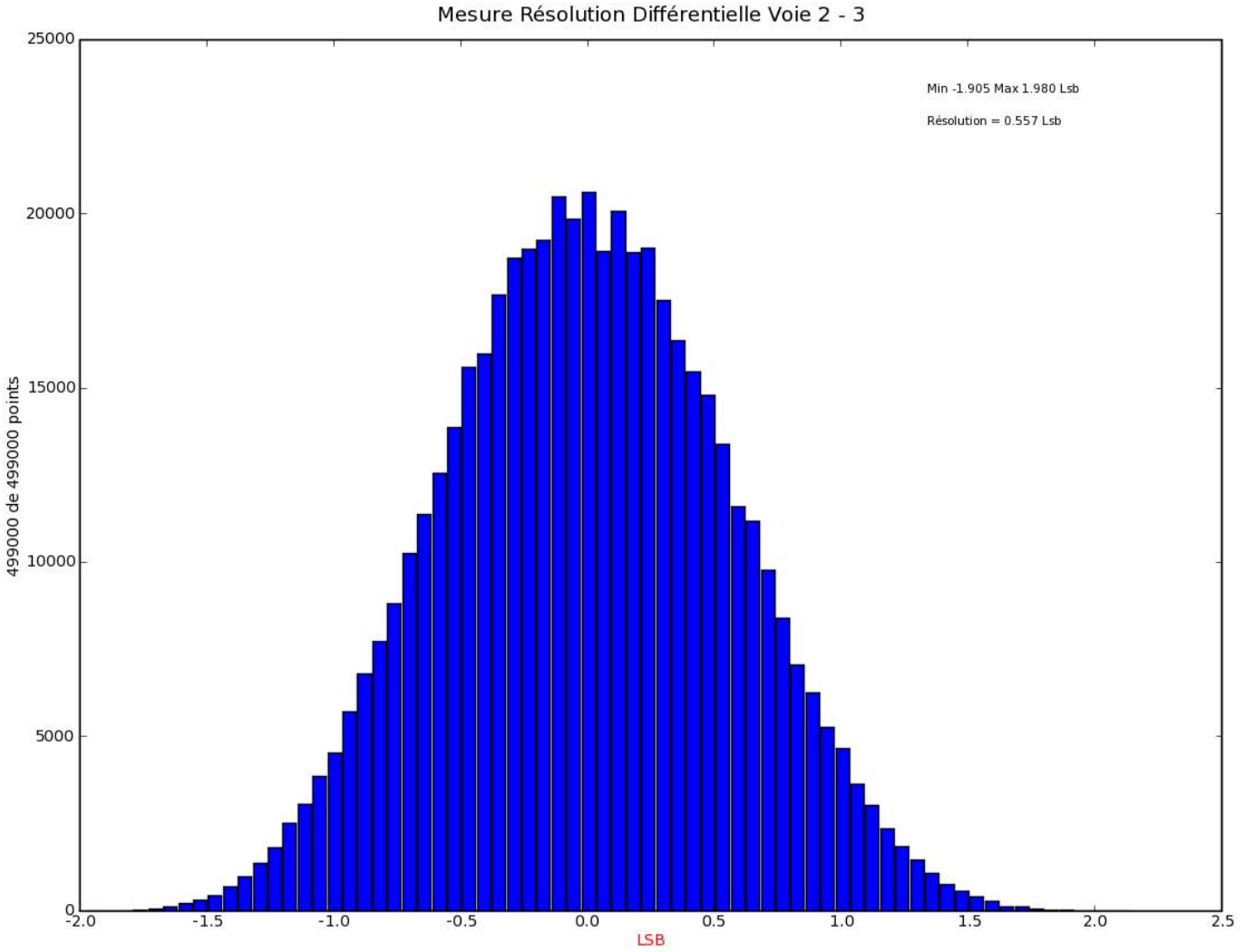
Integral Non Linearity : ± 1.3LSB



Resolution : σ = 71 ps … Requirement=70ps!

DNL for a di





Resolution for a differential time measurement : σ = 109 ps

Summary

- Power:
  - 10mA / DLL + 35mA (LVDS receivers + counter + registers..)
    $\Rightarrow$ **P= 380 mW for 16 channels**
- DNL: **± 0.2LSB**
- Differential DNL: **± 0.024LSB**
- INL: **± 1.3LSB**
- Differential INL: **± 1.98LSB**

THE END