EDIT 2015

Excellence in Detectors and Instrumentation Technologies
Frascati, Oct. 26, 2015

Lecture 2
Semiconductor Detectors

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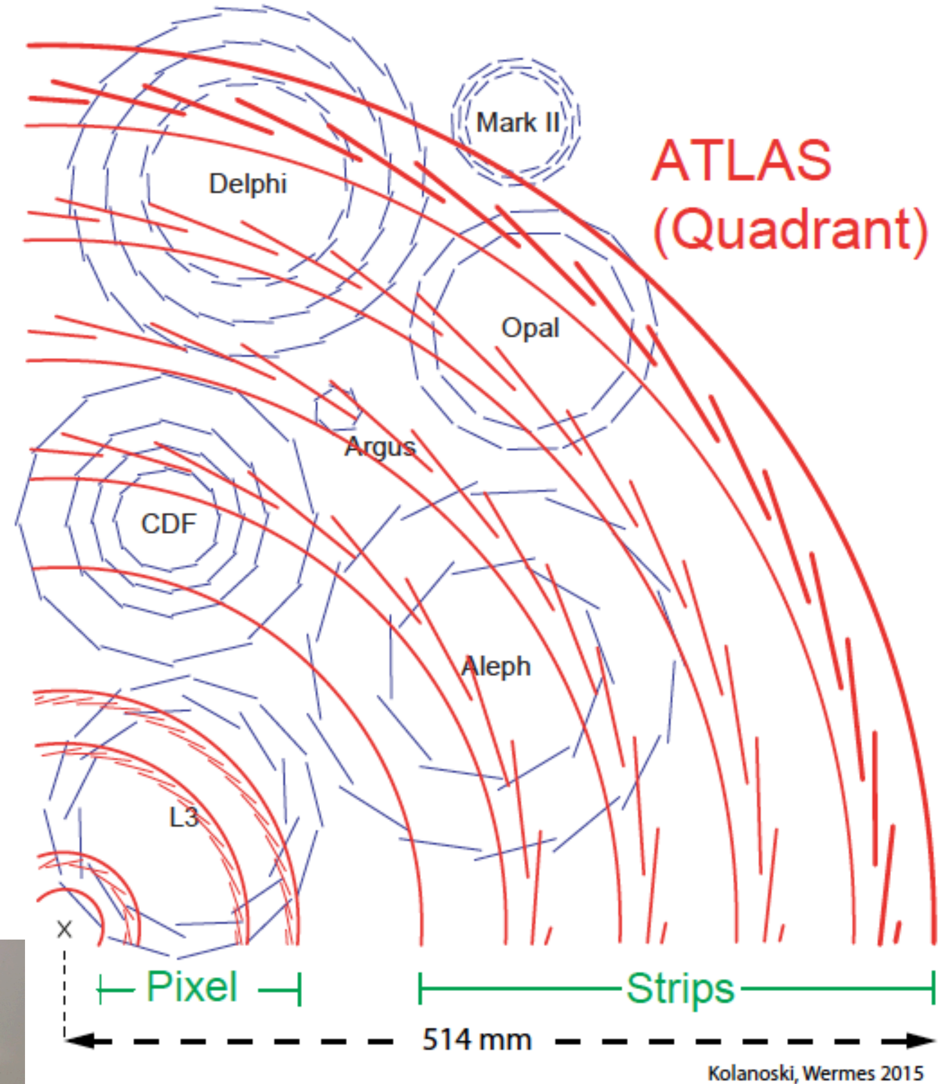
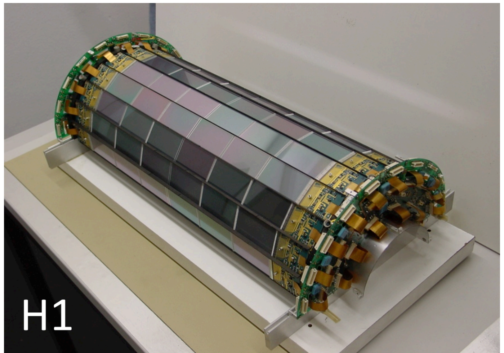
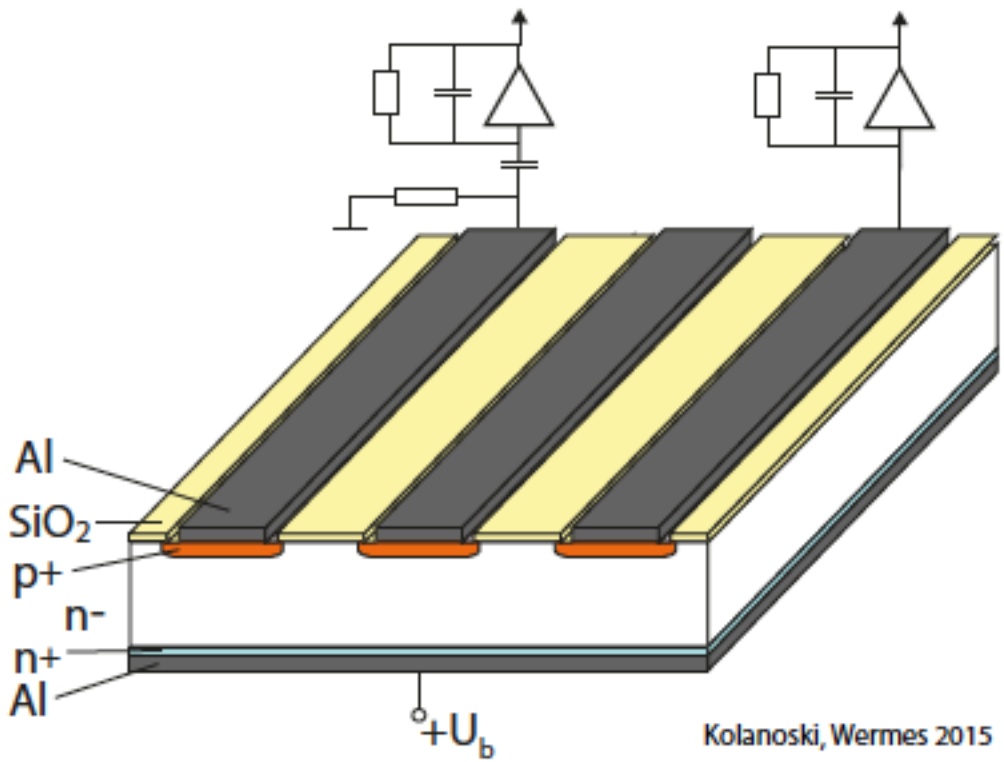
Content Lecture 2

- ❑ Semiconductor Trackers
- ❑ Microstrip Detectors
- ❑ Silicon Drift Detectors
- ❑ Hybrid Pixel Detectors
- ❑ new sensor types 3D-Si, Diamond
- ❑ Radiation Damage
  - sensor damage and curing measures
  - R/O chip damage and cures
- ❑ (Noise in Semiconductors)
- ❑ Monolithic Pixel Detectors
  - DEPFET Pixels
  - MAPS
  - Depleted CMOS Pixels (DMAPS)

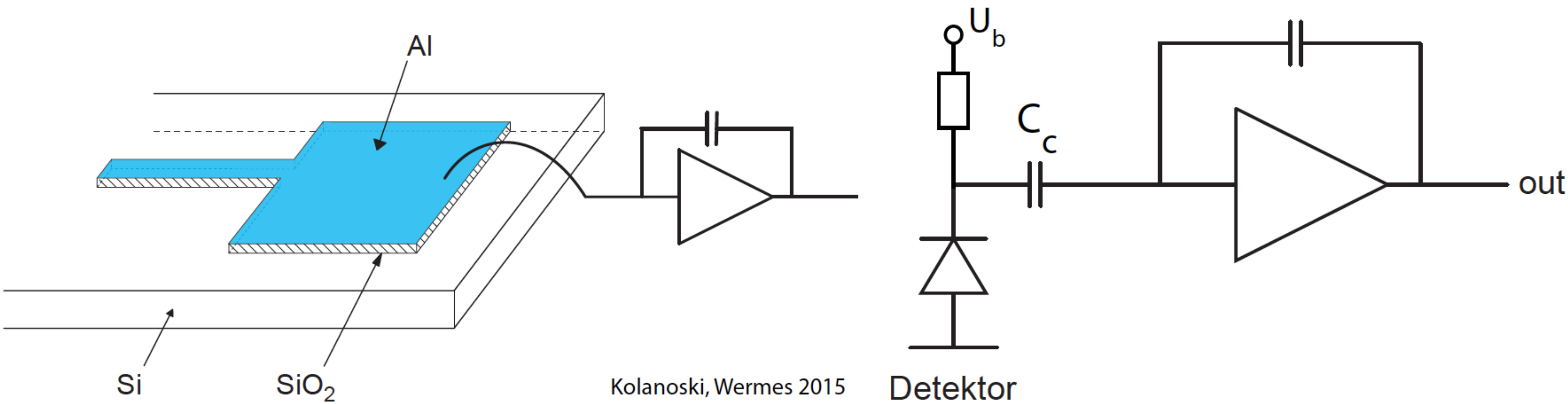




Strip Detectors



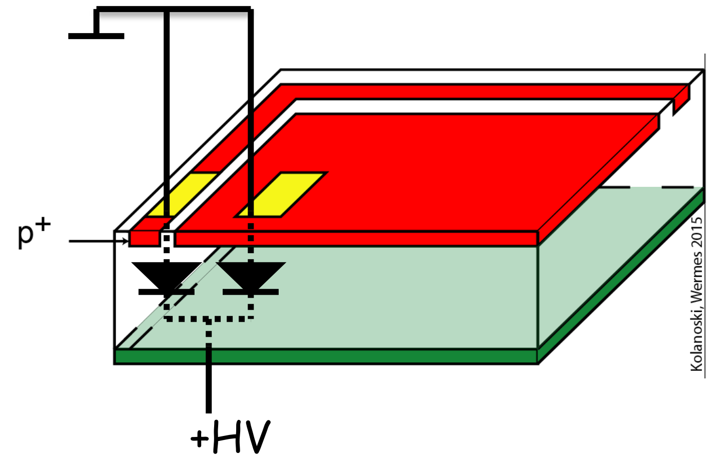
Realisation of AC readout



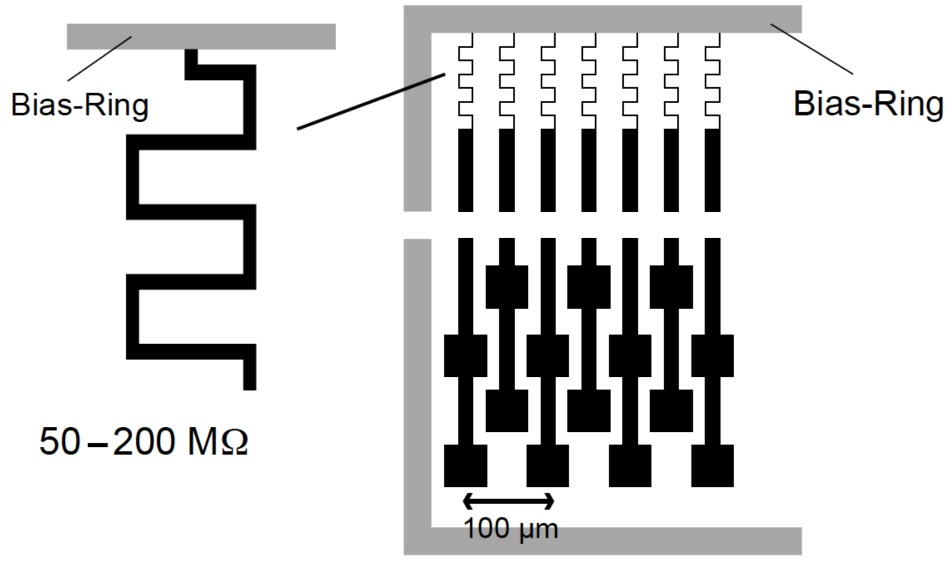
if oxide defect (pin holes) => broken channel

Biasing a strip or a pixel detector

- where is the problem?
  - the problem comes with many channels



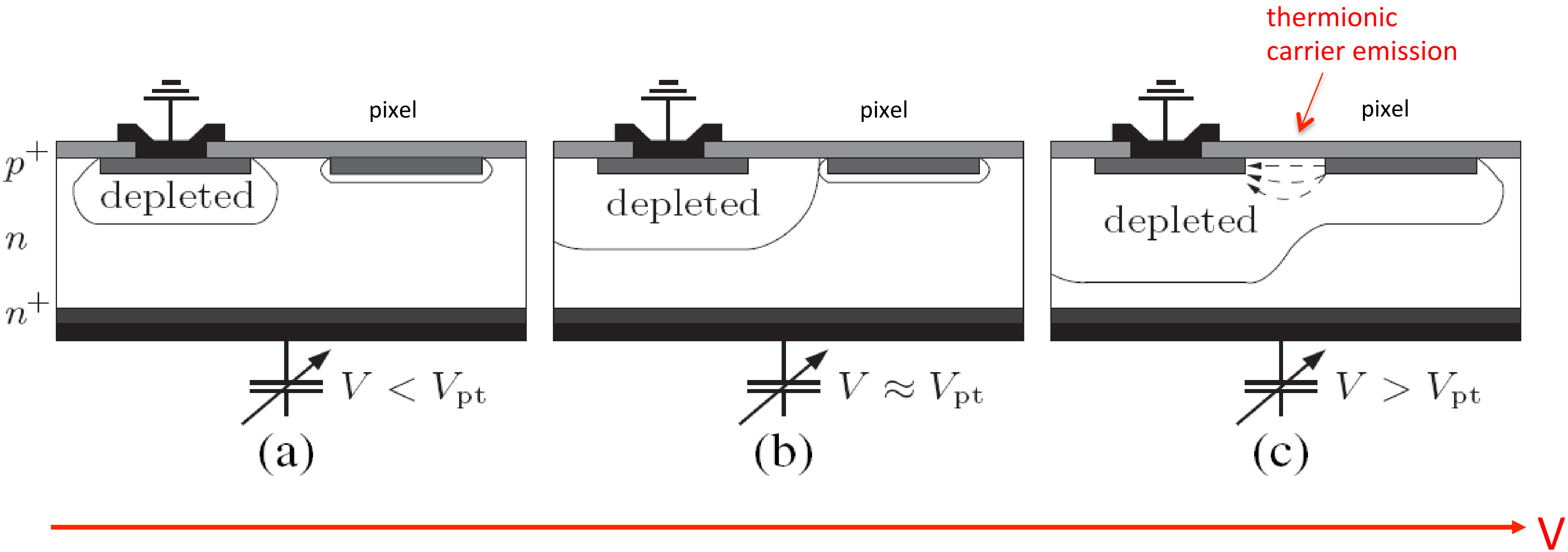
- resistive poly silicon biasing
  - polycrystalline Si on SiO_2 has area resistance of ~100 kΩ/□
  - meander structures can reach 50 – 200 kΩ (for space reasons)



☹ variations

☹ extra processing step

Punch through biasing

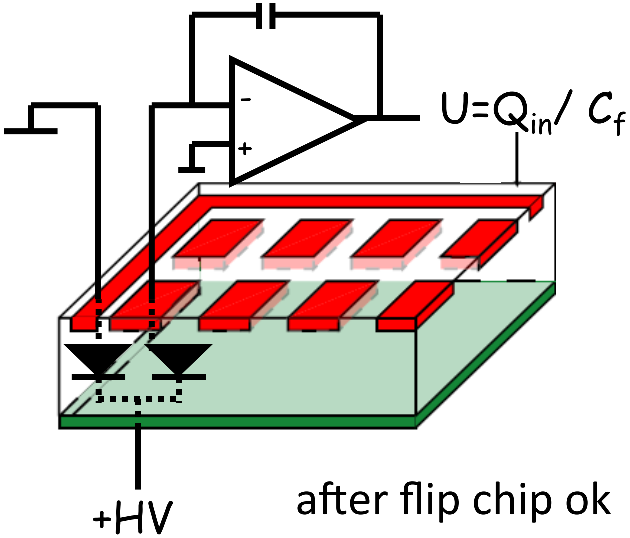


below $V_{\text{punch through}}$

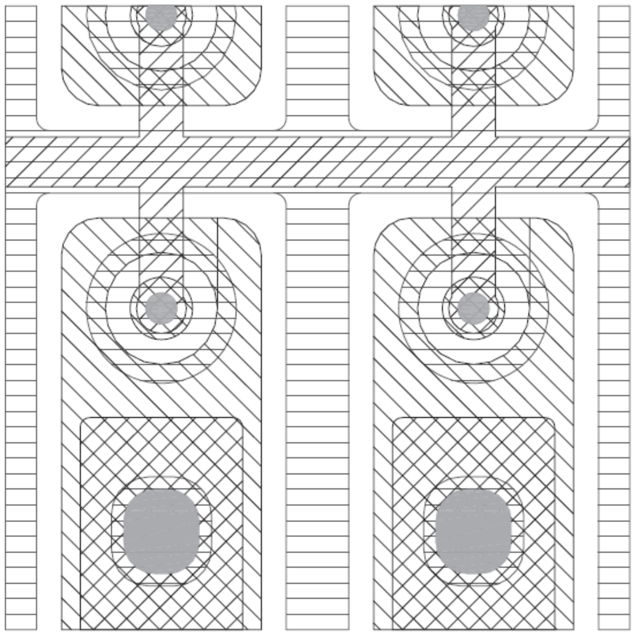
equal $V_{\text{punch through}}$

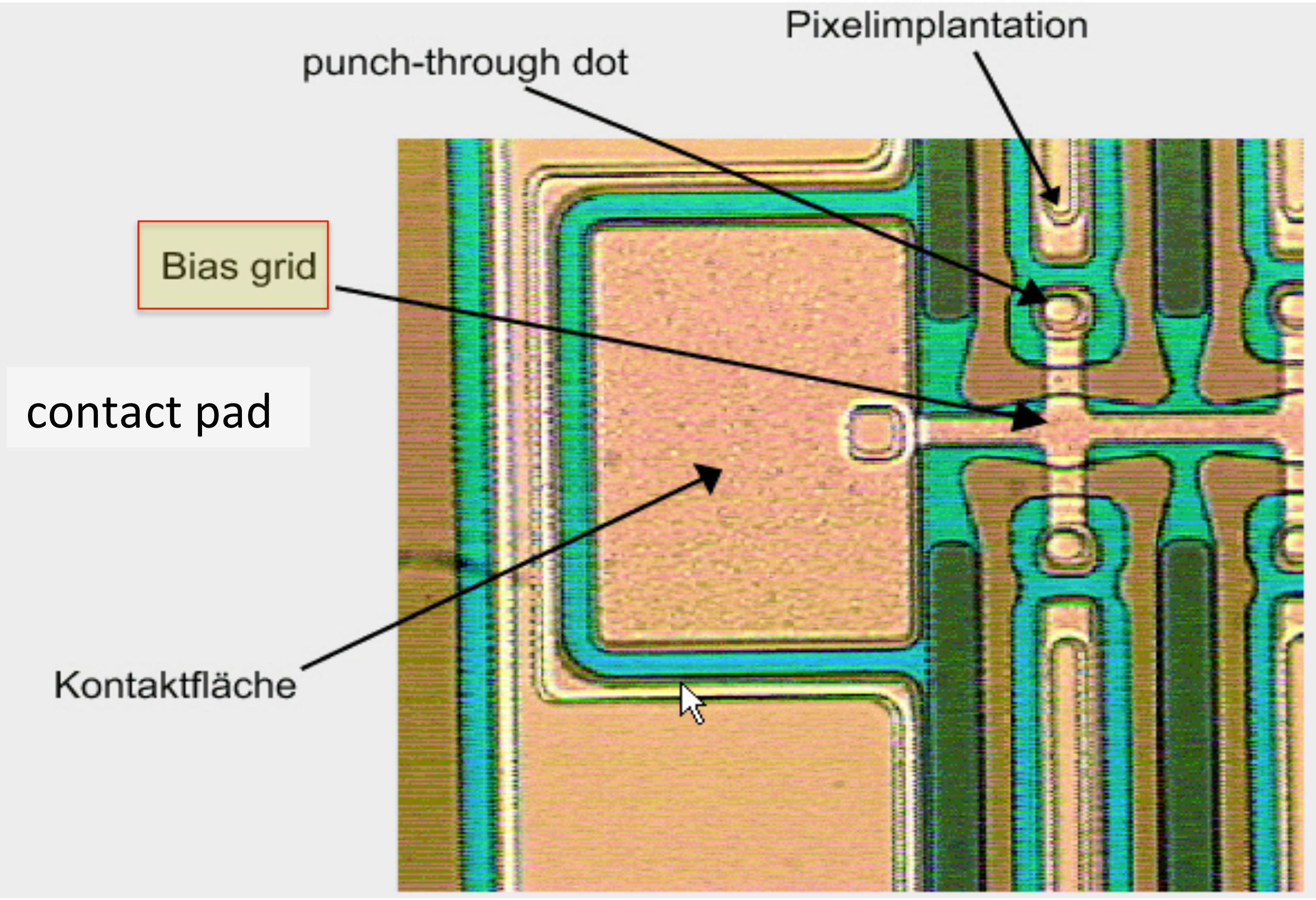
above $V_{\text{punch through}}$

How to bias a pixel detector … with many many channels?



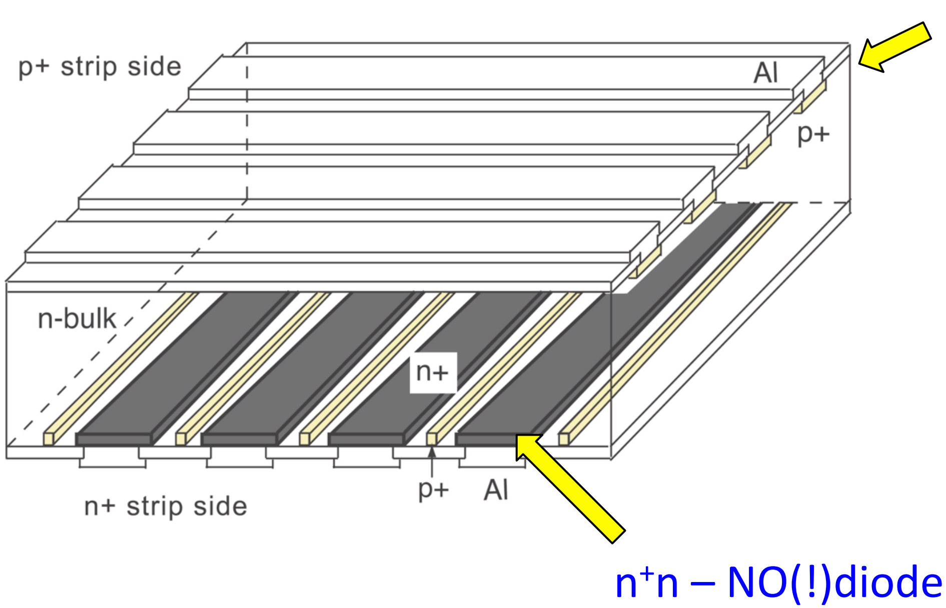
- ❑ answer: through the virtual ground of the preamplifier
- ❑ but one wants to test the sensor w/o chip, i.e. before you put 16 chips on (yield!)



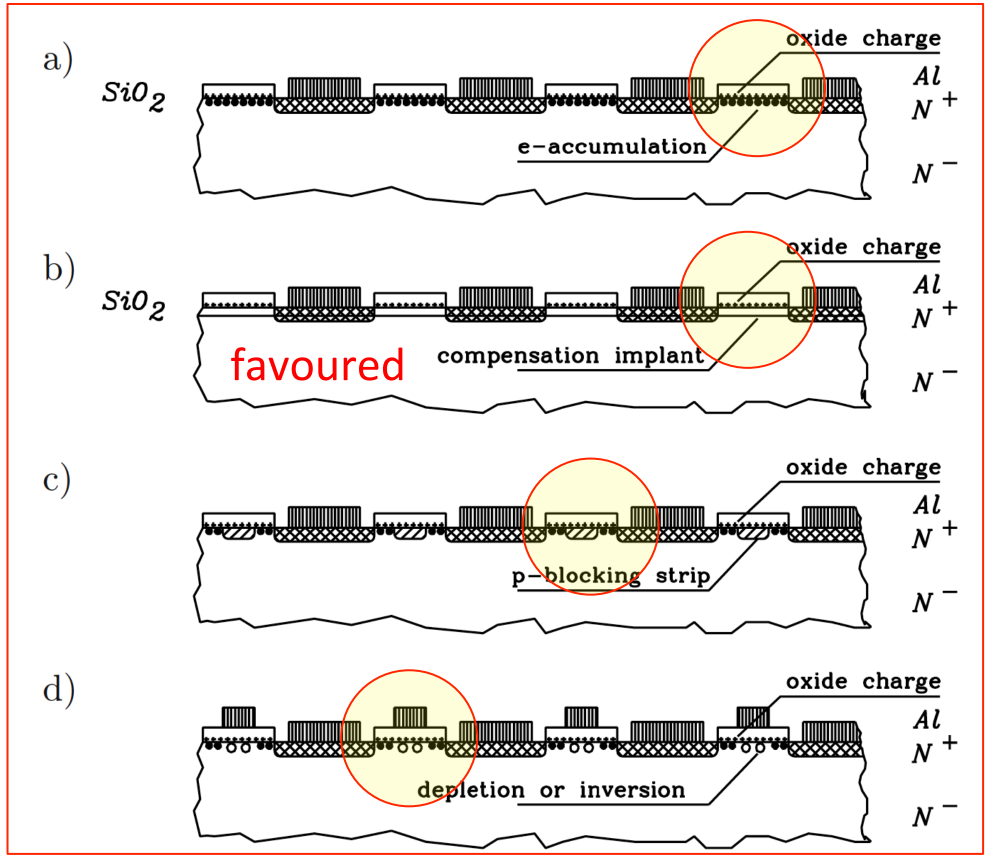


Double sided detectors

- exploit the fact that a signal is induced on both sides of the detector



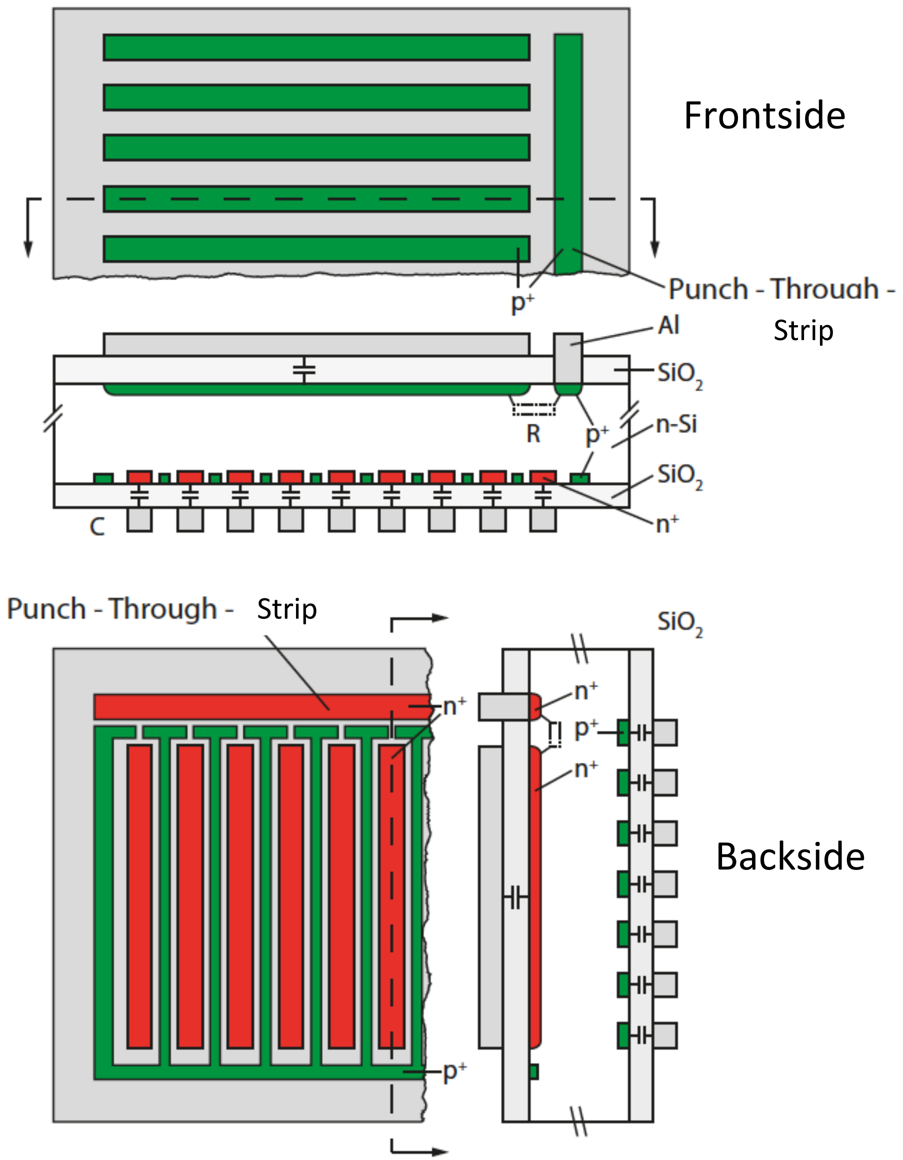
CURES



- but where is the diode?

- need take measures to prevent electron accumulation layer

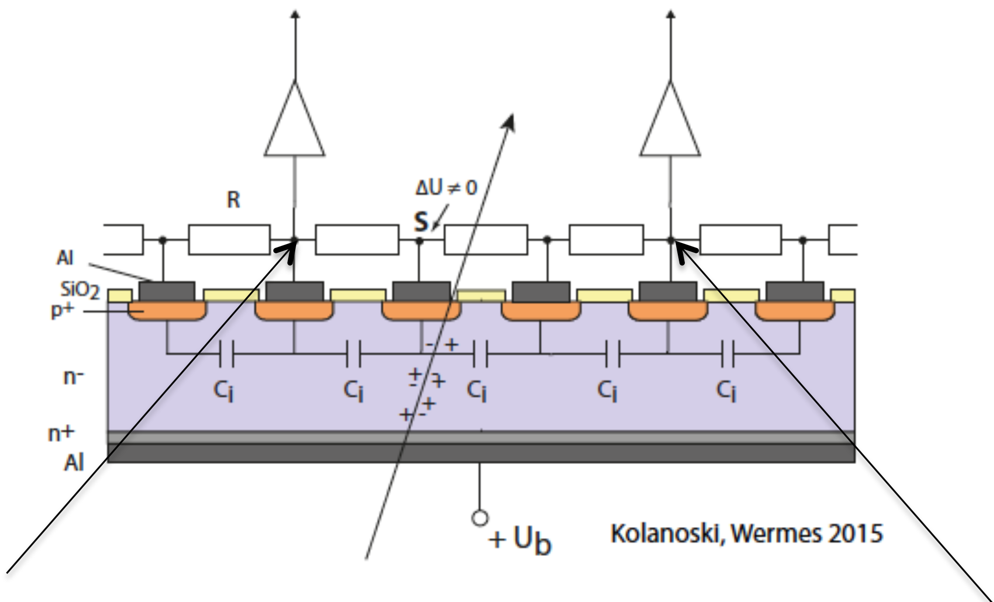
A double sided strip detector layout



from: G. Lutz, Semiconductor Radiation Detectors

Capacitive charge division

- a method to obtain better spatial resolution for a given number of channels
- the output signal is divided according to the series capacitances to either side



$$Q_L = \frac{2}{3}Q \qquad Q_R = \frac{1}{3}Q$$

A typical strip detector module (here ATLAS)

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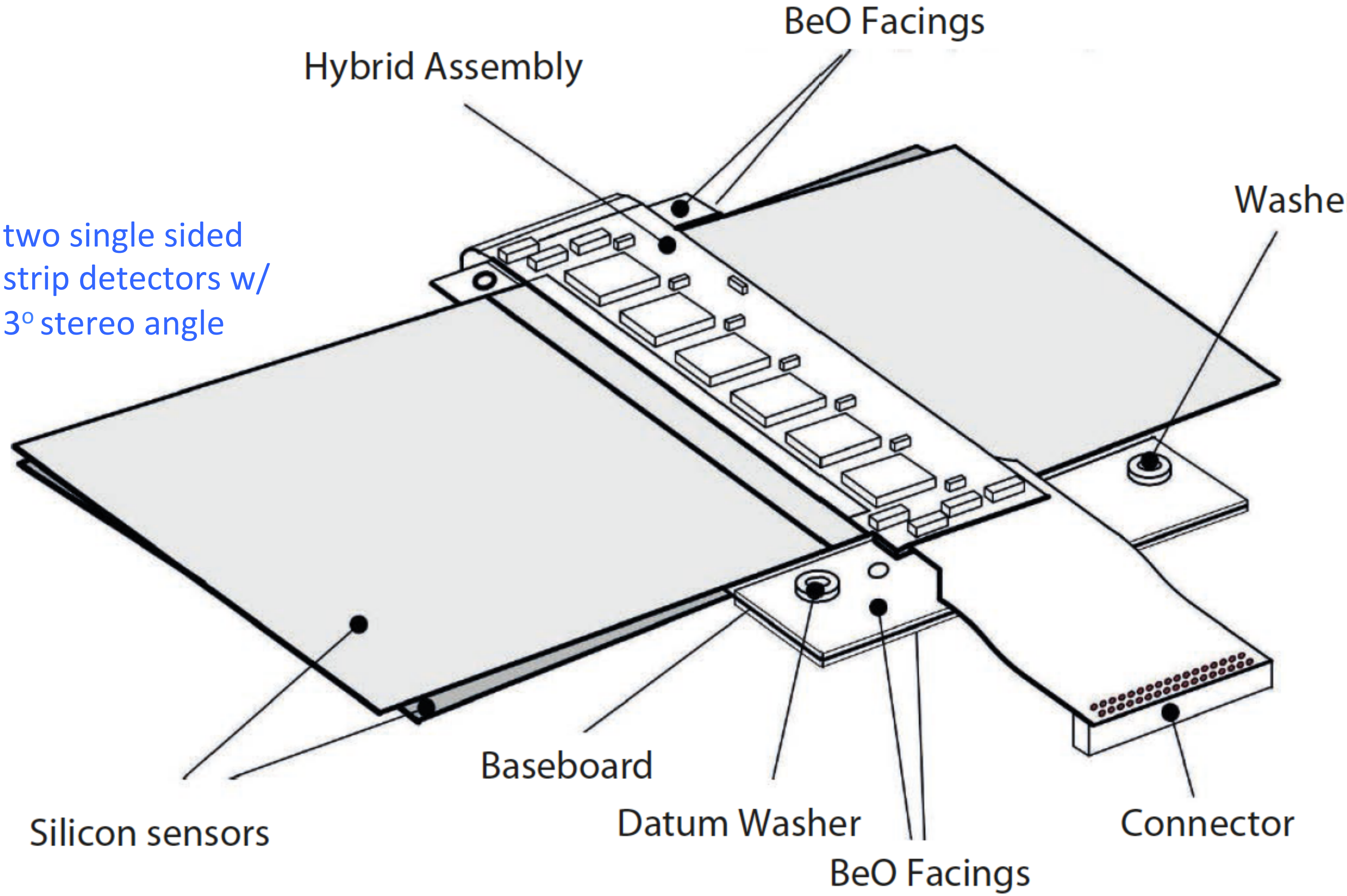
two single sided
strip detectors w/
3^{o} stereo angle



Tracking Detectors: CMS (pp collisions)

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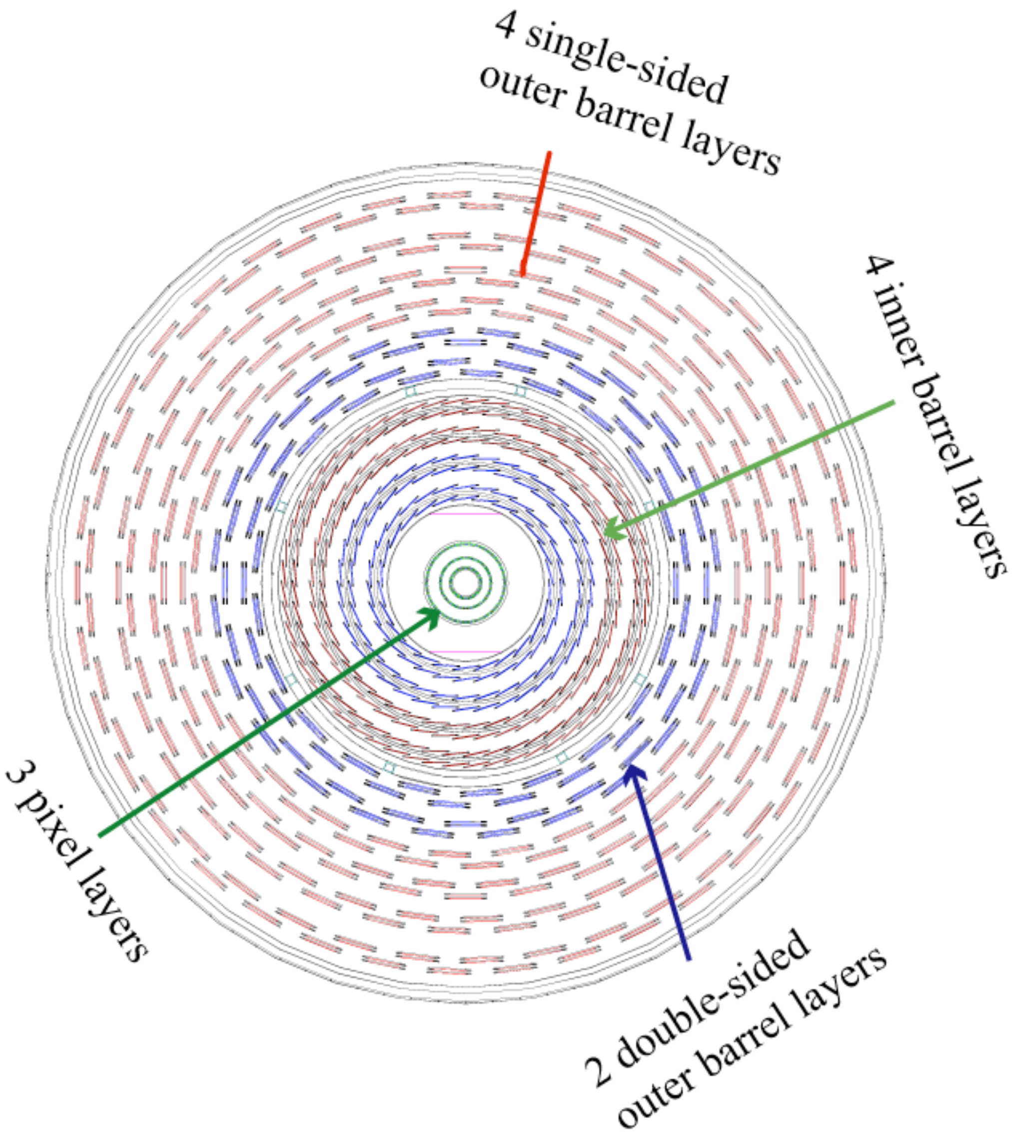
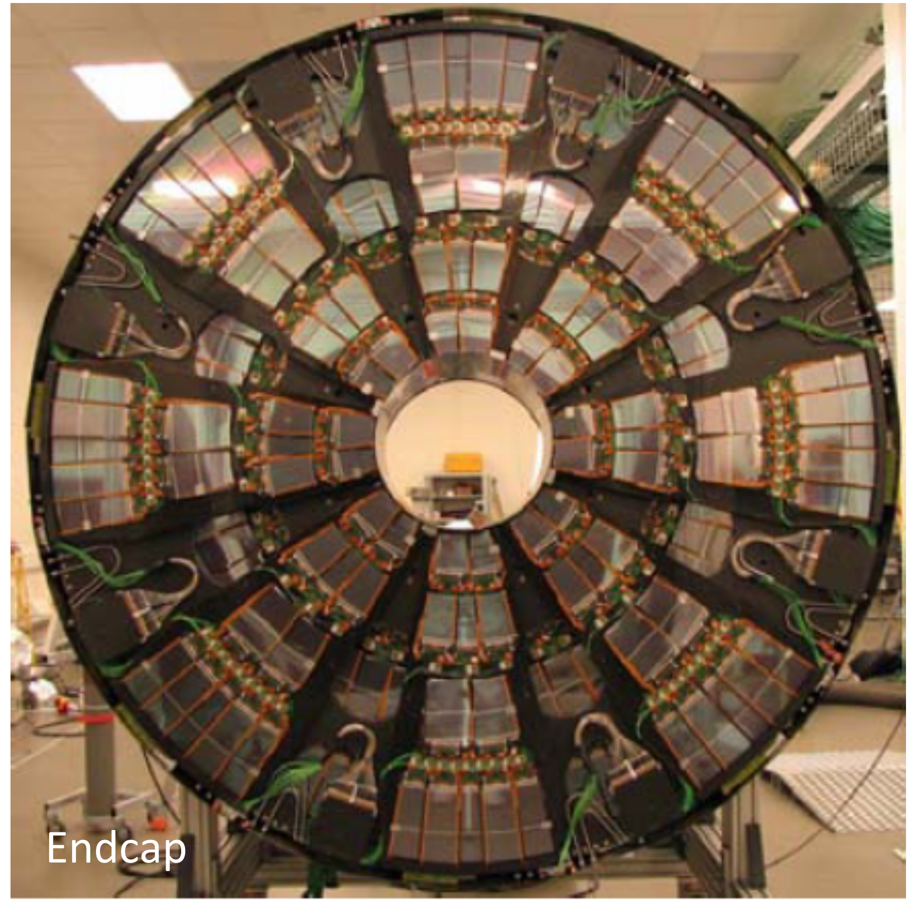
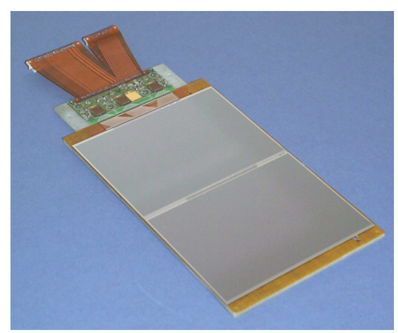
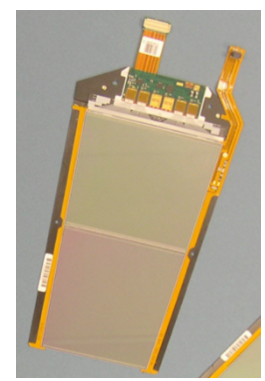






modules

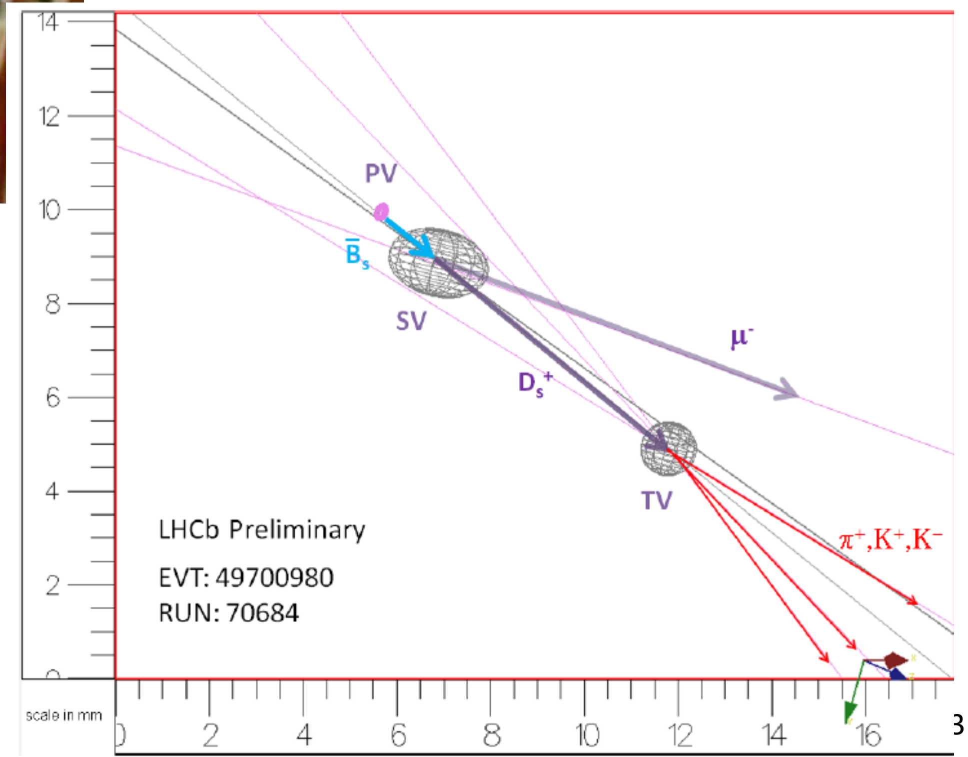


Largest Si – Detector ever (~200 m^2)

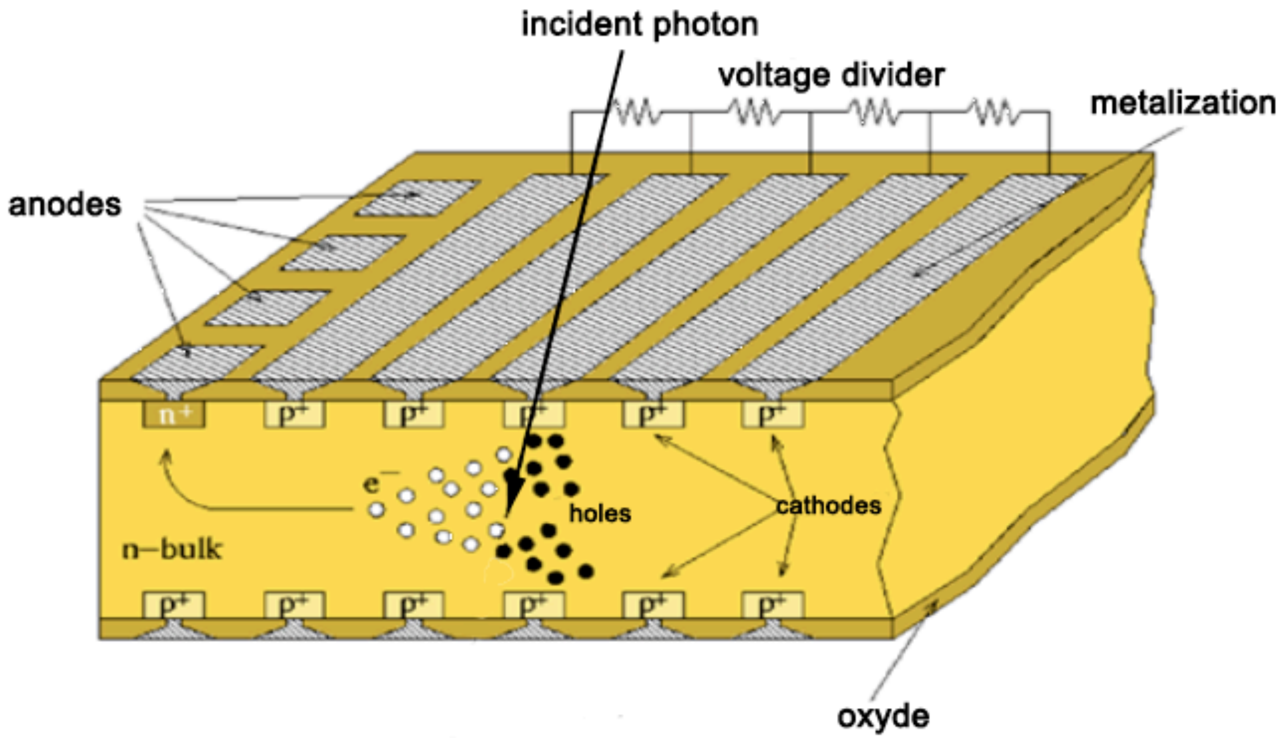
Tracking Detectors LHCb VErtex LOcator

- 42 Si strip detector elements
- 10 µm resolution
- approaches the interaction point down to 7 mm

$$pp \to B_s^0 + X \to D_s^+ \mu^- \bar{\nu}_\mu + X$$
$$\to K^+ K^- \pi^+ + \mu^- \bar{\nu}_\mu + X$$

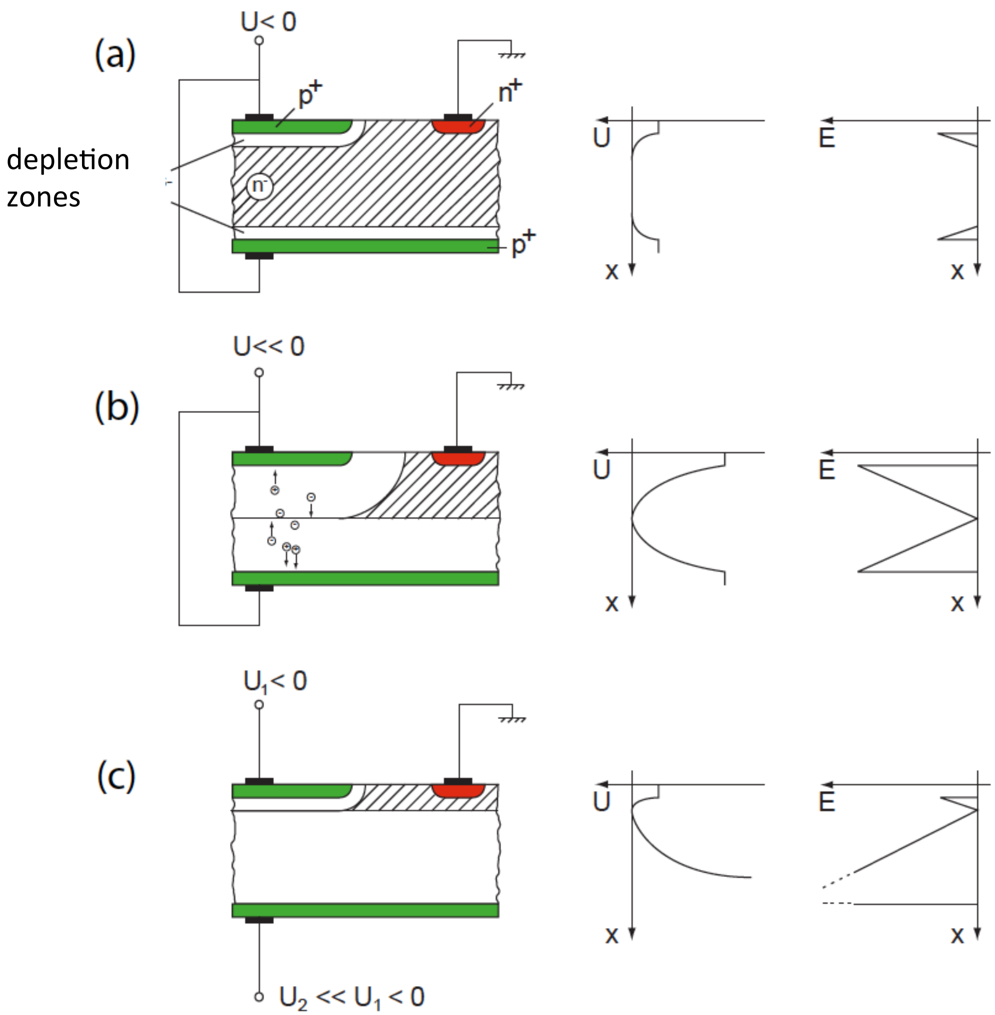


The silicon drift chamber



The principle of sidewards depletion

Gatti, Rehak (1984)



$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho}{\epsilon_0 \epsilon_r}$$

1-dim.
Poisson Equation

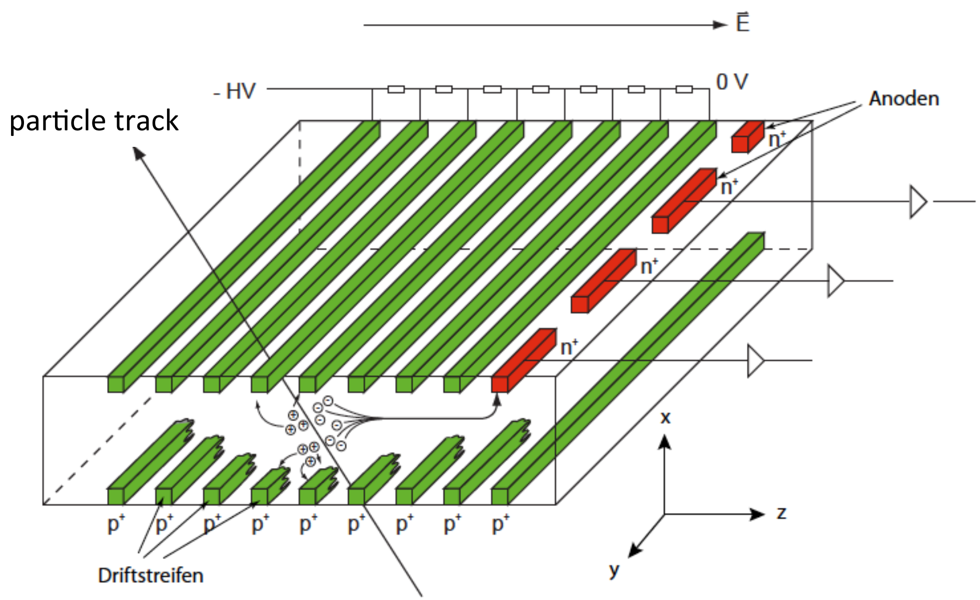
with boundary condition

$$\phi(x = -\tfrac{d}{2}) = \phi(x = \tfrac{d}{2}) = U_0(z)$$

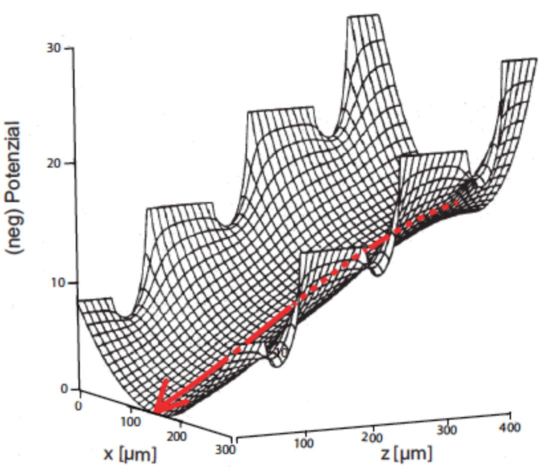
$$\phi(x, z) = U_0(z) - \frac{\rho}{2\epsilon_0 \epsilon_r}\left(x^2 - \frac{d^2}{4}\right)$$

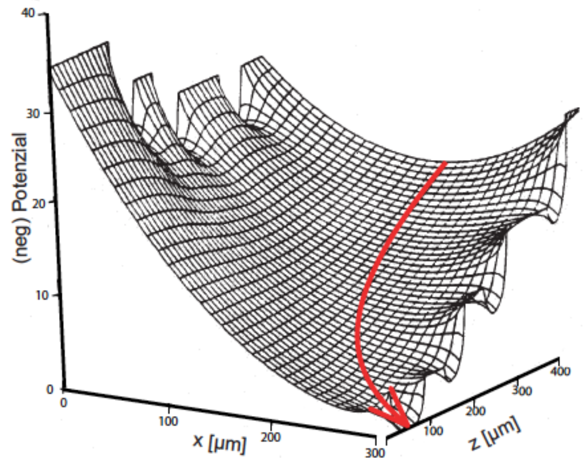
quadratic potential for electrons

The silicon drift chamber principle



Si Drift Chamber Principle

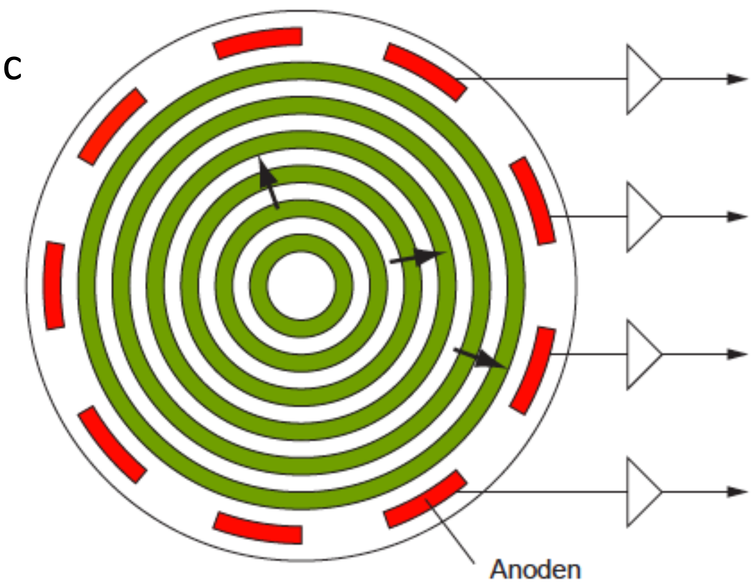


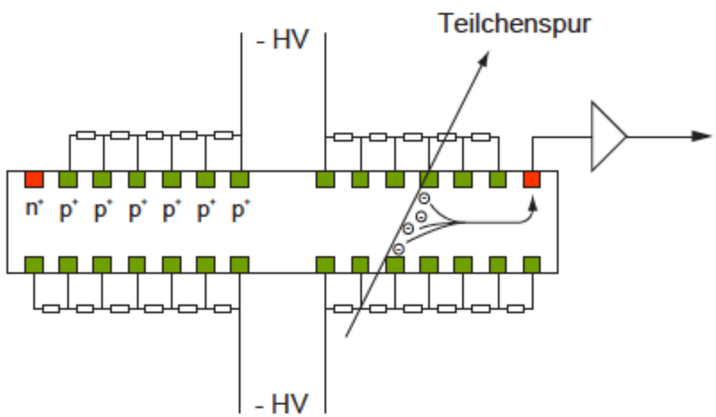


- ❑ add a linear potential gradient on top of the parabolic potential
- ❑ in anode region "push" electrons to anode electrodes
- ❑ PROS
  - 2-dim high resolution (typ. <50µm) readout w/ only few R/O electrodes
  - very good 2-particle separation
- ❑ CON
  - drift times typ. ~µs
    => not useful for high rate exp.
- ❑ application: Heavy Ion Experiments

Heavy Ion Experiment CERES/NA45

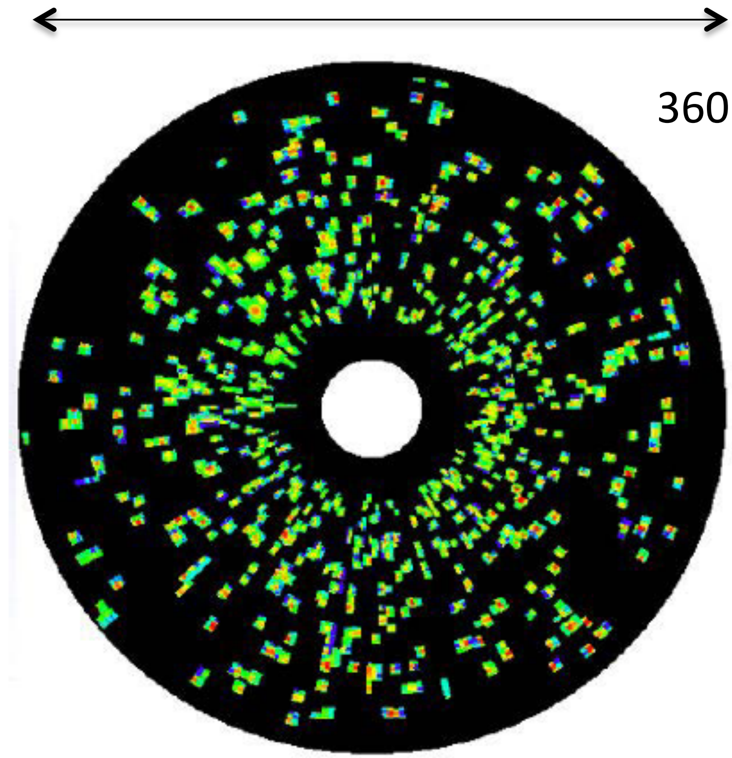
schematic only

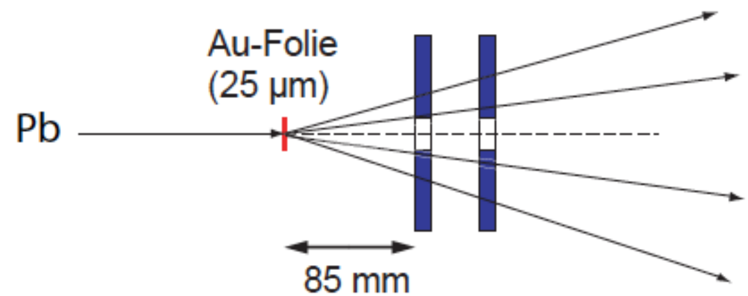




6.4 cm

360 anodes

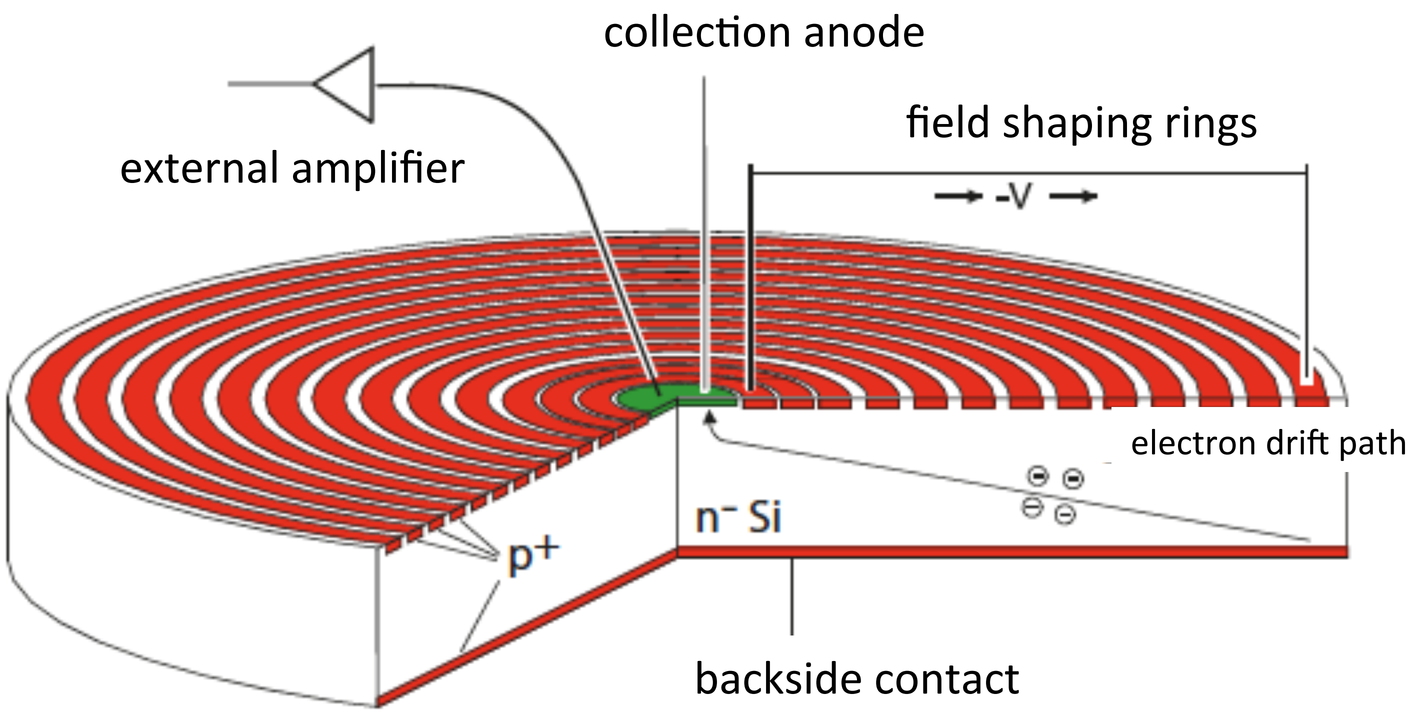




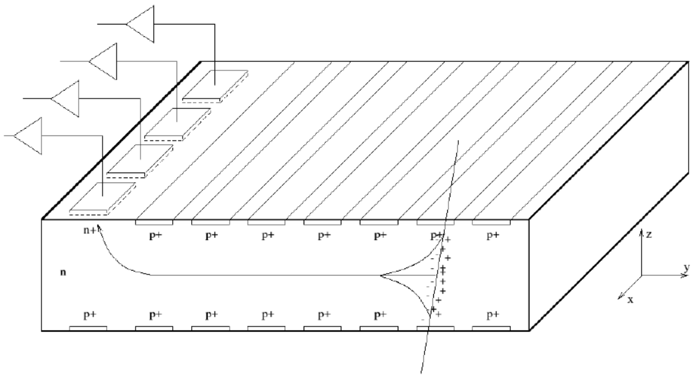
only 360 R/O anodes (every 1°)

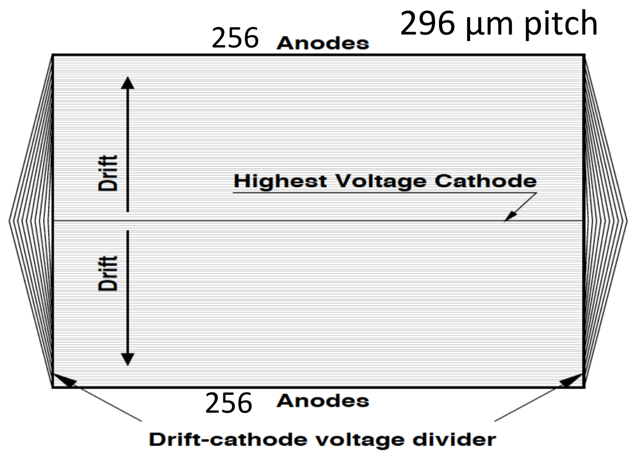
Silicon Drift Chamber for Imaging = SD-Diodes

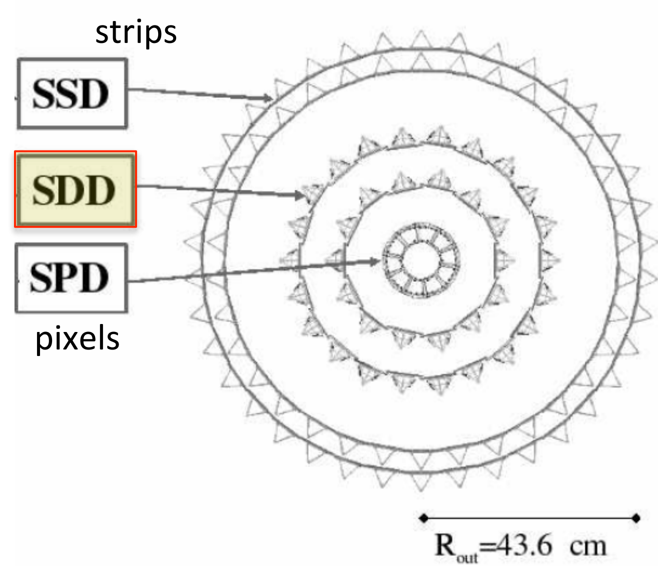
- only **one** anode in center
- small capacitance (10fF) => very low noise (~few e-)
- large sensing area



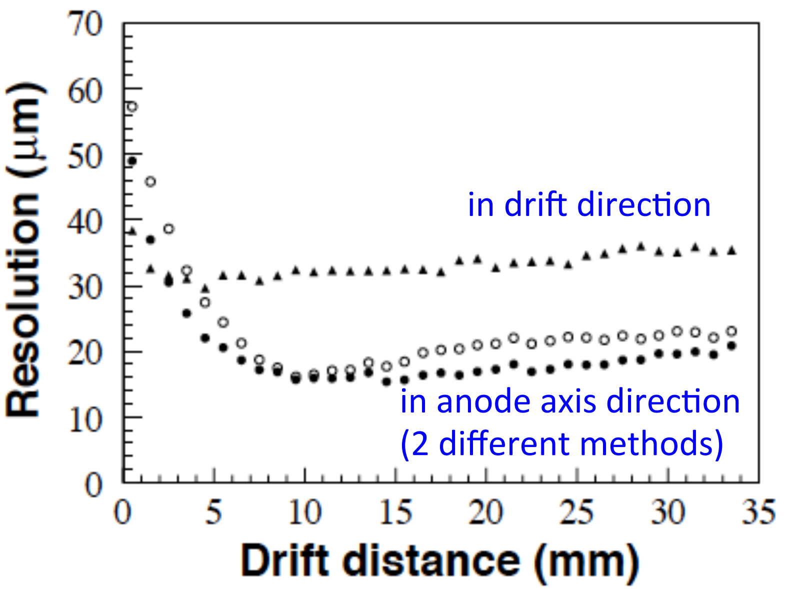
SDCs in ALICE ITS





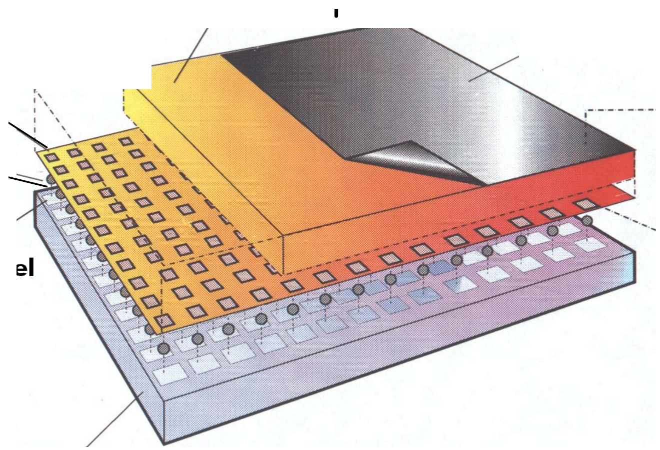


from B. Alessandro et al., 2010_JINST_5_P02008

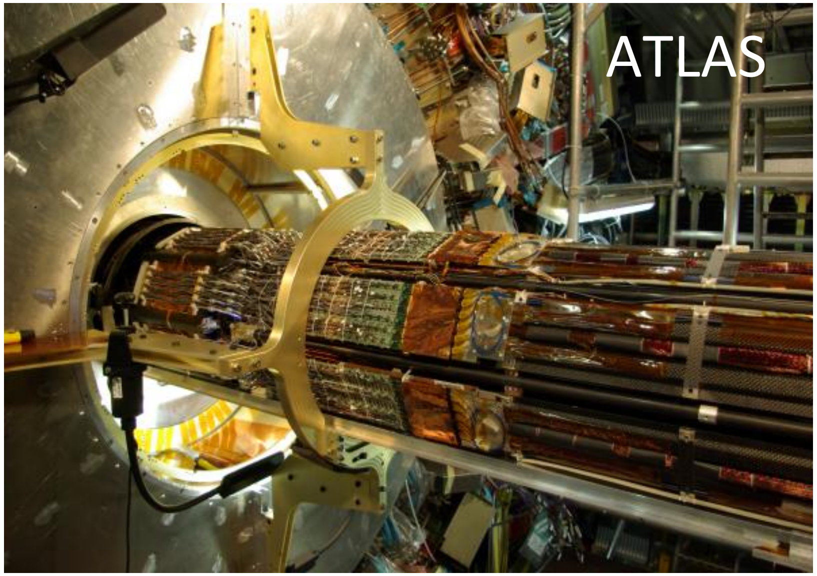


D. Nouais et al., NIM A501 (2003) 119–125

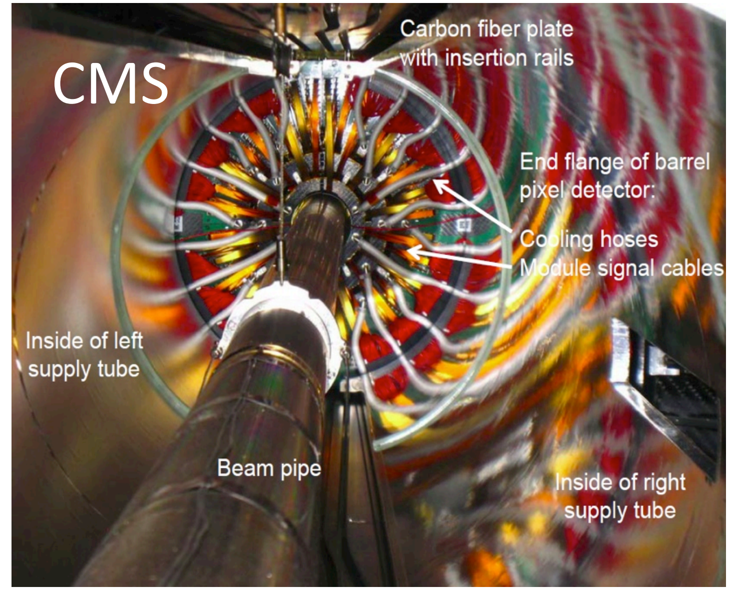
Hybrid Pixel Detectors

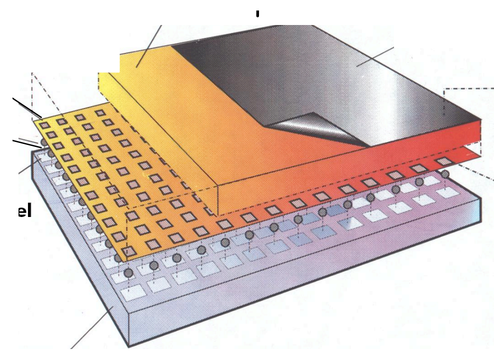


Today's "state of the art" of running pixel detectors

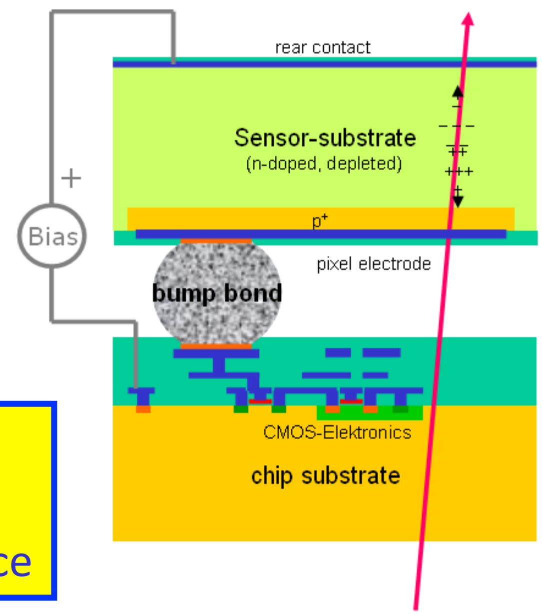


all based on
"Hybrid Pixels"





- amplification by a dedicated R/O chip
- 1-1 cell correspondence



Hybrid Pixel assembly => called „hybridization“

Sensors

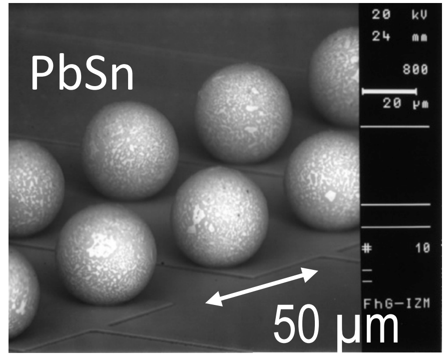
- n^+ in n (oxygenated Si)
- wafer size (Ø 10 cm)
- ~200-250 µm thick

Electronics - Chip

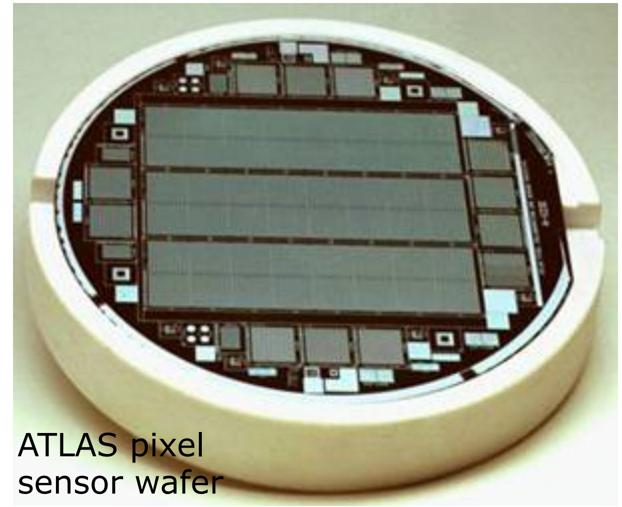
- chip size limited by yield ~1-2.5 cm^2
- wafer size (Ø 20 cm)

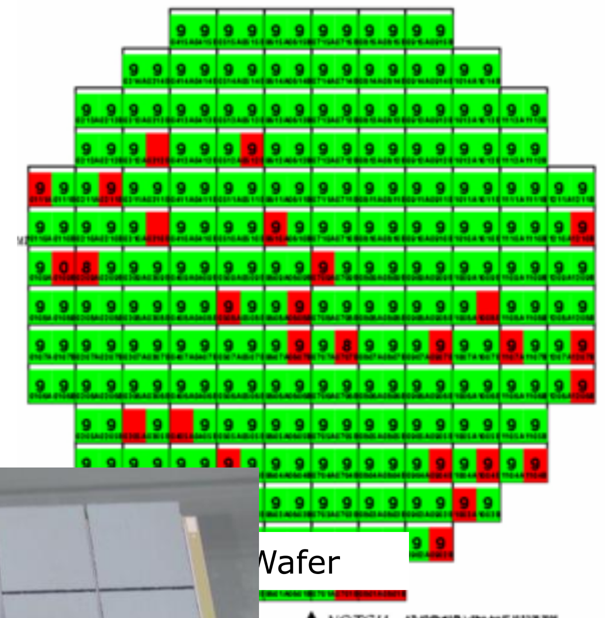
Hybridization

- PbSn (or In) bumps (processing on wafer scale)
- IC wafers thinned after bumping to ~180 µm
- ‚flip-chip‘ to mate the parts
- ~3000 bumps/chip, ~50000 bumps/module

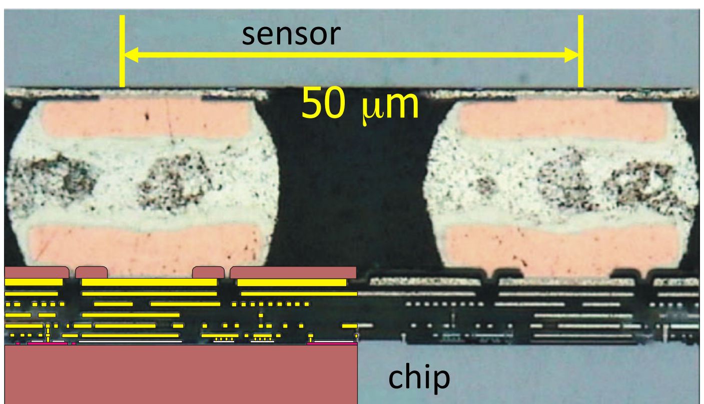


IZM,Berlin





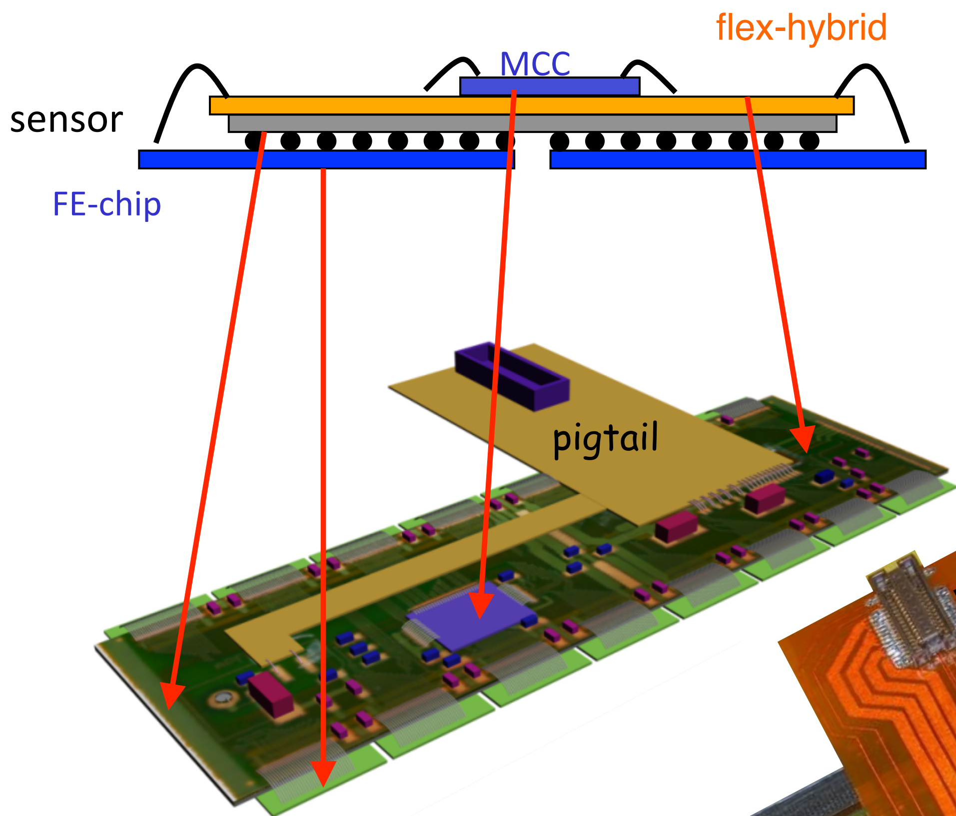
p, 82% yield



ATLAS pixel BARE module

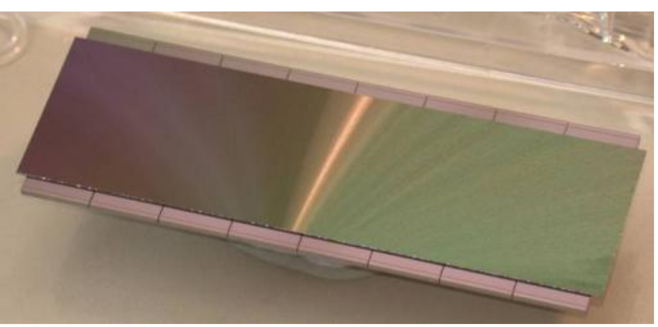
 ATLAS Modul, Foto:IZM, Berlin

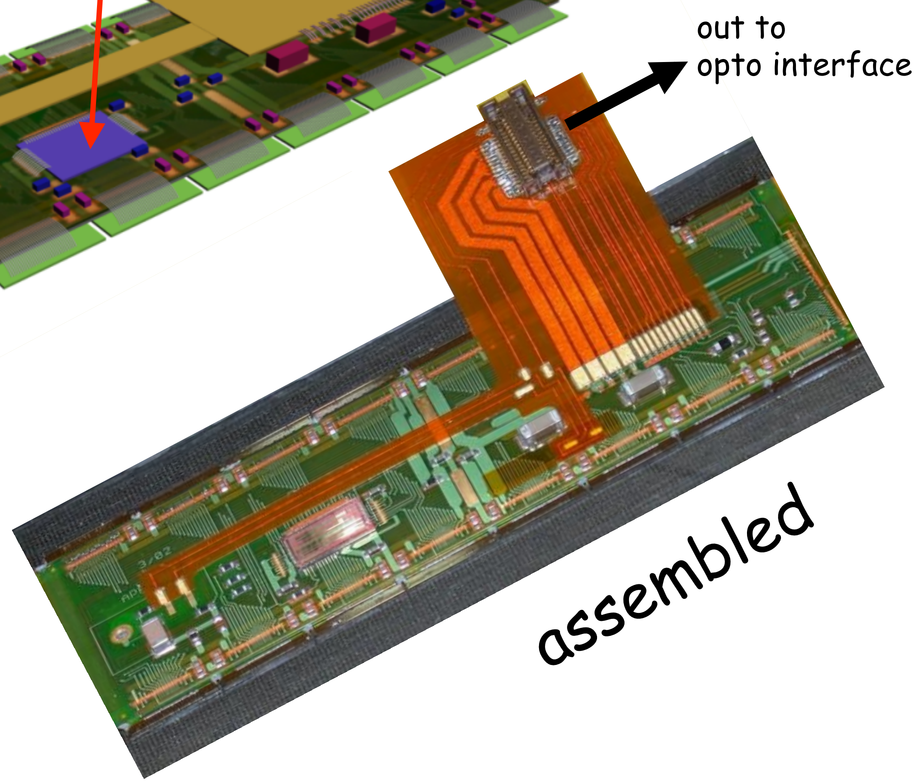
Hybrid Pixel Assembly (here ATLAS)



1 sensor tile
16 FE Chips
1 controller chip (MCC)
46,080 pixels per module
80 Million total

bare

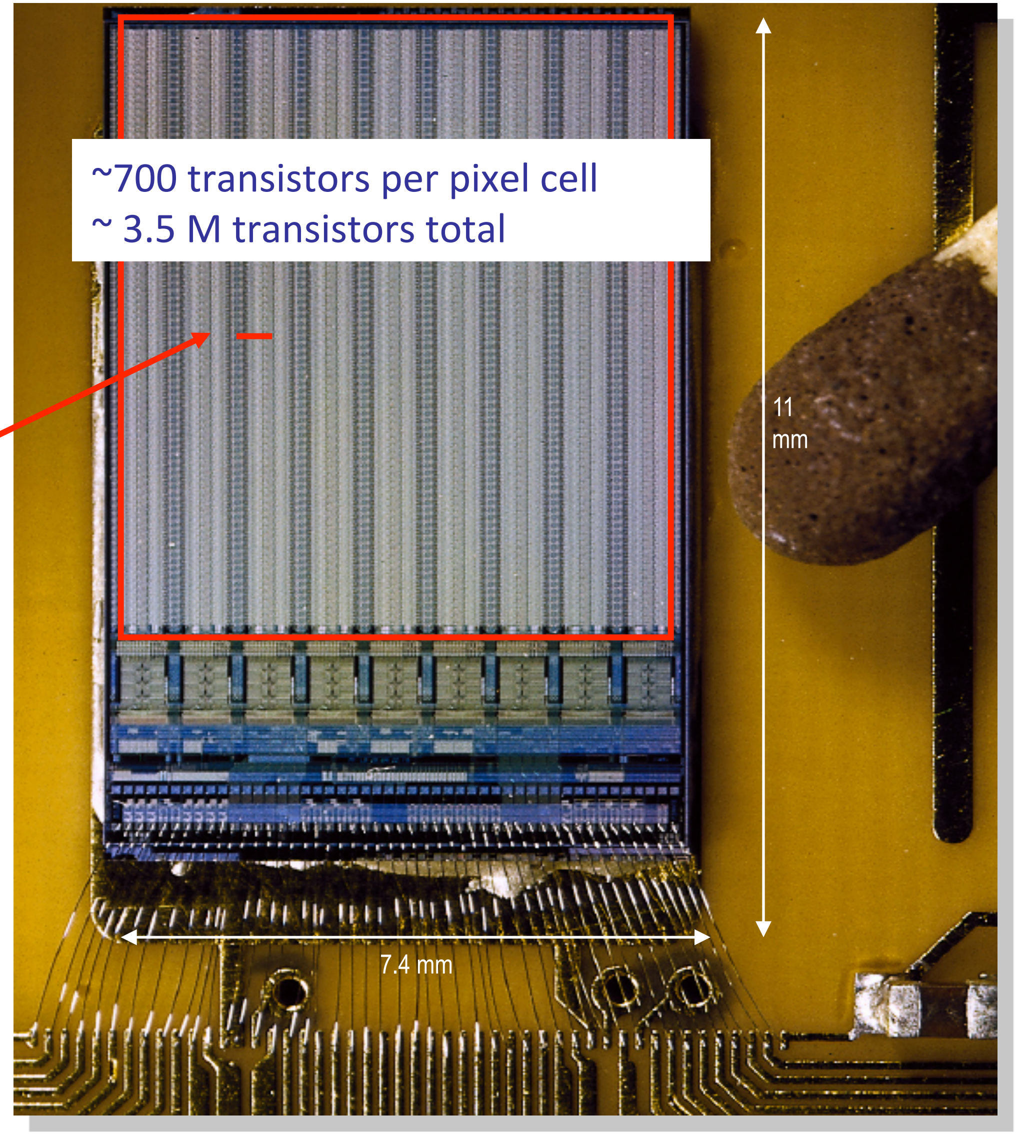




Important: Readout Chips (ASICs)

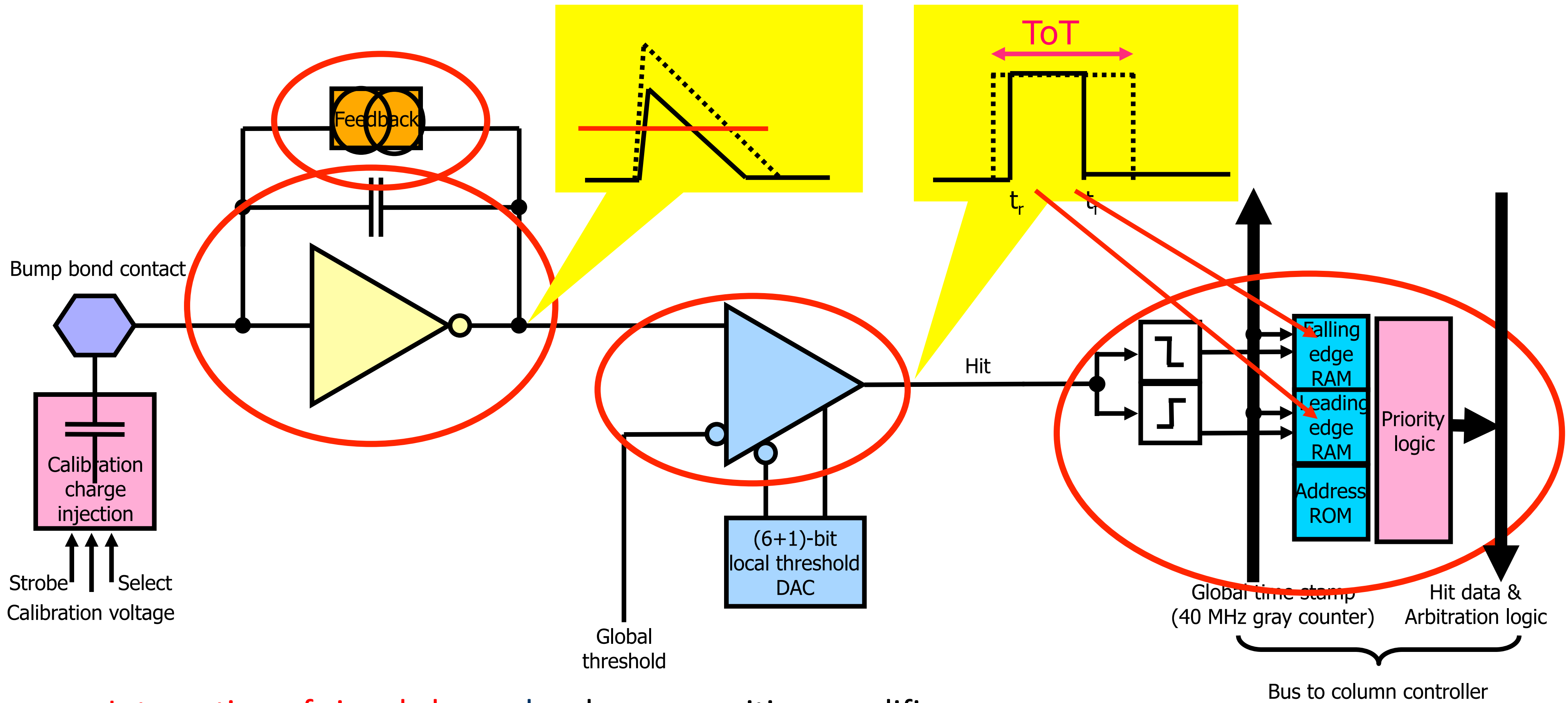
- becomes integral part of the detector
  - micro electronics
  - up to 700 million transistors so far
  - development takes typ. 10 man years

- ATLAS FE-I3
  - 0,25 µm CMOS technology
  - pixel cell size: 50 x 400 µm^2
  - 18 columns x 160 rows = 2880 cells
  - parallel processing in all cells
    - - amplification
    - - zero suppression



L. Blanquart, P. Fischer et al., NIM-A 456 (2001) 217-231

Functions in the cell (binary readout + „poor man‘s“ analog)



- Integration of signal charge by charge sensitive amplifier
- Pulse shaping by feedback circuit with constant current feed back
- Hit detection by comparator
- ~5 bit analog information via „time over threshold“
- storage of address and time stamps in RAM at the periphery

L. Blanquart et al., NIM-A565:178-187, 2006

ATLAS Pixel Frontend Chip

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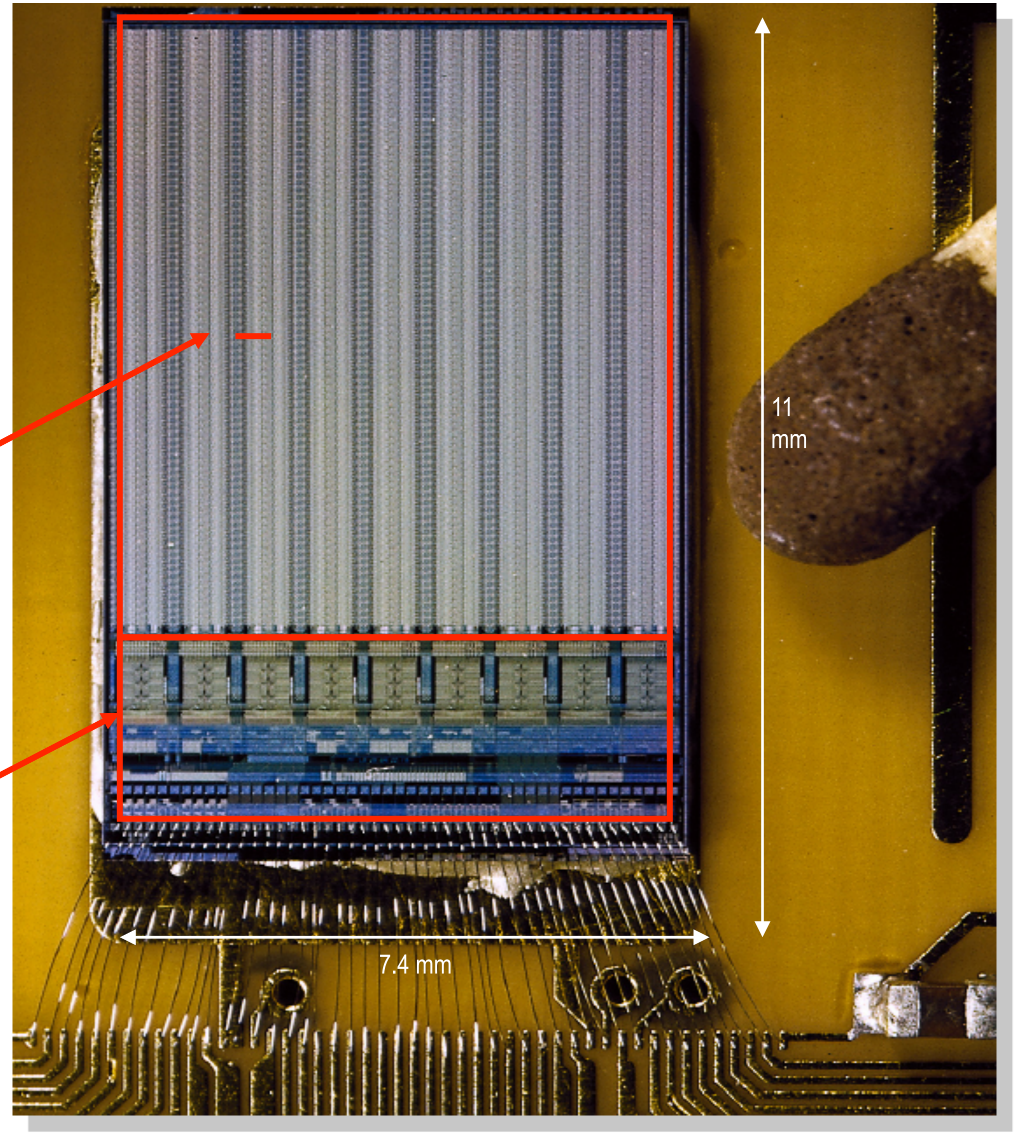
- becomes integral part of the detector
  - micro electronics
  - up to 700 million transistors so far
  - development takes typ. 10 man years

- ATLAS FE-I3
  - 0,25 µm CMOS technology
  - pixel cell size: 50 x 400 µm^2
  - 18 columns x 160 rows = 2880 cells
  - parallel processing in all cells
    - - amplification
    - - zero suppression

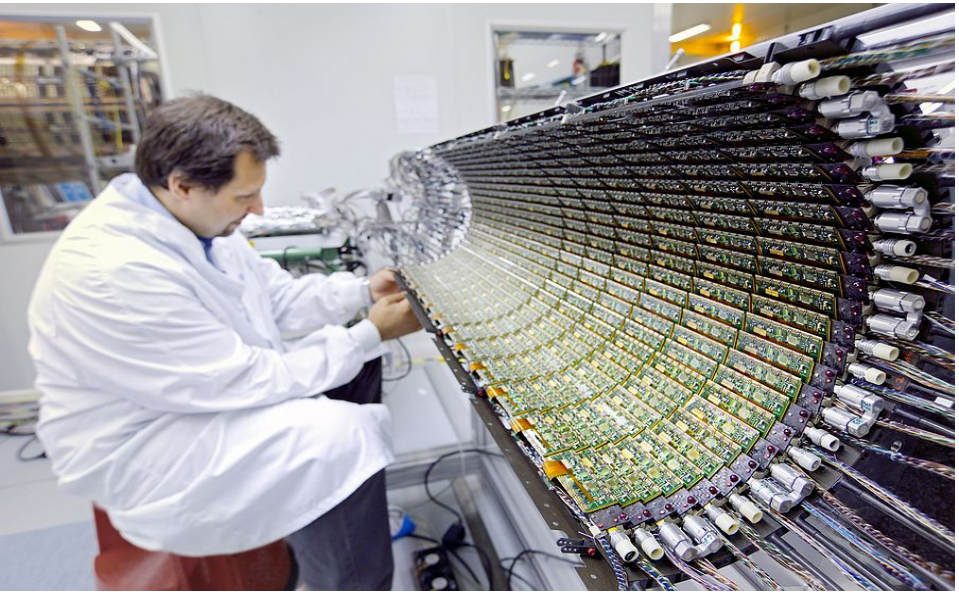
- End of Column logic
    - storage of hit information during trigger latency (2.5 µs)
    - hit selection upon L1 trigger

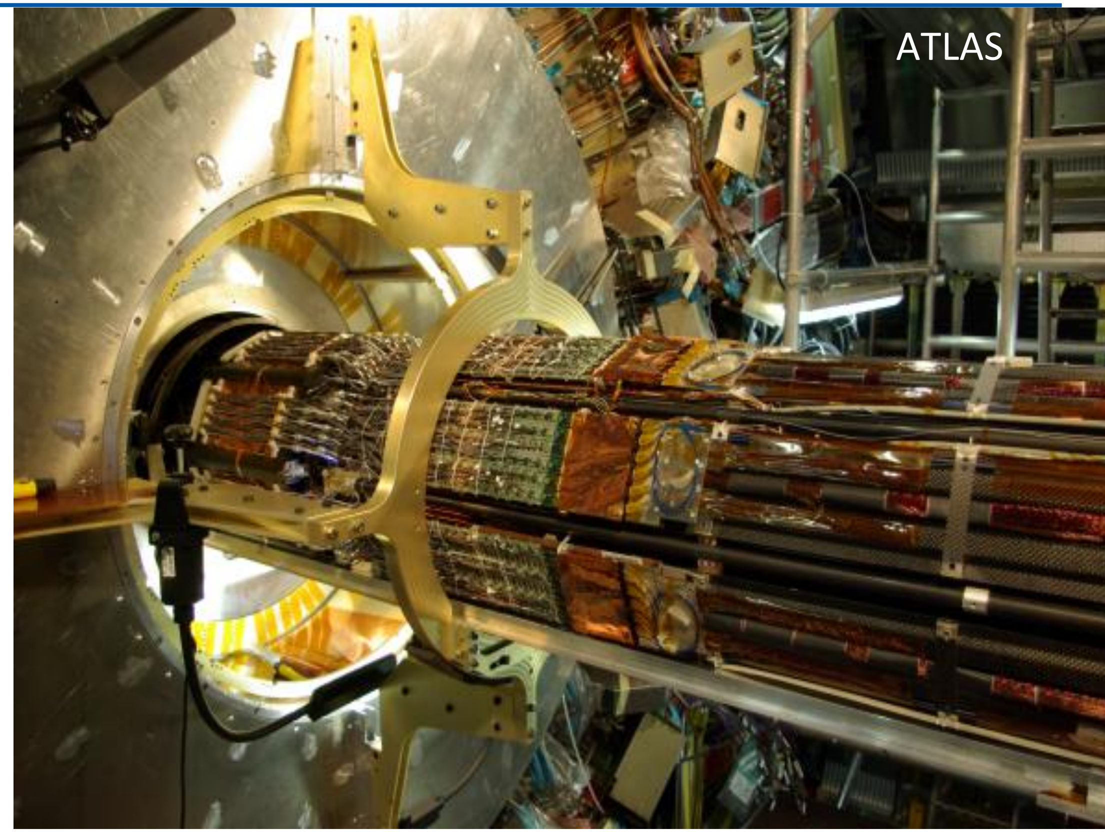


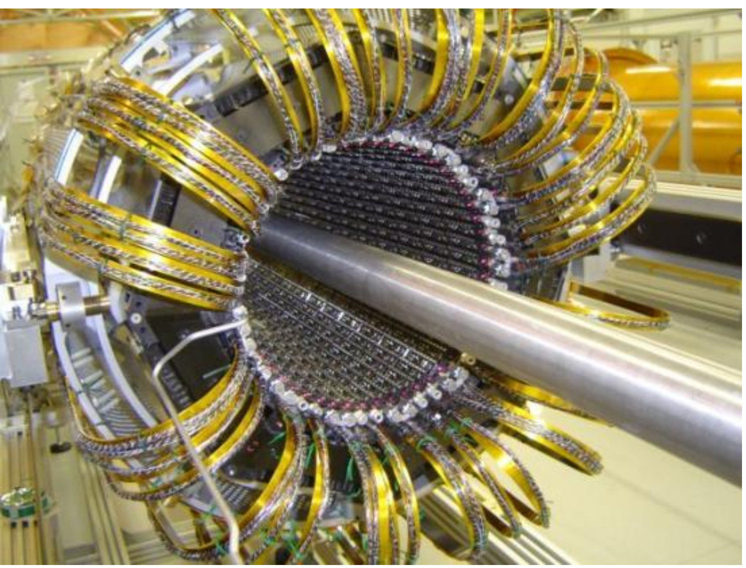
L. Blanquart, P. Fischer et al., NIM-A 456 (2001) 217-231

movement of hits in the column turns out to be the bottle neck at high rates

ATLAS Pixel Detector







- light weight ”carbon-carbon” structures
- cooling (pumped C_3F_8 : boiling point = -25^0)
- T < -6^0 C to limit damage from irradiation

1^{st} Upgrade … (installed 2014)

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IBL = ATLAS' insertable B-Layer

- move closer to IP (5.5 cm -> 3.5 cm)
- higher rate
- higher radiation levels (~$1/r^2$)

FE-I4: larger chip
smaller feature size
higher rate capability

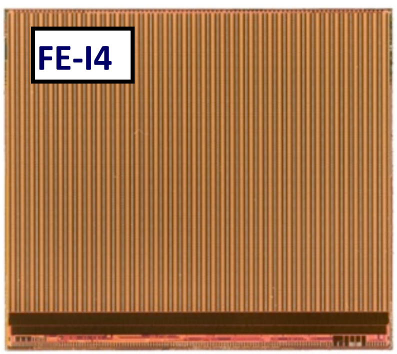
~0.6 × 1.1 cm^2

250 nm technology

pixel size 400 × 50 μm^2

3.5 M transistors

~2 × 2 cm^2

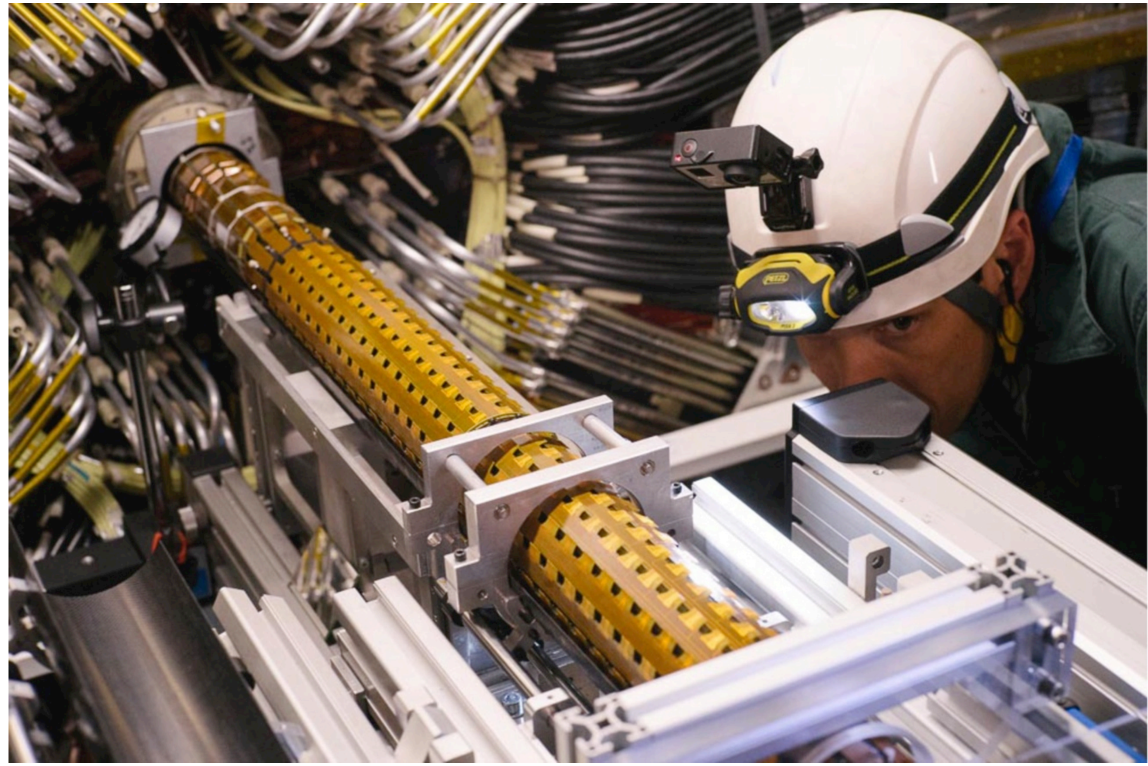


130 nm technology

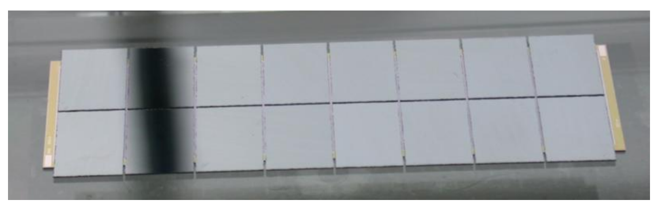
pixel size 250 × 50 μm^2

87 M transistors

installed in ATLAS: May 2014

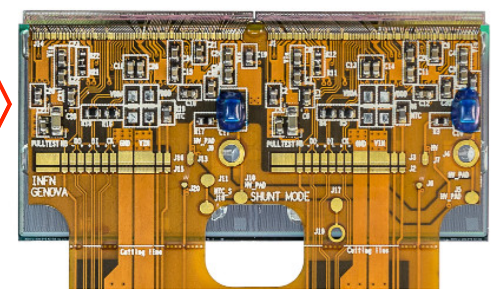


~2 × 5 cm^2



ATLAS Pixel 16-chip module

~2 × 4 cm^2



IBL: 2-chip module

ATLAS IBL in operation

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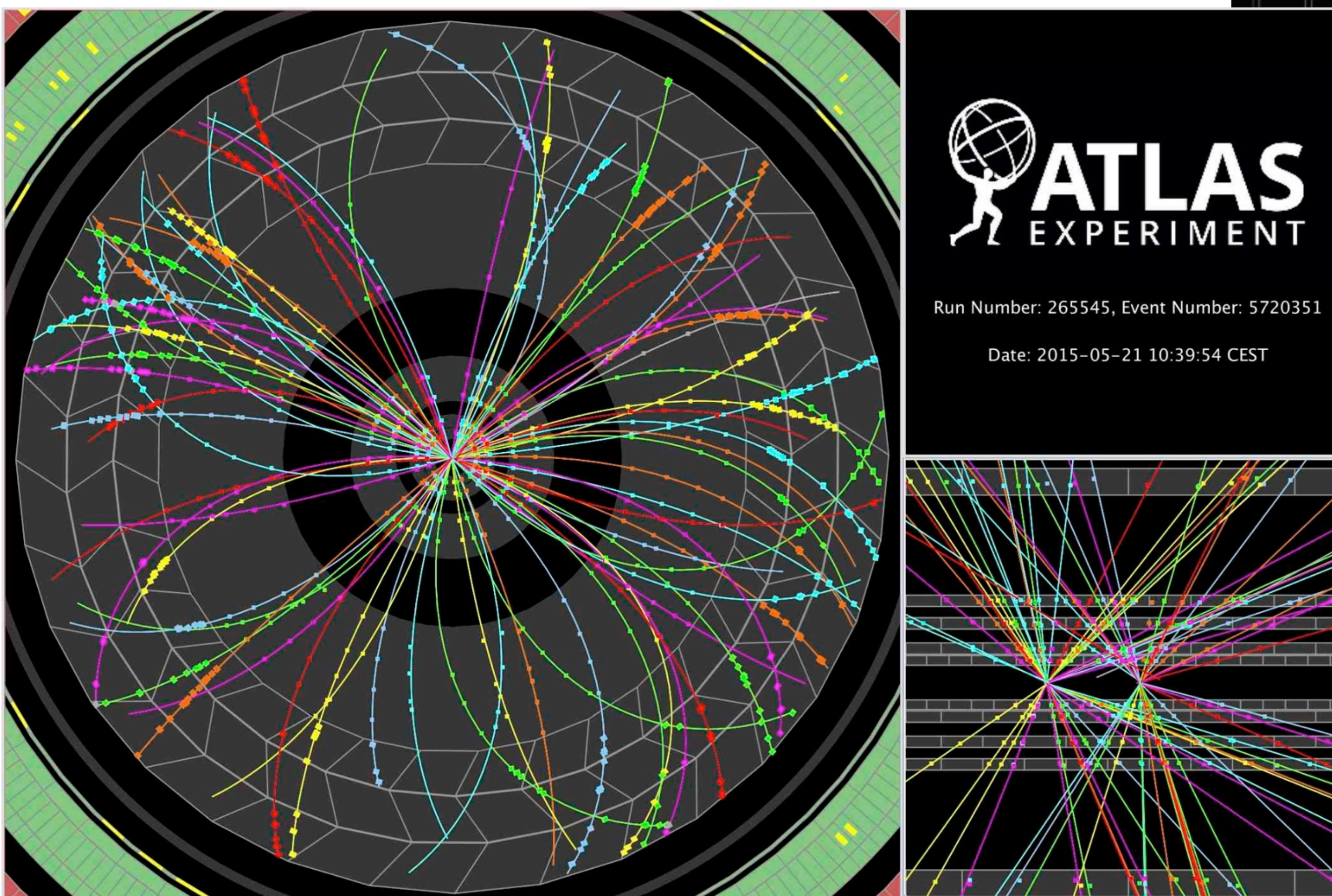
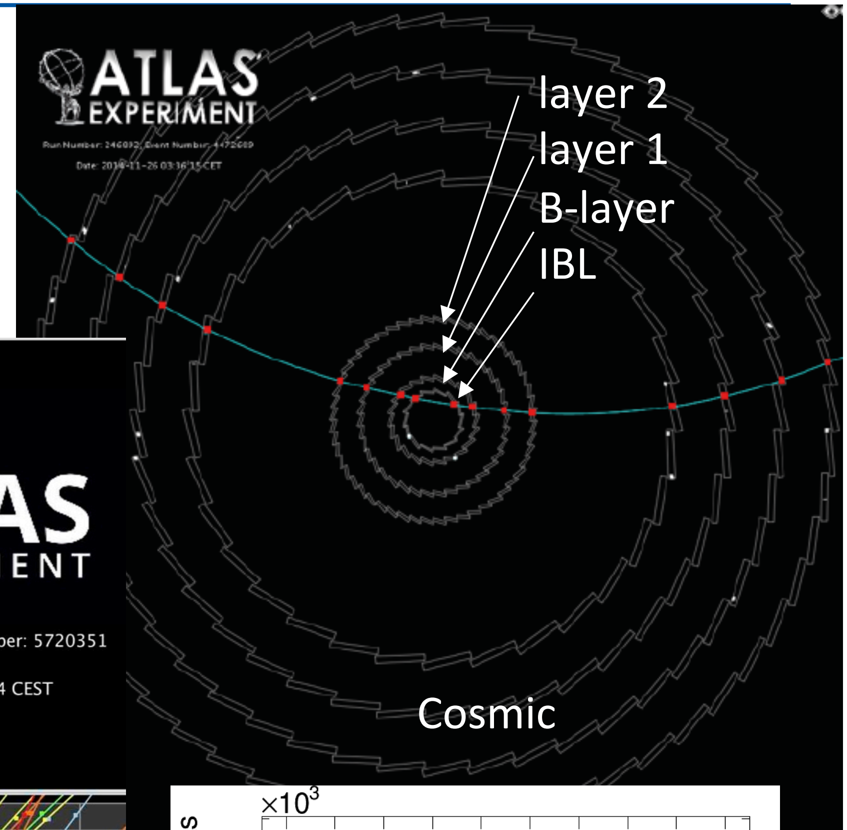
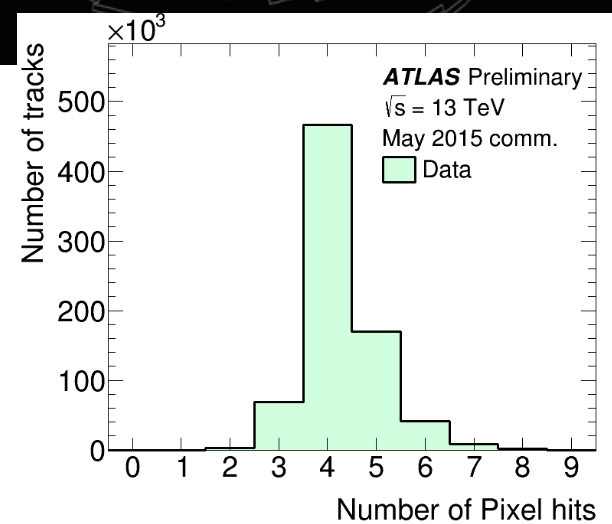
A true 4-hit pixel system!

important for b-quark tagging

13 TeV pp collision, 2 interactions







Radiation Damage

distinguish

- non-ionising energy loss (NIEL) by charged particles or neutrons through interactions with the Si-lattice
  => damages mainly the sensor performance (charge collection)
  measured in terms of "fluence" = particles/cm^2 = flux × time -> n_{eq}/cm^2

- ionising energy loss (IEL) by charged particles (dE/dx) or X-rays (absorption) creates charges, especially in transistor gate oxides
  => damages mainly the chip electronics
  measured in terms of TID = total ionizing dose (in Gy or rad = 100 Gy)

- 10 years LHC ≅ 10^{15} n_{eq}/cm^2 and 600 kGy (60 Mrad)
- ~10 x more at HL-LHC

Semiconductor detectors in the LHC radiation environment

universitätbonn

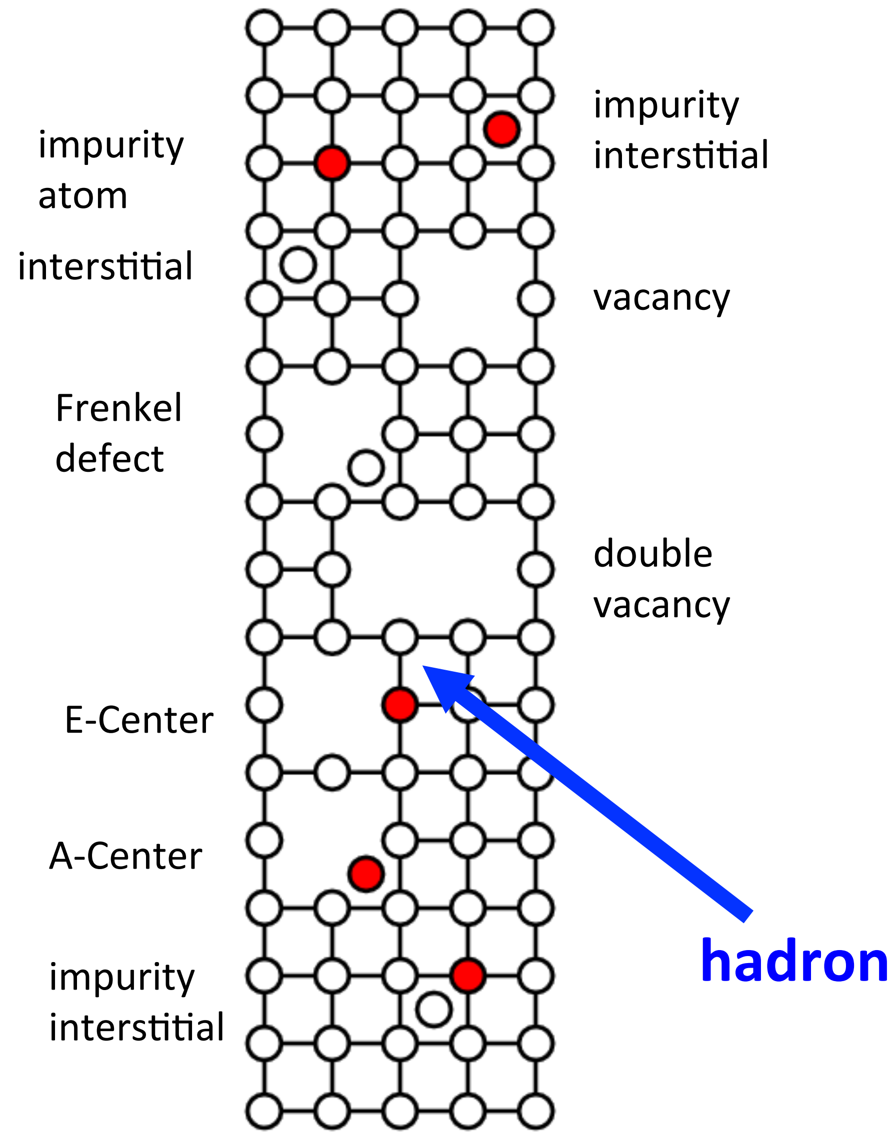
particle interactions with lattice nuclei

NIEL

non-ionizing energy loss (not reversible) normalized to 1 MeV neutron damage

recoiling Si-atom can cause further defects
→ defect clusters (10nm x 200nm)

1. generation/recombination levels in band gap
   → increase of leakage current
2. change of space charge in depleted region
   → change of effective doping concentration
3. trapping centers created
   → trapping of signal charge



Semiconductor detectors in the LHC radiation environment

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particle interactions with lattice nuclei

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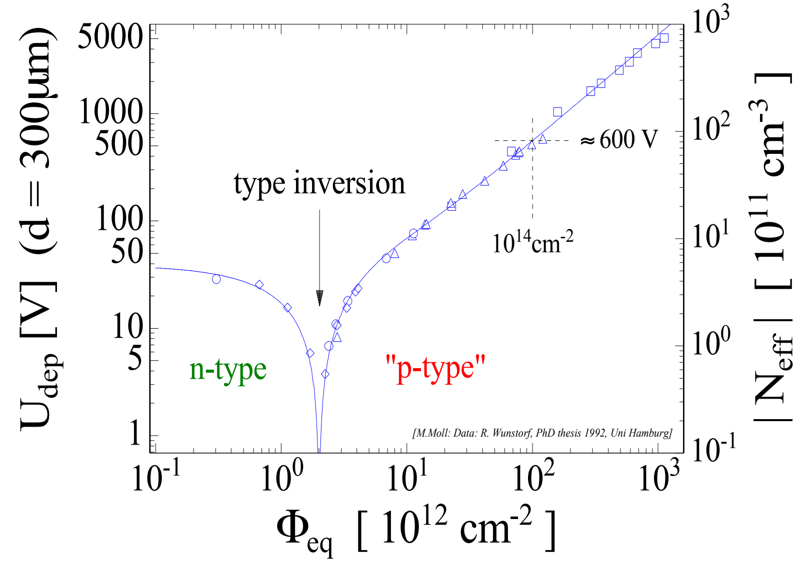
- Change of Depletion Voltage V_{dep} (N_{eff})

.... with particle fluence:

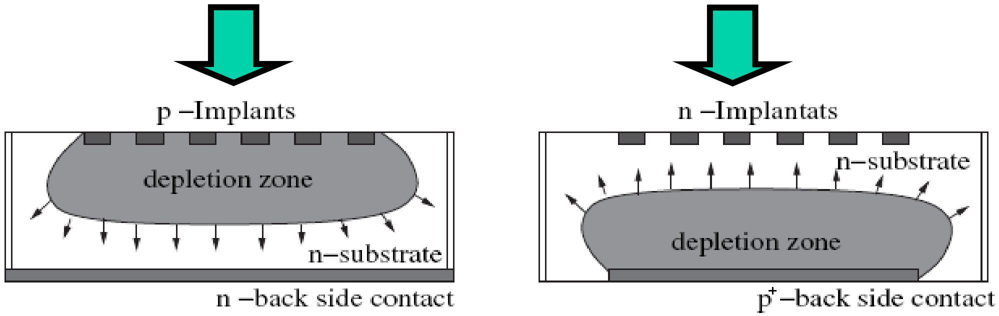


- "Type inversion": N_{eff} changes from positive to negative (Space Charge Sign Inversion)

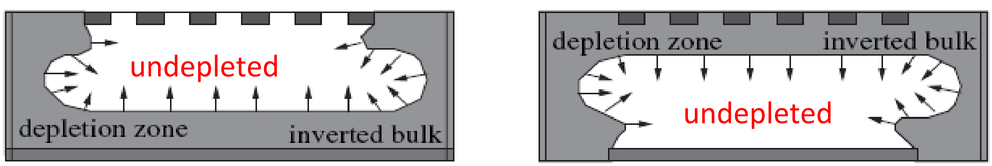
fluence (NIEL) > 10^{15} n_{eq}/cm^2
total dose > 600 kGy / 60 Mrad

Semiconductor detectors in the LHC radiation environment

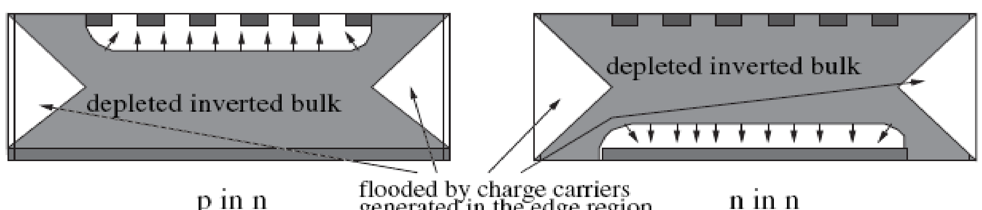
p^+ in n "normal" | n^+ in n



before type inversion



after type inversion

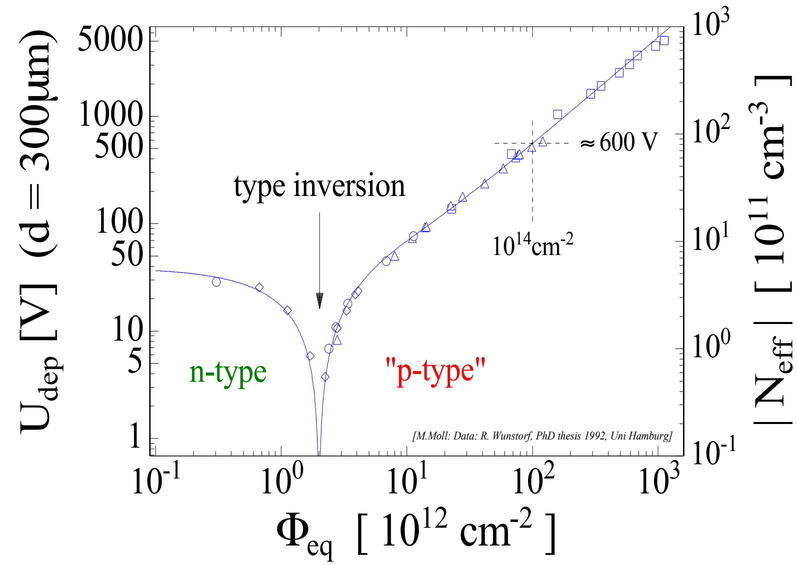


after heavy radiation damage

L. Andricek et al, NIM-A 409 (1998) 184-193

- Change of Depletion Voltage V_{dep} (N_{eff})

.... with particle fluence:



- "Type inversion": N_{eff} changes from positive to negative (Space Charge Sign Inversion)

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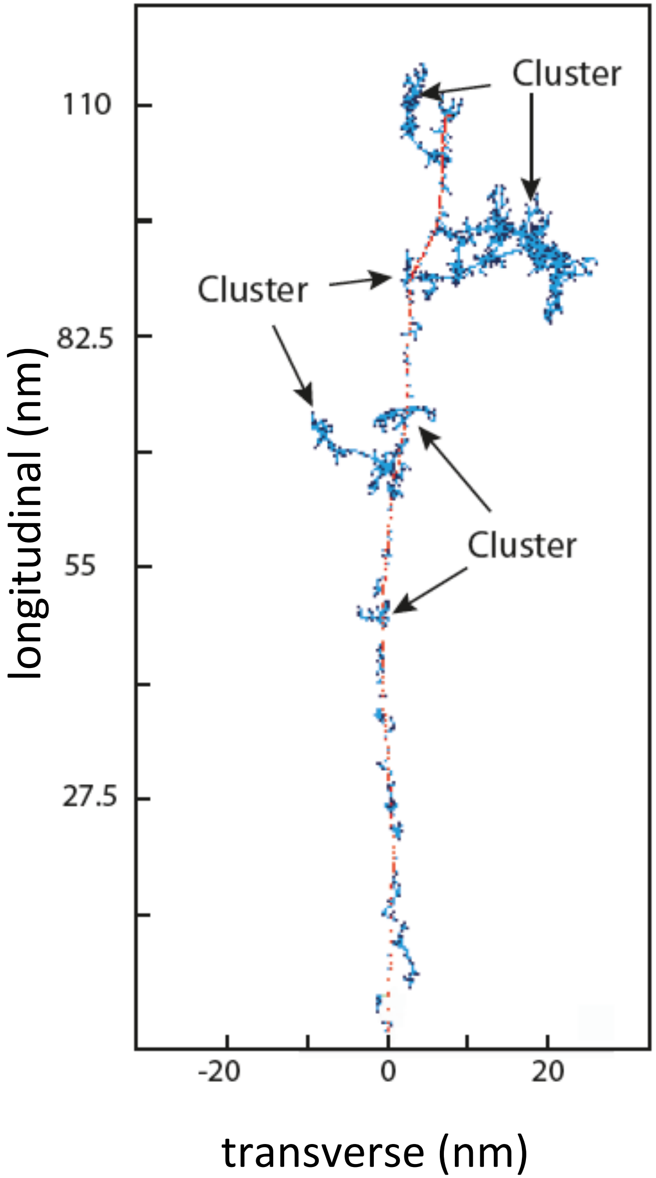
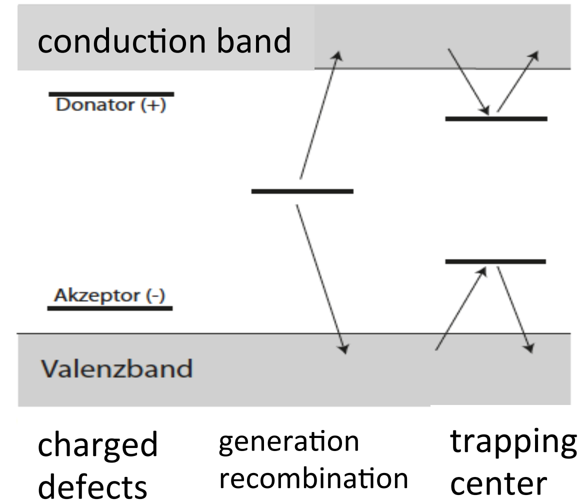
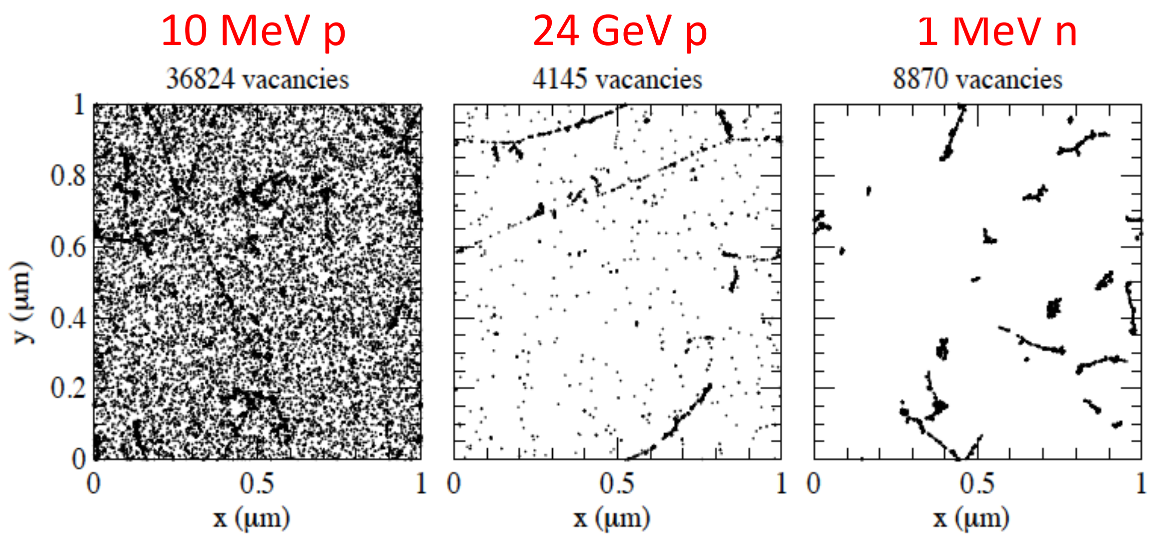
total dose > 600 kGy / 60 Mrad

Radiation Damage (NIEL)

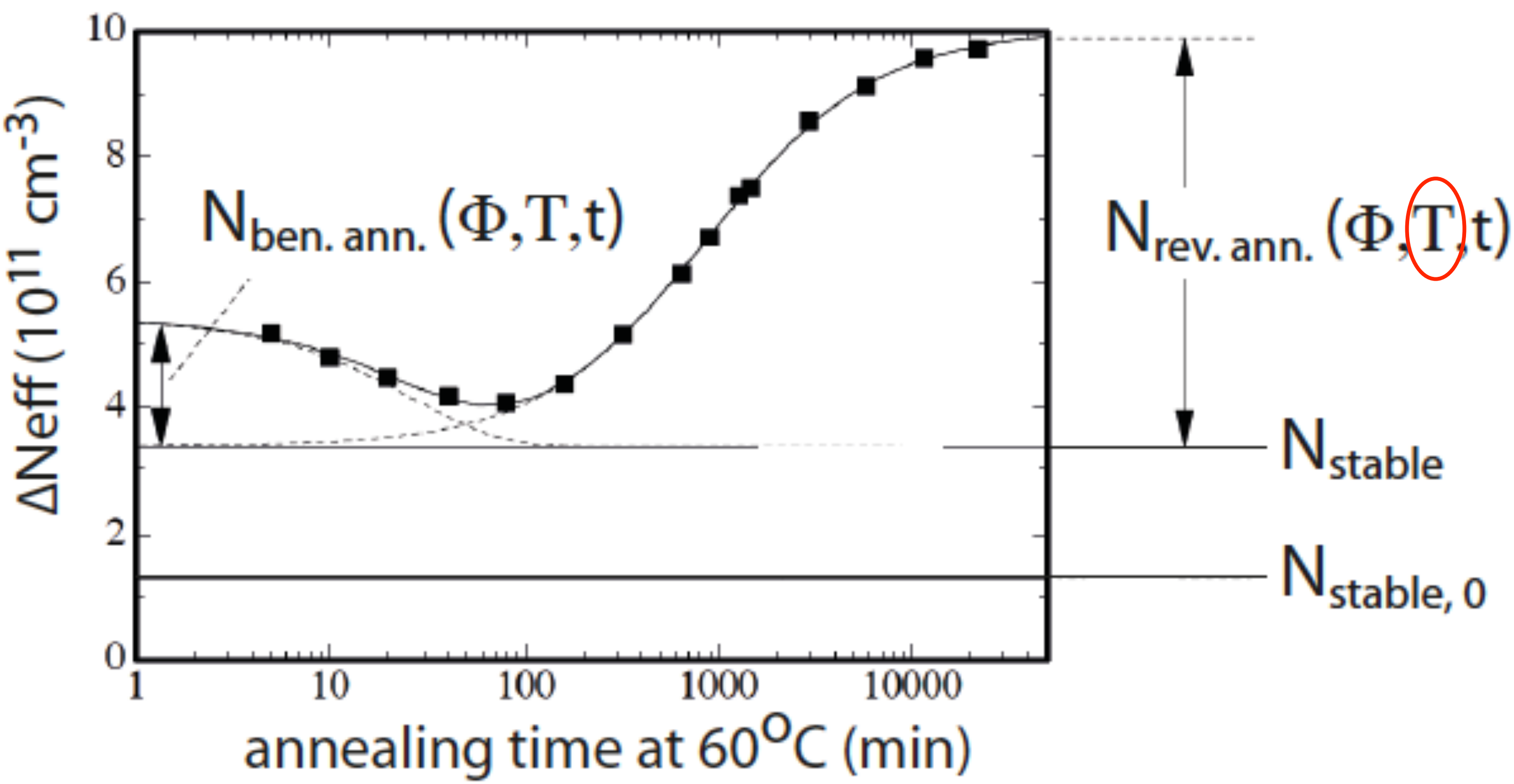


threshold energy to remove a Si-atom from the lattice:
Si - 25 eV, diamond – 43 eV





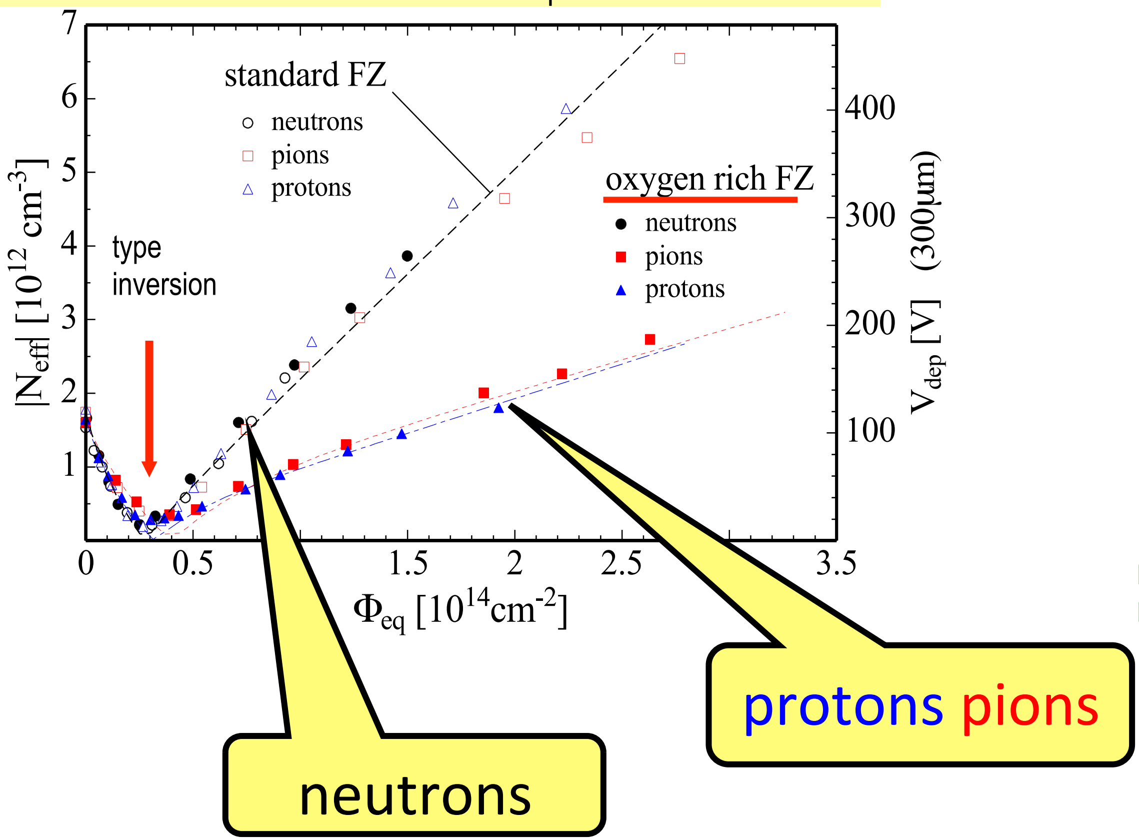
Annealing



- shaking the lattice => beneficial annealing
- too long at a high temperature => defects, that did not harm so far, become active => reverse annealing
- hence: keep detectors cool @ -5 to -10° C

solution: oxygenated FZ silicon

radiation tolerant to 10^{15} n_{eq} / cm^2 (600 kGy)

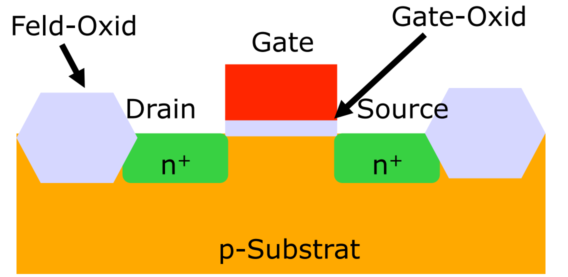


RD50, G. Lindström et al. NIM-A 465 (2001) 60-69

Reason: complex interaction of various (point+cluster) defects:
V_2O interplay with a "shallow donor" that act against each other.
V_2O originating from point defects decreases with oxygenation. For neutrons different => only clusters.

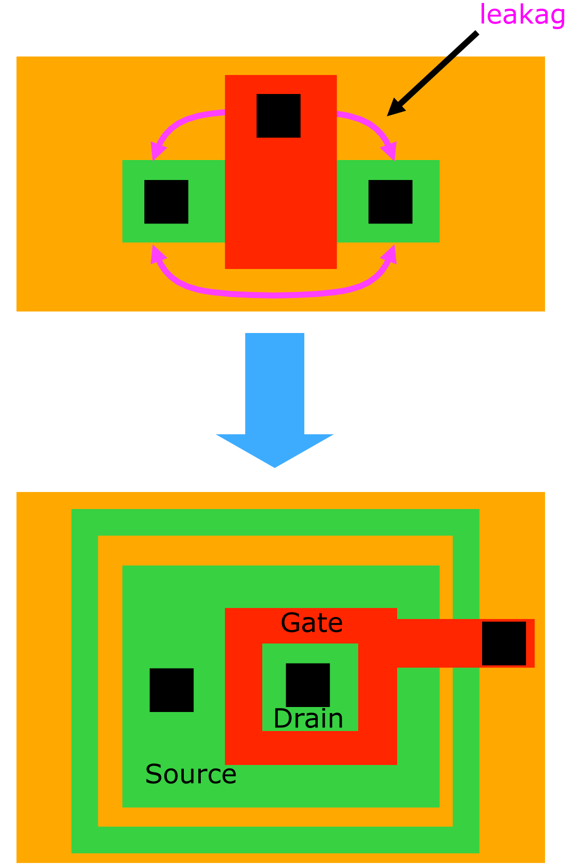
Radiation damage to the FE-electronics … and cure

Effects: generation of positive charges in the SiO_2
and defects in Si - SiO_2 interface



1. Threshold shifts of transistors

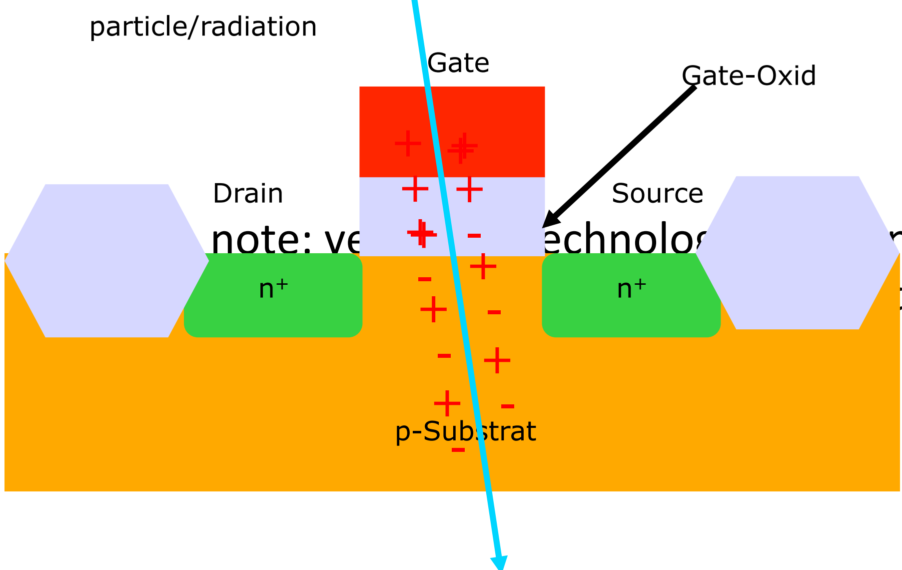
➔ Deep Submicron CMOS technologies with small structure sizes (≤ 350 nm) and thin gate oxides (d_{ox} < 5 nm) → holes tunnel out



2. Leakage currents under the field oxide

➔ Layout of annular transistors with annular gate-electrodes + guard-rings

note: ve … echnolo… new problems … ries



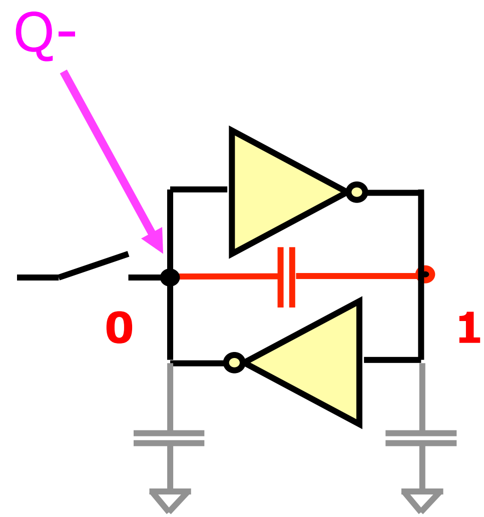
Radiation damage to the FE-electronics … and cure

radiation induced bit errors

("single event upsets" SEU)

large amounts of charge on circuit nodes
- by nuclear reactions, high track densities -
can cause "bit-flip"

2 examples of error resistant logic cells



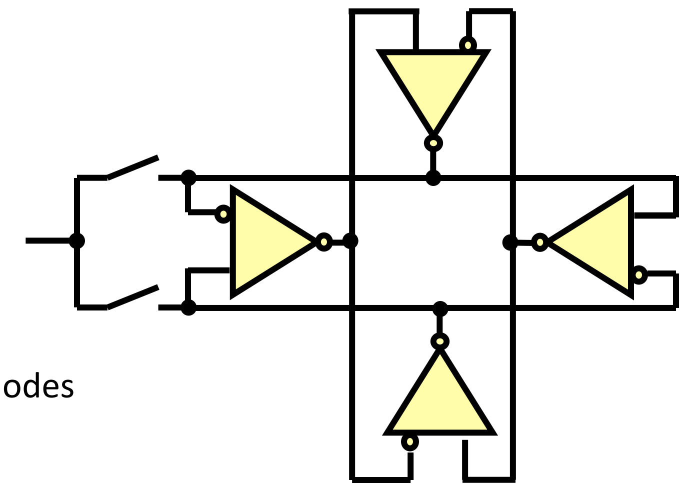
standard SRAM cell

➔ enlarge storage capacitances in SRAM cells:

$Q_{crit} = V_{threshold} \cdot C$

➔ storage cells with redundancy (DICE SRAM cell)

information and its inverse stored on 2+2 independent and cross-coupled nodes
→ temporary flip of one node cannot permanently flip the cell.

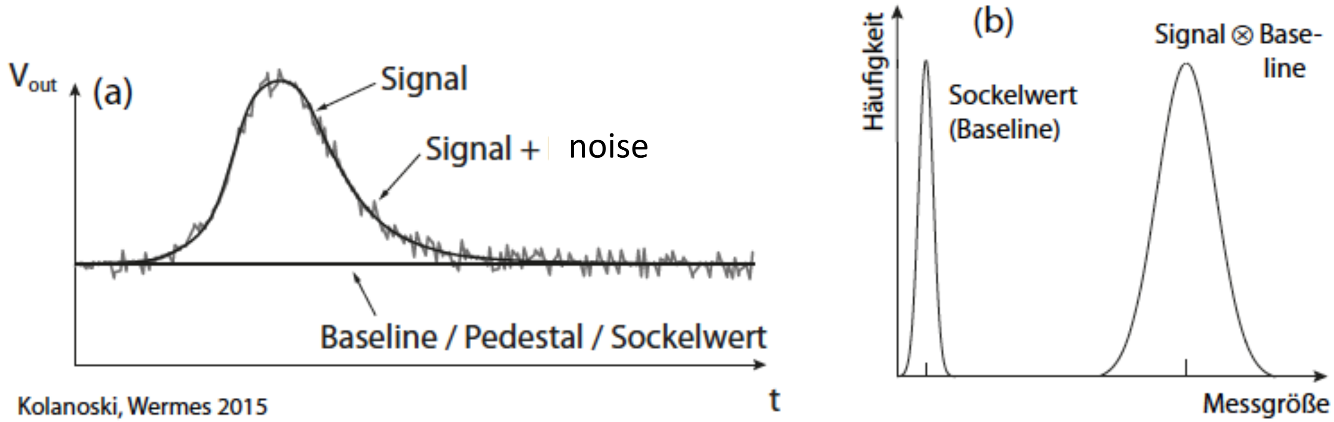


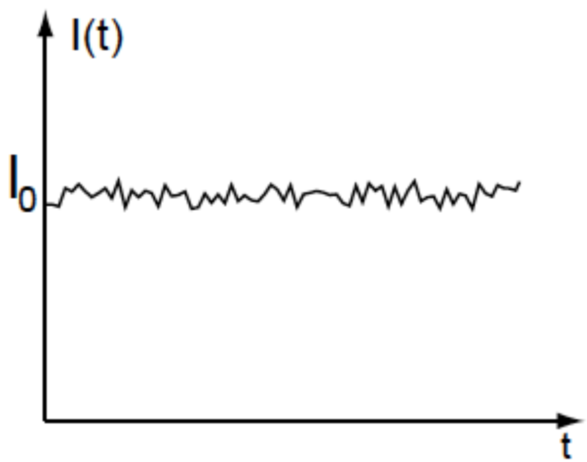
SEU tolerant DICE SRAM cell

Noise

skip noise?

Noise in ionisation detectors



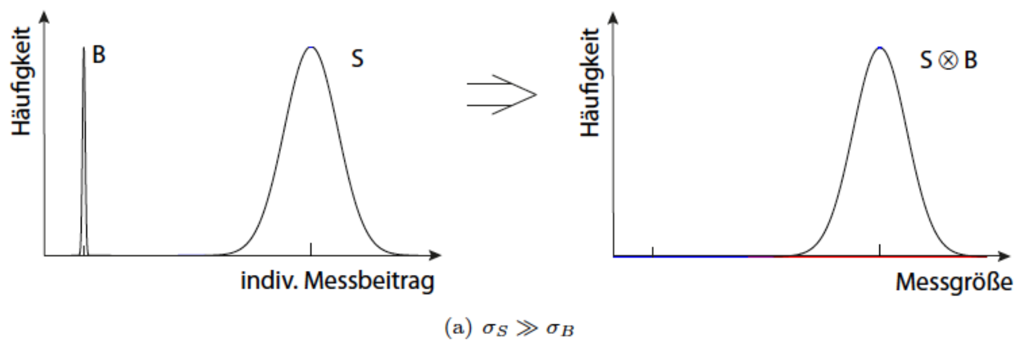


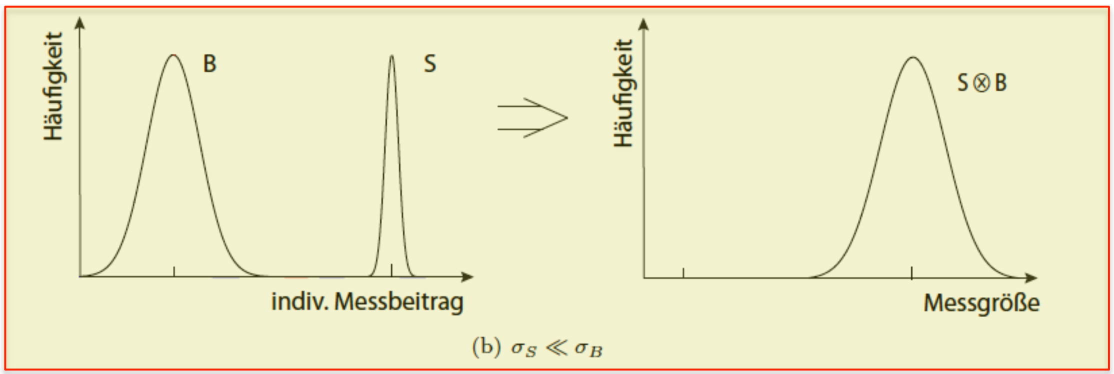
$$\sigma^2 = \lim_{T\to\infty} \frac{1}{T}\int_0^T \left(I(t) - I_0\right)^2 dt$$

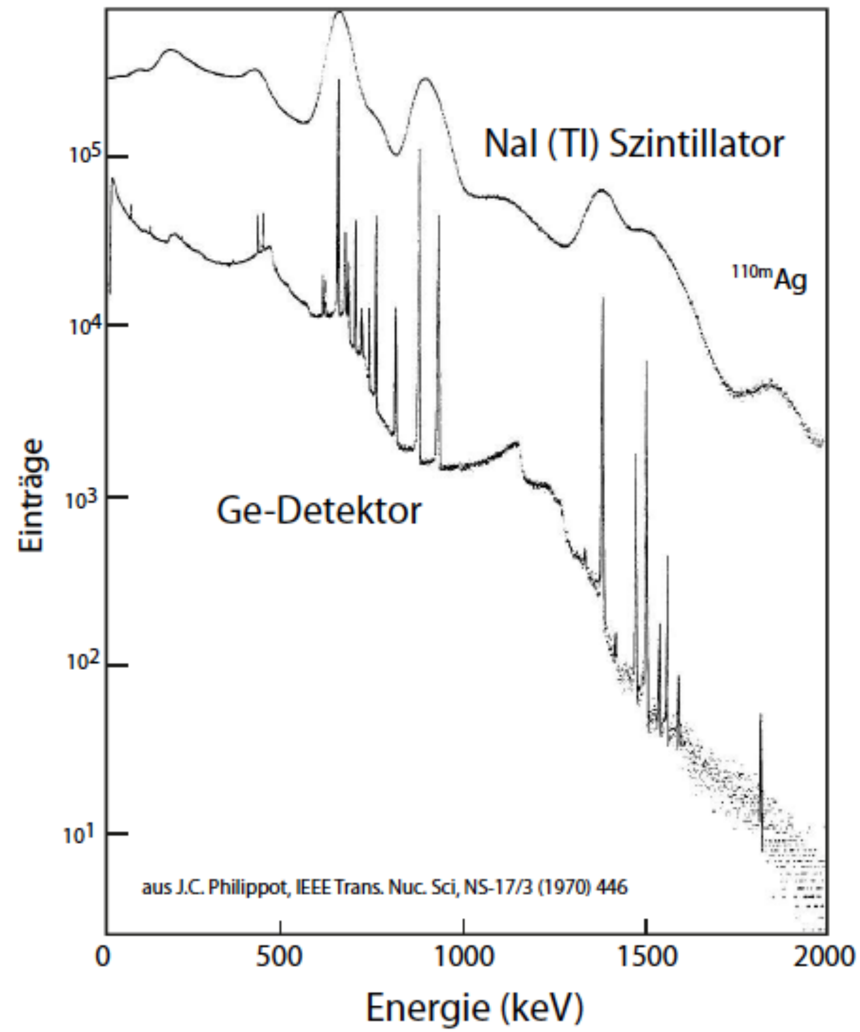
$$dP_n/df = \frac{1}{R}\, d\langle u^2\rangle/df = R\, d\langle i^2\rangle/df$$

When to care about noise …

- always …
- but particularly, when situation is like this







- even if you are not interested in an energy measurement, remember … thresholds

Noise

shot noise

white noise

current noise

resistor noise

switching noise

series noise

flicker noise

popcorn noise

Nyquist Noise

parallel noise

Johnson Noise

kT/C noise

Thermal noise

RTS noise

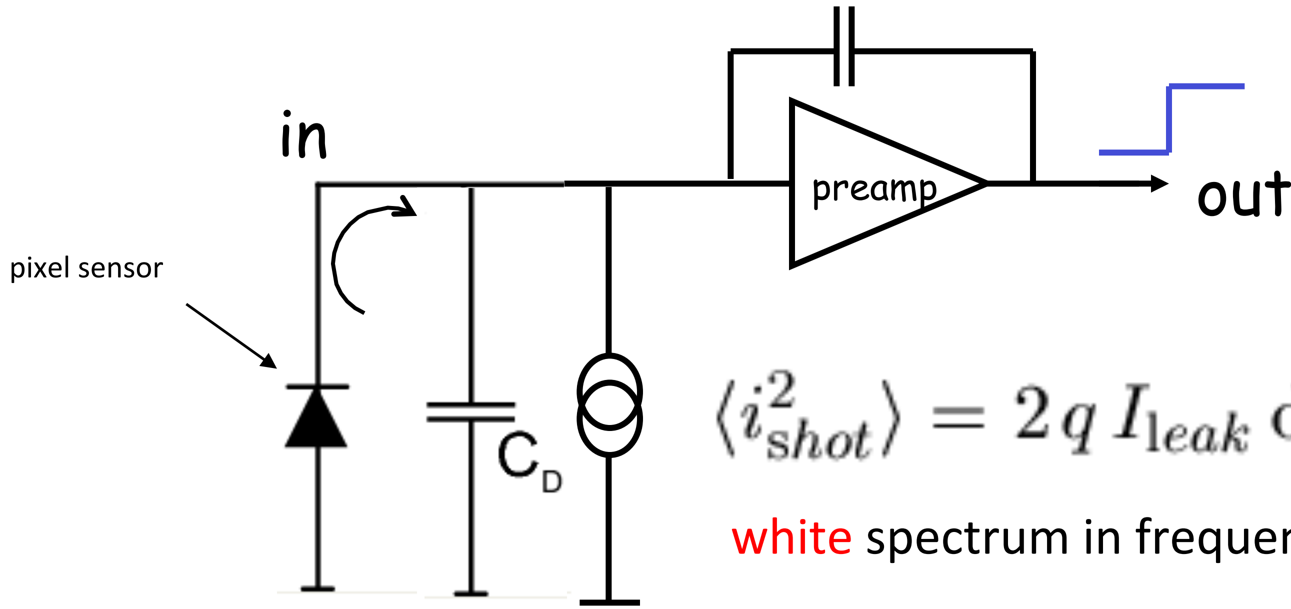
1/f noise

Noise in a pixel/strip detector (ionisation detector)

three physical noise sources:

number fluctuations of quanta	→	1. shot noise	$\langle i^2 \rangle = 2q \langle i \rangle df$
		2. 1/f noise	$\langle i^2 \rangle = const.\ 1/f\ df$
velocity fluctuations of quanta	→	3. thermal noise	$\langle i^2 \rangle = 4kT / R\ df$

where do they appear in a typical pixel detector readout chain ?



$$\langle i_{shot}^2 \rangle = 2q\, I_{leak}\, df$$

white spectrum in frequency f

Noise in a pixel/strip detector (ionisation detector)

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three physical noise sources:

number fluctuations of quanta	→	1. shot noise	$\langle i^2 \rangle = 2q \langle i \rangle \, df$
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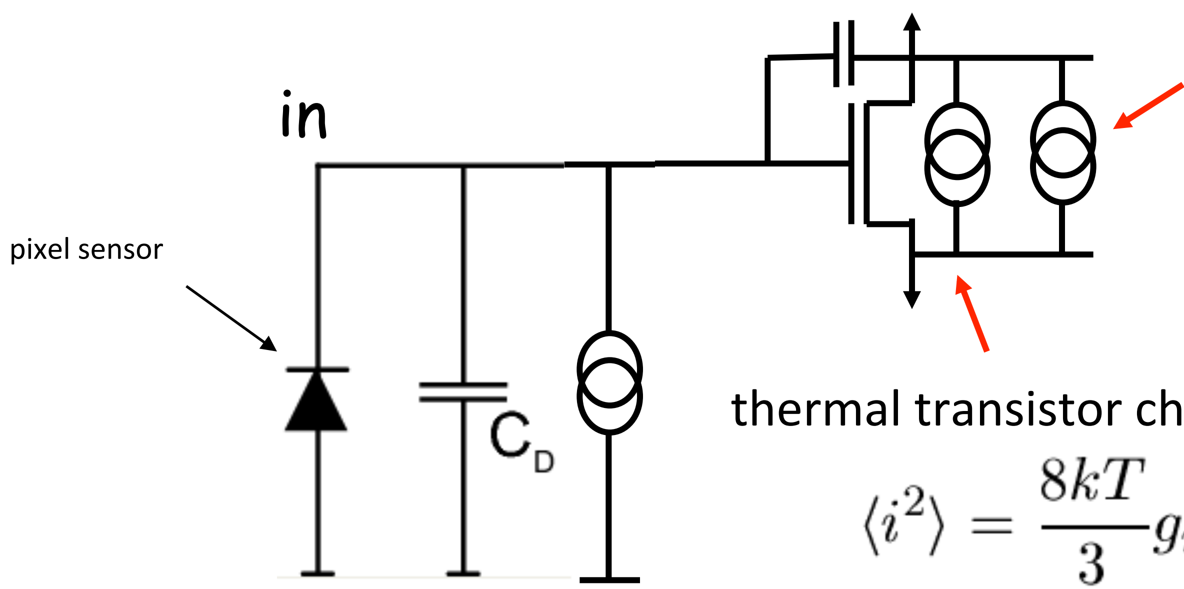

transistor 1/f noise

$$\langle i^2 \rangle = \frac{K_f}{C_{ox} W L} \frac{1}{f} \, \mathrm{d}f$$

thermal transistor channel (white) noise

$$\langle i^2 \rangle = \frac{8kT}{3} g_m \, \mathrm{d}f$$

Noise in a pixel/strip detector (ionisation detector)

three physical noise sources:

number fluctuations of quanta	→	1. shot noise	$\langle i^2 \rangle = 2q \langle i \rangle \, df$
		2. 1/f noise	$\langle i^2 \rangle = \text{const.}\ 1/f \, df$
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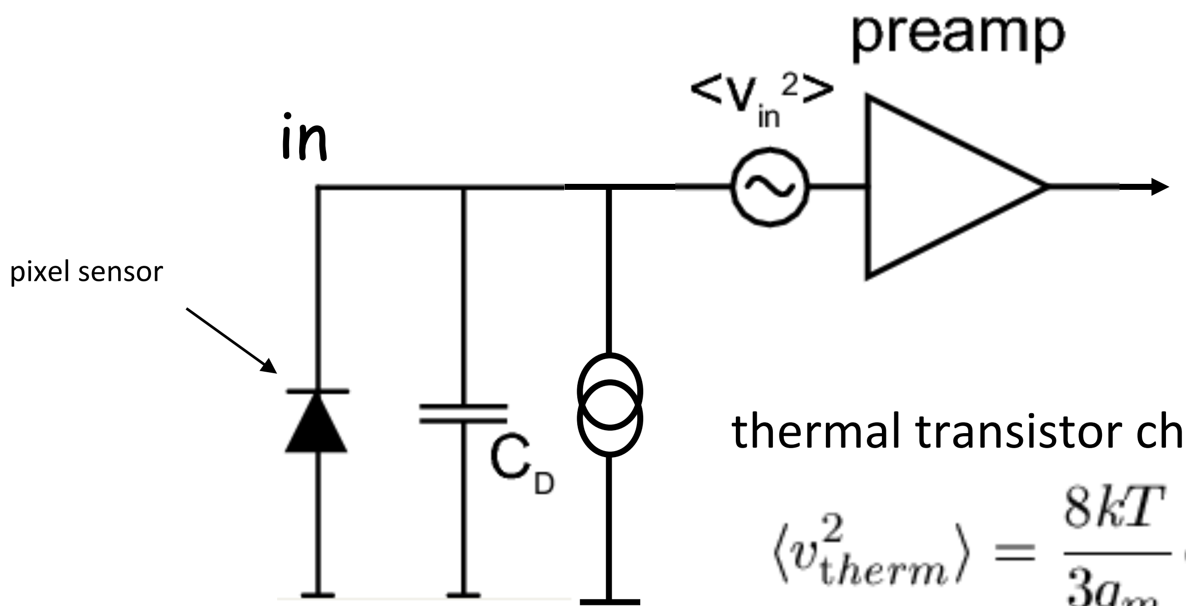

transistor 1/f noise

$$\langle v_{1/f}^2 \rangle = \frac{K_f}{C_{ox} W L} \frac{1}{f} \mathrm{d}f$$

thermal transistor channel noise

$$\langle v_{therm}^2 \rangle = \frac{8kT}{3 g_m} \mathrm{d}f$$

Noise in a pixel/strip detector (ionisation detector)

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equivalent noise charge $$\mathrm{ENC} = \frac{\text{noise output voltage (rms)}}{\text{signal output voltage for the input charge of } 1\mathrm{e}^-}$$

$$ENC^2_{tot} = ENC^2_{shot} + ENC^2_{therm} + ENC^2_{1/f}$$

charge sensitive preamplifier only

$$ENC_{\mathrm{shot}} = \sqrt{\frac{I_{leak}}{2q}\tau_f} = 56e^- \times \sqrt{\frac{I_{leak}}{\mathrm{n}A}\frac{\tau_f}{\mu s}}$$

$$ENC_{\mathrm{therm}} = \frac{C_f}{q}\sqrt{\langle v^2_{\mathrm{therm}}\rangle} = \sqrt{\frac{kT}{q}\frac{2C_D}{3q}\frac{C_f}{C_{load}}} = 104e^- \times \sqrt{\frac{C_D}{100\,\mathrm{fF}}\frac{C_f}{C_{load}}}$$

$$ENC_{1/\mathrm{f}} \approx \frac{C_D}{q}\sqrt{\frac{K_f}{C_{ox}WL}}\sqrt{\ln\left(\tau_f\frac{g_m}{C_{load}}\frac{C_f}{C_D}\right)} = 9e^- \times \frac{C_D}{100\,\mathrm{fF}}(\text{for NMOS trans.})$$

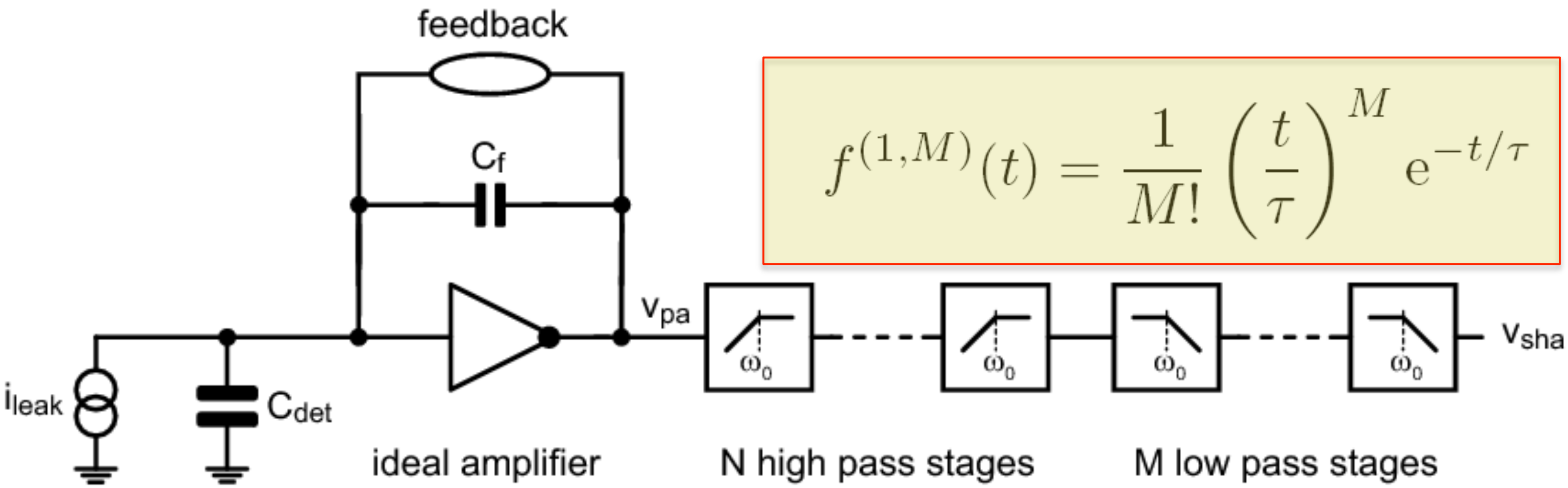
W, L = width and length of trans. gate
K_f = 1/f noise coefficient
C_{ox} = gate oxide capacitance

C_f = feedback capacitance
C_{load} = load capacitance
C_D = detector capacitance
τ_f = feedback time constant

reference
Rossi, Fischer, Rohe, Wermes
Pixel Detectors. Springer 2006

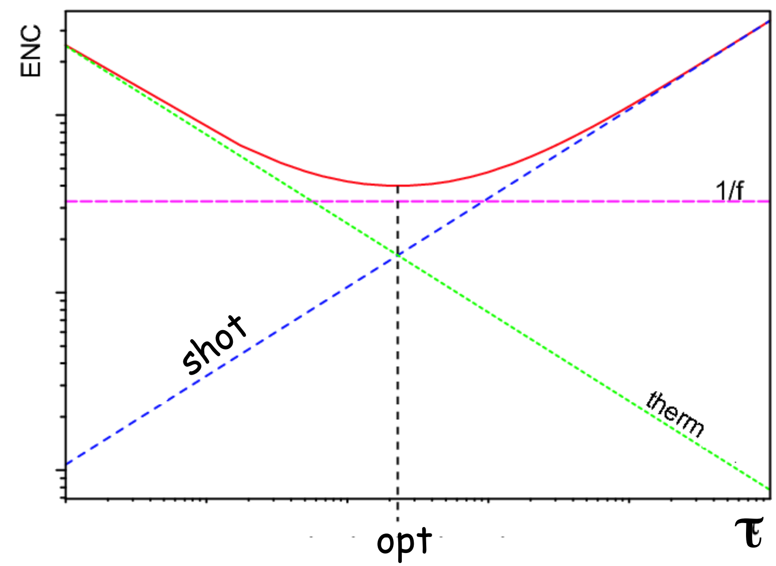
Noise in a pixel/strip detector (ionisation detector)

… with an additional filter amplifier (shaper) being the band width limiter



$$f^{(1,M)}(t) = \frac{1}{M!}\left(\frac{t}{\tau}\right)^{M} e^{-t/\tau}$$

$$\mathrm{ENC}^2(e^2) = 11\, I_0(\mathrm{nA})\, \tau(\mathrm{ns}) + 740\, \frac{1}{WL(\mu\mathrm{m}^2)}\, C_D^2(100\,\mathrm{fF}) + 4000\, \frac{1}{g_m(\mathrm{mS})}\, \frac{C_D^2(100\,\mathrm{fF})}{\tau(\mathrm{ns})}$$



Noise in a pixel/strip detector (ionisation detector)

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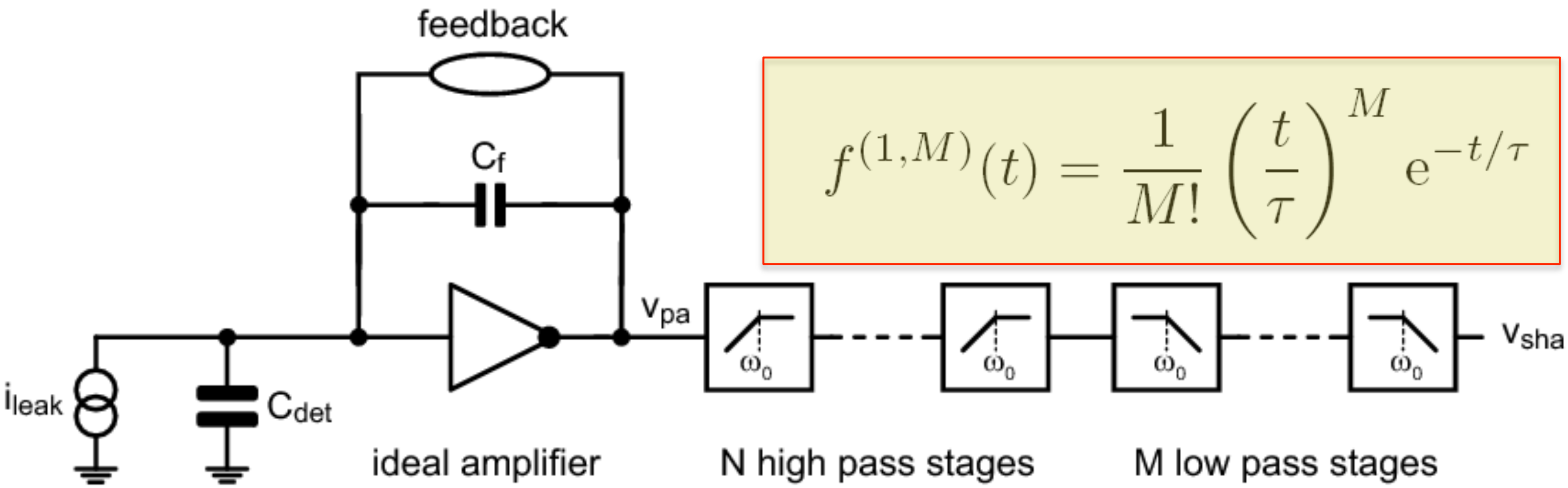
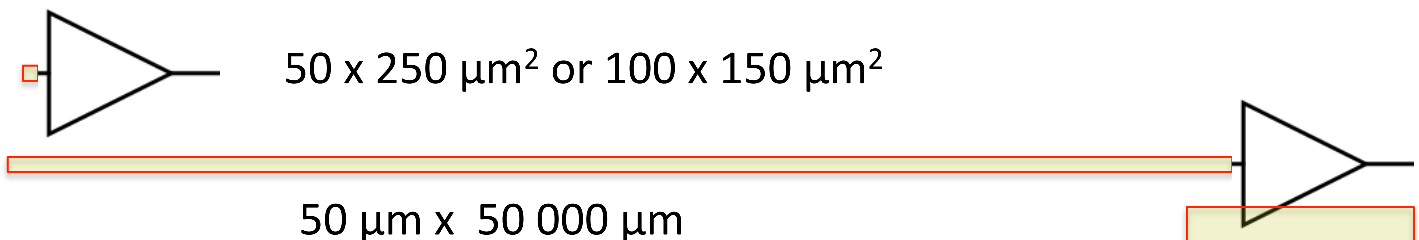


$$f^{(1,M)}(t) = \frac{1}{M!}\left(\frac{t}{\tau}\right)^{M} e^{-t/\tau}$$

comparing pixels and strips



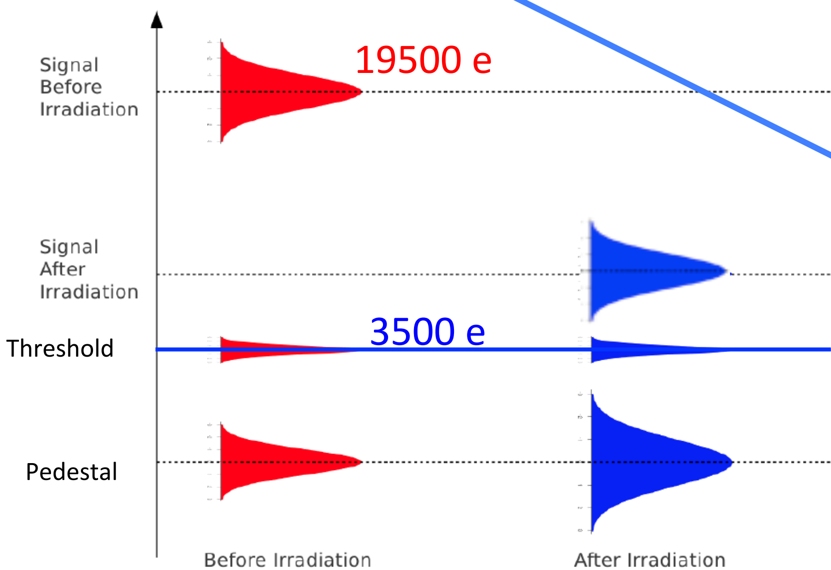
	C_D	I_0	τ	W	L	g_m	ENC therm	ENC 1/f	ENC shot	ENC tot
pixel	200 fF	1 nA	50 ns	20 µm	0.5 µm	0.5 mS	25 e⁻	17 e⁻	24 e⁻	**40 e⁻**
strip	20 pF	1 µA	50 ns	2000 µm	0.4 µm	5 mS	800 e⁻	200 e⁻	750 e⁻	**1100 e⁻**

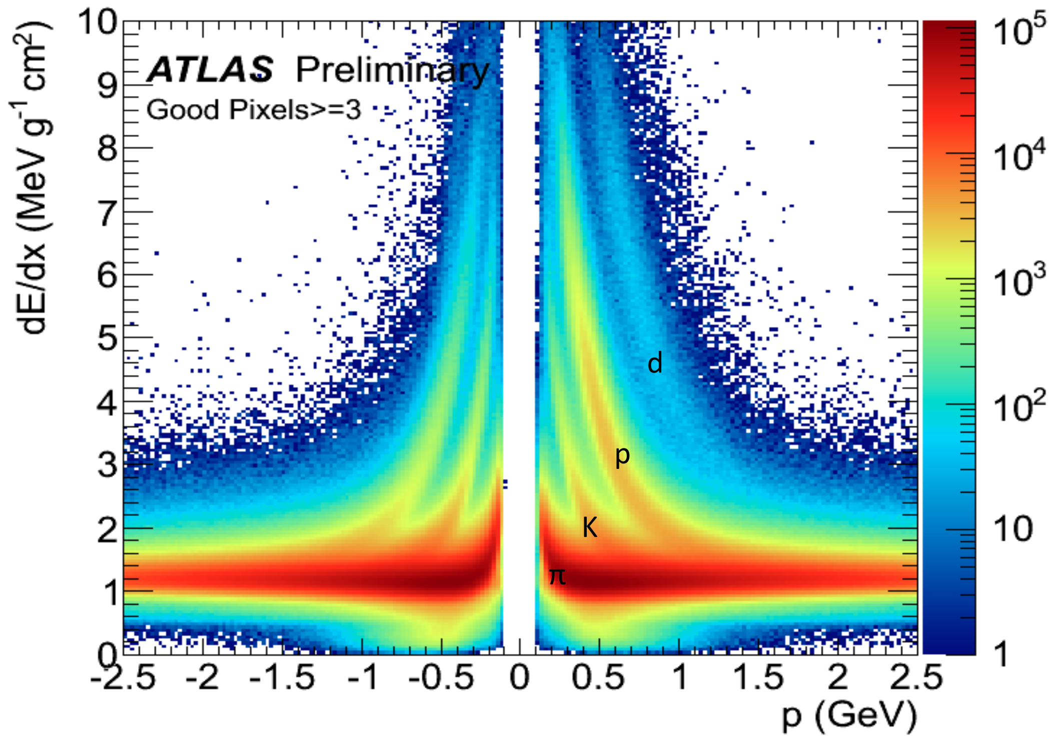
The typical S/N situation (... here ATLAS pixels)

Signal of a high energy particle ≙ 19500 e^- → <10000 e^- after irradiation

Charge on more than 1 pixel => S/N > 30 → S/N ~ 10

- ❑ Discriminator thresholds = 3500 e, ~40 e spread, ~170 e noise
- ❑ 99.8% data taking efficiency
- ❑ 95.9% of detector operational
- ❑ ca. 10 µm x 100 µm resolution (track angle dependent)
- ❑ 12% dE/dx resolution





C. Gemme et al., ATLAS-CONF-2011-016

How to make things better?

- more radiation hard?

- less complex?

- less expensive?

How to make sensors more radiation hard?

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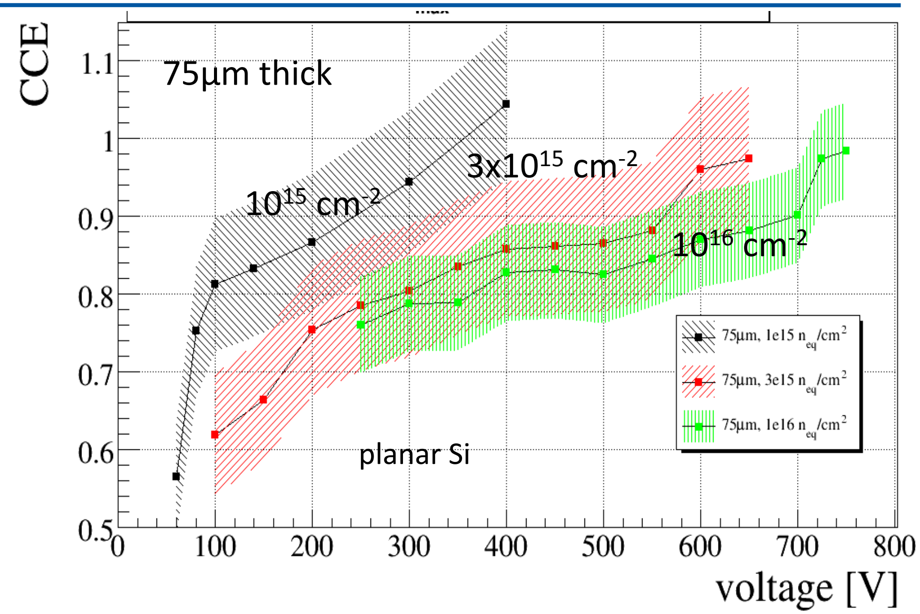
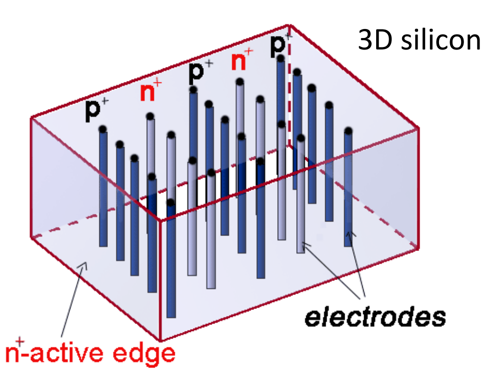
Planar sensors: (PPS collab.)

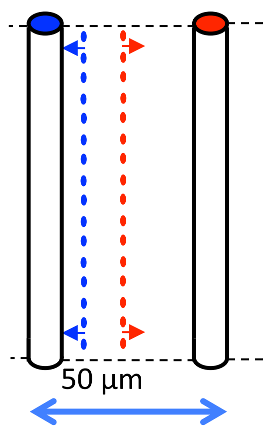
- work at 2x10^{16} n_{eq}/cm^2
- but need high bias voltage
- n in n (inner), n in p (outer layers)
- slim edges (guard ring optimization)



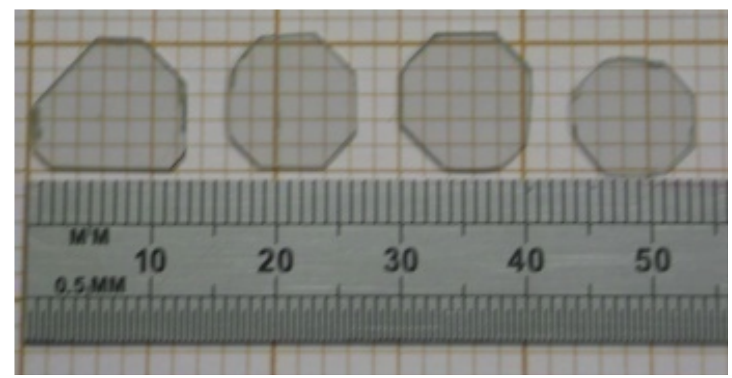
3D-Si sensors: (3D-Si collab.) → special geometry

- 50 µm electrode spacing → V_{bias} ~200 V only
- option for inner layers





mono-crystalline CVD diamond



current focus on poly-crystalline pixel modules (ATLAS DBM)

Diamond sensors: (RD42 & DBM collab)

- ~2000e at 2x10^{16} n_{eq} cm^2 → need low thresh.
- but S/N potentially better than Si at high fluence

skip 3D and CVD?

Hybrid Pixel Detectors @ LHC: PROs and CONs

- complex signal processing already in pixel cells possible
  - zero suppression
  - temporary storage of hits during L1 latency
- radiation hardness to 10^{15} n_{eq}/cm^2
- spatial resolution ~ 10 – 15 μm

PRO

… but also

- relatively large material budget: ~ 3% X_0 per layer (1% X_0 @ ALICE)
  - cooling, services
- complex and laborious module production
  - bump-bonding / flip-chip → expensive
  - many production steps
  - expensive

CON

Rate and radiation challenges at the innermost pixel layers

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Hybrid Pixels

	BX time	Particle Rate	Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	Mrad per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	2×10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	25	10000	2×10^{16}	> 500
LHC Heavy Ions (6×10^{27} cm^{-2} s^{-1})	20.000	10	$>10^{13}$	0.7
RHIC (8×10^{27} cm^{-2}s^{-1})	110	3,8	few 10^{12}	0.2
SuperKEKB (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	0.4

Monolithic Pixels

- lower rates
- lower radiation
- smaller pixels
- less material
- better resolution

DEPFET: Belle II
MAPS: STAR@RHIC
and future
ALICE ITS

assumed lifetimes:
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

NEW developments

DEPFET Pixels -> Belle II

Monolithic Pixels -> STAR@RHIC, ALICE

(Mixed?) Monolithic/Hybrid -> LHC Upgrade?

(Semi)-Monolithic Pixel Detector Projects

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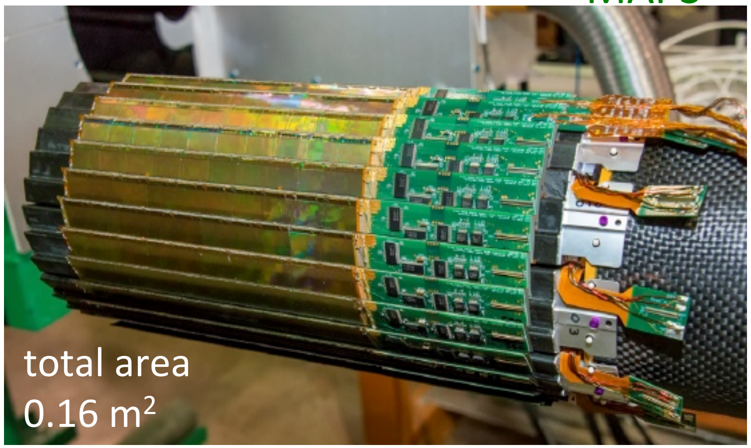
STAR / RHIC

MAPS



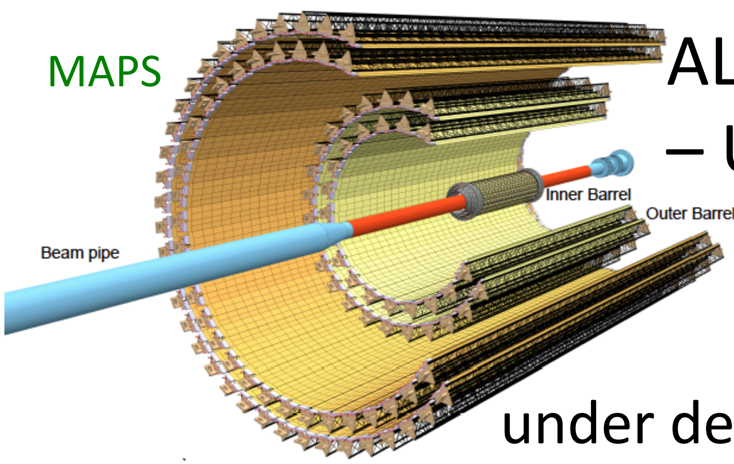
in operation since 2014

(Belle II)

DEPFET

in production for 2017

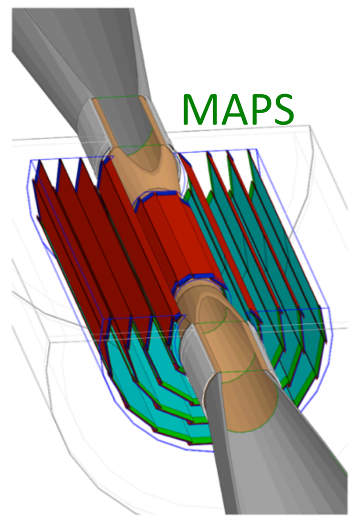
MAPS



ALICE – Upgrade

total area
~10 m^2

under development
target: 2018

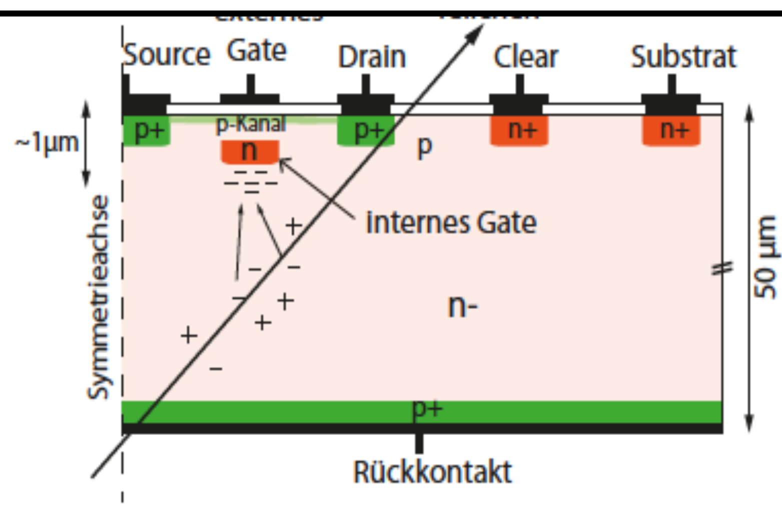


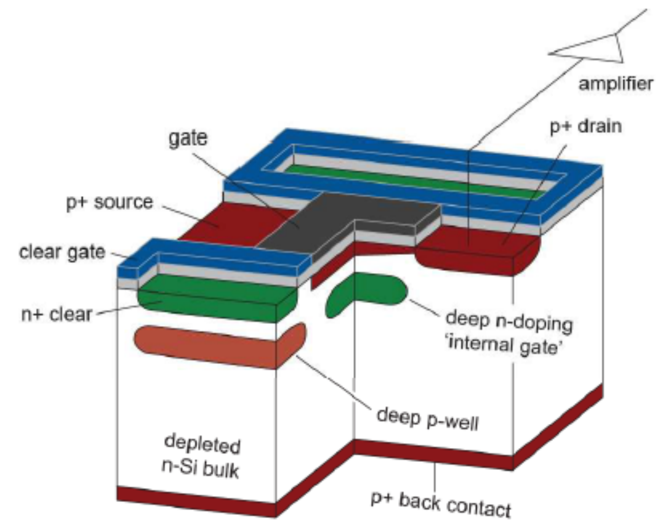
ILC

total area
? m^2

current baseline

DEPFET Pixels





How does a DEPFET work?

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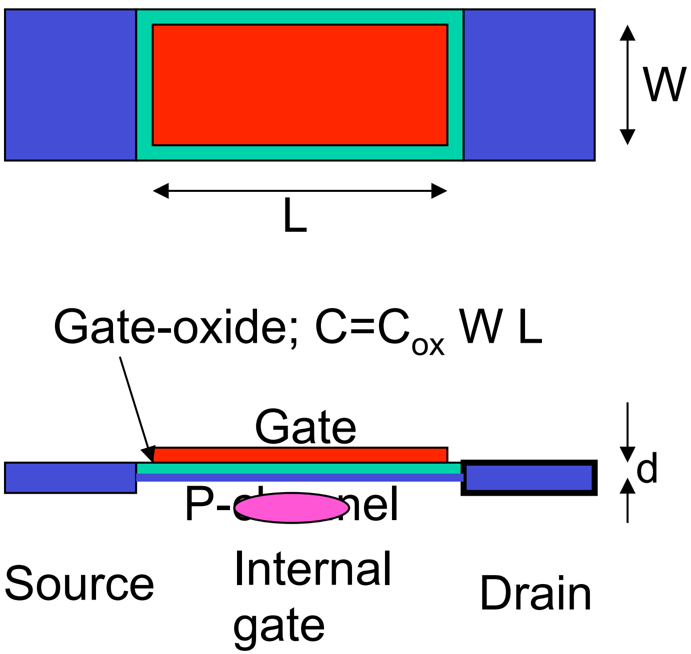

A charge q in the internal gate induces a mirror charge αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha q / C = \alpha q / (C_{ox} W L)$ which in turn changes the transistor current I_d .

FET in saturation:

$$I_d = \frac{W}{2L} \mu C_{ox} \left(V_G + \frac{\alpha q_s}{C_{ox} WL} - V_{th} \right)^2$$

I_d: source-drain current
C_{ox}: sheet capacitance of gate oxide
W,L: Gate width and length
μ: mobility (p-channel: holes)
V_g: gate voltage
V_{th}: threshold voltage

Conversion factor:

$$g_q = \frac{dI_d}{dq_s} = \frac{\alpha\mu}{L^2} \left(V_G + \frac{\alpha q_s}{C_{ox} WL} - V_{th} \right) = \alpha \sqrt{2 \frac{I_d \mu}{L^3 W C_{ox}}}$$

q

$$g_m : g_q = \alpha \frac{g_m}{WLC_{ox}} = \alpha \frac{g_m}{C}$$

How does a DEPFET work?

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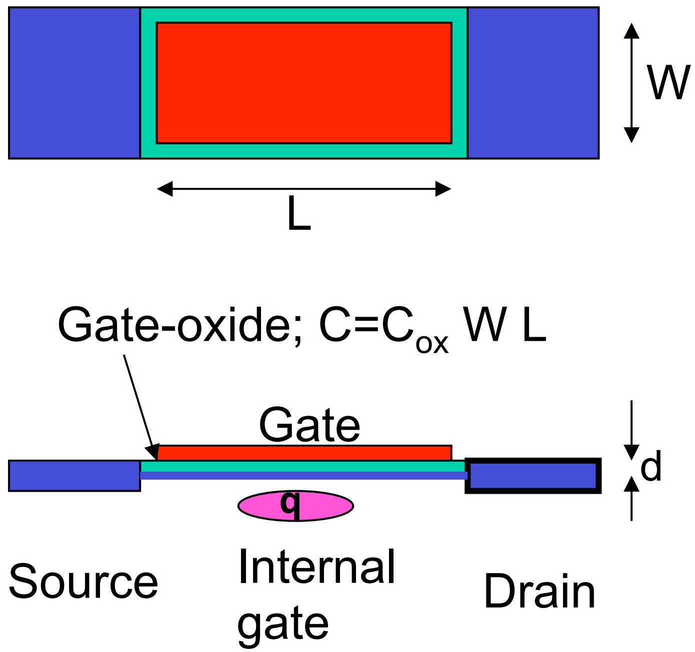
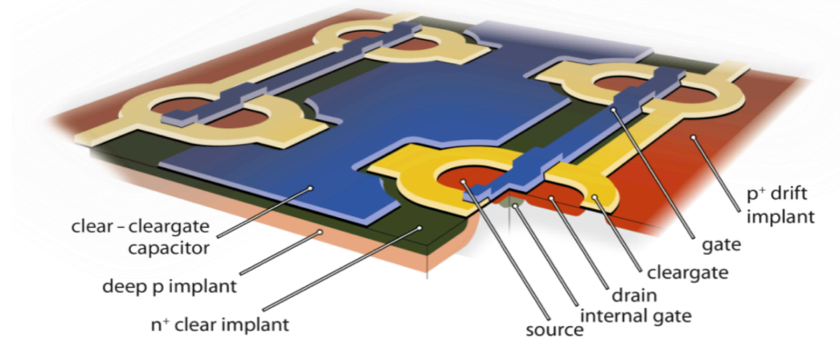
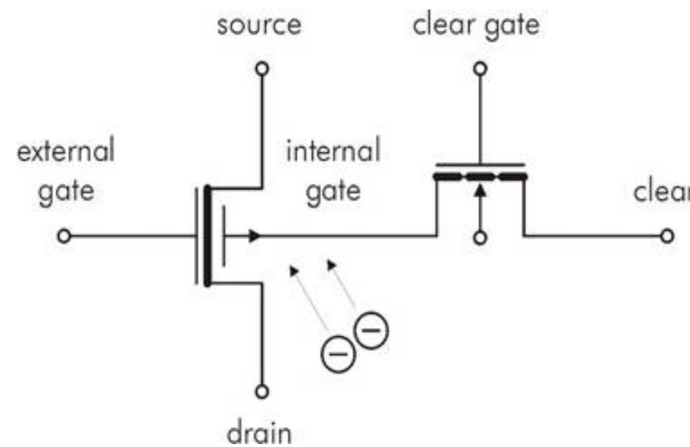


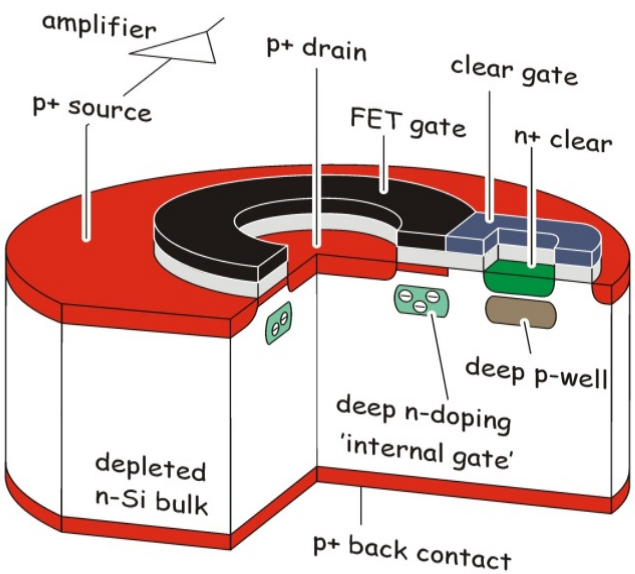


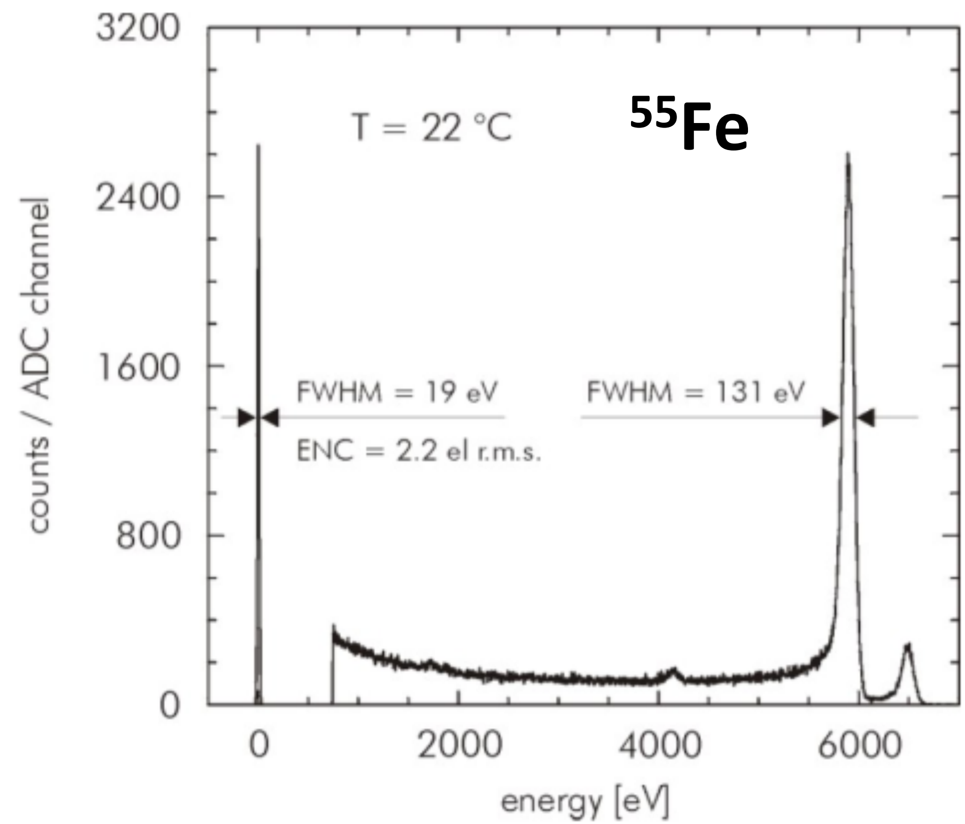


A charge q in the internal gate induces a mirror charge αq in the channel (α <1 due to stray capacitance). This mirror charge is compensated by a change of the gate voltage: $\Delta V = \alpha\, q / C = \alpha\, q / (C_{ox}\, W\, L)$ which in turn changes the transistor current I_d .

- Internal amplification g_q~ 500 pA/e^-
- Small intrinsic noise
- Sensitive off-state, no power consumption

DEPFET Pixels for Imaging



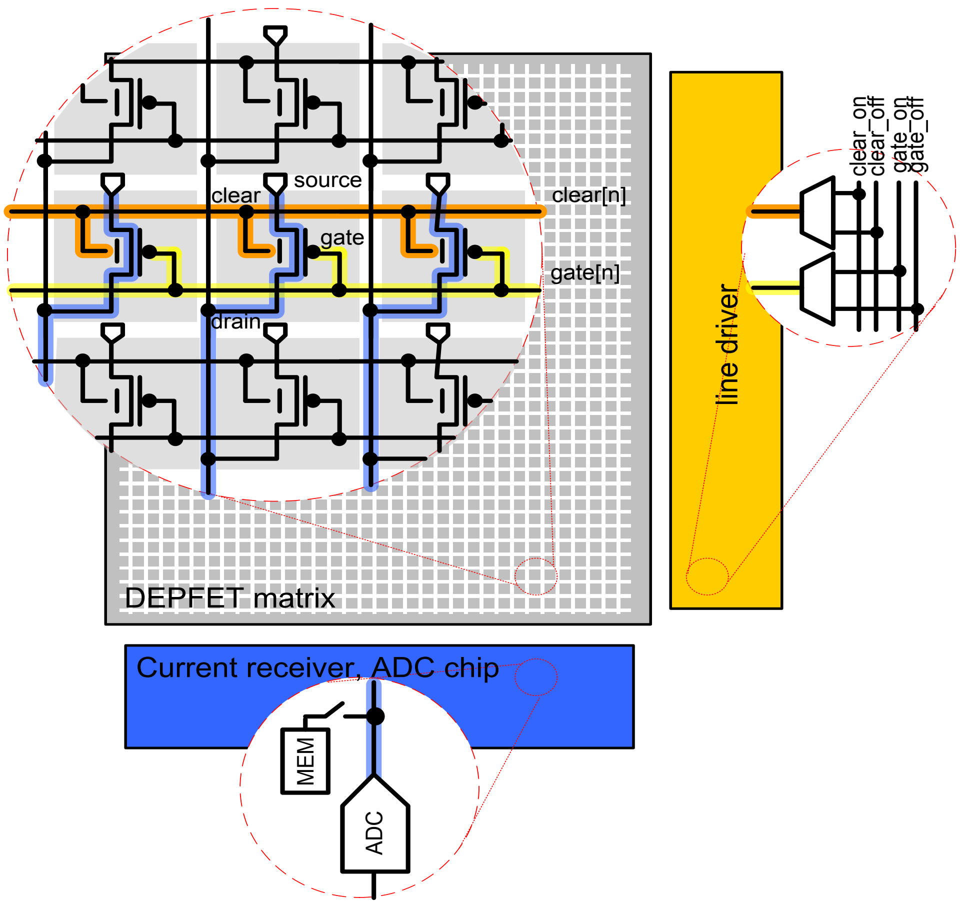


Developed for X-ray astronomy (XEUS mission)
Energy resolution **131 eV** (5.9 keV Fe55)
Noise ENC=**2.2 e$^-$** (T=22 ^{o}C)
Shaping time τ= 10 µs

excellent noise performance due to

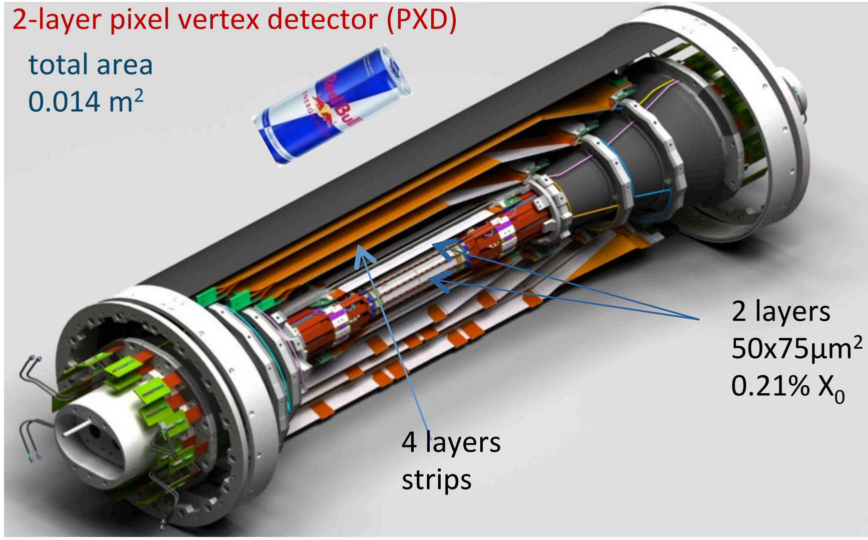
- small capacitance (gate – channel)
- long shaping time (10 µs)

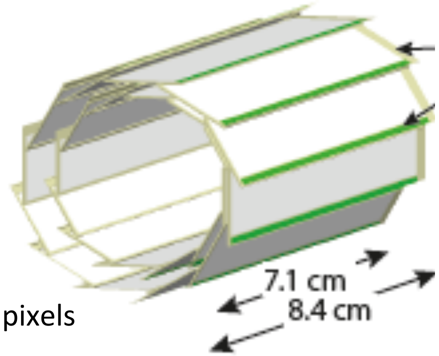
DEPFET pixel array

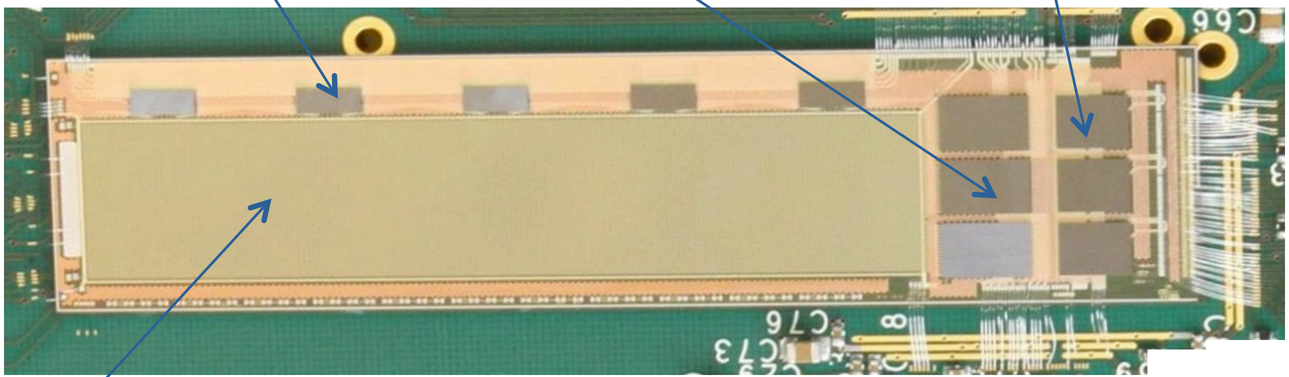


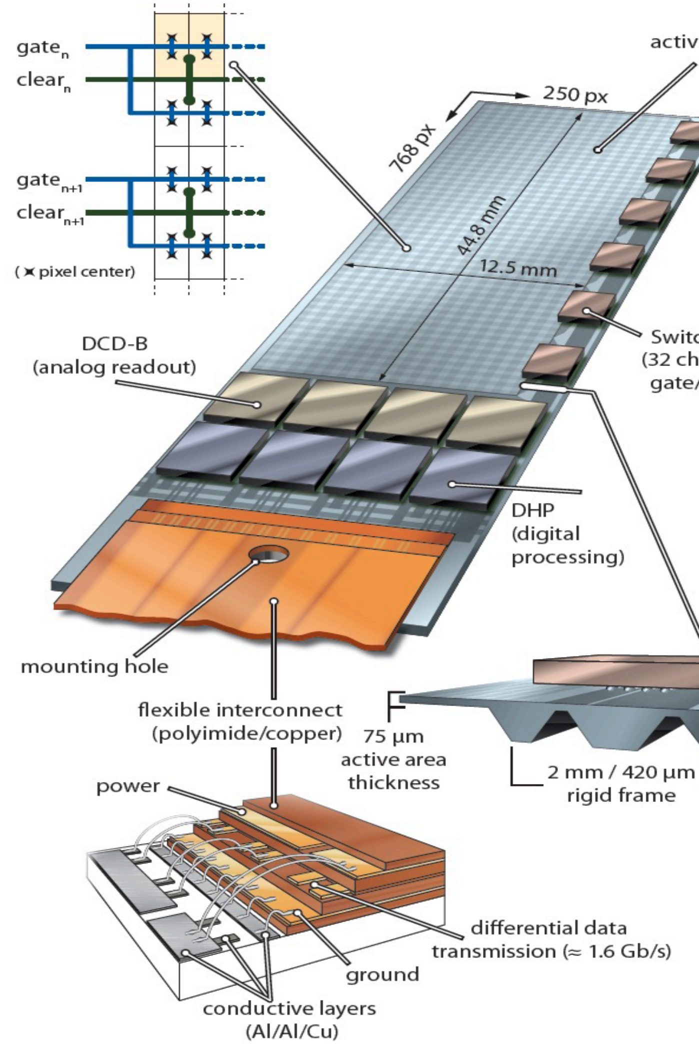
- DEPFET pixel transistors arranged in a matrix
- row wise select -> column wise readout of transistor (drain) currents
- Gate and clear lines need a steering chip
- Long drain readout lines to keep material out of the acceptance region
- 100 ns per row
  20 µs per frame

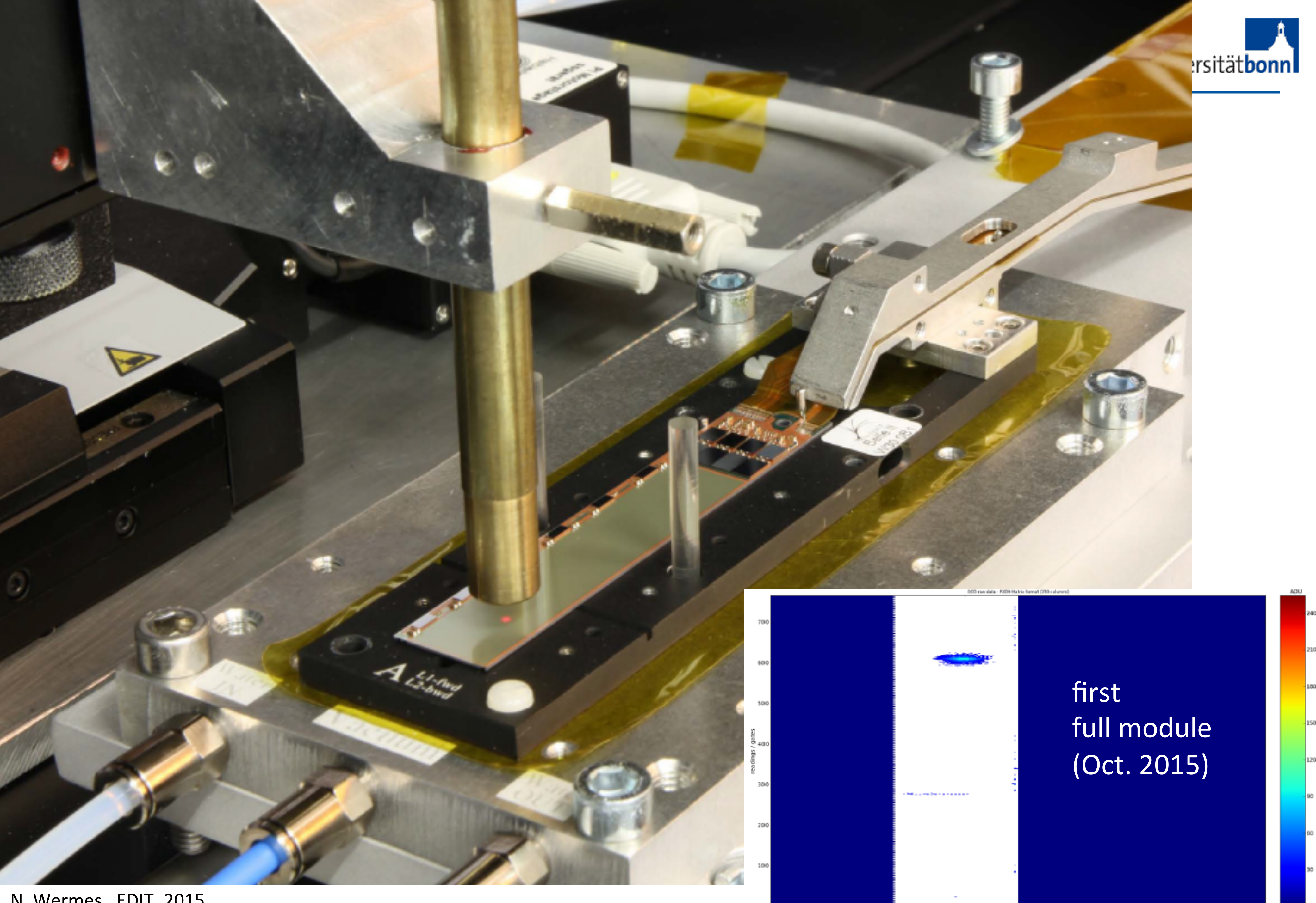
DEPFET PXD ... very different from LHC pixels



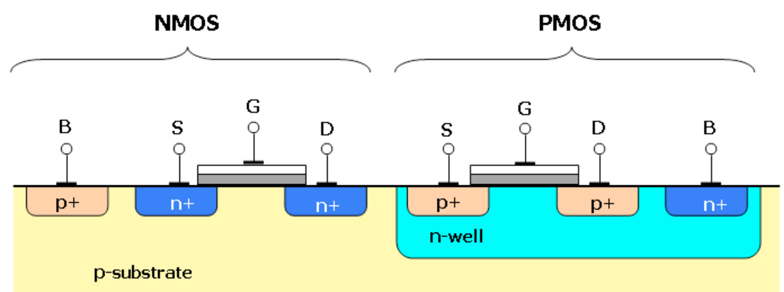






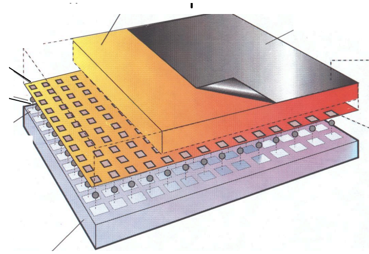

A
L1-fwd
L2-bwd
first
full module
(Oct. 2015)
ADU

CMOS Pixels (sometimes called MAPS)

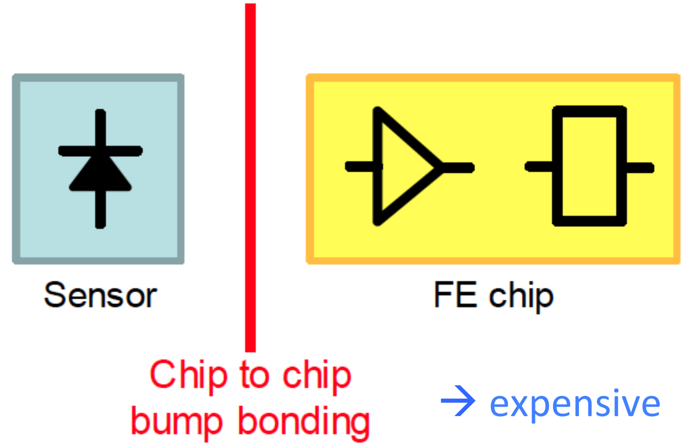


skip ?

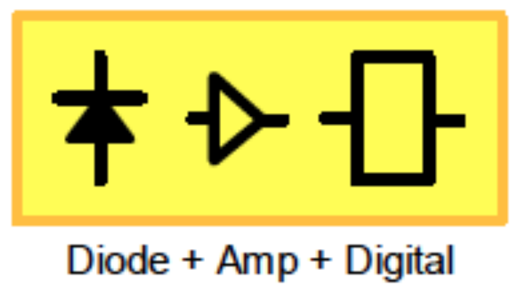
From HYBRID to monolithic pixel detectors



- standard HYBRID pixels
  - various sensors: planar-Si, 3D-Si, diamond
  - mixed signal R/O chip (FE-I3, FE-I4, ROC ...)

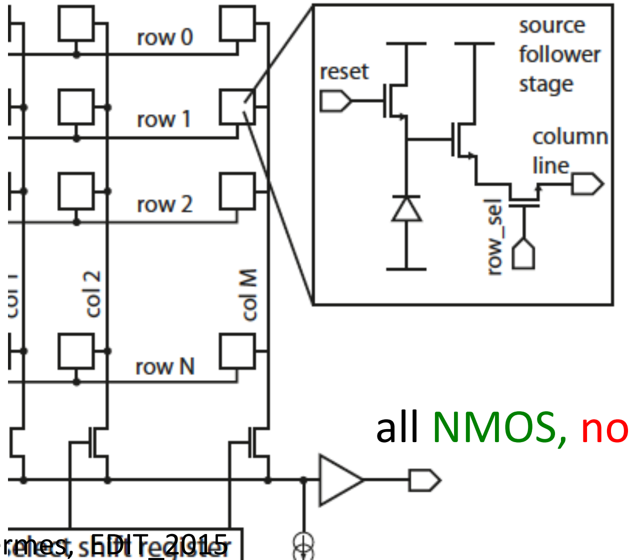


- Monolithic Active Pixel Sensors
  - MAPS using CMOS with Q-collection in epi-layer (usually by diffusion → recent advances)
  - depleted DMAPS using HR substrate or HV process to create depletion region: $d \sim \sqrt{\rho \cdot V}$
  - CMOS on SOI



MAPS - epi

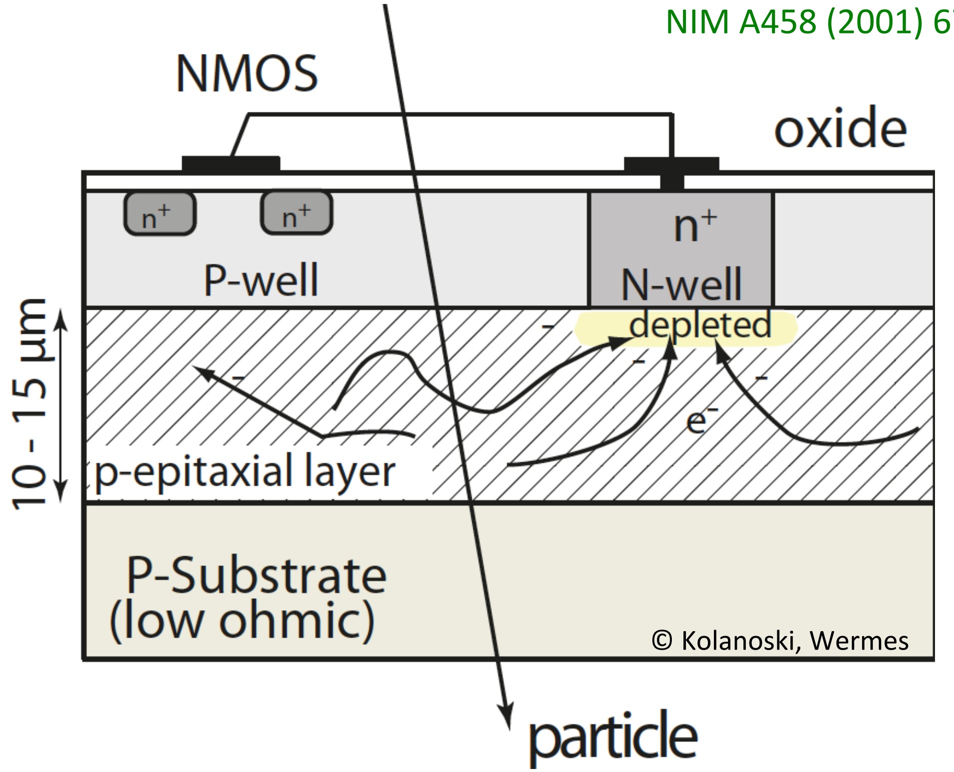
+ 'standard CMOS' process
+ fewer interconnections
+ very thin ... low mass
+ low power
+ small pixel size
+ CMOS circuitry, but limited to NMOS
– small signal
– slow charge collection
– frame readout, rolling shutter
– area limited by chip size
– radiation tolerance



all NMOS, no PMOS

CMOS with epi-layer as active layer

R. Turchetta et al
NIM A458 (2001) 677-689

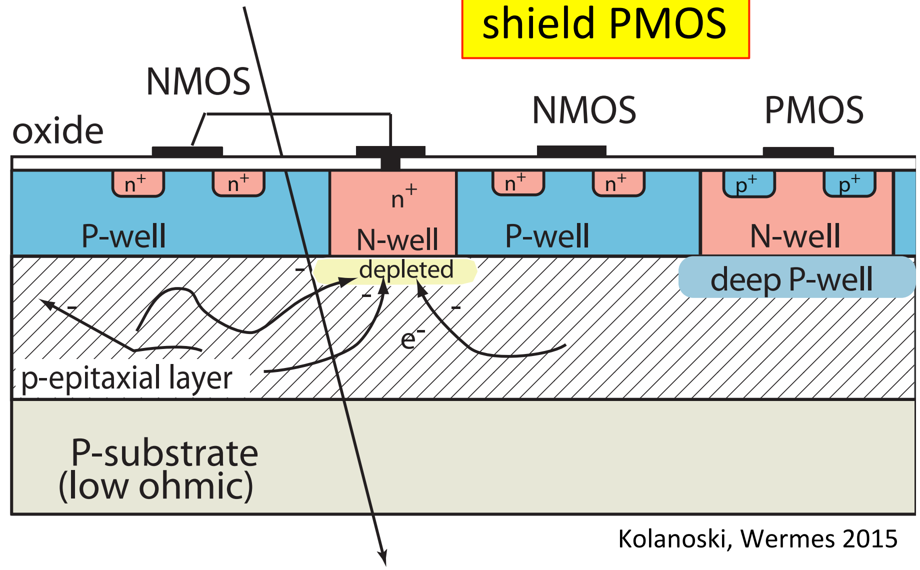


- realized 2014
  in STAR experiment
- target for ALICE upgrade

MAPS – epi: PROBLEM

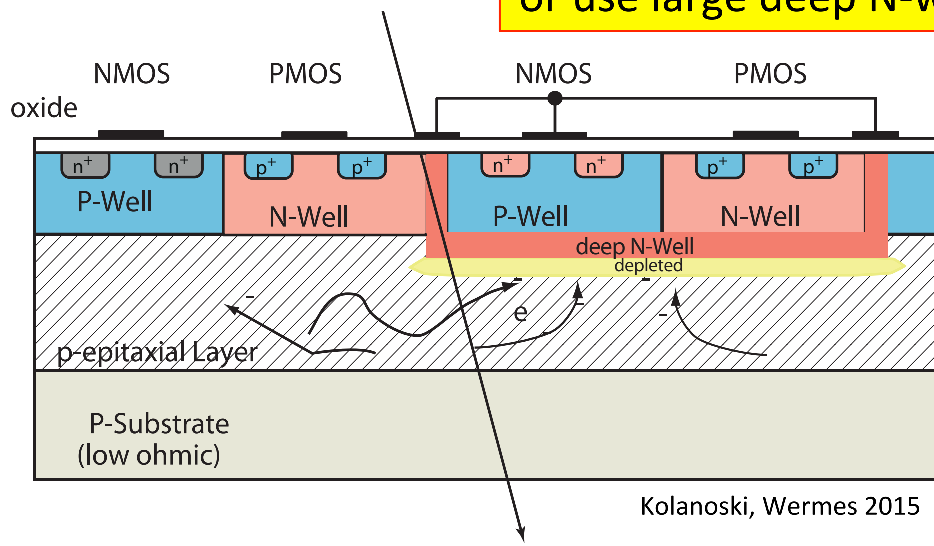
+ ‘standard CMOS’ process
+ fewer interconnections
+ very thin ... low mass
+ low power
+ small pixel size
+ CMOS circuitry, but limited to NMOS
– small signal
– slow charge collection
– frame readout, rolling shutter
– area limited by chip size
– radiation tolerance

shield PMOS



Kolanoski, Wermes 2015

or use large deep N-well



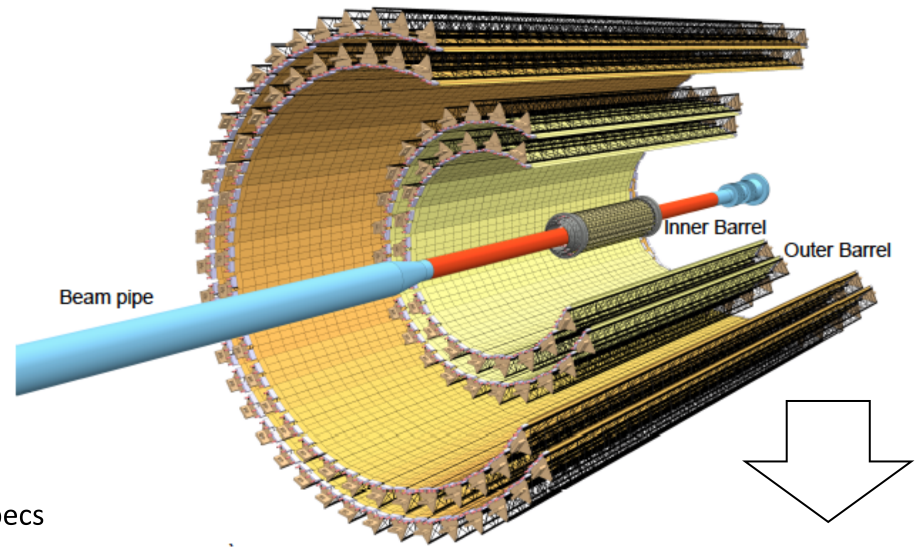
Kolanoski, Wermes 2015

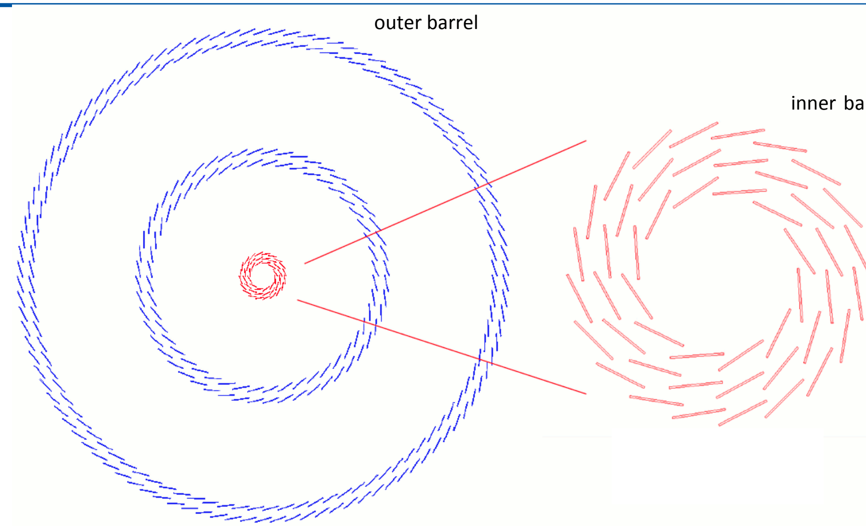
important:
multiple wells

MAPS for ALICE (2018) and for the ILC (20xx?)

ALICE

10.7m^2

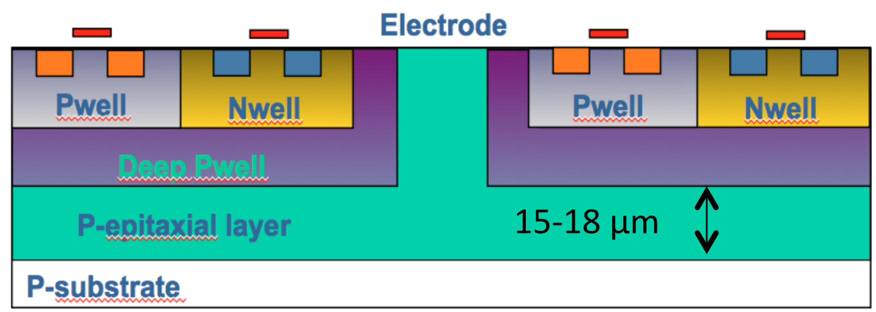




specs

Parameter	Inner barrel	Outer barrel
Max. silicon thickness	50 µm	
Intrinsic spatial resolution	5 µm	30 µm
Chip size	15 mm × 30 mm ($r\phi \times z$)	
Max. dead area on chip	2 mm ($r\phi$), 25 µm (z)	
Max. power density	300 mW/cm^2	100 mW/cm^2
Max. integration time	30 µs	
Max. dead time	10 % at 50 kHz Pb–Pb	
Min. detection efficiency	99 %	
Max. fake hit rate	10^{-5}	
TID radiation hardness[a]	700 krad	10 krad
NIEL radiation hardness[a]	10^{13} 1 MeV n_{eq}/cm^2	3×10^{10} 1 MeV n_{eq}/cm^2

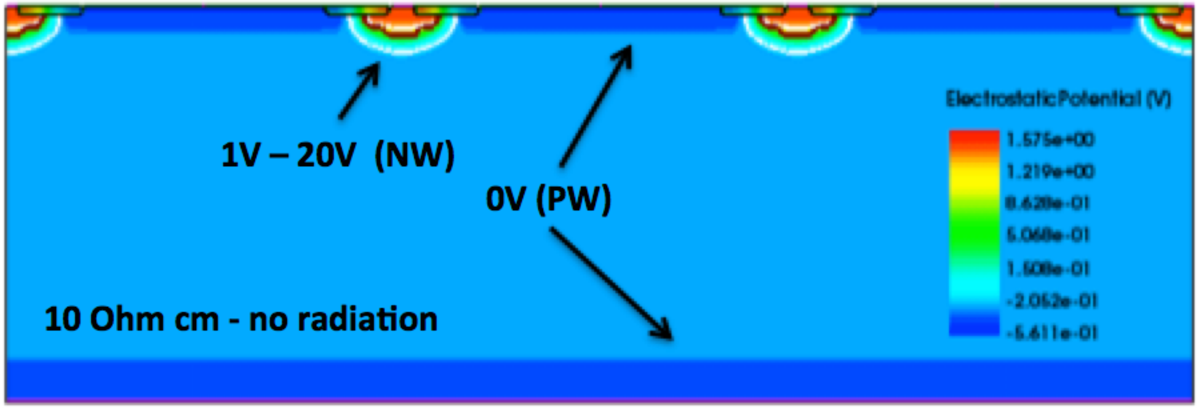
[a] This includes a safety factor of ten



skip HV/HR?

What is needed to make CMOS pixels also usable in the LHC radiation environment?

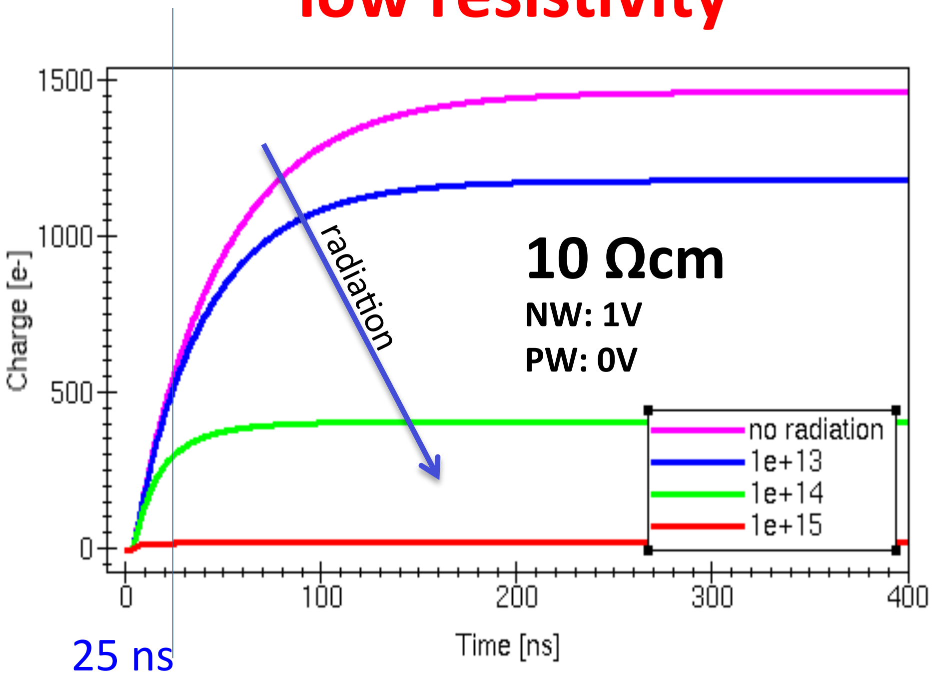
TCAD simulations: resistivity – voltage – fill factor



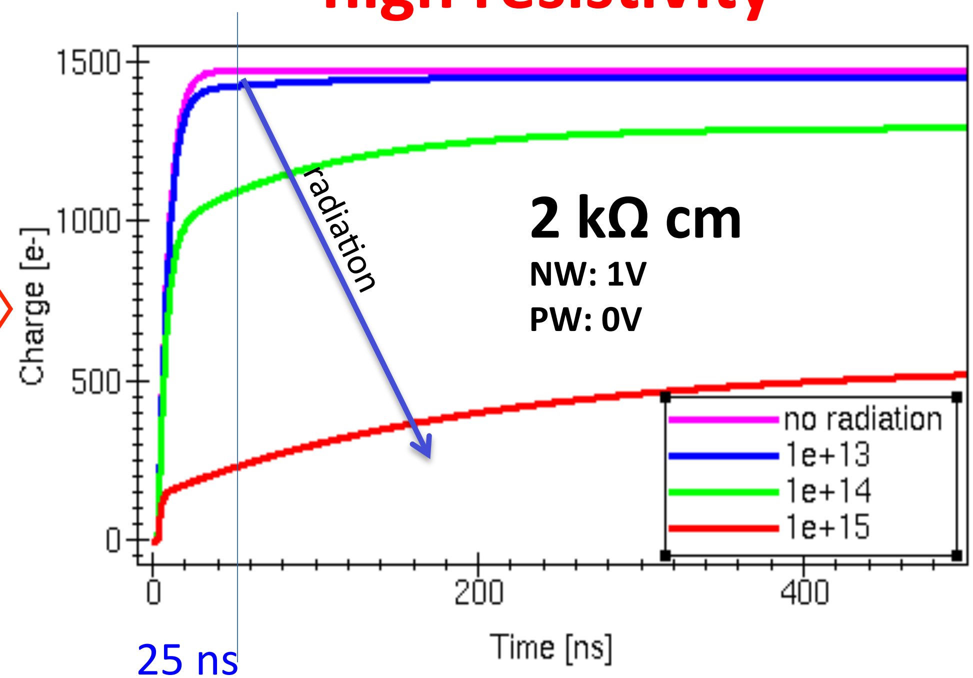
Substrate: 10 Ωcm – 2kΩ cm
Nwell: 1V – 20 V
Pwell: 0V

from Tomasz Hemperek

low resistivity



high resistivity



TCAD simulations: resistivity – voltage – fill factor

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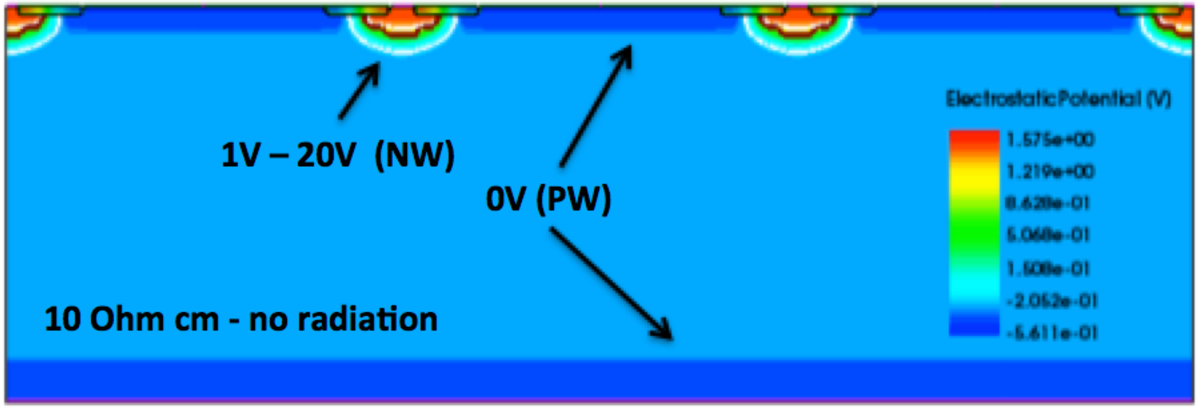

Substrate: 10 Ωcm – 2kΩ cm
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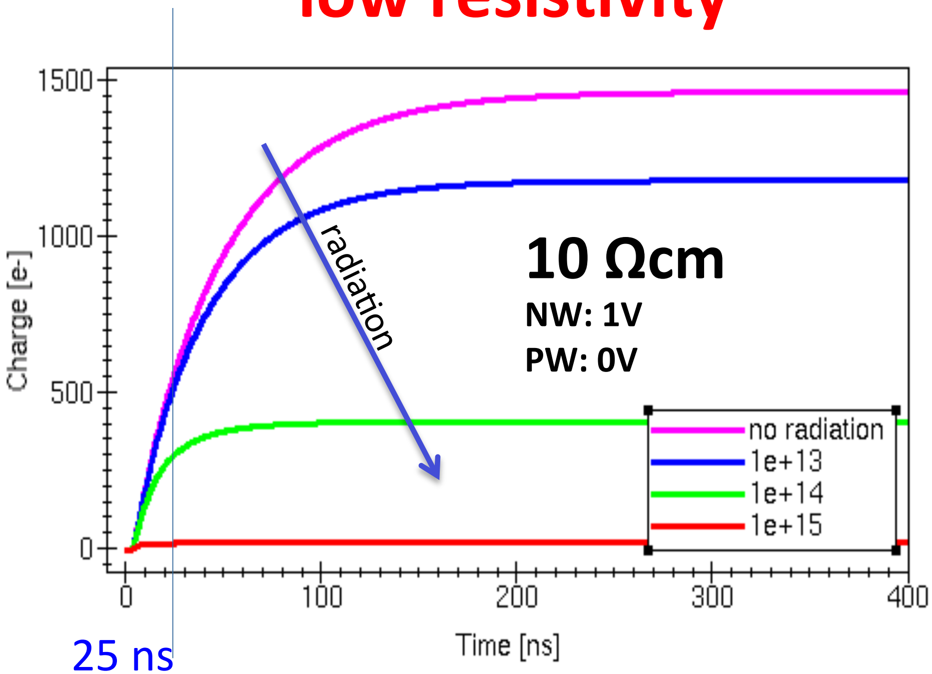
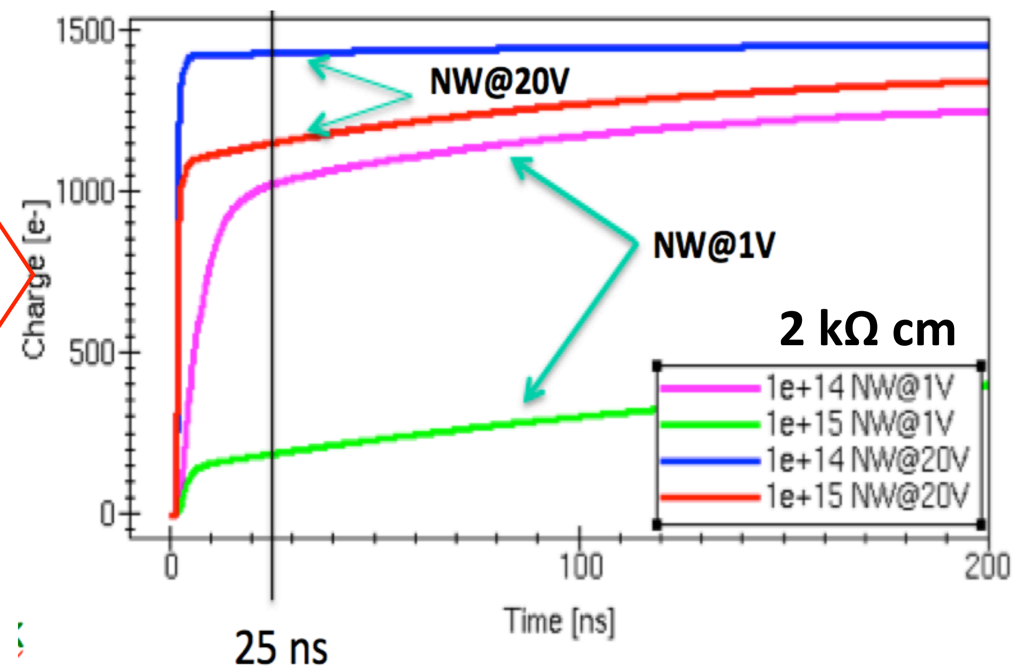
from Tomasz Hemperek

low resistivity



HR plus (high) voltage



Fill Factor influence: here at 10^{15} n_{eq}/cm^2

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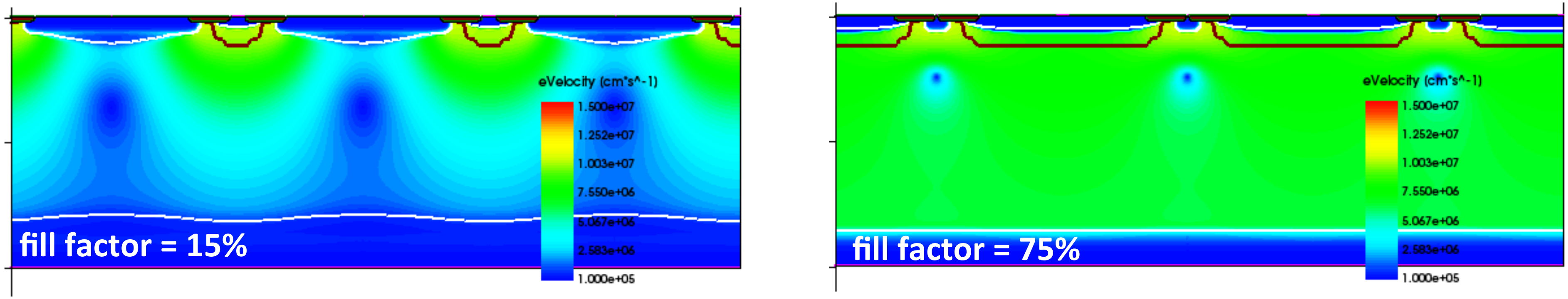
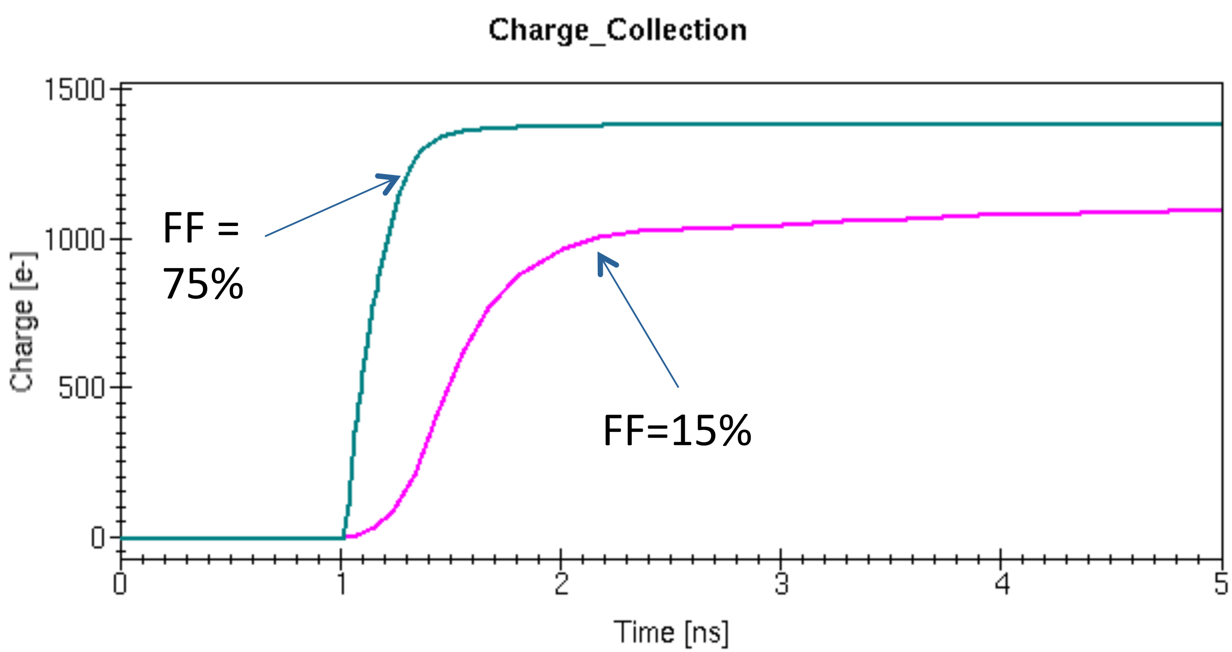
Electron Velocity



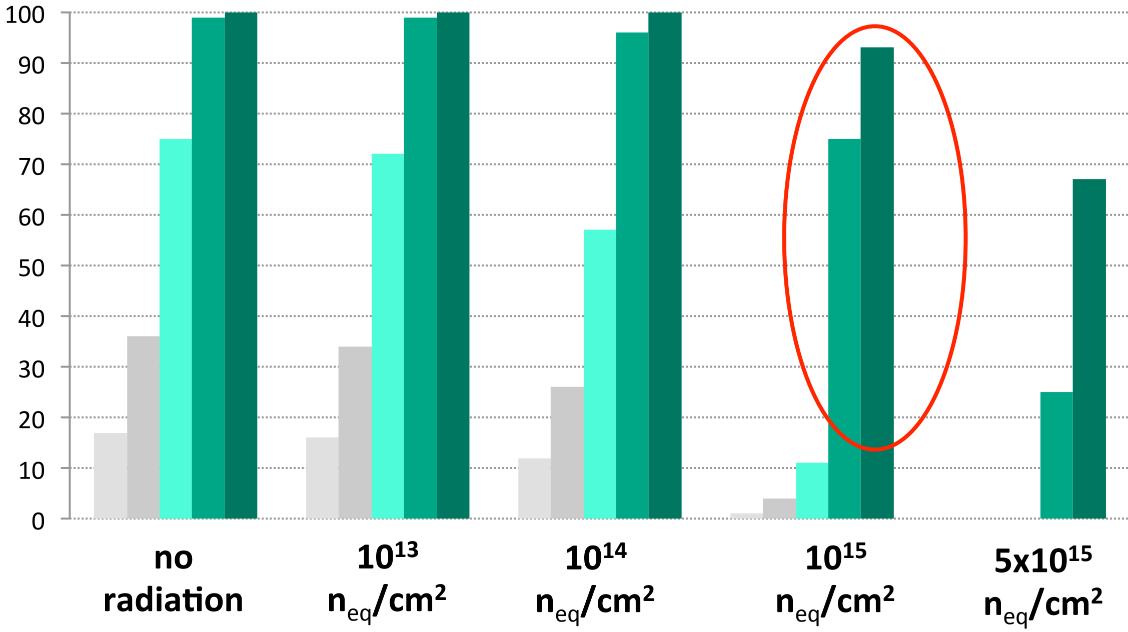


NW: 20V
PW: 0V
Substrate:2kΩ cm
Dose: 10^{15} n_{eq}/cm^2

Tomasz Hemperek

Summary: Resistivity, Voltage, Fill-Factor

fraction of collected charge in first 10ns



	substrate resistivity [Ωcm]	Bias [V]	Fill Factor [%]
	10	1	15
	10	20	15
	2k	1	15
	2k	20	15
	2k	20	75

from Tomasz Hemperek

Current approaches (a classification)

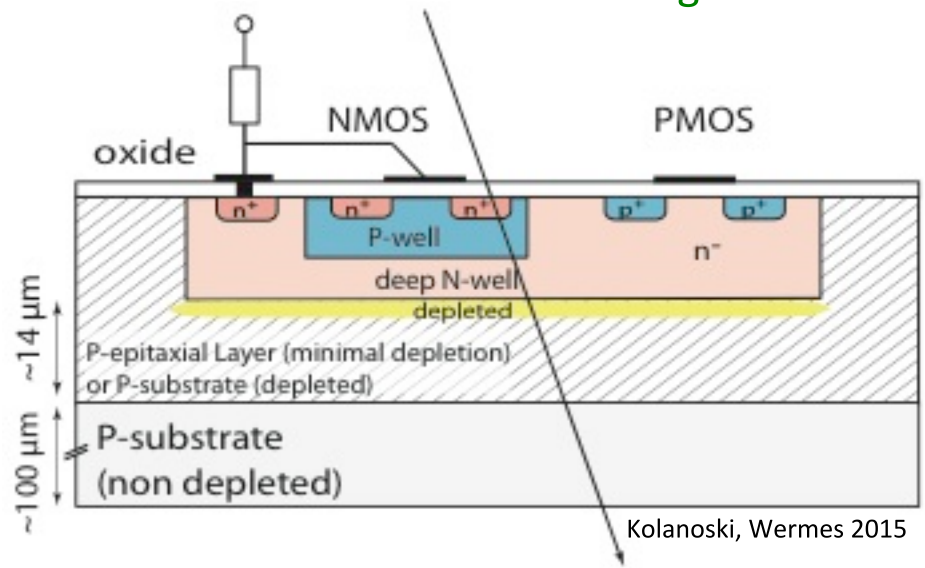
HV - CMOS

e.g. AMS technology

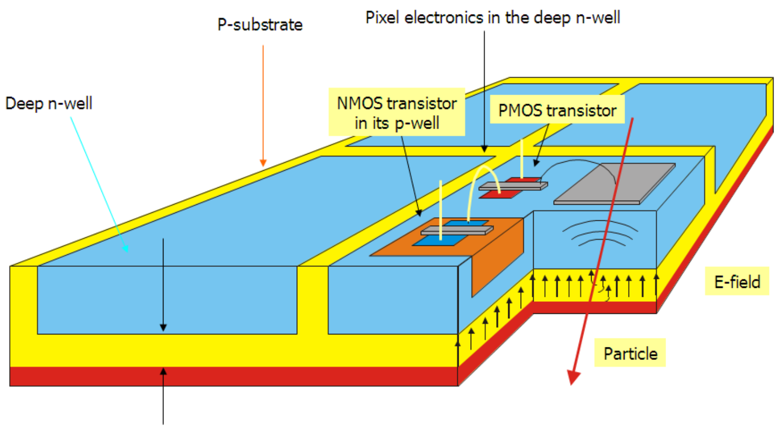
$$d \sim \sqrt{\rho \cdot V}$$

I. Peric et al.

Nucl.Instrum.Meth. A582 (2007) 876-885
Nucl.Instrum.Meth. A765 (2014) 172-176



Kolanoski, Wermes 2015



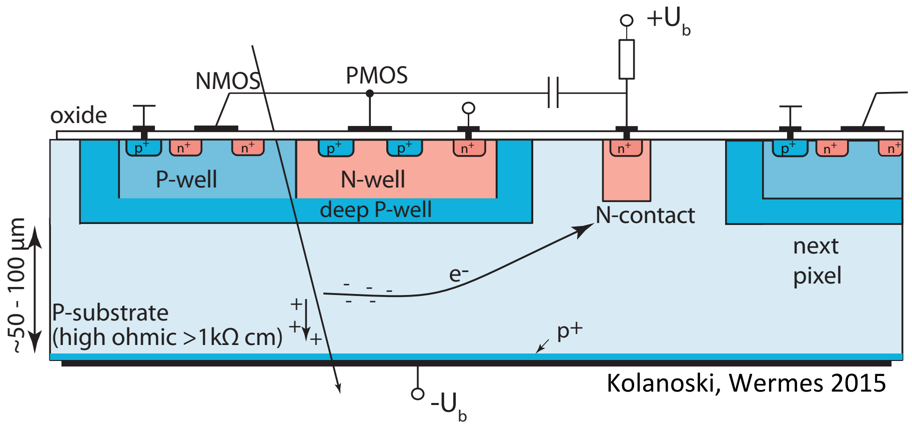
- AMS 350 nm and 180 nm HV process (p-bulk) ... 60-100 V
- deep n-well to put nMOS (in extra p-well) and pMOS (limitation)
- ~10 - 15 µm depletion depth → 1-2 ke signal
- various pixel sizes (~20 x 20 to 50 x 125 µm²)
- can also replace „sensor“ (amplified signal) in a „hybrid pixel“ bonding (bump, **glue**, other...) to FE-chip => **CCPD**

Current approaches (a classification)

HR - CMOS

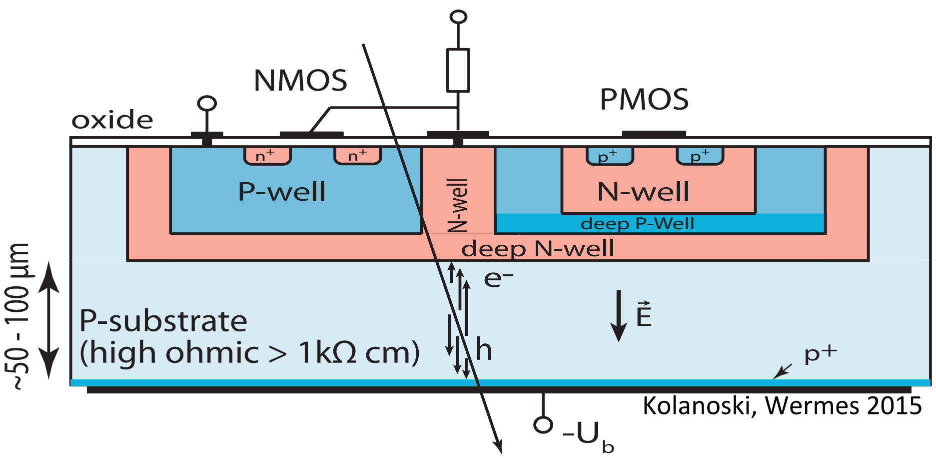
$$d \sim \sqrt{\rho \cdot V}$$

Mattiazzo, S,. W. Snoeys et al.
NIM A718 (2013) 288-291
Havranek, Hemperek, Krüger, NW et al.
JINST 10 (2015) 02, P02013



- (D)MAPS like configuration but w/ depleted bulk
- small collection node
- long drift path

=> **smaller C, more trapping**



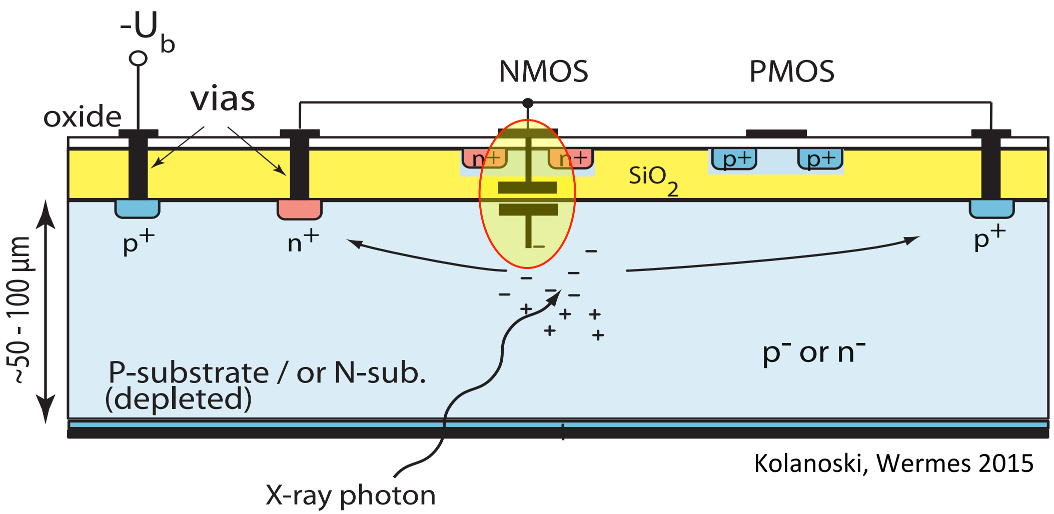
- deep n and deep p wells
- large collection node
- short drift path

=> **larger C, less trapping**

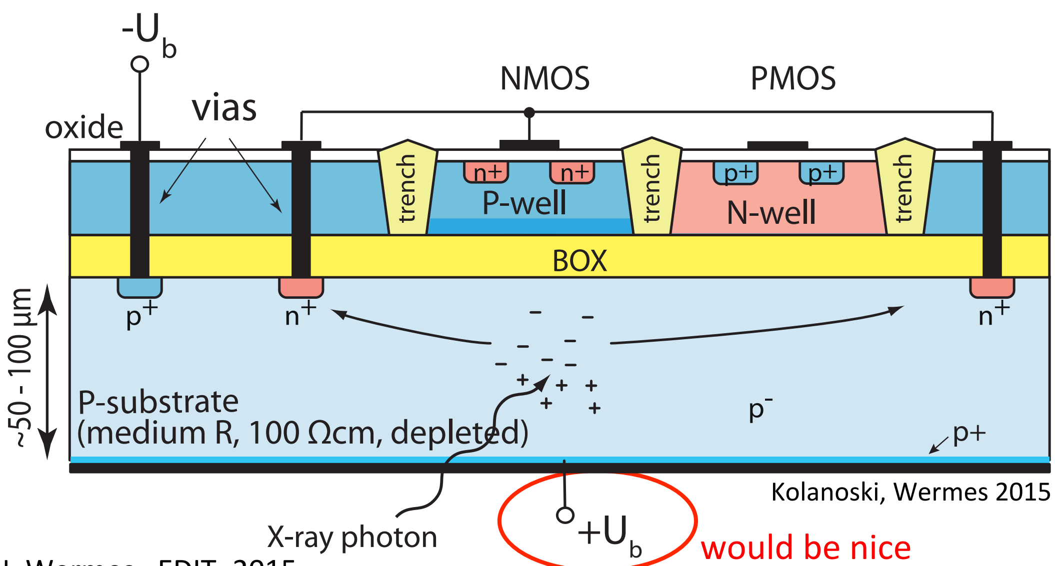
Current approaches (a classification)

CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$

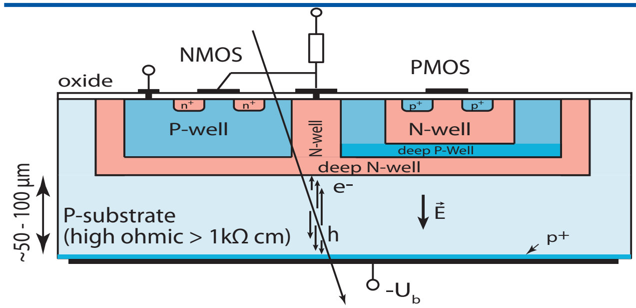


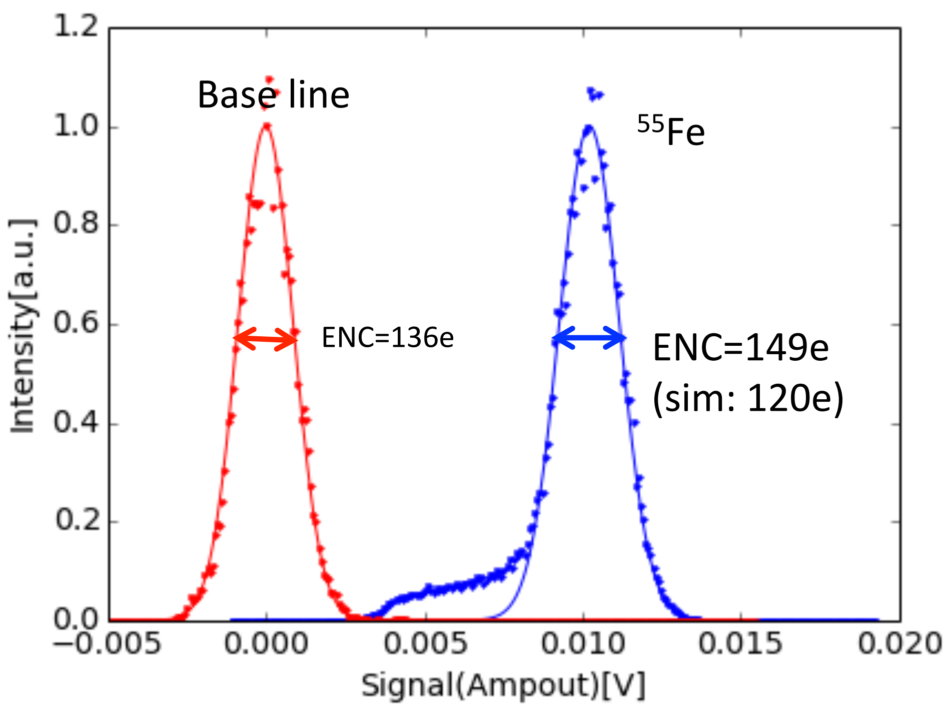
- **FD-SOI**
- OKI/LAPIS/KEK
  Y. Arai et al.
- issues
  - back gate effect
  - radiation issues due to BOX
- cures invented in recent years
- but not suited for LHC - pp

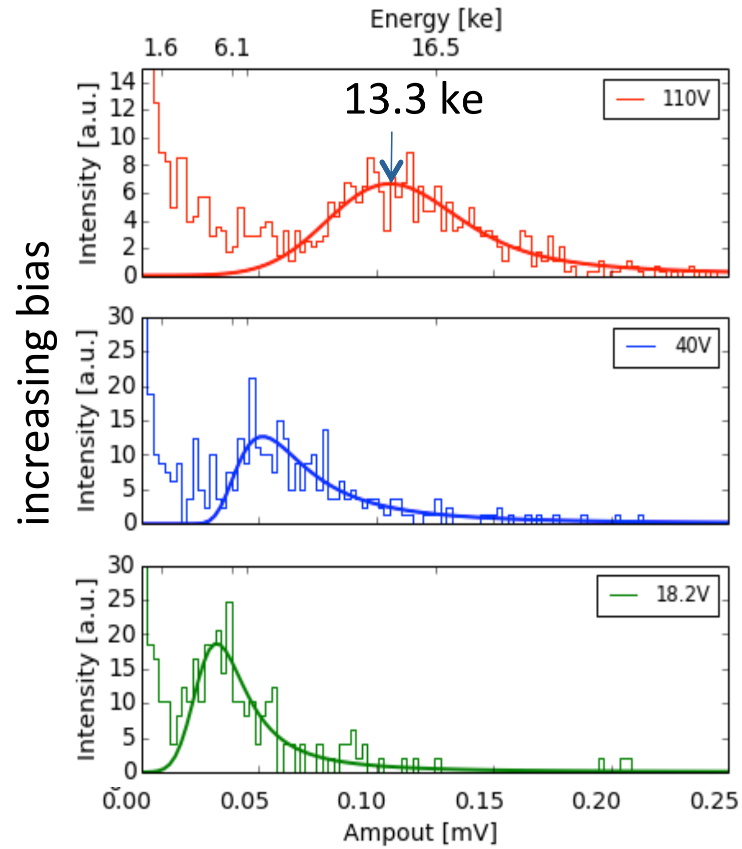


- **HV-SOI (thick film)**
- Hemperek, Kishishita, Krüger, NW
  doi:10.1016/j.nima.2015.02.052
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

Prototype results are encouraging …

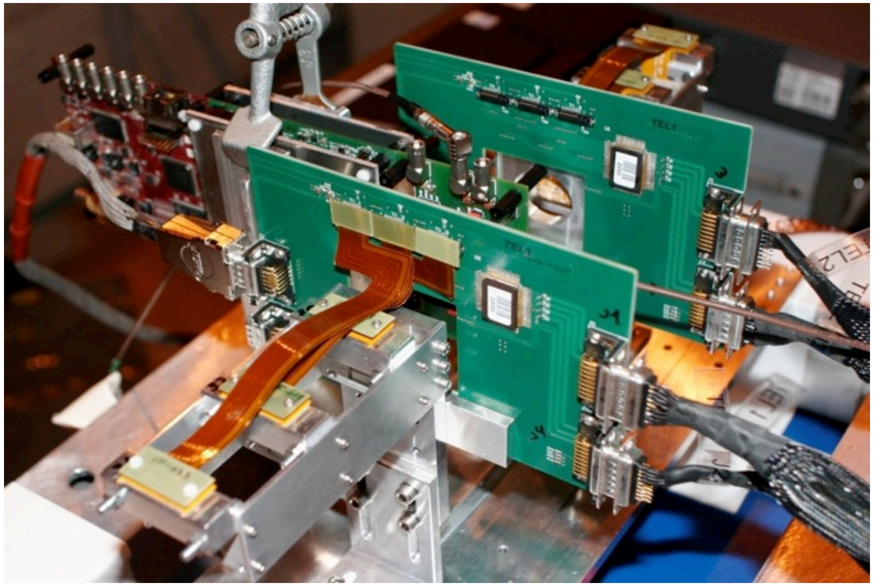


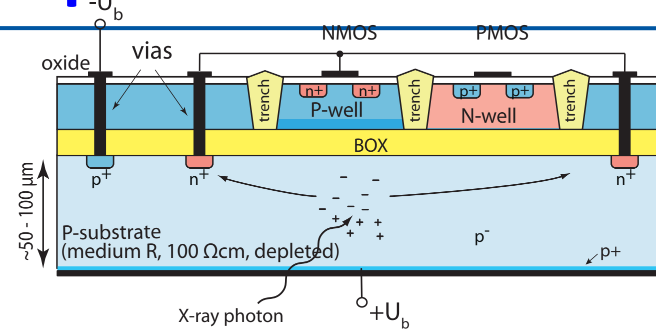


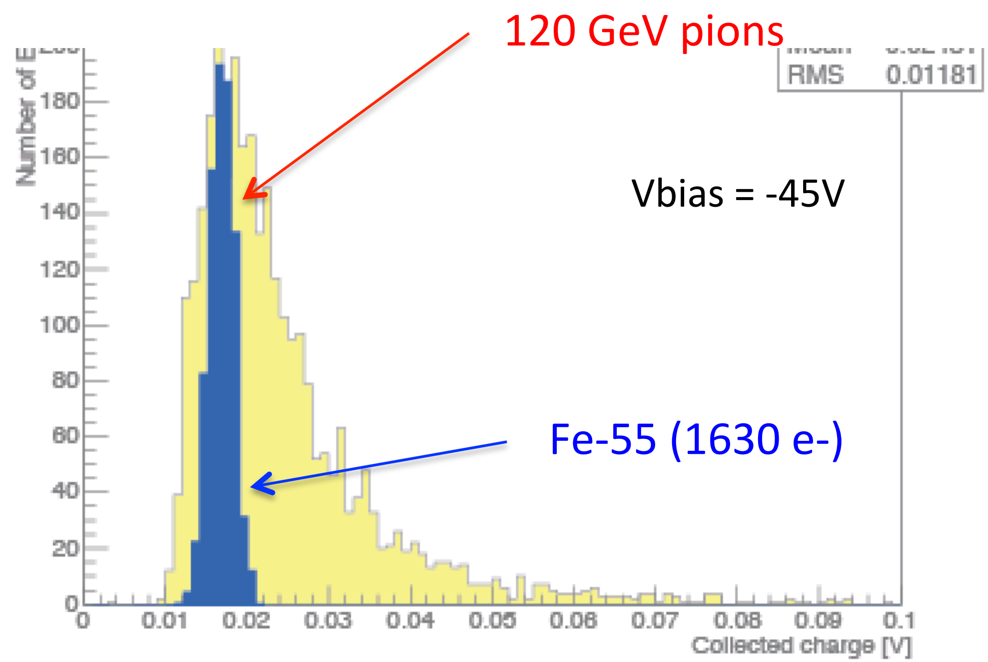


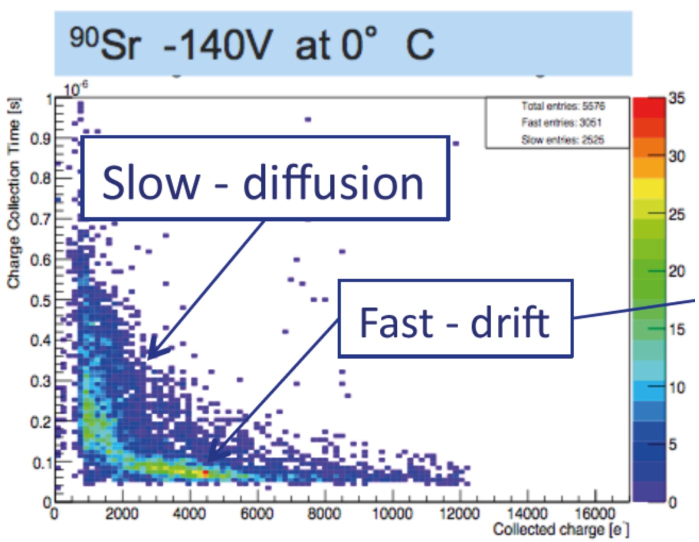
test beam @ 3.2 GeV e⁻

XBT01 in test beam - 50x50µm^2 pixel









Depletion depth ≈ 31µm
Calculated depth = 36µm (@100 Ωcm, -45V)

observation:
charge collected from high-field (fast drift) and low field (slow diffusion) regions

Conclusions

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Semiconductor micro pattern detectors are essential for particle tracking and imaging and new developments are at the forefront of technological advances

- They are the working horse choice for present and future tracking detectors
- There is a large momentum in R&D and building of new detectors for the LHC upgrade
- R&D profits from modern micro technologies and their rapid progress
- Applications spin off to imaging (synchrotron light, X-ray astronomy, medical ...)

Further Reading

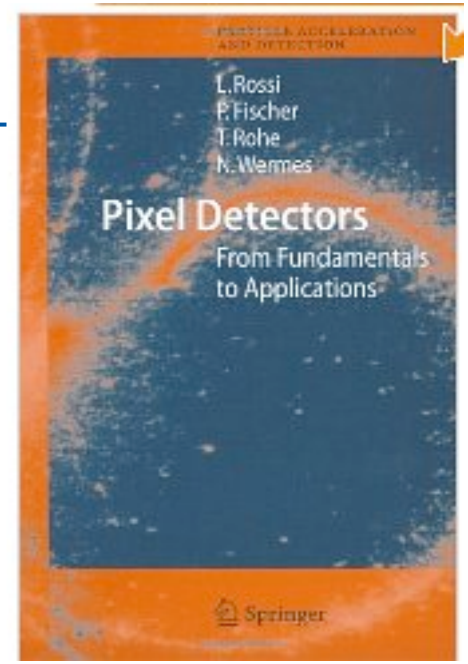
- G. Lutz, "Semiconductor Radiation Detectors",
  Springer Berlin-Heidelberg-New York, 1999.

- Rossi, Fischer, Rohe, Wermes,
  "Pixel Detectors: From Fundamentals to Applications",
  Springer Berlin-Heidelberg-New York, 2006, (ISBN 3-540-283324)

- ATLAS Inner Detector, Aad, G. et al. JINST 3 (2008), P07007.
  CMS Silicon Detector, JINST 3 (2008), S08004,
  ALICE ITS, JINST 3 (2008), S08002.

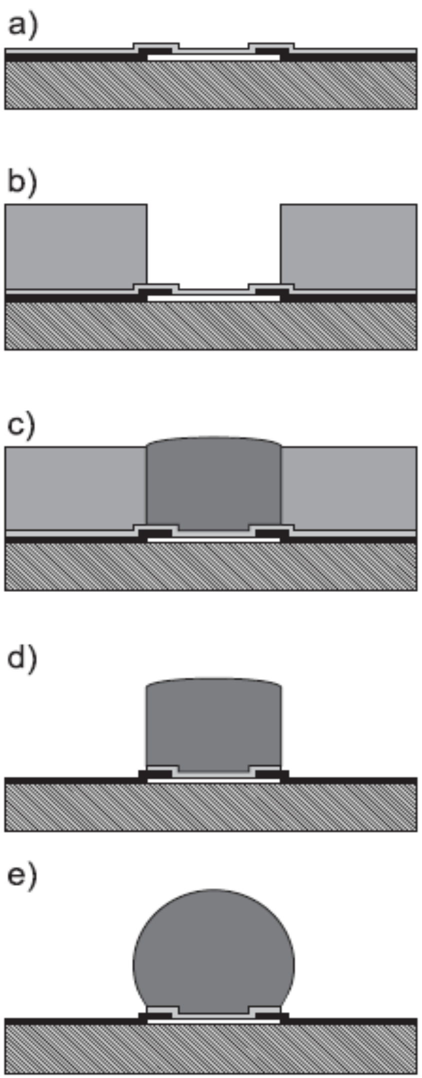
- review pixel papers
  - N. Wermes, "From Hybrid to CMOS Pixels ... a possibility for LHC's pixel future?"
    arXiv:1509.09052 [physics.ins-det], subm. to JINST (2015)
  - N. Wermes, "Pixel Detectors for Charged Particles"
    Nucl.Instrum.Meth. A604 (2009) 370-379, arxiv:physics/0811.4577

- Kolanoski, H. and Wermes, N.
  Particle Detectors – Fundamentals and Applications, Springer (2016)
  in print, English Edition to follow.



Backup

Solder bumping & flip chip process



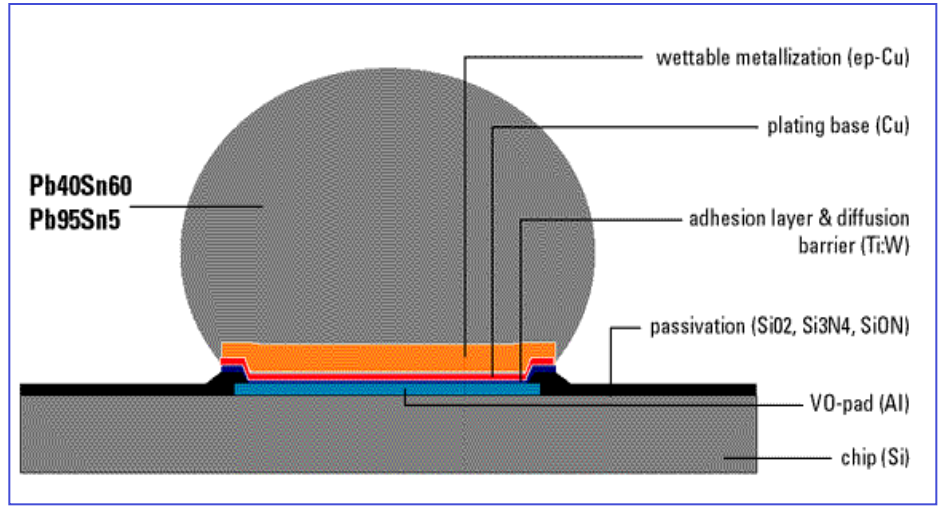
a) Sputter etching and sputtering of the plating base / UBM

b) Spin coating and printing of Photoresist

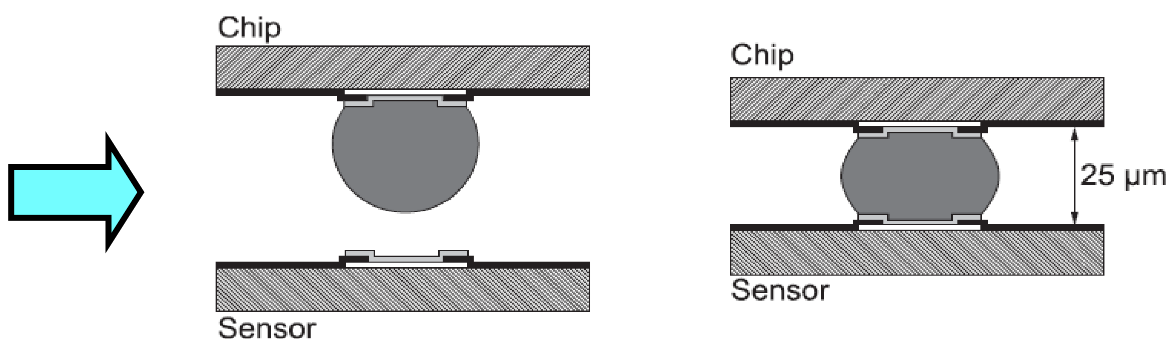
c) Electroplating of Cu and PbSn

d) Resist stripping and wet etching of the plating base

e) Reflow

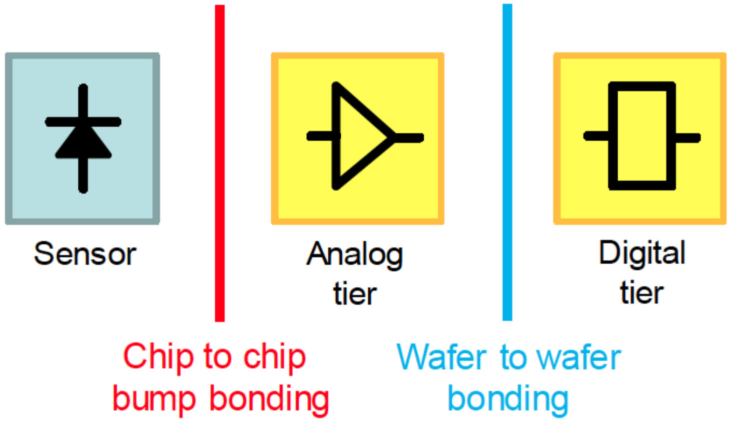


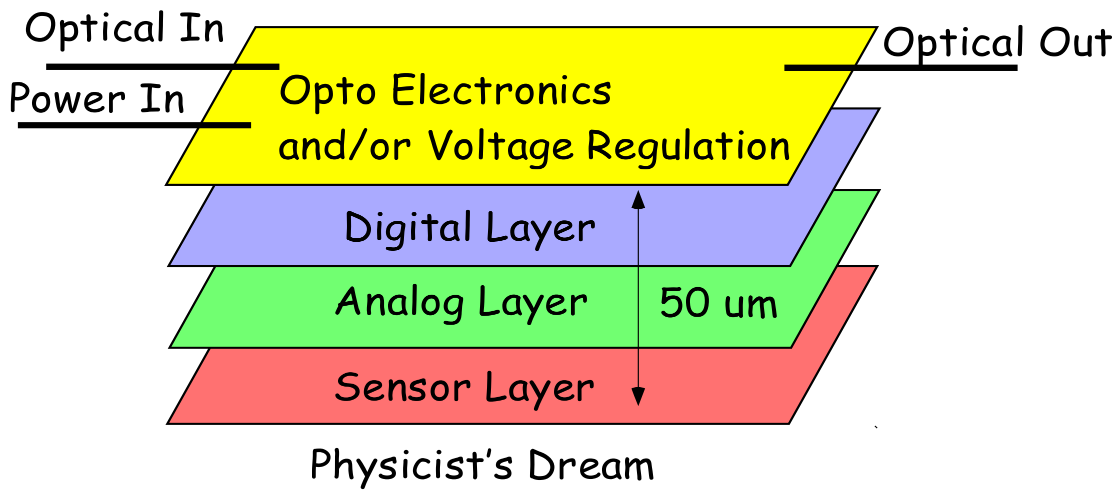
Flip-Chip

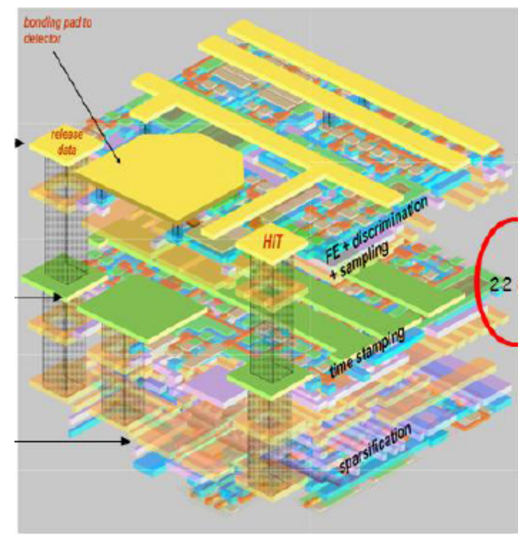


3D integration …

… various CMOS layers







3D integration promises

- higher granularity (smaller pixel size)
- lower power
- large active over total area ratio
- dedicated technology for each functional layer
- but: complex fabrication → yield is an issue