VHDL COUNTER

Implement an up/down counter using a spartan3A/3AN board. The counter must have a LOAD, UP, DOWN and RESET signals mapped on the board according to Figure 1.

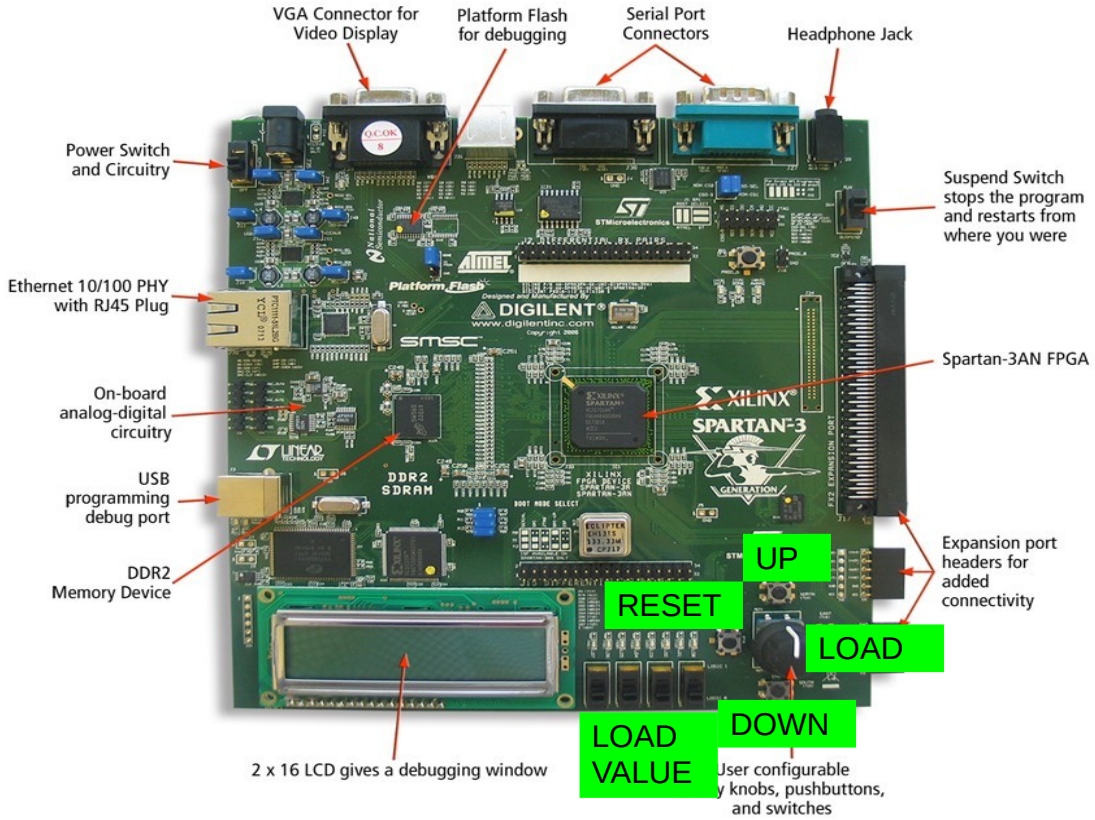

Figure 1: Board signal map

Design the counter according to the block diagram shown in fig. 2 and 3. The blocks **Top_Count**, **debouce** and **pulse_gen**, together with the **UCF** file are already contained in the **contatore_edit** project. **Freq_divider** and **counter** must be designed according to the following requirements:

freq_divider: must implement a 16 bits division, while **counter** must have asynchronous reset and up/down/load features.

Suggestion for behavioral simulation: decrease the **freq_divider** value (for example use 2^4 in such a way you can check the counter functionality in the default time window display).

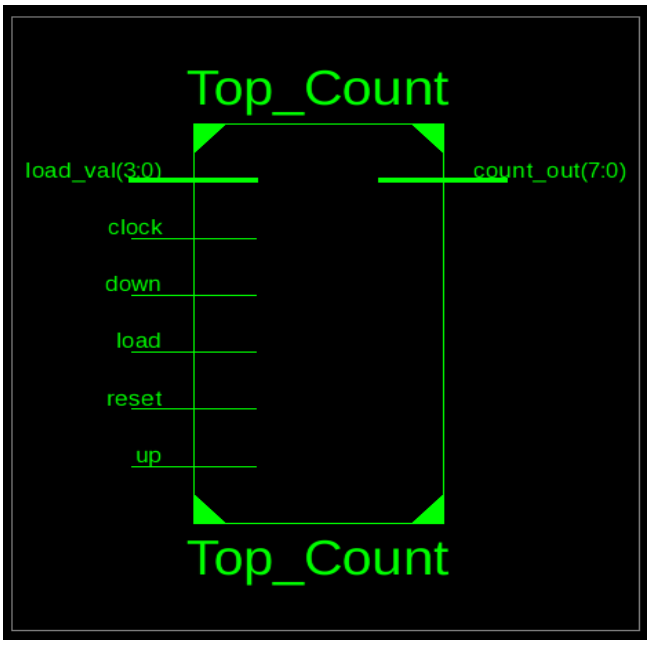

Figure 2: Top_Count block diagram (the I/O signals are mapped in the ucf file)

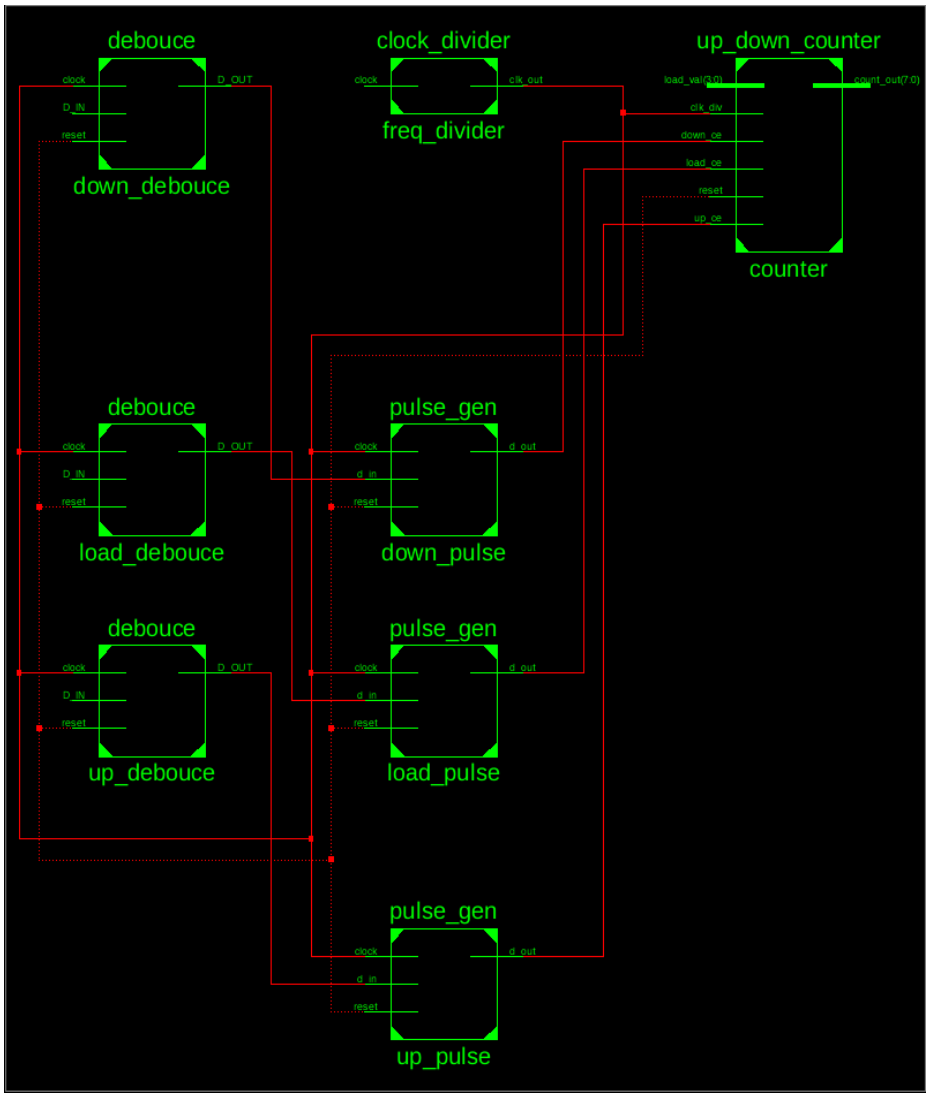

Figure 3: Top_Counter internal block diagram