## XILINX ISE AND SPARTAN 3AN TUTORIAL

## SYNTETIZE AND SIMULATION------

This tutorial will show you how to create a simple Xilinx ISE project based on the Spartan-3 Board. It will be implemented a simple decoder circuit that uses the switches on the board as inputs and the eight LEDs as outputs. There are several parts in this tutorial. Part I shows the basics of creating a simulating a project in Xilinx ISE. Part 2 shows how to generate the bit file that will be used to program the SPARTAN 3AN/3A BOARD FPGA internal memory. Part 3 shows how to program the board.

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Select File → New Project

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New Project	Wizard	
Create New Pro	ect	
Specify project location	and type.	
Enter a name, locati	ons, and comment for the project	
Name:	decoder	
Location:	C:\Users\felici\Desktop\XILINX-EDIT\decoder	
Working Directory:	C:\Users\felici\Desktop\XILINX-EDIT\decoder	
Description:		
Select the type of to	p-level source for the project	
Top-level source typ	e:	
HDL		•
More Info		Next Cancel

Select a project location and name. For this tutorial we will name the project "decoder".

Click Next and select the Spartan 3AN Starter Kit (or the Spartan 3A Kit)in the Evaluation Development Board category (check Preferred Language field: must be VHDL).

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secify device and project properties. elect the device and design flow for the pr	roject	
Property Name	Value	
Evaluation Development Board	Spartan-3AN Starter Kit	
Product Category	All	
Family	Spartan3A and Spartan3AN	
Device	XC3S700AN	
Package	FGG484	
Speed	-4	
Top-Level Source Type	HDL	
Synthesis Tool	XST (VHDL/Verilog)	-
Simulator	ISim (VHDL/Verilog)	
Preferred Language	VHDL	
Property Specification in Project File	Store all values	
Manual Compile Order		
VHDL Source Analysis Standard	VHDL-93	

Click Next and Finish. Right-click and select New Source.

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Select VHDL Module and assign "decoder" name.

New Source Wizard		×
Select Source Type Select Source Type, file name and its location. C UP (CORE Generator & Architecture Wizard) Schematic User Document Verilog Test Fixture VHDL Library P VHDL Library P VHDL Package VHDL Test Bench Embedded Processor	File name: decoder  Location: C:\Users\felici\Desktop\XILINX-EDIT\decoder Z:\Users\felici\Desktop\XILINX-EDIT\decoder	
More Info	Next Ca	ncel

You can now specify the inputs and outputs for the decoder. These will be inserted into an automatically generated template of the VHDL file. We have one 3-bit input ("sel") and one 8- bit output ("y"):

Define Module						
Specify ports for module.						
Entity name decoder						
Architecture name Behavioral						
Port Name	Direction	n	Bus	MSB	LSB	
sel	in	-	V	2	0	
У	out	-	V	7	0	
	in	-				
	in	•				
	in	•				
	in	•				
	in	-				
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Click Next. A summary window will be shown.

6	) Ne	ew Source W	ïzard				
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	Entity name: Architecture Port Definitio	decoder name: Behav	ioral				
		sel	Bus:	2:0	in		
		у	DUS:	7.0	our		
		)					
	More Info	J				Finish	Cancel

Click Finish and decoder.vhd will be shown in the top-left sources and on the window editor.

You are required to describe the behavior of the decoder using statements in the architecture body. In this example we will use conditional signal assignment statements; insert the code between **begin** and **end**.

```
25 --use IEEE.NUMERIC STD.ALL;
26
   -- Uncomment the following library declaration if instantiating
27
    -- any Xilinx primitives in this code.
28
   --library UNISIM;
29
30 --use UNISIM.VComponents.all;
31
   entity decoder is
32
33
       Port ( sel : in STD_LOGIC_VECTOR (2 downto 0);
              y : out STD LOGIC VECTOR (7 downto 0));
34
35 end decoder;
36
37
    architecture Behavioral of decoder is
38
39 begin
40
       y <= "00000001" when sel = "000" else</pre>
41
             "00000010" when sel = "001" else
42
             "00000100" when sel = "010" else
43
             "00001000" when sel = "011" else
44
             "00010000" when sel = "100" else
45
             "00100000" when sel = "101" else
46
             "01000000" when sel = "110" else
47
             "10000000";
48
49
50 end Behavioral:
51
E 0
```

## Select again New Source



Select VHDL Test Bench and assign the name decoder\_tb.

Selecting Next the "Associate Source" panel will be shown. Click Next and Finish. The "decoder\_tb.vhd" is shown in the editor panel.



Look at the file produced. Insert the instructions after the comment -- insert stimulus here.

```
76
 77
78
       -- Stimulus process
       stim_proc: process
79
80
      begin
         -- hold reset state for 100 ns.
81
          wait for 100 ns;
82
         -- insert stimulus here
83
84
          wait for clk period*5;
         sel <= "000"
85
         wait for clk_period*5;
86
87
         sel <= "001"
88
         wait for clk period*5;
89
         sel <= "010"
         wait for clk_period*5;
90
91
         sel <= "100"
         wait for clk_period*5;
sel <= "101"</pre>
92
93
94
         wait for clk_period*5;
          sel <= "110"
95
         wait for clk_period*5;
96
         sel <= "111"
97
98
99
100
         wait;
101
      end process;
100
```

Modify also the clk sections of code as shown

```
--Inputs
signal sel : std_logic_vector(2 downto 0) := (others => '0');
--Outputs
signal y : std_logic_vector(7 downto 0);
-- No clocks detected in port list. Replace <clock> below with
-- appropriate port name
constant clk period : time := 10 ns;
signal clk: std_logic;
           BEGIN
              -- Instantiate the Unit Under Test (UUT)
              uut: decoder PORT MAP (
                     sel => sel,
                     у => у
                   );
                -- Clock process definitions
              clk_process :process
              begin
                 clk <= '0';
                 wait for clk_period/2;
                 clk <= '1';
                 wait for clk_period/2;
              end process;
```

or remove all the **clk** sections and change the "wait for clk\_period\*5;" to "wait for 50 ns".

Check that Implementation is selected in the Project Manager View panel that and double-click Syntetize-XST.

ISE Project Navigator (P.20131013) - C:\Users\fe	elici\D	esktop\XILINX-EDIT-21\decoder\decoder.xise - [D	esign Summary (Syn	thesized	d)]				e ex	-
E File Edit View Project Source Proces	ss Tr	ools Window Layout Help							- 8	×
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🕮 🖨 🖾 xc3s700an-4fgg484	(5	Pinout Report	Target Device:	xc3s700	an-4fgg484	• E	Errors:	No Er	rors	
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Select **Simulate** in the **Project Manager View**. Some errors will be shown in the console. Correct them (add semicolon after **sel** statement) and save the project. The errors should disappear.

ISE Project Navigator (P.20131013) - C:\Users\fe	ici\Desktop\XILINX-EDIT-21\decoder\decoder.xise - [decoder_tb.vhd*]	
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Vew:	<pre>77 77 79 stim_process 79 stim_proc: process 80 begin 81 hold reset state for 100 ns. 82 wait for 100 ns; 83 insert stimulus here 84 wait for clk_period*5; 85 sel &lt;= "000" 86 wait for clk_period*5; 87 sel &lt;= "001" 88 wait for clk_period*5; 99 wait for clk_period*5; 90 wait for clk_period*5; 91 sel &lt;= "100" 92 wait for clk_period*5; 93 sel &lt;= "101" 94 wait for clk_period*5; 95 sel &lt;= "111" 95 sel &lt;= "111" 96 wait; 101 end process; 102 103 END;</pre>	×
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	3 30 begin	
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□□ □ III xc3s/00an-4fgg484	= 83 insert stimulus nere	
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	A set to out, and set of the set	
62	87 sel <= "010":	
	88 Wait for clk period*5:	
-	34 89 sel <= "010";	
ш.	30 wait for clk period*5;	
۰ III +	91 sel <= "100";	
	92 wait for clk_period*5;	
Rev Controcesses Running	93 sel <= "101";	
No single design module is selected.	94 wait for clk_period*5;	
🖭 🙃 🐲 Design Utilities	95 sel <= "110";	
×4	96 Walt for city period s;	
	97 set <= "111";	
	98	
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	103 END;	
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Select "decoder\_tb" in the hierarchy window and expand ISim Simulator



Double-click Simulate Behavioral Model.



Simulation window will show the result of simulation.

			78.392 ns		234, 171	ns					
		10		1200				1400			
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PROJECT IMPLEMENTATION-----

Again select New Source

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select **Implementation Constraint Files** (you will have to check the Spartan 3AN specifications to find out UCF constraints for **slide switches** and **leds**) and assign the name "decoder\_ucf" to the file, click next

New Source Wizard Select Source type, fle name and its location. BMM File CoRE Generator & Architecture Wizard) MEM File Schematic User Document Werlog Test Fixture VHDL Library VHDL Package WHDL Library Embedded Processor	File name: decoder_ucf_ Location: C:\Users\felki\Desktop\VILINX-EDIT-21\decoder
More Info	Next Cancel

A summary window shows up, click finish.



Now we have to map our signals to the board input/output. From the board user guide



we get the map of the UCF constraint file for the Slide Switches and leds.

NET	"SW<0>"	LOC =	"V8"	<b>IOSTANDARD</b> = LVCMOS33	;
NET	"SW<1>"	LOC =	"U10"	<b>IOSTANDARD</b> = LVCMOS33	;
NET	"SW<2>"	LOC =	"U8"	<b>IOSTANDARD</b> = LVCMOS33	;
NET	"SW<3>"	LOC =	"Т9"	<b>IOSTANDARD</b> = LVCMOS33	;

Figure 2-2: UCF Constraints for Slide Switches



Figure 2-12: Eight Discrete LEDs

NET	"LED<7>"	LOC =	"W21"	IOSTANDARD	= LVCMOS33	SLEW = SLOW	DRIVE = 8 ;
NET	"LED<6>"	LOC =	"Y22"	IOSTANDARD	= LVCMOS33	SLEW = SLOW	DRIVE = 8 ;
NET	"LED<5>"	LOC =	"V20"	IOSTANDARD	= LVCMOS33	SLEW = SLOW	DRIVE = 8 ;
NET	"LED<4>"	LOC =	"V19"	IOSTANDARD	= LVCMOS33	SLEW = SLOW	DRIVE = 8 ;
NET	"LED<3>"	LOC =	"U19"	IOSTANDARD	= LVCMOS33	SLEW = SLOW	DRIVE = 8 ;
NET	"LED<2>"	LOC =	"U20"	IOSTANDARD	= LVCMOS33	SLEW = SLOW	DRIVE = 8 ;
NET	"LED<1>"	LOC =	"T19"	IOSTANDARD	= LVCMOS33	SLEW = SLOW	DRIVE = 8 ;
NET	"LED<0>"	LOC =	"R20"	IOSTANDARD	= LVCMOS33	SLEW = SLOW	DRIVE = 8 ;

Figure 2-13: UCF Constraints for Eight Discrete LEDs

Add our constraint file assigning the nets of our project

```
NET "sel<0>" LOC = "V8" | IOSTANDARD = LVCMOS33 ;

NET "sel<1>" LOC = "U10" | IOSTANDARD = LVCMOS33 ;

NET "sel<2>" LOC = "U8" | IOSTANDARD = LVCMOS33 ;

NET "sel<2>" LOC = "U8" | IOSTANDARD = LVCMOS33 ;

NET "_{9}<1>CC = "_{2}2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{6}<6>" LOC = "_{2}2" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{2}0" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{2}0" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{2}0" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{2}0" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{2}0" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{2}0" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{1}19" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{1}19" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{1}19" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{1}19" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{1}19" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{1}19" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;

NET "_{2}<5>" LOC = "_{1}19" | IOSTANDARD = LVCMOS33 | SLEW = SLOW | DRIVE = 8 ;
```

Now we're ready to implement our project. Double-click generate programming file



ISE Project Navigator (P.20131013) - C:\Users\fe	s/felici\Desktop\XILINX-EDIT-21\decoder\decoder.xise - [decoder_ucf.ucf]	- • ×	
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Design ↔ □ & ×			
View:  Vi	<pre>3 NET "sel&lt;1&gt;" LOC = "VO"   IOSIANDARD = LVCMOS33; 3 NET "sel&lt;1&gt;" LOC = "U10"   IOSIANDARD = LVCMOS33;</pre>		
decoder	4 NET "sel<2>" LOC = "US"   IOSTANDARD = LVCMOS33 ;		
- Carter and the second	6 NET "y<7>" LOC = "W21"   IOSTANDARD = LVCMOS33   SLEW = SLOW   DRIVE = 7 NET "6<6>" LOC = "Y22"   IOSTANDARD = LVCMOS33   SLEW = SLOW   DRIVE =	8; 8;	
decoder_ucf.ucf	8 NET "Y<5>" LOC = "V20"   IOSTANDARD = LVCMOS33   SLEW = SLOW   DRIVE =	8 ;	
a	<pre>4 10 NET "y&lt;3&gt;" LOC = "U19"   IOSTANDARD = LVCMOS33   SLEW = SLOW   DRIVE =</pre>	8;	
	11 NET "Y<2>" LOC = "U2O"   IOSTANDARD = LVCMOS33   SLEW = SLOW   DRIVE = 12 NET "Y<1>" LOC = "T19"   IOSTANDARD = LVCMOS33   SLEW = SLOW   DRIVE =	8;	
□ □	13 NET "y<0>" LOC = "R20"   IOSTANDARD = LVCMOS33   SLEW = SLOW   DRIVE =	8 ;	
<→	15		
No Processes Running			
Processes: decoder - Behavioral			
Design Utilities			
Synthesize - XST			
Entropy Content Design     Generate Programming File			
Configure Target Device     Analyze Design Using ChipScope			
		4	
- Start Cosign C Files Libraries	ies 👔 Design Summary (Programming File Generated) 🔝 📋 decoder_tb.vhd 🗵 📋 decoder_ucf.ucf 🗵 🗎 decoder	.vhd ⊠	
Console		⇔⊡₽×	
Frocess "Generate Post-Place & 1	Route Static Timing" completed successfully	<b>^</b>	
Started : "Generate Programming	ng File".		
Command Line: bitgen -intstyle ise -f decoder.ut decoder.ncd			
Process "Generate Programming File" completed successfully			
· ·			
📋 Console 😣 Errors 🔬 Warnings 😿 I	Find in Files Results		
		Ln 15 Col 1 UCF	

## PROGRAM THE DEVICE------

Double-click Configure Target Device



A warning window appear. Click **OK** 



The **Impact** window shows up. Double-click **Boundary Scan** to detect connected devices and then initialize the chain.

SE IMPACT (P.20131013)	×
File Edit View Operations Output Debug Window Help	
MPACT Flows ++ D 8 ×	
Boundary Scan     BystemACE     Create PROM File (PROM File Format     WebTalk Data	
MPACT Processes ↔ □ ♂ ×	
Console	⇔⊡₽×
4 m	* *
Console Console Verors 1 Warnings	

ISE iMPACT (P.20131013) - [Boundary Scan]		A COMPANY AND A COMPANY	
🐼 File Edit View Operations Output	Debug Window	Help	_ <i>8</i> ×
🗋 🏓 🖥 🔓 🖀 🗯 🔁 🗖 .	₽ №?		
IMPACT Flows ↔ □ 중 ×			
Boundary Scan       SystemACE       Craste RPOM File (PROM File Format       Craste RPOM File Verbalk Data			
		Right click to Add Devi	ce or Initialize JTAG chain
IMPACT Processes ↔ □ ₽ ×			
Avaliable Operations are:			
		Boundary Scan	
Console			+□♂×
Console 🙆 Errors 🔥 Warnings			F
			No Cable Connection No File Open

Two components are detected. The FPGA and The EEPROM. Click Yes to assign the files.

SE iMPACT (P.20131013) - [Boundary Scan]		
😵 File Edit View Operations Output I	Debug Window Help	_ <i>6</i> ×
🗋 🌶 🖶 🔓 🗄 🖼 🖼 🌾 🗖	<i>₽</i> №?	
MPACT Flows     ↔ ☐ ♂ ×       Image: Soundary Scan     Image: Soundary Scan       Image: Soundary Scan     Image: Soundary Scan <td>TDI     Enume     Enume       xc3s700a     xc104s       bypass     bypass</td> <td>Auto Assign Configuration Files Query Dialog</td>	TDI     Enume     Enume       xc3s700a     xc104s       bypass     bypass	Auto Assign Configuration Files Query Dialog
Available Operations are:		Don't show this message again, save the setting in preference.
	Boundary Scan	
Console		+□5×
done. PROGRESS_END - End Operation. Elapsed time = 0 sec.		۰ ۲
Console Console Warnings		,, , ,, , ,, , ,, , ,, , ,, , ,, , ,, , , , , , , , , , , , , , , , , , , ,

The FPGA is firstly selected together with a browser. Select the "decoder.bit" file and click **Open**.

SE IMPACT (P.20131013) - [Boundary Scan]			
😵 File Edit View Operations Output D	ebug \	Window Help	_ 8 ×
🗋 🆻 🛃 🕺 🗅 🔓 🗙 🗄 🖽 🖼		<b>□</b> <i>P R</i>	
MPACT Flows ↔ □ 8 ×			
Boundary Scan     SystemACE     Create PROM File (PROM File Format     WebTalk Data	TDI —	2012991 201400	
		xc3s700a xcf04s	
	TDO	bihasa pihasa	
		Assign New Configuration File	? <u>×</u>
		Look in: Look in: C: Users \felici \Desktop \XILINX-EDIT-21\decoder	o 📑 🖽 🗉
MPACT Processes ↔ ☐ ♂ × Available Operations are:	*	Image: Stress of the stress	Open Cancel
Console		Files of type: All Design Files (*, bit *, rbt *, nky *, isc *, hsd)	■ Bypass
done. PROGRESS_END - End Operation. Elapsed time = 0 sec.			Cancel All
<			
Console C Errors 🔬 Warnings		Configuration Disform Cabl	LICP 6 MHz ush he
l		Configuration Platform Cable	USD-NS

Click **No** in the next window and then **Bypass** (note that the decoder.bit file has been assigned to the FPGA)

SE iMPACT (P.20131013) - [Boundary Scan]		
😵 File Edit View Operations Output	Debug Window Help	- 8 ×
🗋 ờ 🛃 📫 🛗 🖽 🖄 🌐 🔚 🗖	1 P 12	
MPACT Flows ↔ □	Right click device to select operations	
Boundary Scan     SystemACE     Greete PROM File (PROM File Format     WebTalk Data		
	xc3s700a xcf04s decoder.bit bypass	
	Attach SPI or BPI PROM	
PPPALI Processes     Image: Constructions are:       Get Device ID     Get Device ID       Get Device Signature/Usercode       Read Device Status	This device supports attached Flash PROMs. Do you want to attach an SPI or BPI PROM to this device? Yes No	
	Identify Succeeded	
	Correction of the second secon	
Console	Davice vc3e700a encceeefulu	⇔⊡e™×
<pre></pre>		
Console S Errors 🔥 Warnings		
	Configuration Platform Cable USB 6 M	Hz usb-hs

A summary window appear. Click **OK**.

Finally we have to download the .bit file in the FPGA. Right-click the FPGA and select Program

SE iMPACT (P.20131013) - [Boundary Scan]		
🛞 File Edit View Operations Output Deb	bug Window Help	- 8 ×
🗋 🏓 🛃   🐰 🗈 🖺 🗙 🗄 🖬 🗰 💥 :	티 않는 🔁 🗇 🤌 📢	
MPACT Flows ↔ □ & ×		
Boundary Scan         SystemACE         Create PROM File (PROM File Format         Create PROM File (PROM File Format         WebTalk Data         T         MPACT Processes         ↔ □ ₽ ×         Available Operations are:	TDI Program Get Device IID TDO TDO TDO TDO TDO TDO TDO TDO TDO TD	
	Boundary Scan	
Console		+ □ & ×
<pre>③ INFO:iMPACT:501 - '1': Added Devi</pre>	ice xc3s700a successfully.	A
		*
		•
Console V Errors A warnings	Cor	nfiguration Platform Cable USB 6 MHz usb-hs

A confirm window shows-up. Congratulation, you've programmed your first FPGA.