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FPGAs
A short introduction

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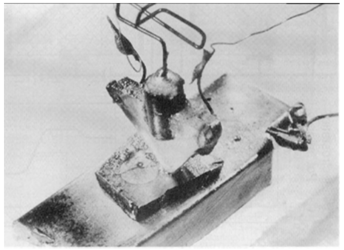
LNF-INFN

EVOLUTION OF INTEGRATED CIRCUITS

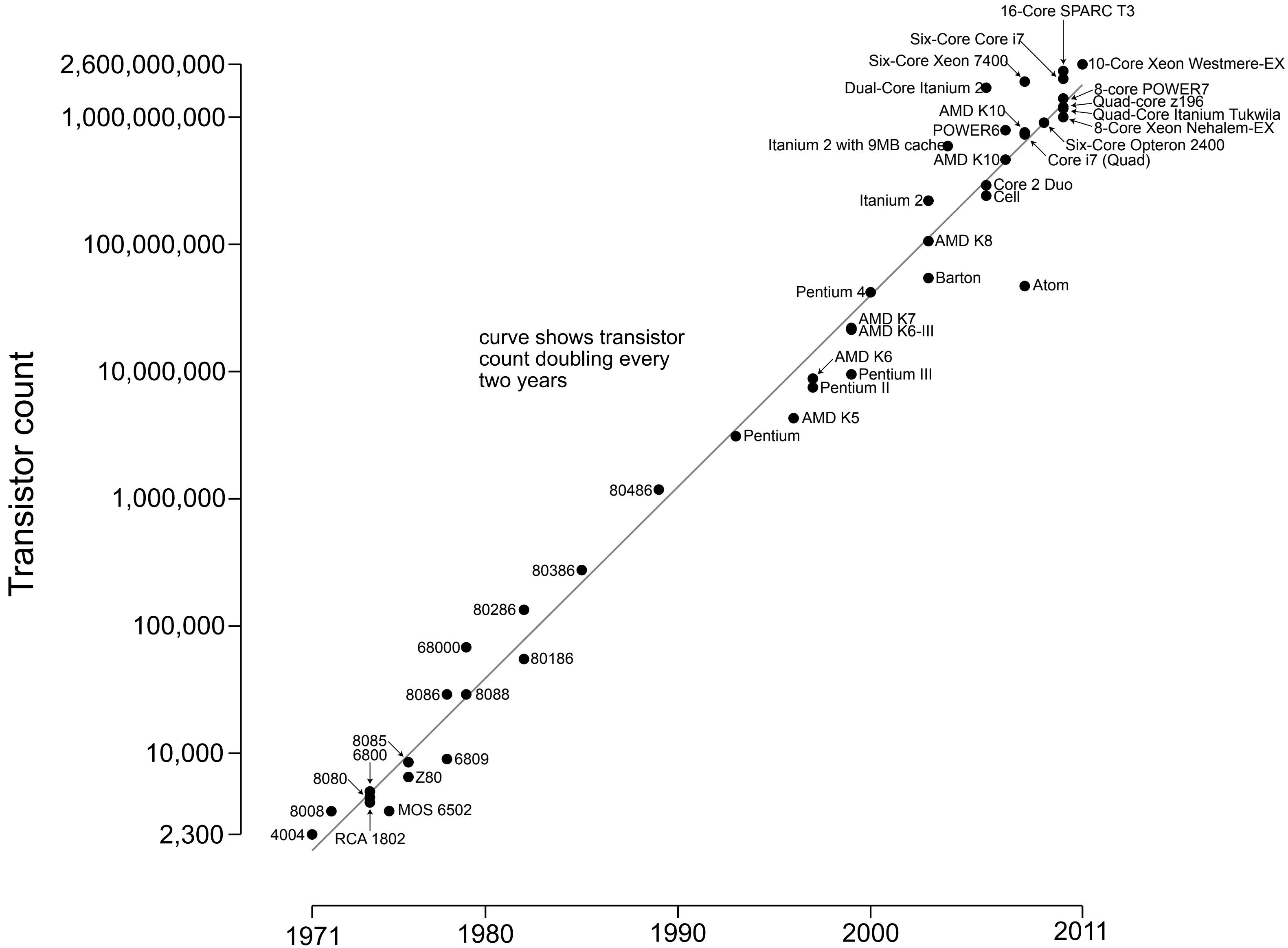
- 1948: invention of transistors (Bell Labs)



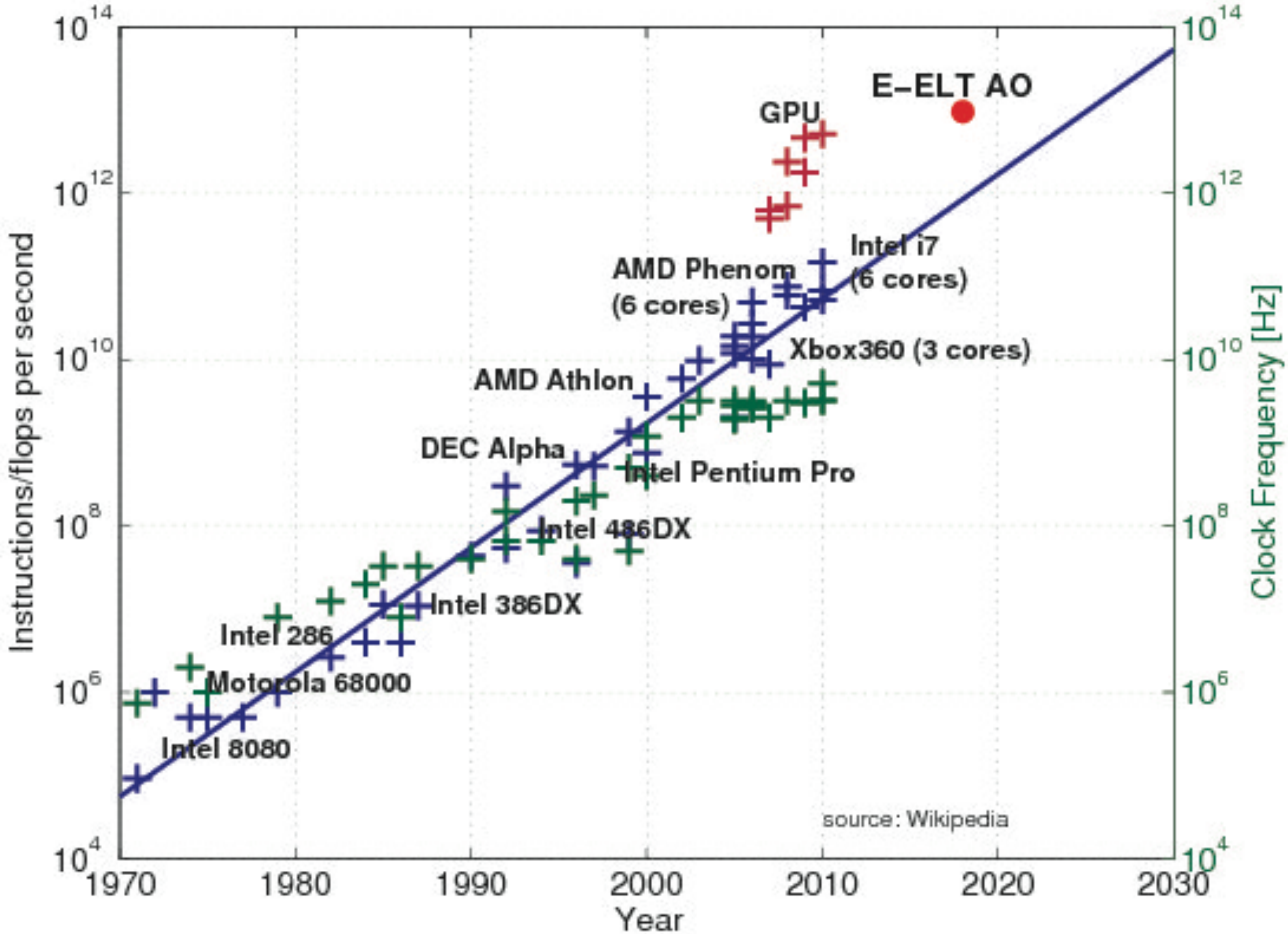
Source Bell Labs

- 1958: Invention of Integrated Circuits
  - The idea of making a whole circuit-transistors, wires, and everything else-was invented by Jack Kilby at Texas Instruments and Robert Noyce at Fairchild Semiconductor almost at the same time
- 1965: Moore's Law
  - In 1965, Gordon Moore at Intel made a prediction that semiconductor technology will double its effectiveness every 18 months

MOORE'S LAW


Transistor count
2,600,000,000
1,000,000,000
100,000,000
10,000,000
1,000,000
100,000
10,000
2,300
1971
1980
1990
2000
2011
curve shows transistor count doubling every two years
16-Core SPARC T3
Six-Core Core i7
Six-Core Xeon 7400
10-Core Xeon Westmere-EX
Dual-Core Itanium 2
8-core POWER7
Quad-core z196
Quad-Core Itanium Tukwila
8-Core Xeon Nehalem-EX
AMD K10
POWER6
Six-Core Opteron 2400
Itanium 2 with 9MB cache
AMD K10
Core i7 (Quad)
Core 2 Duo
Cell
Itanium 2
AMD K8
Barton
Atom
Pentium 4
AMD K7
AMD K6-III
AMD K6
Pentium III
Pentium II
AMD K5
Pentium
80486
80386
80286
68000
80186
8086
8088
8085
6800
6809
8080
Z80
8008
MOS 6502
4004
RCA 1802

MICROPROCESSORS CLOCK FREQUENCIES



CLASSIFICATION OF INTEGRATED CIRCUITS

- Microprocessors
- Memory chips (SRAM, DRAM, Flash, ROM, PROM)
- Standard Components (74LS..)
- Application-Specific Integrated Circuits
  - Widely used in communication, network, and multimedia systems
  - For a given application, ASIC solutions are normally more effective than the solutions based on running software on microprocessors
  - Many chips in cellular phones, network routers, and game consoles are ASICs
  - Most SoC (Systems-on-a-Chip) chips are ASICs
  - Programmable devices (PLA/PAL-CPLD-FPGA)

ASIC DESIGN METHODOLOGIES

ASIC DESIGN

Full-custom design

- This approach is extremely slow, expensive
- It is only used to design very high performance systems

Standard-cell based design

- This approach is reasonable fast, less expensive
- Most ASICs are currently designed using this method

Gate-array based design

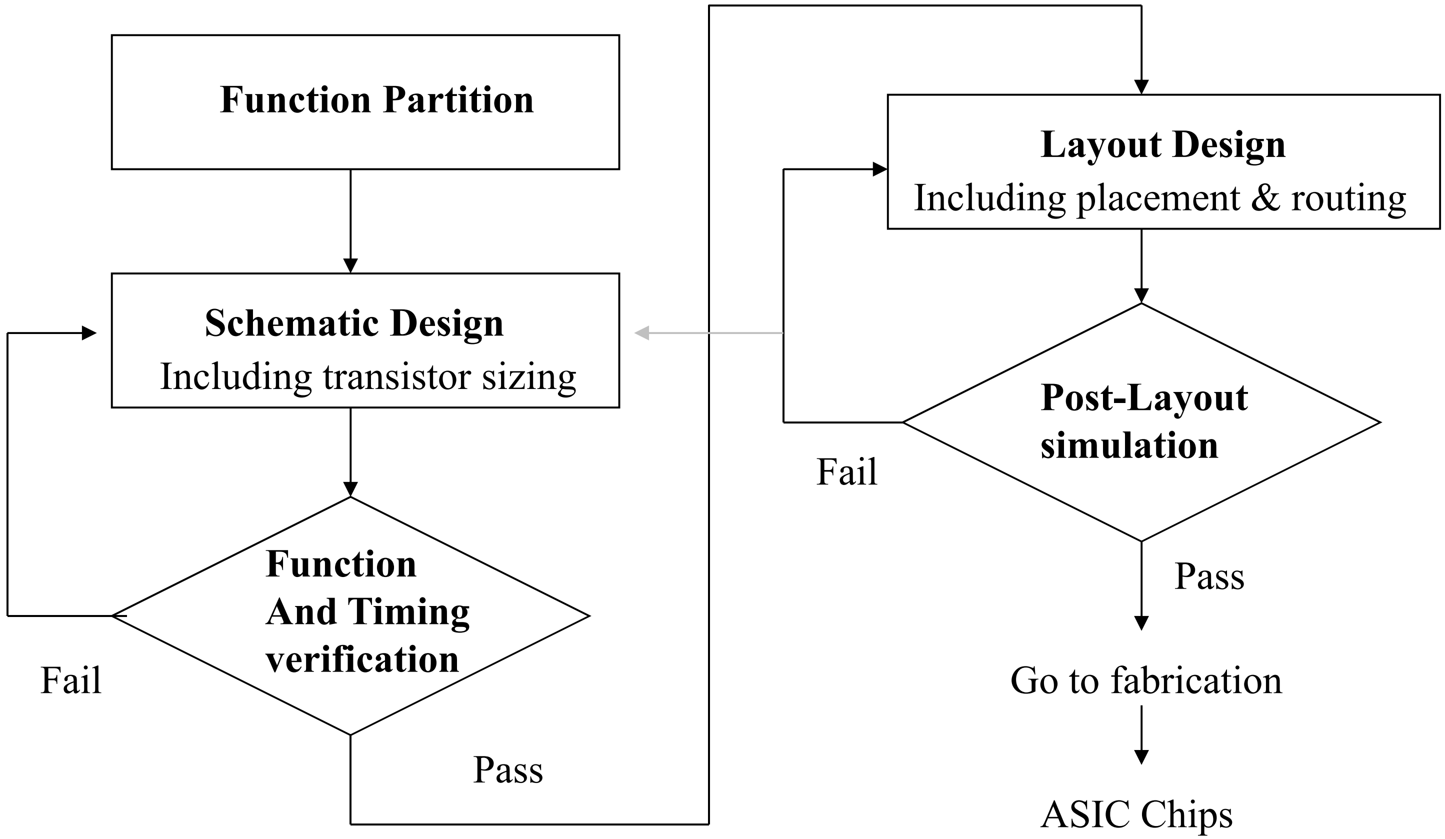
- This approach is fast and less expensive
- ASIC performance are relatively slow

FPGA DESIGN

FPGA based design

- The design process is very fast and cost effective
- ASIC performance are slow

FULL-CUSTOM DESIGN METHODOLOGY



IT IS A TIME CONSUMING MANUAL PROCESS. NO PRE-DEVELOPED LIBRARY ARE REQUIRED

Pros: complete flexibility, high degree of optimization in performance, power consumption and application area

Cons: large amount of design effort, expensive, time to market

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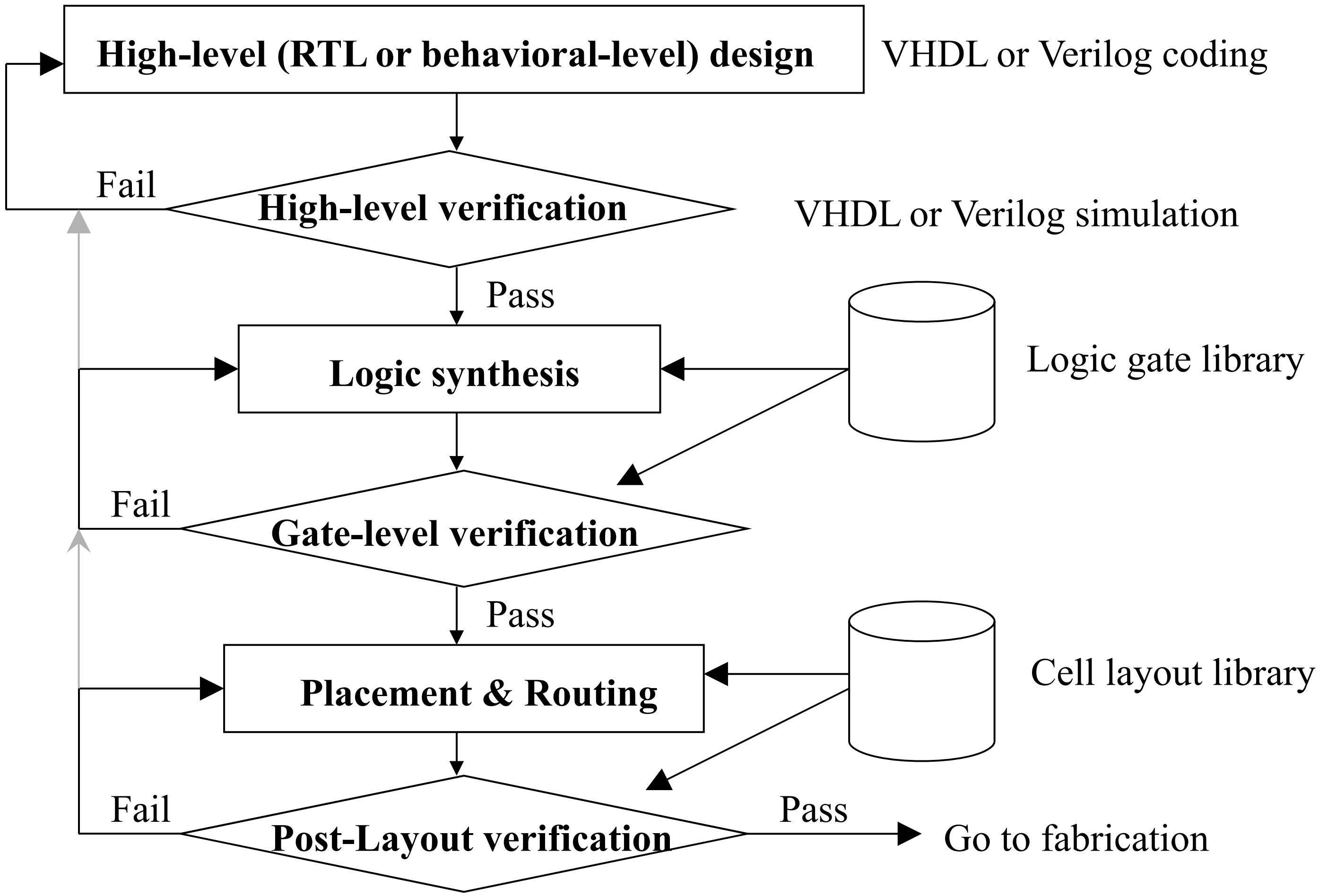
STANDARD-CELL BASED DESIGN METHODOLOGY

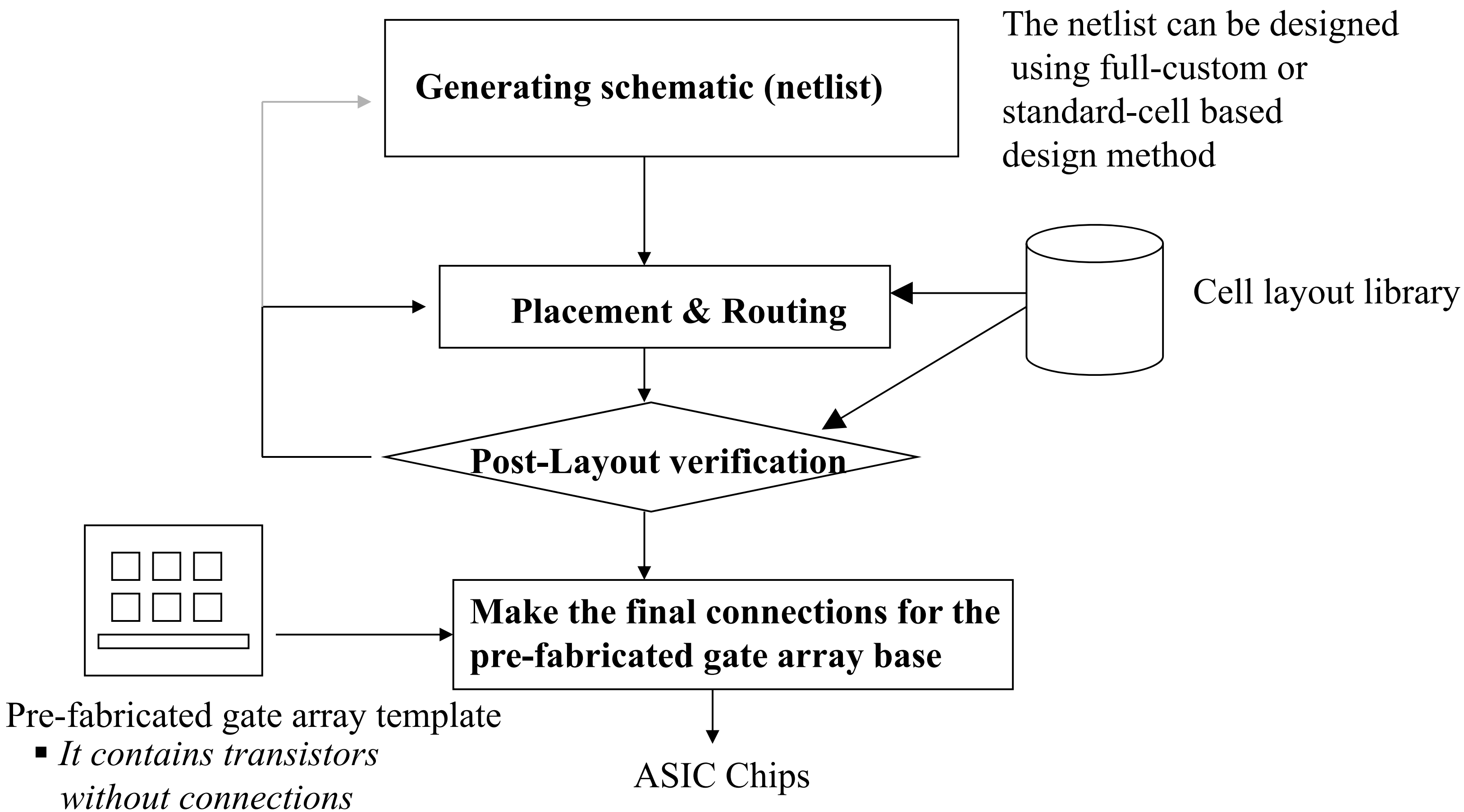


IT IS HIGHLY AUTOMATED. NEED PRE-DEVELOPED LIBRARIES

Pros: save design time and money. Reduce risk compared to a full-custom design

Cons: still incurs high non-recurring-engineering (NRE) cost and long manufacture time

GATE-ARRAY BASED DESIGN METHODOLOGY

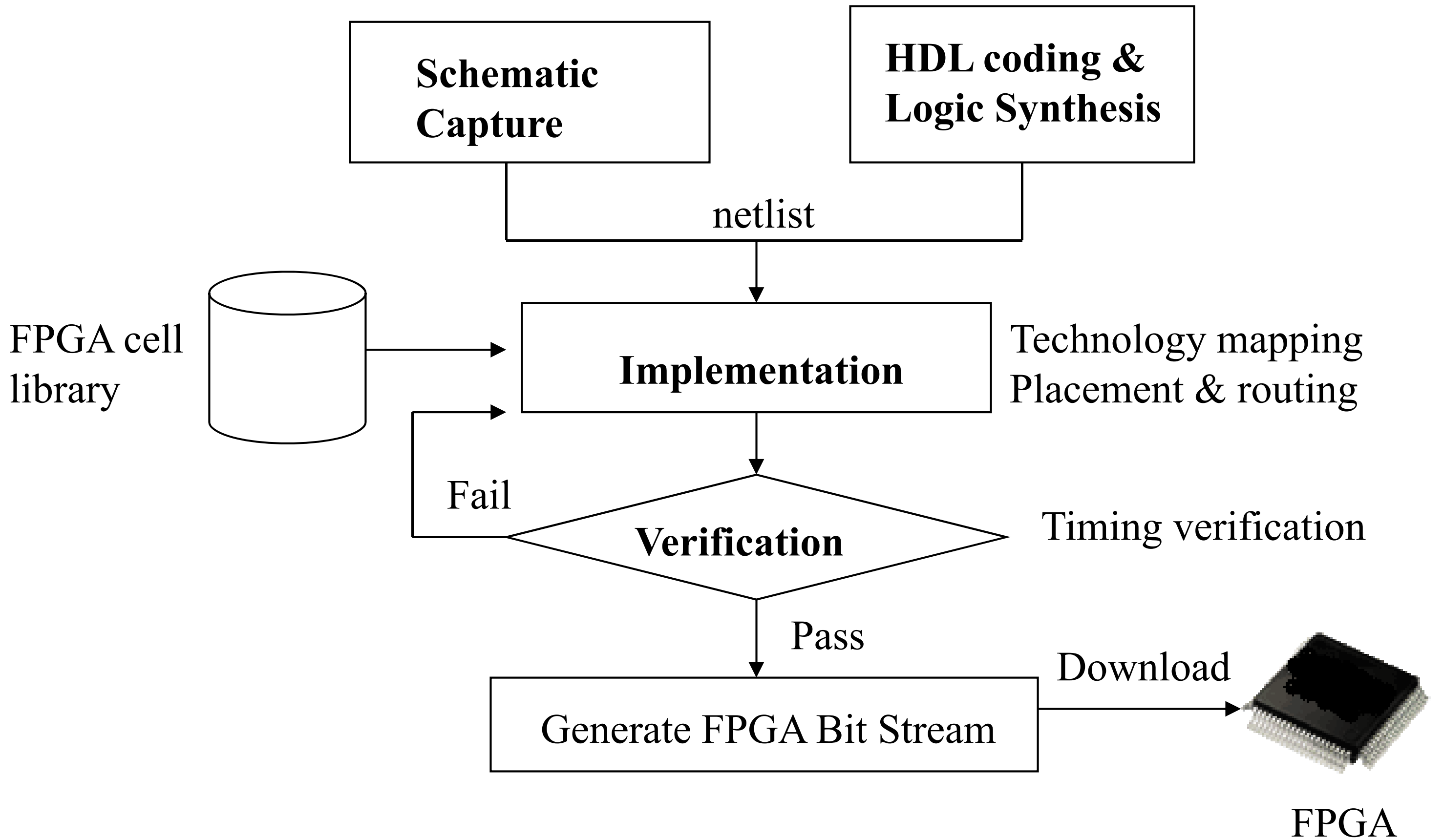


FASTER THAN THE STANDARD-CELLS BASED APPROACH AS PART OF THE FABRICATION PROCESS HAS BEEN DONE

Pros: cost saving (fabrication cost of a large number of identical templates wafers is amortized over different customers), shorter manufacture lead time

Cons: performances not as good as full-custom or standard-cell-based ICs

FPGA BASED DESIGN METHODOLOGY



THIS APPRACH HAS EXTREMELY FAST TURN-OUT TIME SINCE THE FPGA DEVICES HAS BEEN ALREADY FABRICATED

COMPARISON OF DESIGN METODOLOGIES

	Full-custom design	Standard-cell based design	Gate-array based design	FPGA-based design
Speed	+++	++	+	-
Integration density	+++	++	+	--
High-volume device cost	++	++	+	+
low-volume device cost	---	--	+	+++
Custom mask layer	All	All	Some	None
Fabrication time	---	--	-	+++
Time to Market	---	--	++	+++
Risk reduction	---	--	-	+++
Future design modification	---	--	-	+++

+ desirable; - not desirable

FPGA ADVANTAGES AND APPLICATIONS

- FPGAs

  Pros: Fast turn-out time, re-programming capability, dynamic reconfiguration capability

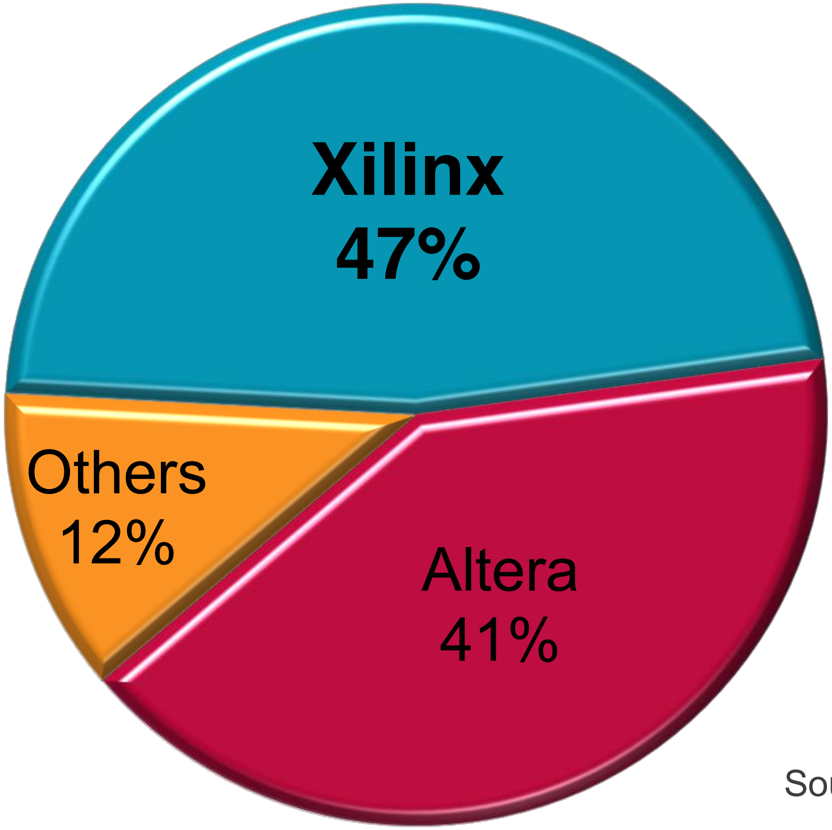
  Cons: performances and integration are not as good as full-custom or standard-cell-based ICs, power consumption

NB: integration issue mitigated by SoC technology (microprocessors + FPGA in the same device)

- FPGA APPLICATIONS
  - Ideal platform for prototyping
  - Providing fast implementation to reduce time-to-market
  - Cost effective solutions for products with small volumes on demand
  - Implementing hardware systems requiring re-programming flexibility
  - Implementing dynamically re-configurable systems

FPGA MARKET

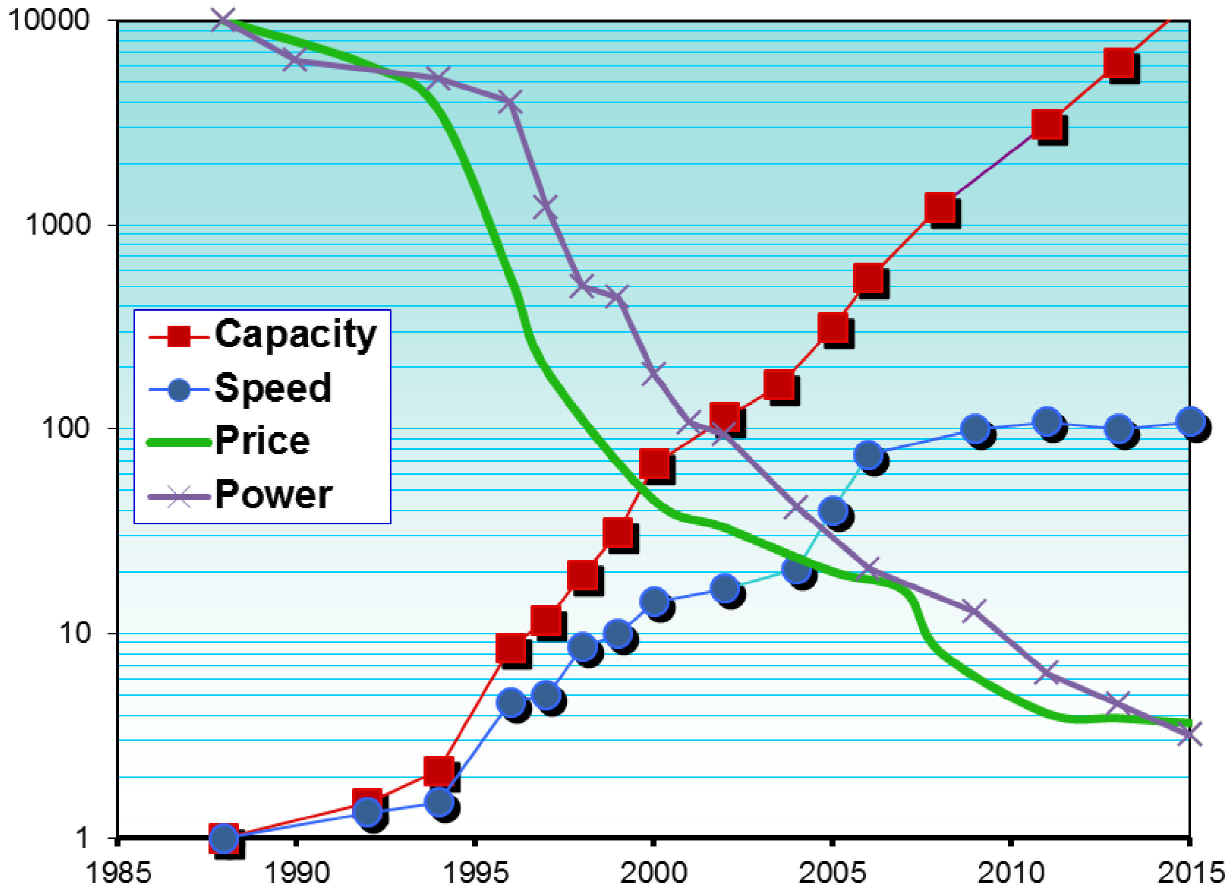
PLD Market Segment Share Calendar Year 2011



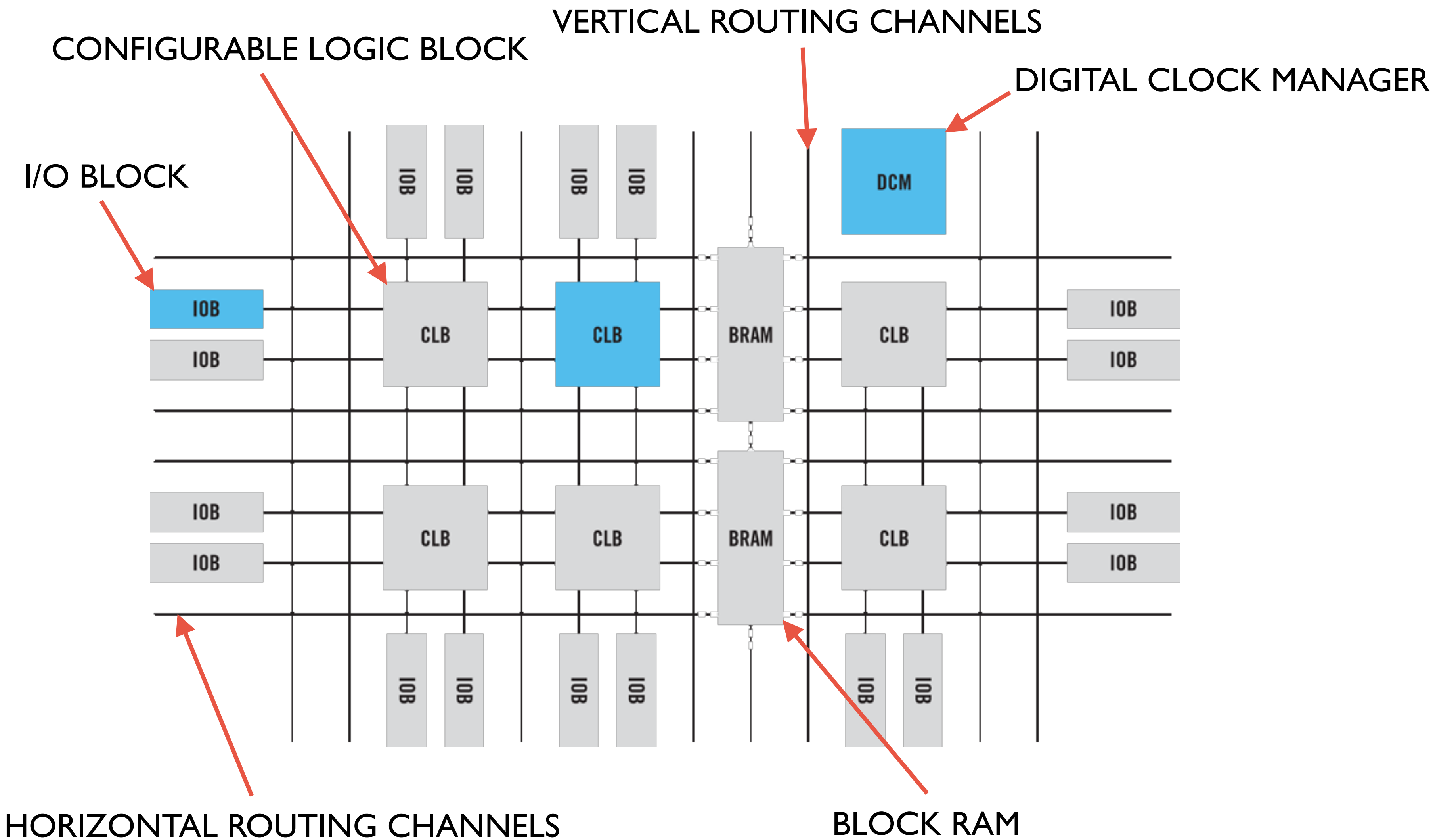
Source: iSuppli

FPGAs AND MOORE'S LAW

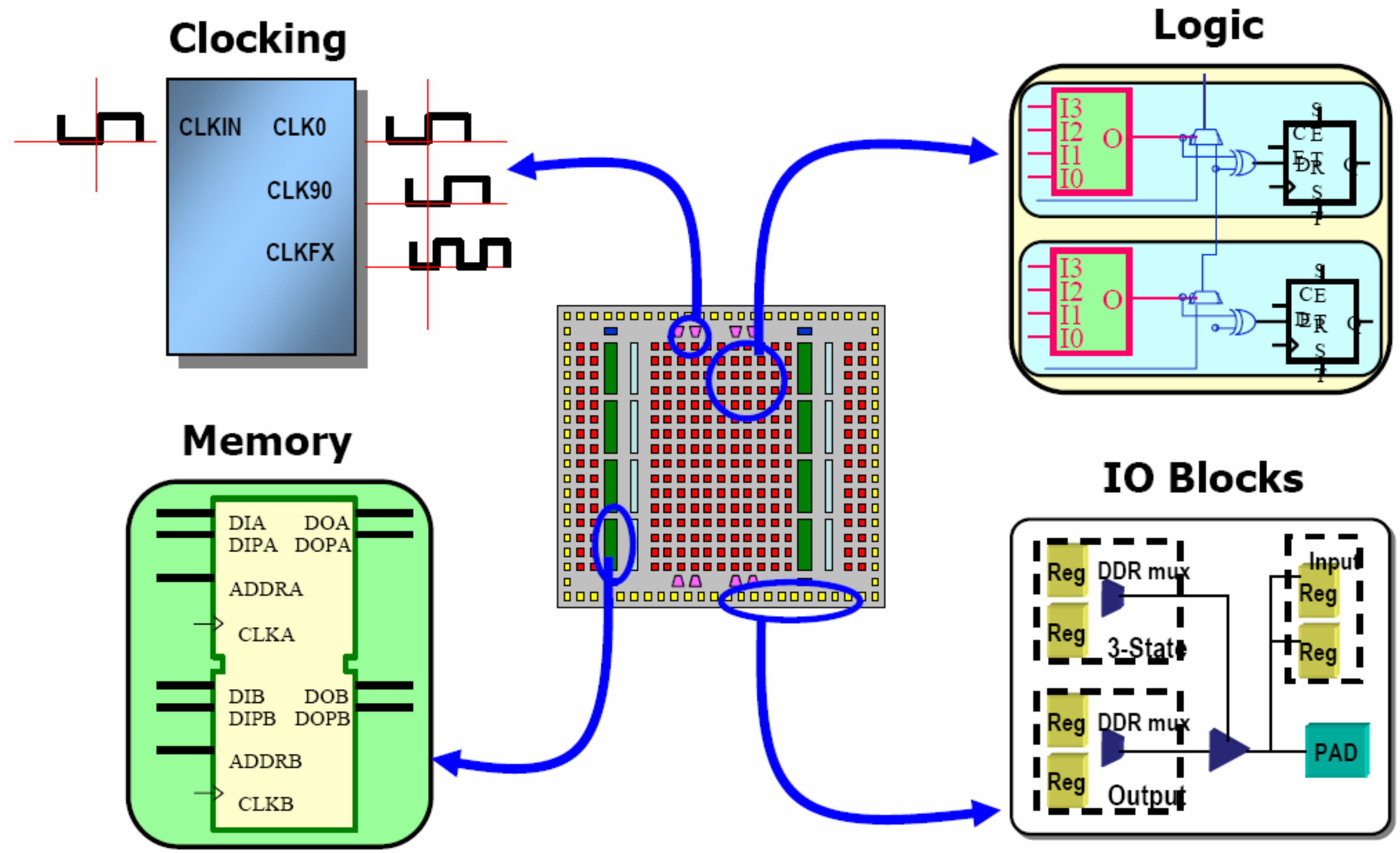
- **10,000x More Logic**
  - Plus Embedded IP
    - Memory
    - Microprocessor
    - DSP
    - Gigabit Serial I/O
- **100x Faster**
- **5000x Lower Power**
- **10,000x Lower Cost**



TYPICAL FPGA ARCHITECTURE - I

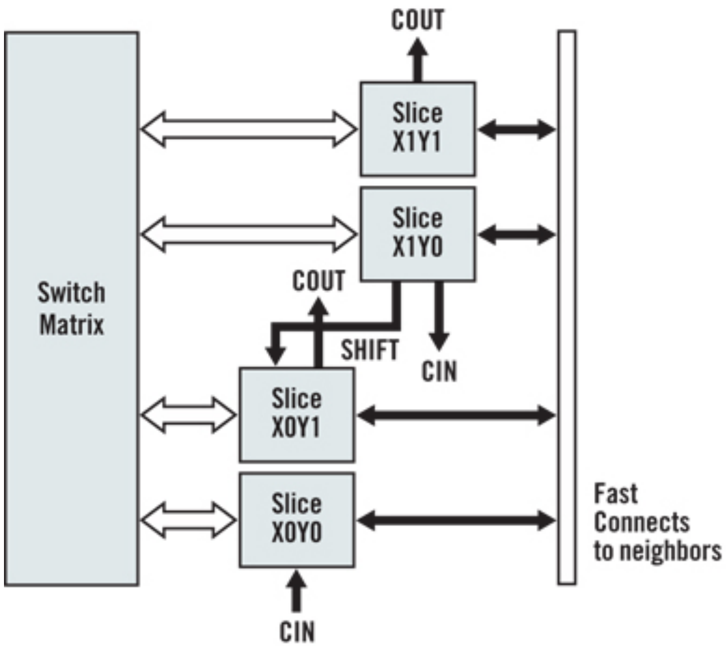


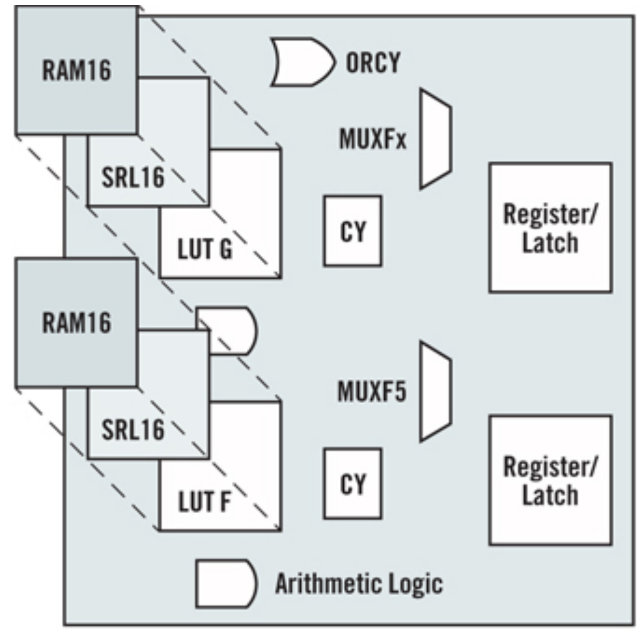
TYPICAL FPGA ARCHITECTURE - 2



CONFIGURABLE LOGIC BLOCKS (CLBs)

BASIC CONFIGURABLE LOGIC BLOCK STRUCTURE

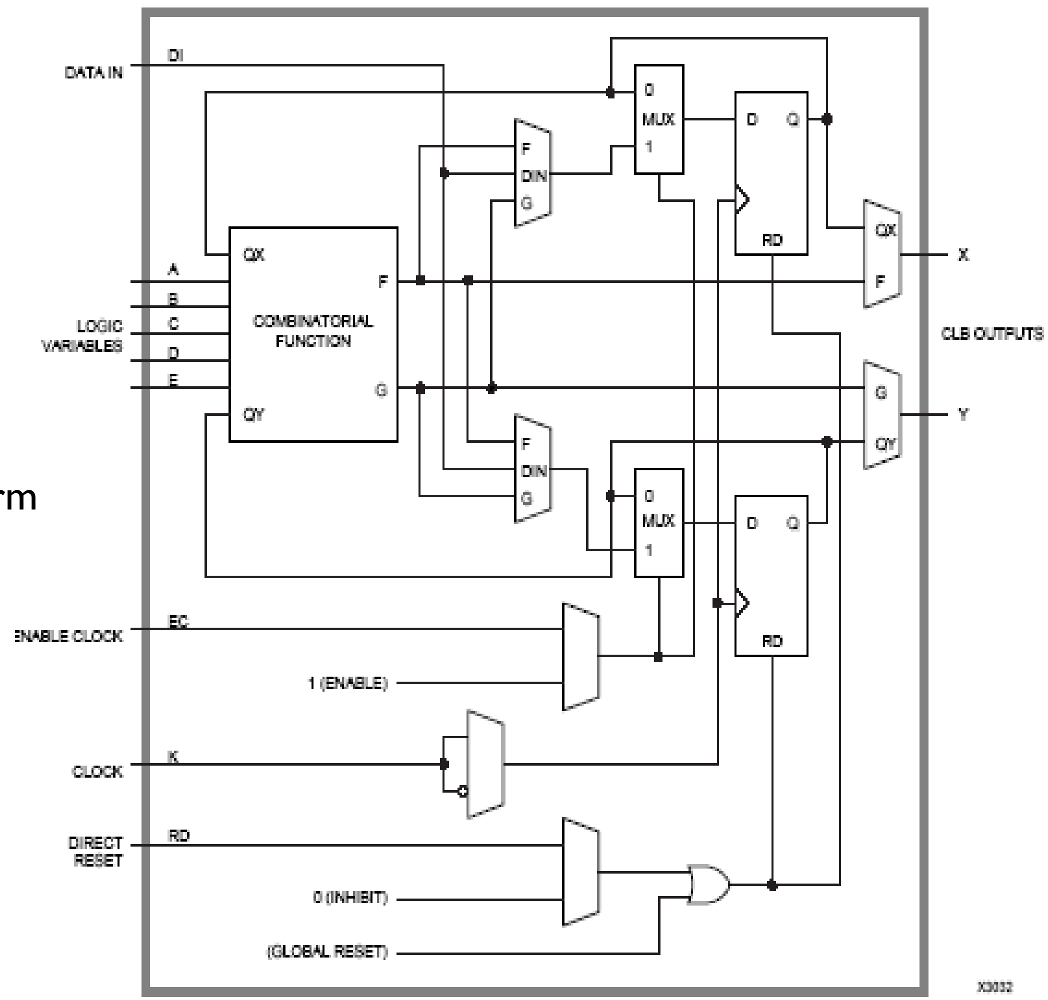




- CLB is the basic logic unit in a FPGA
- Every CLB consists of a configurable switch matrix with 4 or 6 inputs, some selection circuitry (MUX, etc), and flip-flops
- The switch matrix is highly flexible and can be configured to handle combinatorial logic, shift registers or RAM

CLBs - DETAILS

- CLBs contain RAM memory cells
- CLBs can be configured to realize any function of 5 or 4 variables
- Functions are stored in the true table form
- Trapezoidal blocks represent multiplexer
- Multiplexer can be programmed to implement to select one input

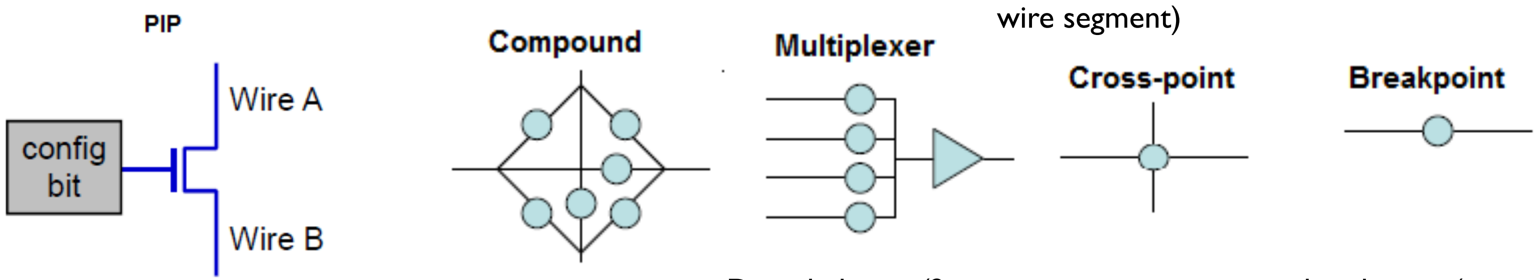


INTERCONNECT

- Flexible interconnect routing routes the signals between CLBs and to and from I/Os

Six break-points PIPs

cross-point (connect vertical or horizontal wire segment)



Decoded mux (2n cross-points connected to a single output)

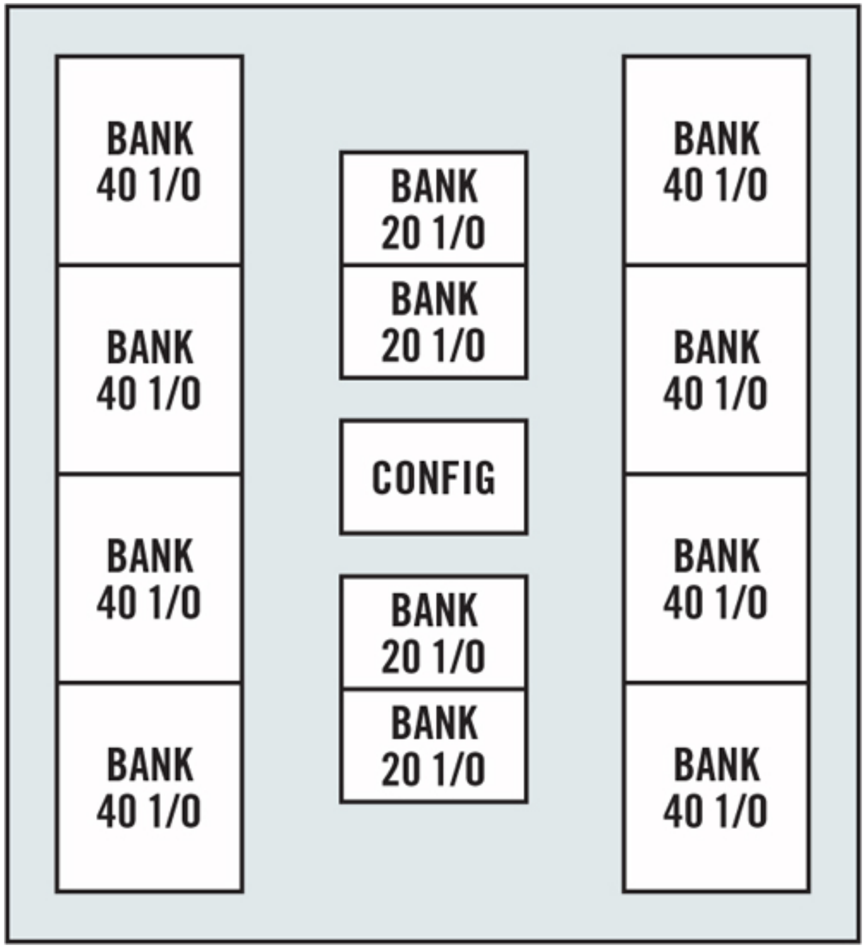
breakpoint (connects or isolate 2 wire segments)

- Flexible interconnect routing routes the signals between CLBs and to and from I/Os
- Routing comes in several flavors, from that designed to interconnect between CLBs to fast horizontal and vertical long lines spanning the device to global low-skew routing for Clocking and other global signals
- The design software makes the interconnect routing task hidden to the user unless specified otherwise, thus significantly reducing design complexity

SELECTIO (IOBs)

BASIC SELECTIO (IOBs) STRUCTURE

- Today's FPGAs provide support for dozens of I/O standards thus providing the ideal interface bridge in your system
- I/O in FPGAs is grouped in banks with each bank independently able to support different I/O standards
- Today's leading FPGAs provide over a dozen I/O banks, thus allowing flexibility in I/O support.



MEMORY AND CLOCK MANAGEMENT

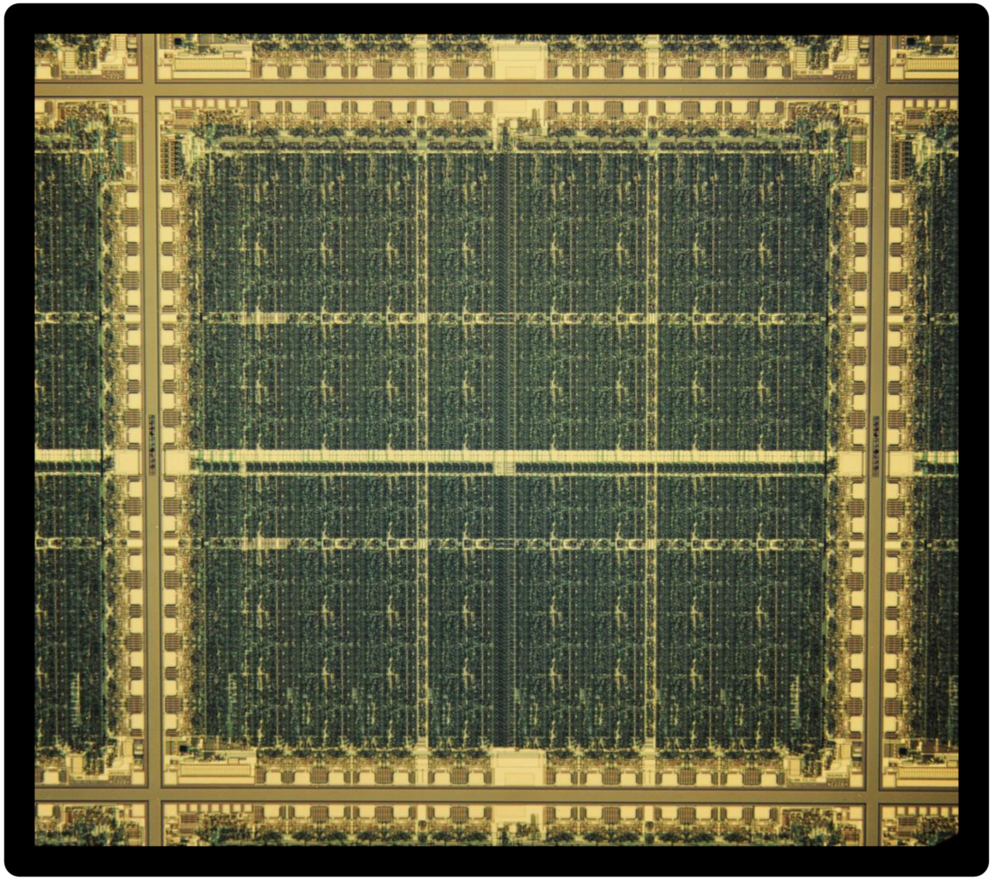
- MEMORY
  - Embedded Block RAM memory is available in most FPGAs, which allows for on-chip memory in your design.
  - Xilinx FPGAs provide up to 10Mbits of on-chip memory in 36kbit blocks that can support true dual-port operation

- COMPLETE CLOCK MANAGEMENT
  - Digital clock management is provided by most FPGAs in the industry (all Xilinx FPGAs have this feature).
  - The most advanced FPGAs from Xilinx offer both digital clock management and phase-looped locking that provide precision clock synthesis combined with jitter reduction and filtering.

XC2064 - THE FIRST FPGA (1985)

- 64 flip flops
- 128 3-LUTs
- 58 I/O pins
- 18MHz (toggle)

- 2um 2LM



2015 - XILINX FPGAs

Features	Artix™-7	Kintex™-7	Virtex®-7	Spartan®-6	Virtex-6
Logic Cells	215,000	480,000	2,000,000	150,000	760,000
BlockRAM	13Mb	34Mb	68Mb	4.8Mb	38Mb
DSP Slices	740	1,920	3,600	180	2,016
DSP Performance (symmetric FIR)	930GMACS	2,845GMACS	5,335GMACS	140GMACS	2,419GMACS
Transceiver Count	16	32	96	8	72
Transceiver Speed	6.6Gb/s	12.5Gb/s	28.05Gb/s	3.2Gb/s	11.18Gb/s
Total Transceiver Bandwidth (full duplex)	211Gb/s	800Gb/s	2,784Gb/s	50Gb/s	536Gb/s
Memory Interface (DDR3)	1,066Mb/s	1,866Mb/s	1,866Mb/s	800Mb/s	1,066Mb/s
PCI Express® Interface	x4 Gen2	Gen2x8	Gen3x8	Gen1x1	Gen2x8
Analog Mixed Signal (AMS)/XADC	Yes	Yes	Yes	-	Yes
Configuration AES	Yes	Yes	Yes	Yes	Yes
I/O Pins	500	500	1,200	576	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V
EasyPath™ Cost Reduction Solution	-	Yes	Yes	-	Yes

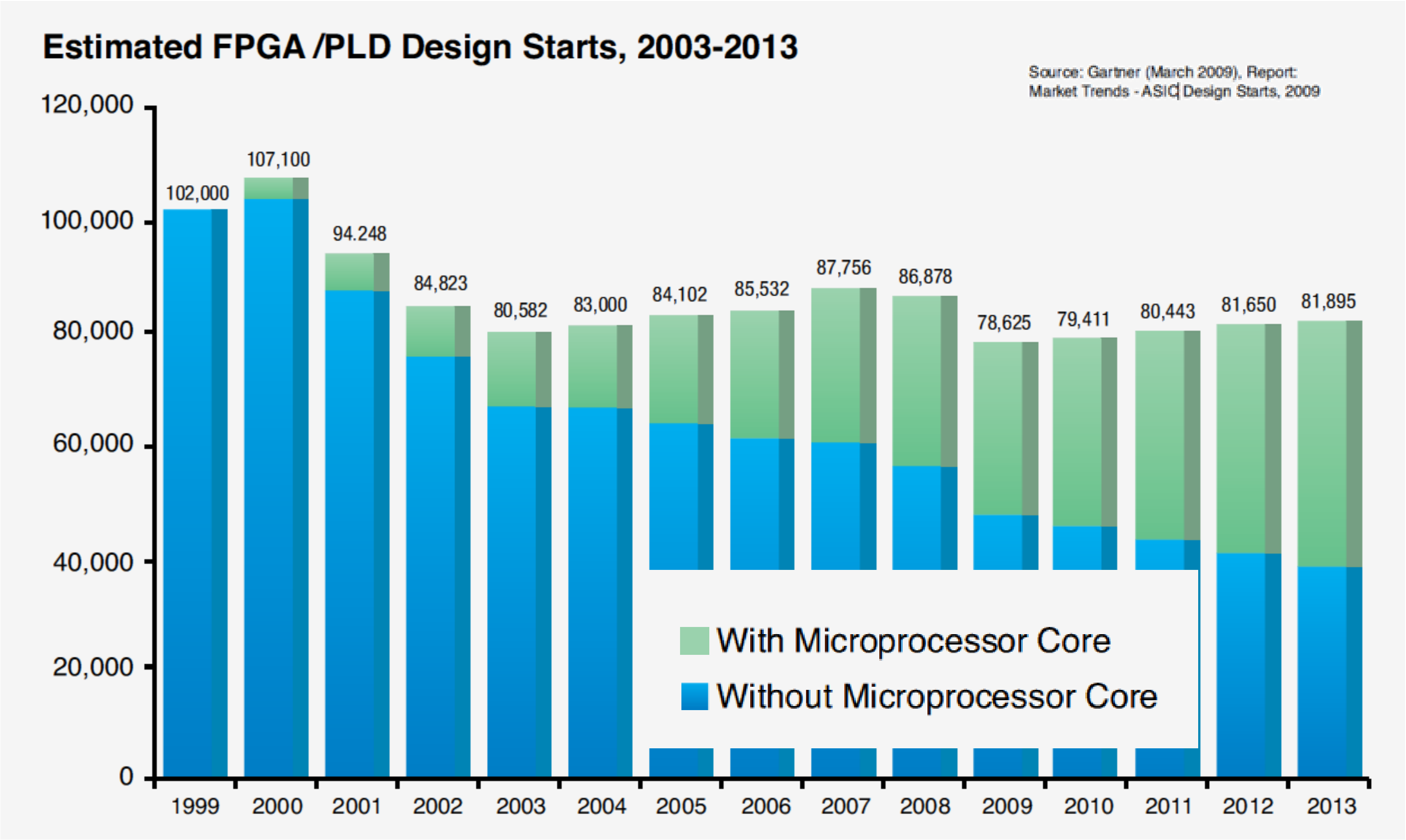
FPGAs APPLICATIONS

- Aerospace and Defense
  - Avionics/DO-254
  - Communications
  - Missiles & Munitions
  - Secure Solutions
  - Space
- Medical Electronics
- ASIC Prototyping
- Audio
  - Connectivity Solutions
  - Portable Electronics
  - Radio
  - Digital Signal Processing (DSP)
- Automotive
  - High Resolution Video
  - Image Processing
  - Vehicle Networking and Connectivity
  - Automotive Infotainment
- Broadcast
  - Real-Time Video Engine
  - EdgeQAM
  - Encoders
  - Displays
  - Switches and Routers
- Consumer Electronics
  - Digital Displays
  - Digital Cameras
  - Multi-function Printers
  - Portable Electronics
  - Set-top Boxes
- High Performance Computing
  - Servers
  - Super Computers
  - SIGINT Systems
  - High-end RADARs
  - High-end Beam Forming Systems
  - Data Mining Systems
- Industrial
  - Industrial Imaging
  - Industrial Networking
  - Motor Control
- Medical
  - Ultrasound
  - CT Scanner
  - MRI
  - X-ray
  - PET
  - Surgical Systems

FPGAs APPLICATIONS

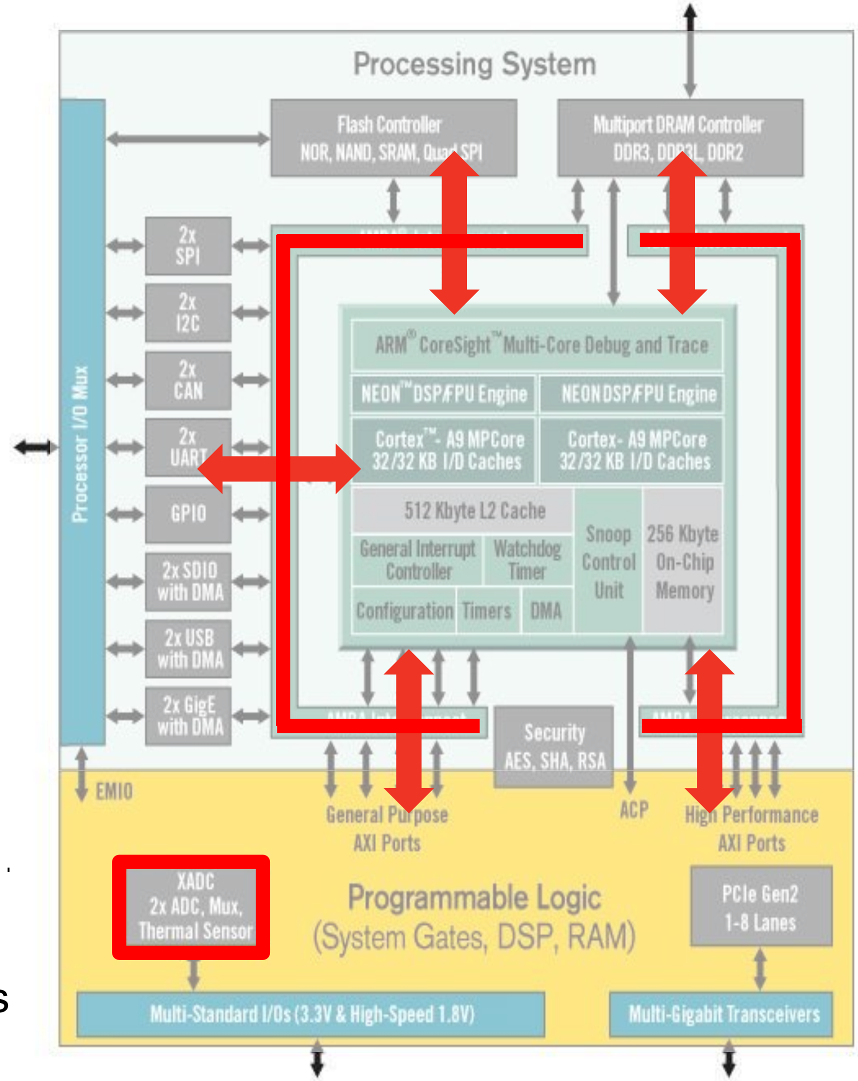
- Scientific Instruments
  - Lock-in amplifiers
  - Boxcar averagers
  - Phase-locked loops
- Security
  - Industrial Imaging
  - Secure Solutions
  - Image Processing
- Video & Image Processing
  - High Resolution Video
  - Video Over IP Gateway
  - Digital Displays
  - Industrial Imaging
- Wired Communications
  - Optical Transport Networks
  - Network Processing
  - Connectivity Interfaces
- Wireless Communications
  - Baseband
  - Connectivity Interfaces
  - Mobile Backhaul
  - Radio

HARDWARE AND SOFTWARE PROGRAMMABILITY: ASSP SoC

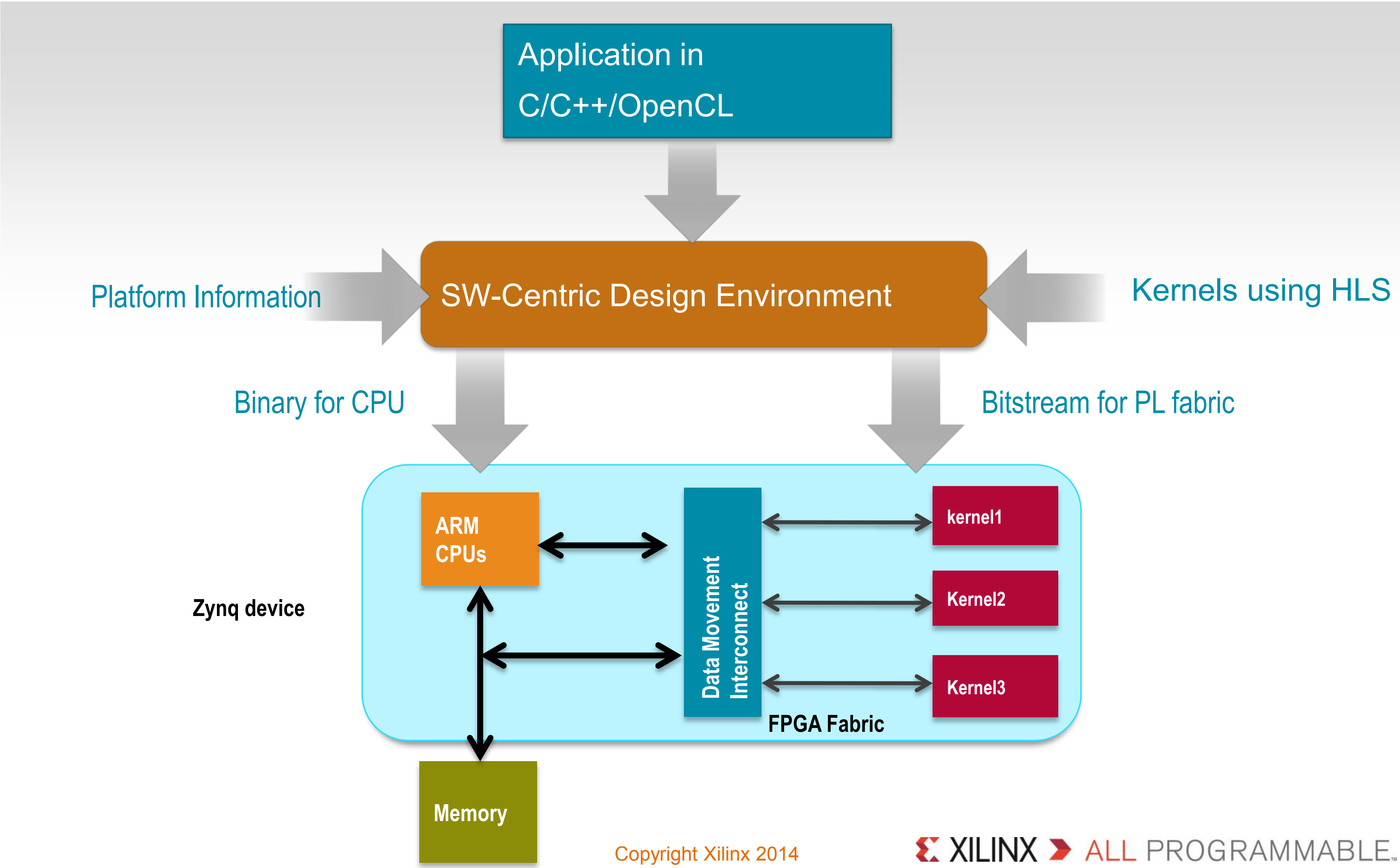


Zynq All-Programmable SoC

- **Processor System (PS)**
  - 2x ARM9 866MHz-1GHz 32K/32K I/D Caches
  - 512KB shared L2 Cache
  - 256KB On-chip memory
  - Memory controller
  - Bus interfaces, timers
  - Libraries, OSs, middleware
- **Programmable Logic (PL)**
  - 28K – 440K LCs
  - 240K – 3MB RAM
  - 80 – 2020 DSP blocks
  - I/O, Transceivers, PCIe, Ethernet…
- **Programmable ADC**
  - Inputs from Voltage, Temp sensors
- **AMBA AXI bus fabric**

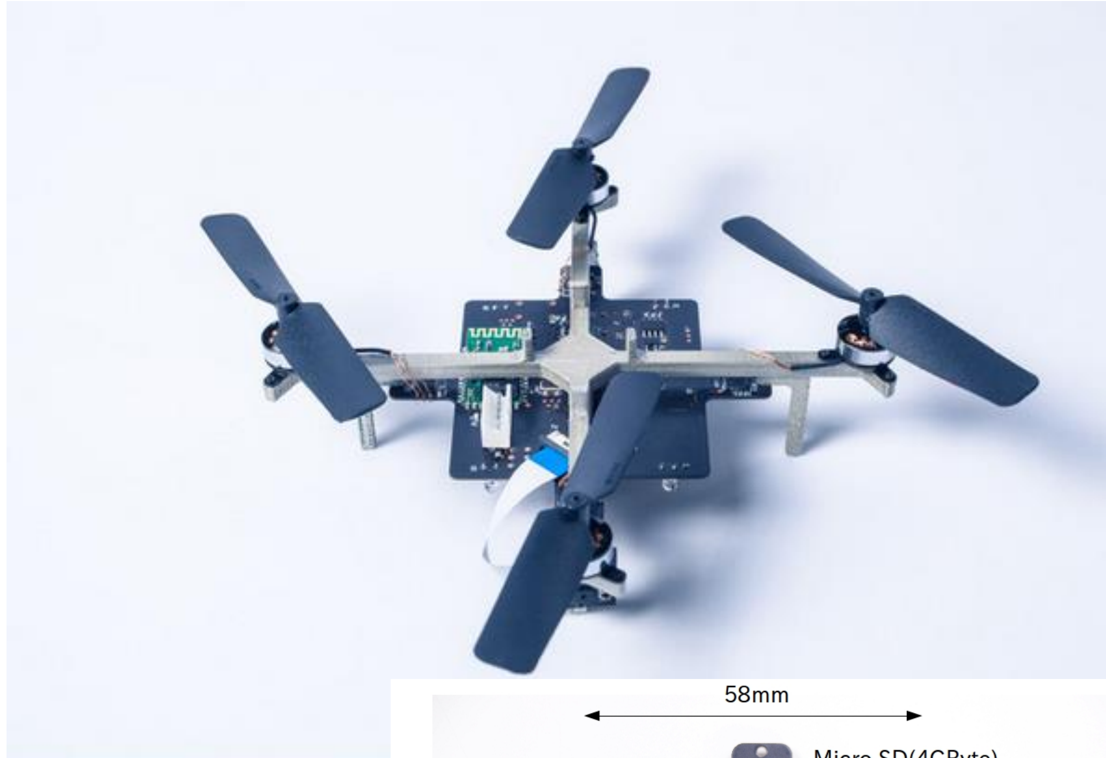


ALL-PROGRAMMABLE PROGRAMMING

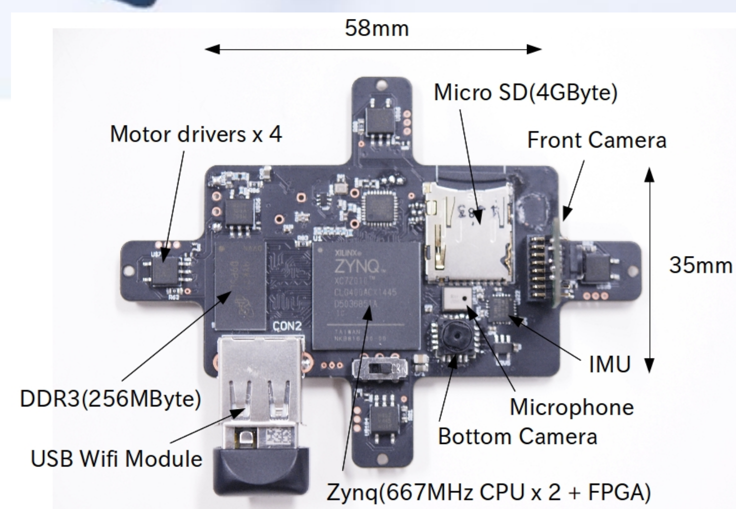


A NICE ZYNQ APPLICATION

Phenox



- 2 cameras
- Microphone
- 4 motors
- Autonomous
- Avoids obstacles
- Responds to audio signals and hand gestures
- Programmable aerial platform
- Programmed with OpenCL



http://phenoxlab.com

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