

Front-End electronics in particle physics EDIT school

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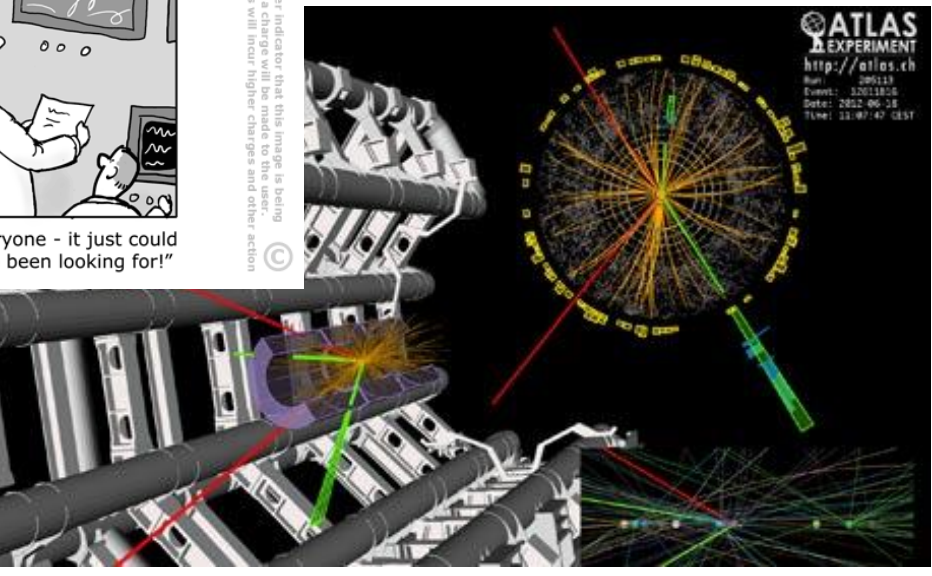
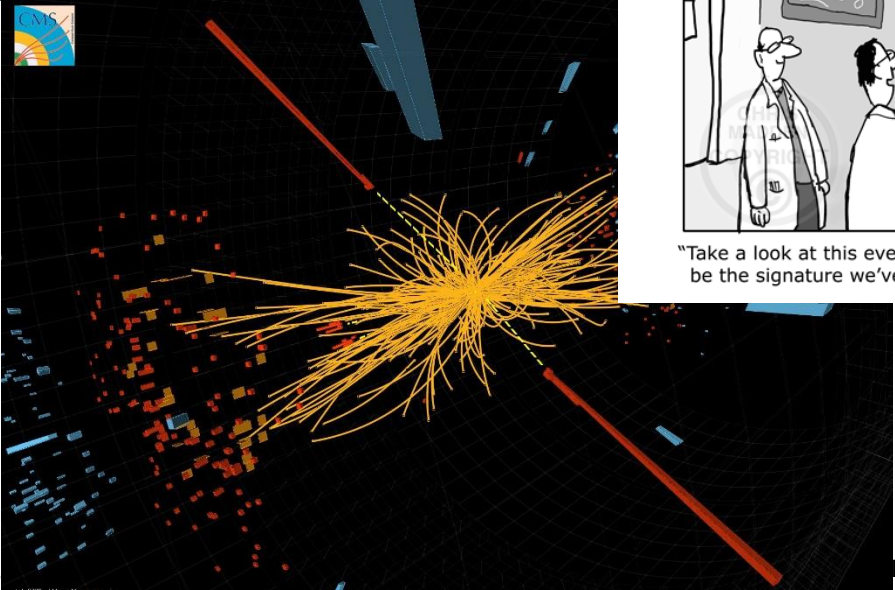
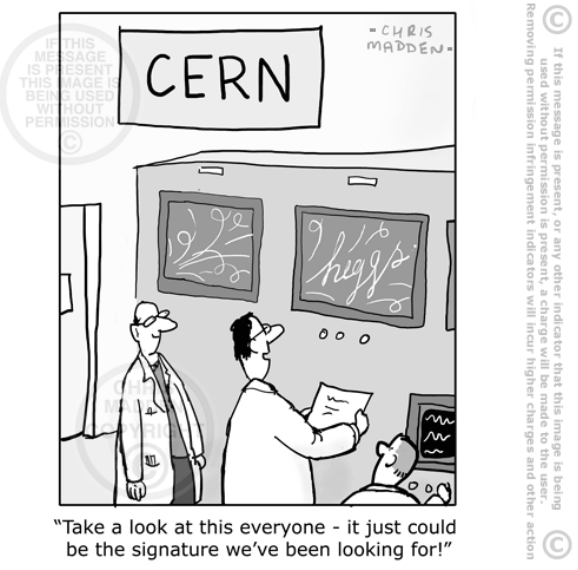
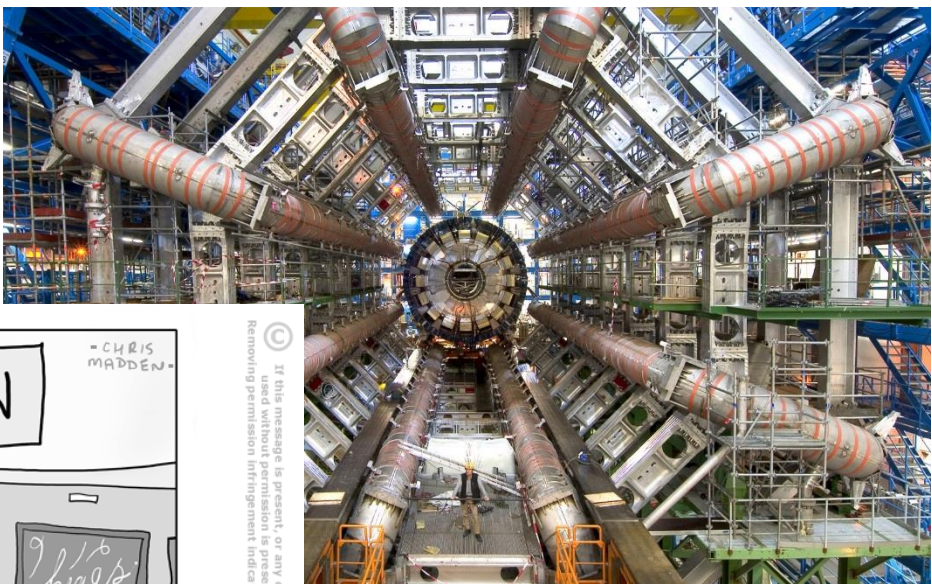
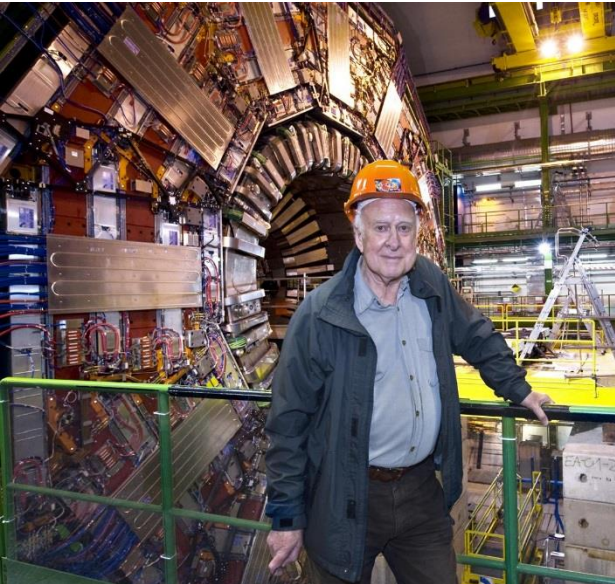
1. Low noise charge preamps : pixel readout
2. Large dynamic range : calorimeters
3. High speed designs : sipm readout
4. Trends and future

Lectures for physicists, not electronics engineers => will concentrate on front-end and performance of detector, not on detailed engineering

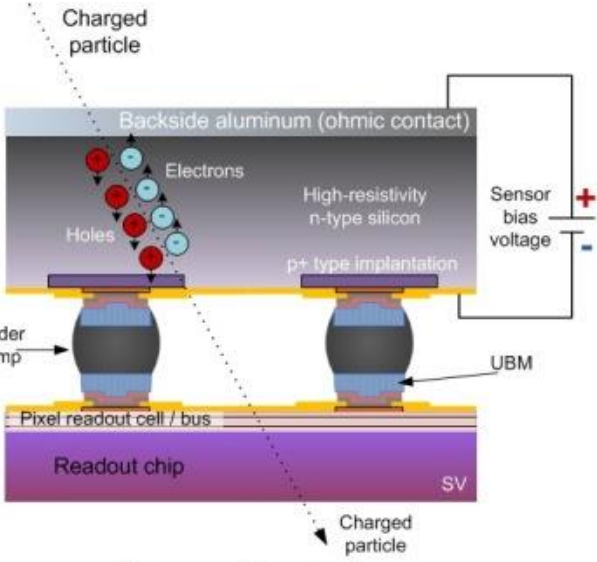
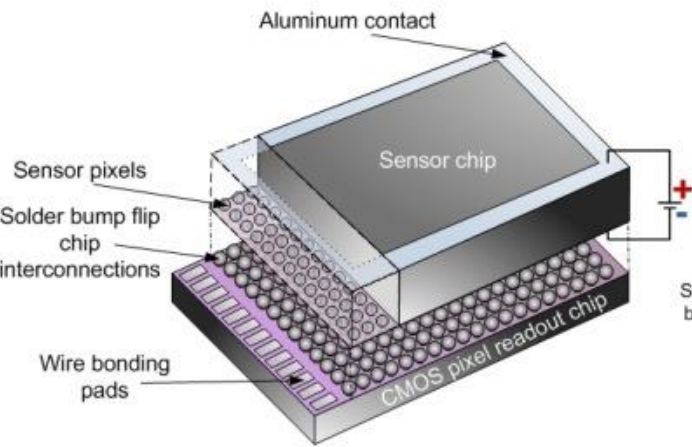
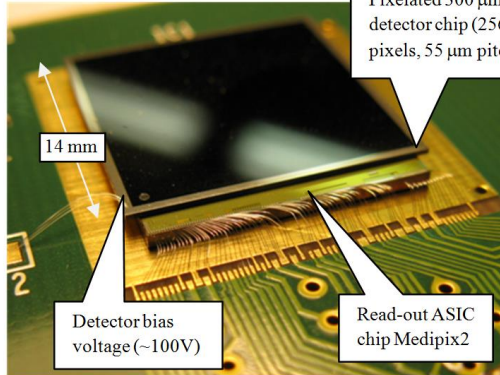
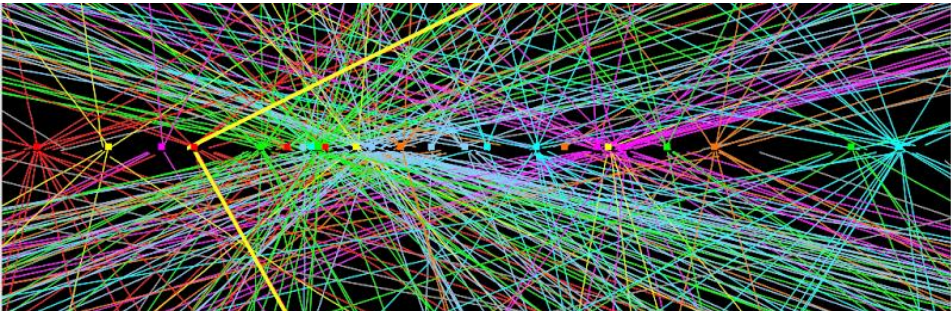
Many more slides than allocated time : don't be afraid !
I will skip many details : they are for further reference

No prerequisites needed (apart from $R=U/I$)

- A lot of electronics in the experiments...which impacts the detectors

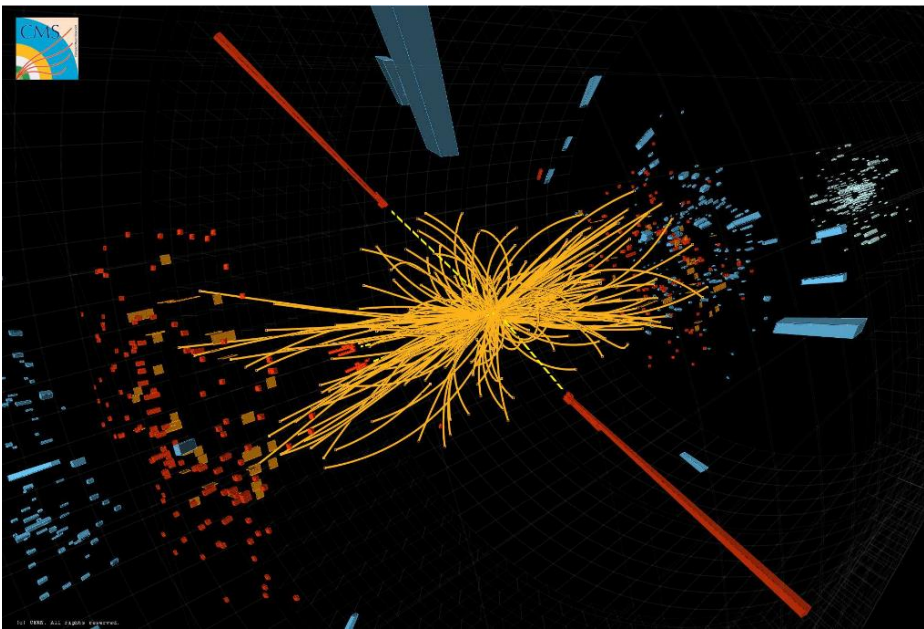
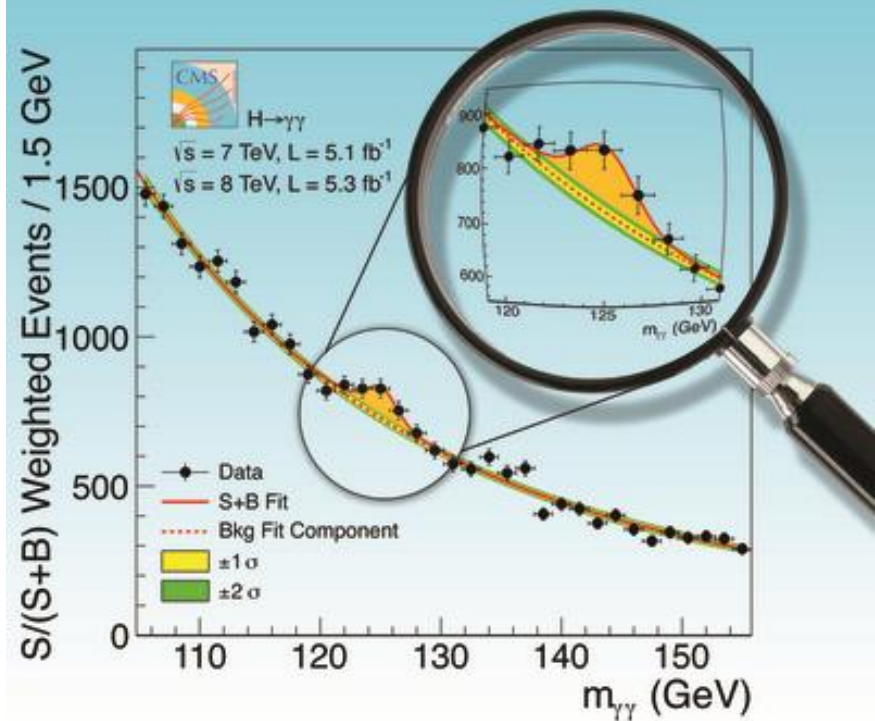


- Measurement of (charged) particle tracks
 - millions of pixels (~100 μm)
 - binary readout at 40 MHz
 - High radiation levels
 - Made possible by ASICs

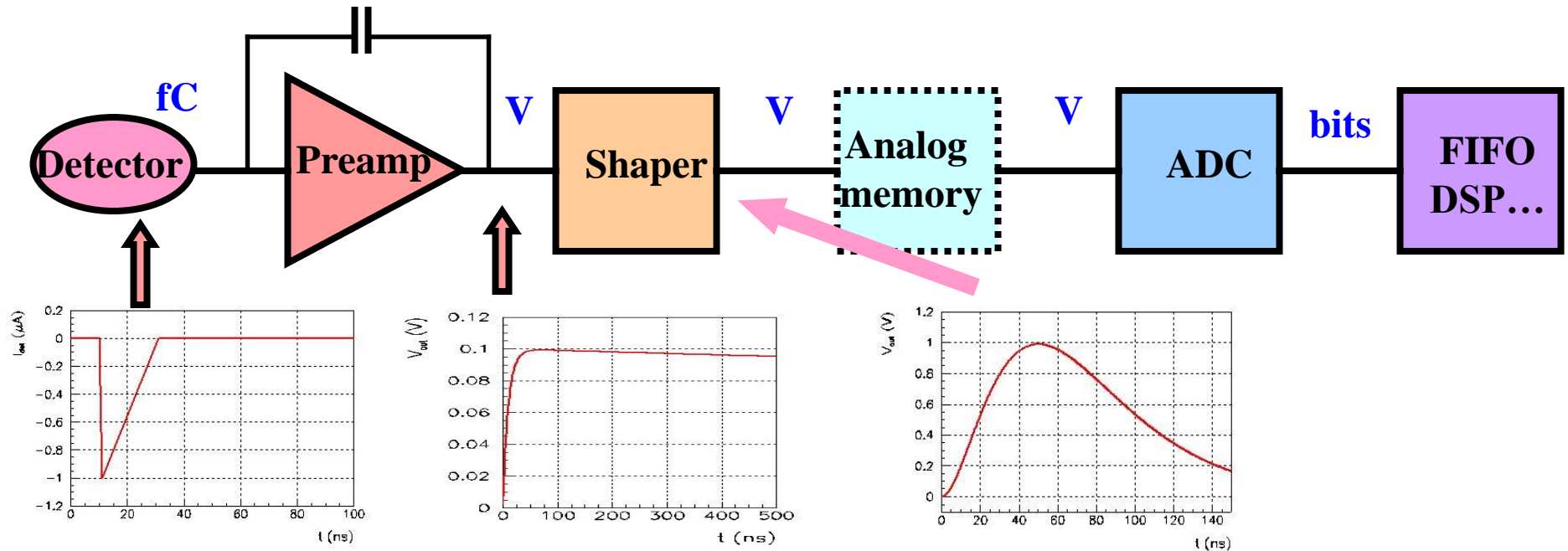


- Large dynamic range (10^4 - 10^5)
- High Precision $\sim 1\%$
 - Importance of low noise, uniformity, linearity...
 - Importance of calibration

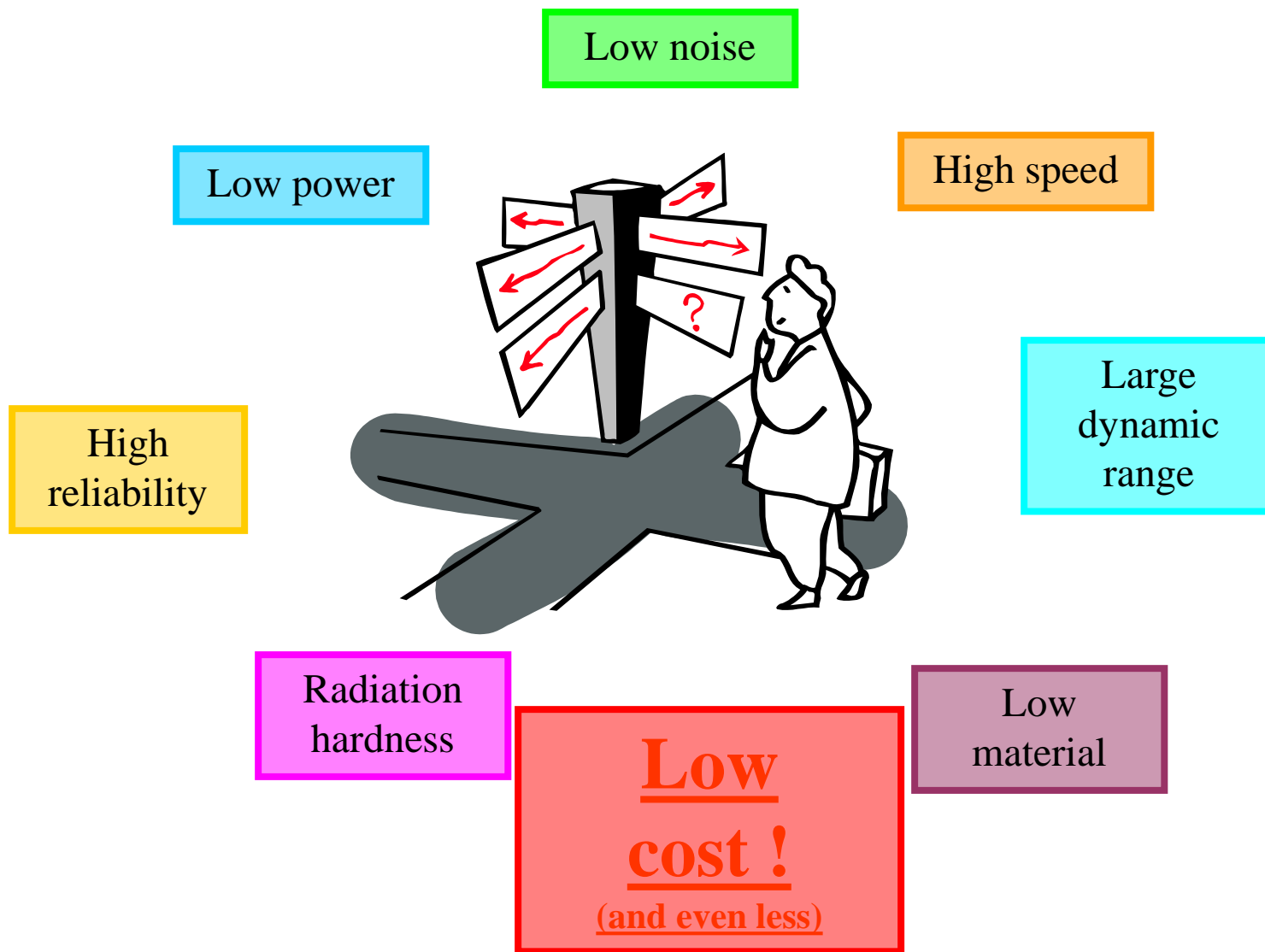
H \rightarrow $\gamma\gamma$ in CMS calorimeter



- Most front-ends follow a similar architecture

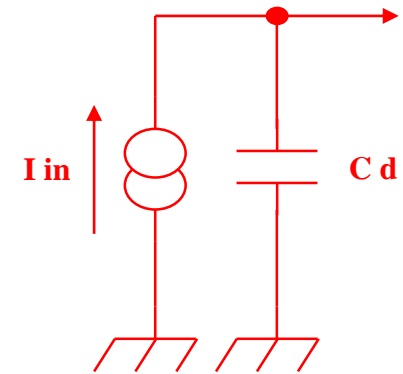


- n Very small signals (fC) -> need **amplification**
- n Measurement of **amplitude** and/or **time** (ADCs, discris, TDCs)
- n Several thousands to millions of channels
- n **Trends** : high speed, low power



Detector modelization

- Detector = capacitance C_d
 - Pixels/strips : 0.1-10 pF
 - PMs/SiPMs : 3-300 pF
 - Ionization chambers 10-1000 pF
 - Sometimes effect of transmission line
- Signal : current source
 - Pixels : $\sim 100e^-/\mu\text{m}$
 - PMs : 1 photoelectron $\rightarrow 10^5\text{-}10^7 e^-$
 - Modelized as an impulse (Dirac) :
 $i(t) = Q_0 \delta(t)$
- Missing :
 - High Voltage bias
 - Connections, grounding
 - Neighbours
 - Calibration...



Detector modelization



CMS pixel module



ATLAS LAr calorimeter

Vacuum Photomultipliers

$$G = 10^5 - 10^7$$

$$C_d \sim 10 \text{ pF}$$

$$L \sim 10 \text{ nH}$$

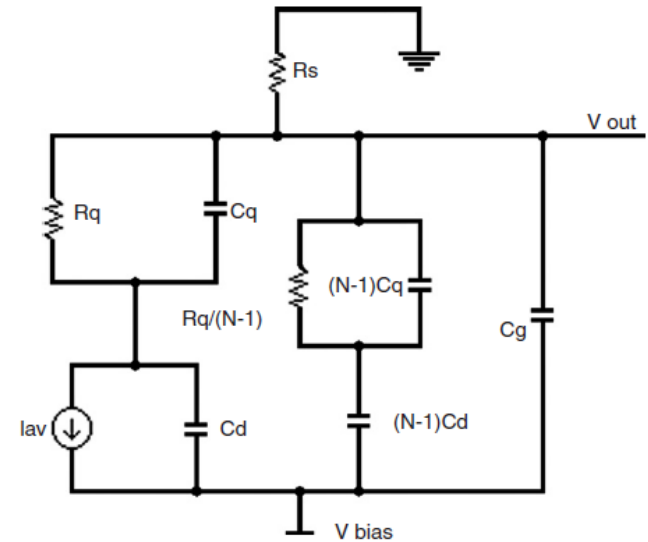
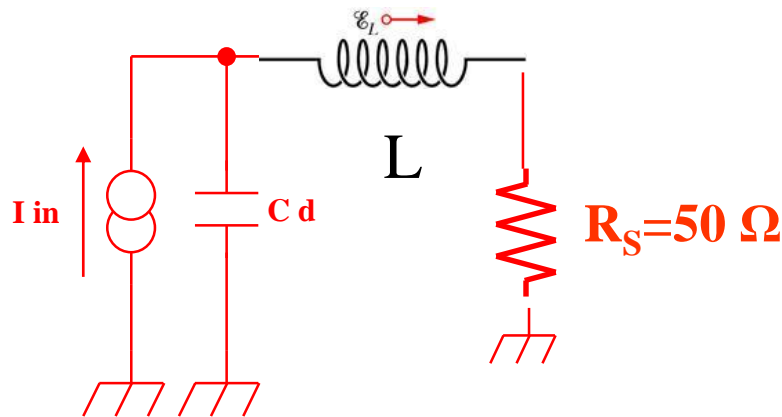
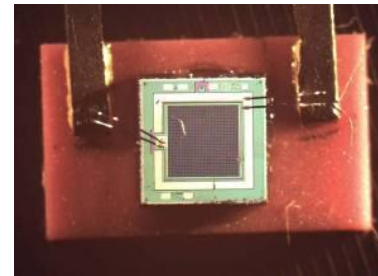


Silicon Photomultipliers

$$G = 10^5 - 10^7$$

$$C = 10 - 400 \text{ pF}$$

$$L = 1 - 10 \text{ nH}$$



Optimizing signal shape for timing

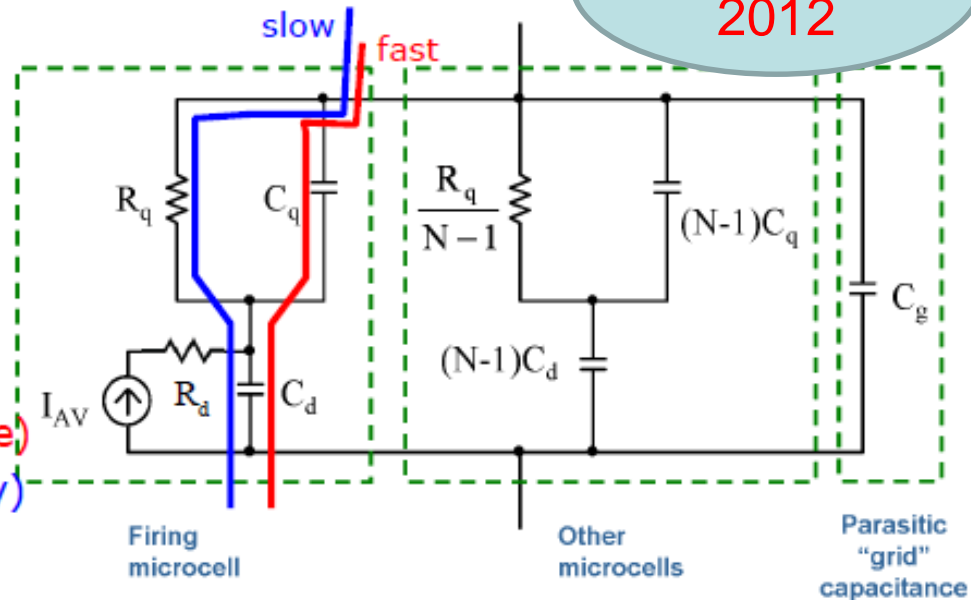
Collazuol 2012

Single cell model $\rightarrow (R_d || C_d) + (R_q || C_q)$

SiPM + load $\rightarrow (||Z_{cell}) || C_{grid} + Z_{load}$

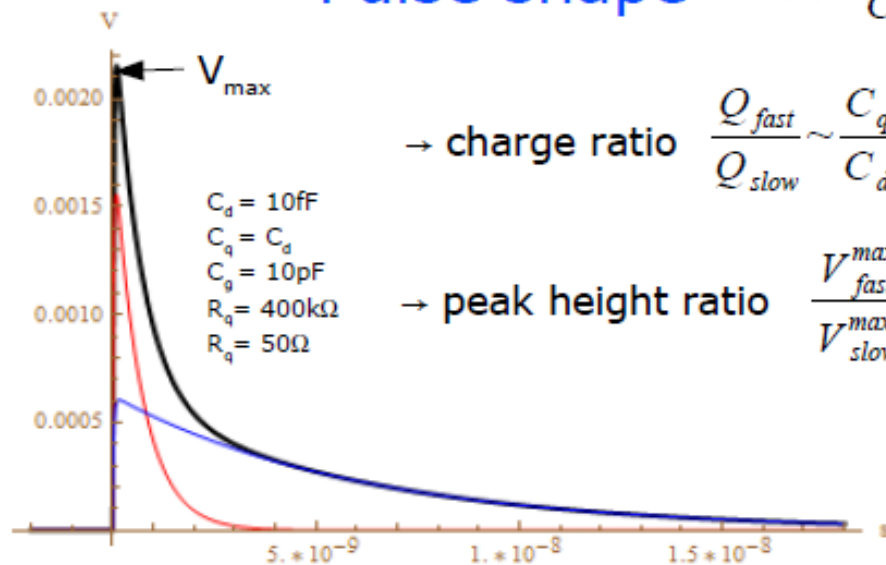
Signal = **slow** pulse ($\tau_{d (rise)}, \tau_{q-slow (fall)}$) + **fast** pulse ($\tau_{d (rise)}, \tau_{q-fast (fall)}$)

- $\tau_{d (rise)} \sim R_d (C_q + C_d)$
- $\tau_{q-fast (fall)} = R_{load} C_{tot}$ (fast; parasitic spike)
- $\tau_{q-slow (fall)} = R_q (C_q + C_d)$ (slow; cell recovery)



Pulse shape

$$V(t) \approx \frac{Q}{C_q + C_d} \left(\frac{C_q}{C_{tot}} e^{-\frac{t}{\tau_{FAST}}} + \frac{R_{load}}{R_q} \frac{C_d}{C_q + C_d} e^{-\frac{t}{\tau_{SLOW}}} \right)$$



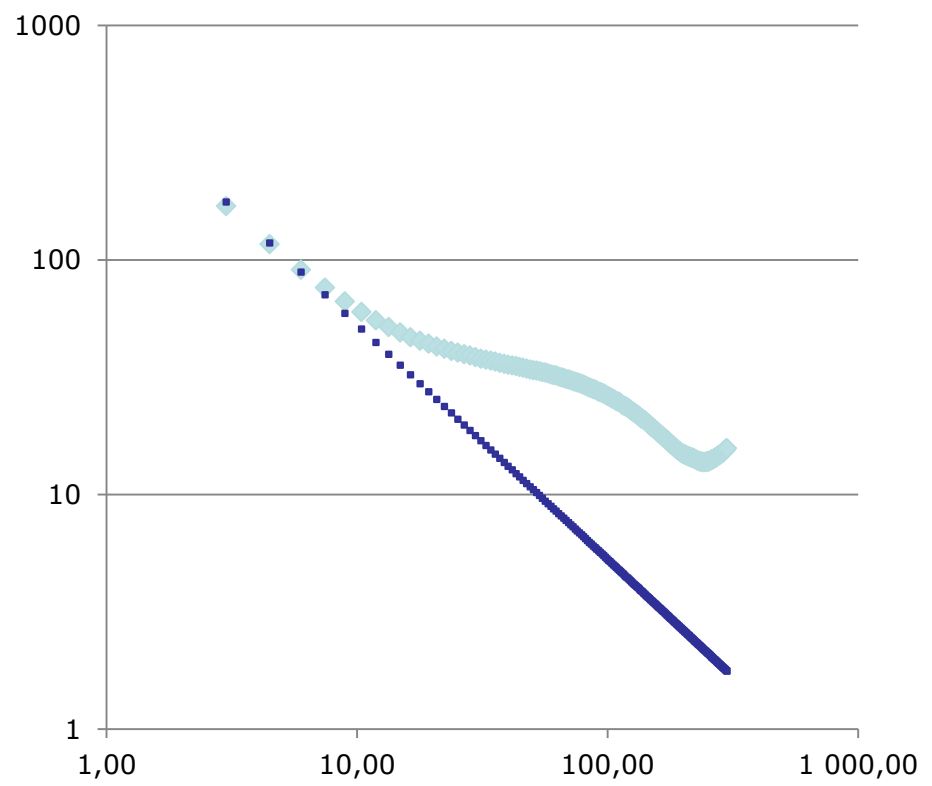
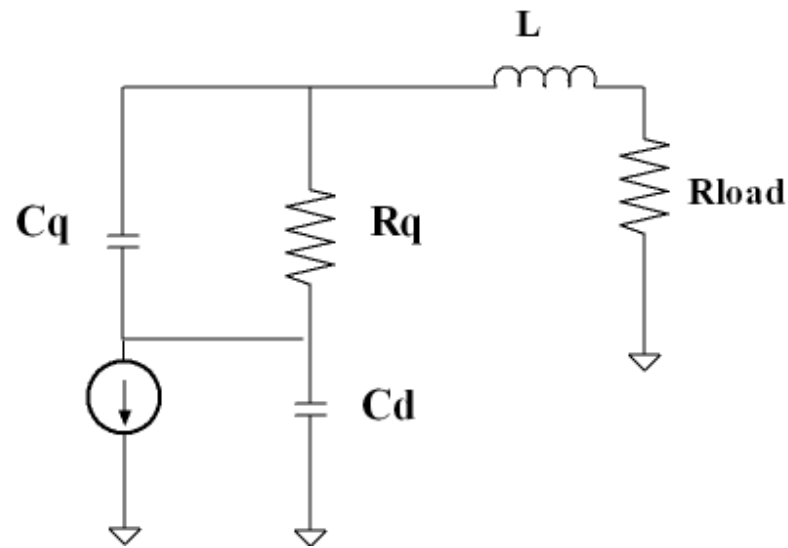
→ charge ratio $\frac{Q_{fast}}{Q_{slow}} \sim \frac{C_q}{C_d}$

→ peak height ratio $\frac{V_{fast}^{max}}{V_{slow}^{max}} \sim \frac{C_q^2 R_q}{C_d C_{tot} R_{load}}$ increasing with R_q and $1/R_{load}$ (and C_q of course)

Increasing C_q/C_d or/and R_q/R_{load}
 → spike enhancement
 → better timing

SiPM impedance and model

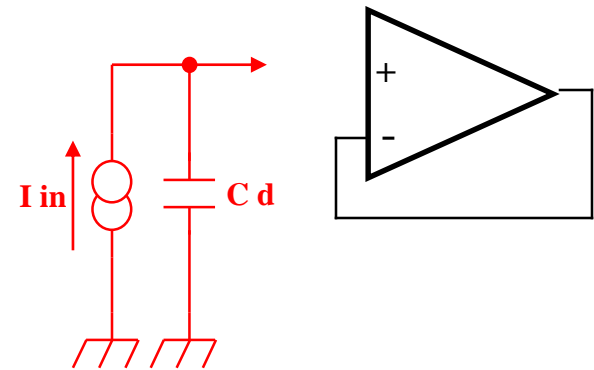
- RLC too simple, inaccurate at high frequency
- CdRqCqLR OK
 - May better explain HF noise behaviour



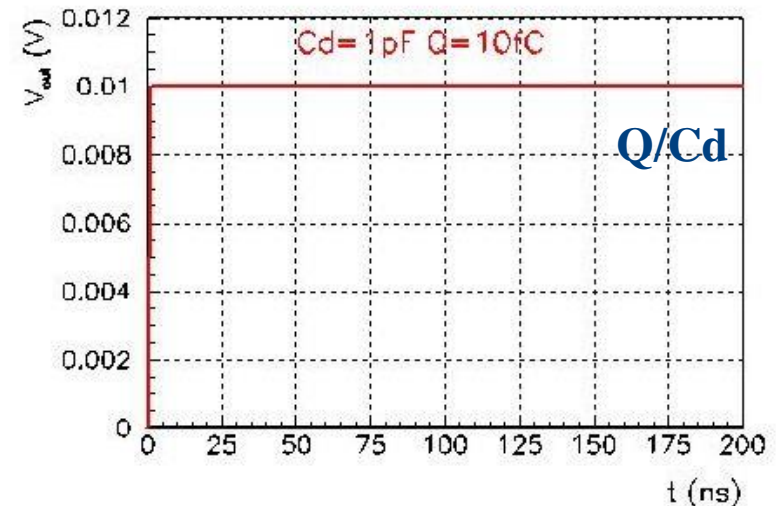
Measured impedance
MPPC HPK 3x3 mm
Line : C = 320 pF

Reading the signal

- Signal
 - Signal = current source
 - Detector = capacitance C_d
 - Quantity to measure
 - Charge => integrator + ADC
 - Time => discriminator + TDC
- Integrating on C_d
 - Simple : $V = Q/C_d$
 - « Gain » : $1/C_d$: 1 pF -> 1 mV/fC
 - Need a follower to buffer the voltage... => parasitic capacitance
 - Gain loss, possible non-linearities
 - crosstalk
 - Need to empty C_d ...



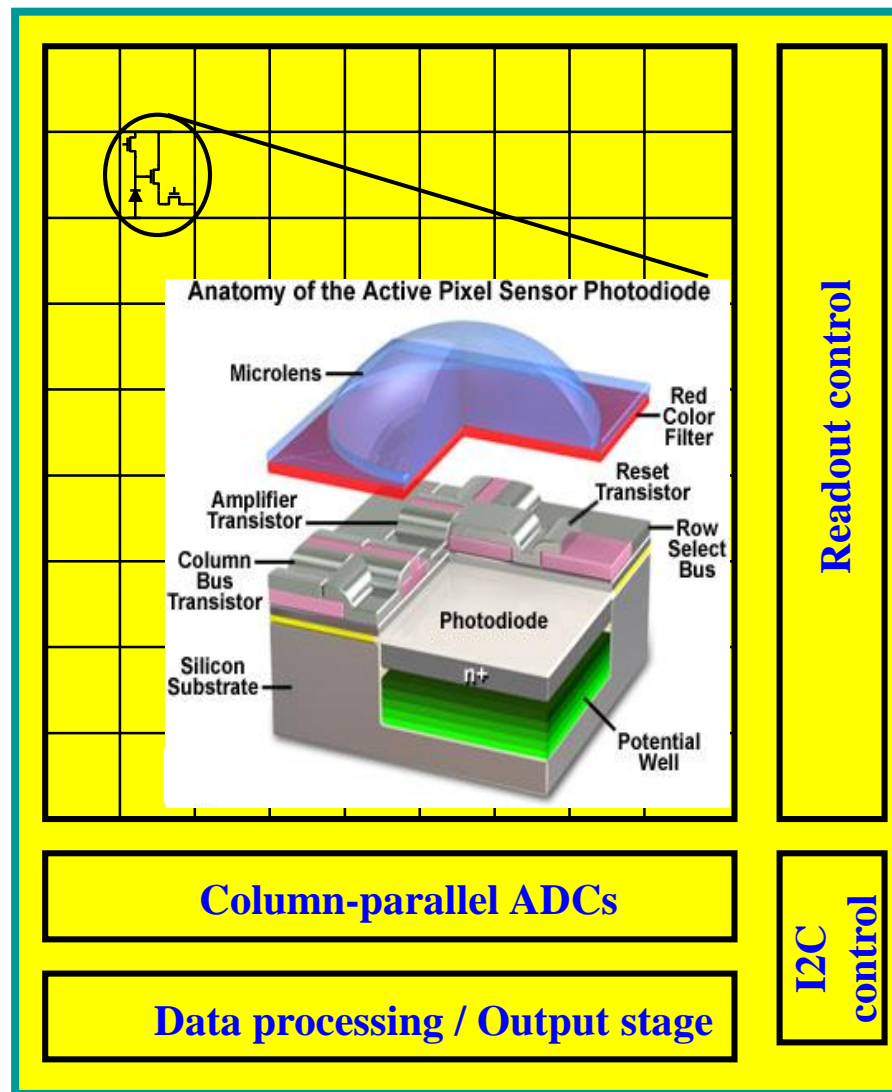
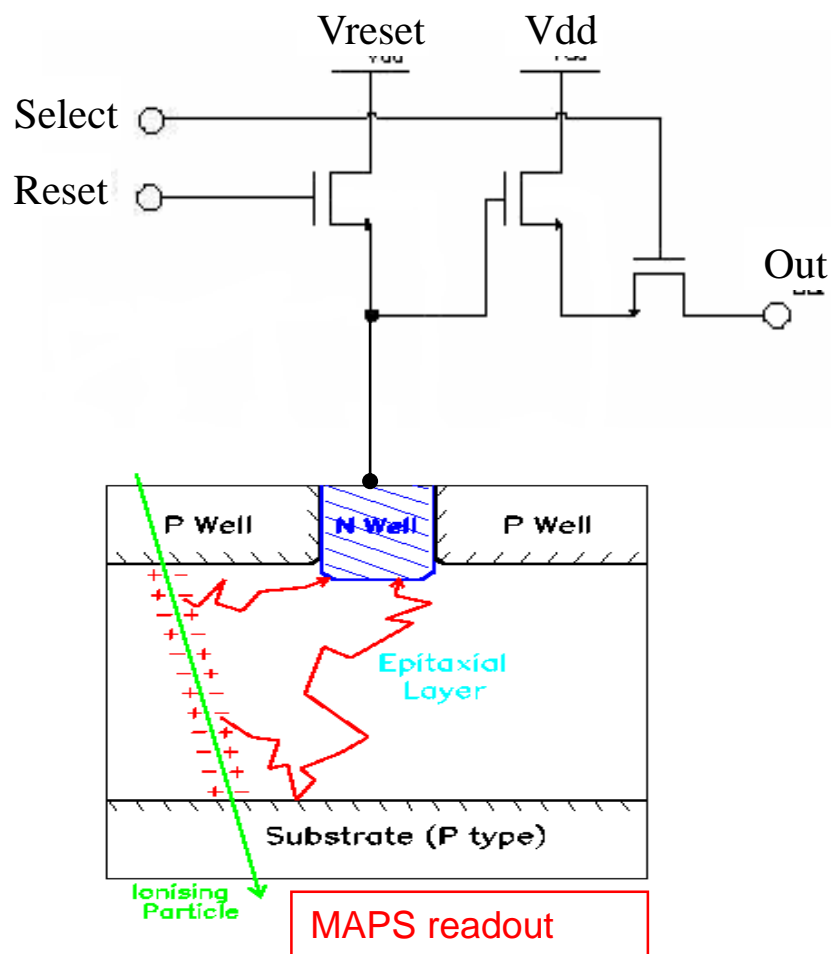
Voltage readout

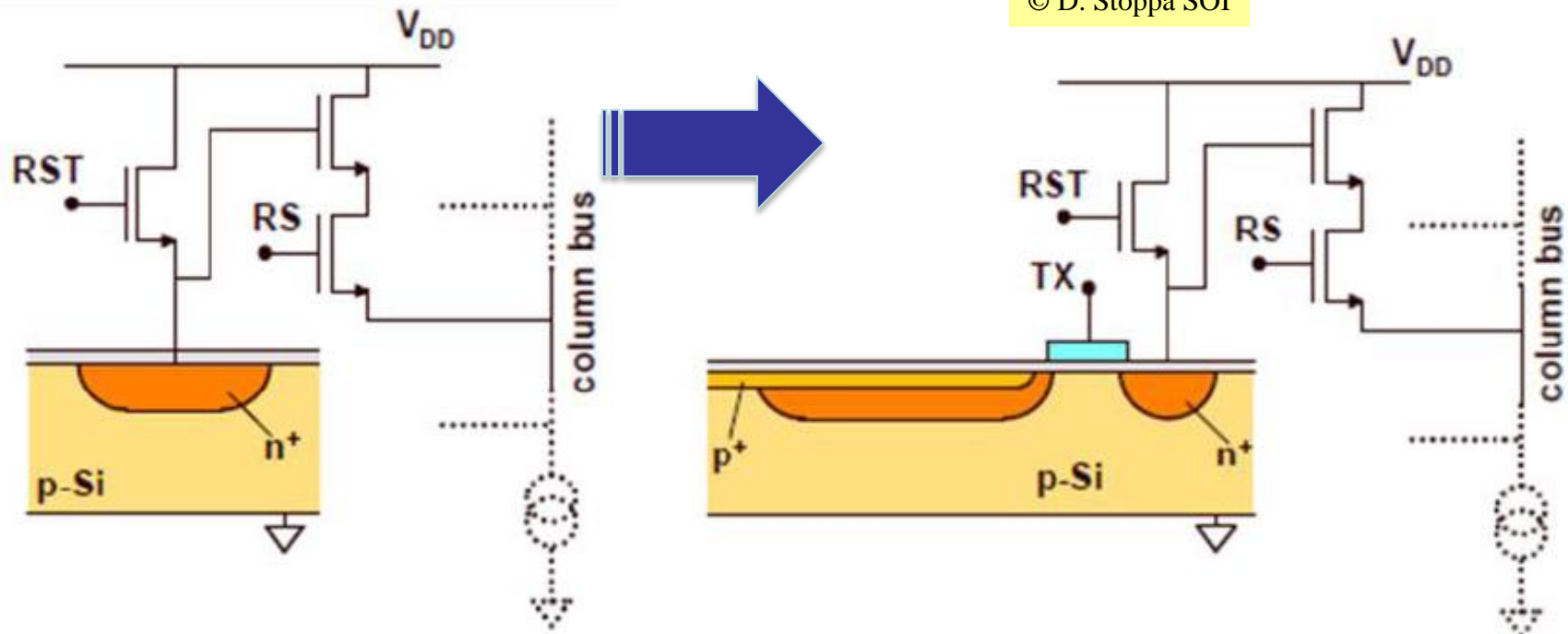


Impulse response

Example : Monolithic active pixels

- Epitaxial layer forms sensitive volume (2-20 μm)
- Charge collection by diffusion
- Read $\sim 100\text{ e}^-$ on $\text{Cd} \sim 10\text{fF} = \text{few mV}$

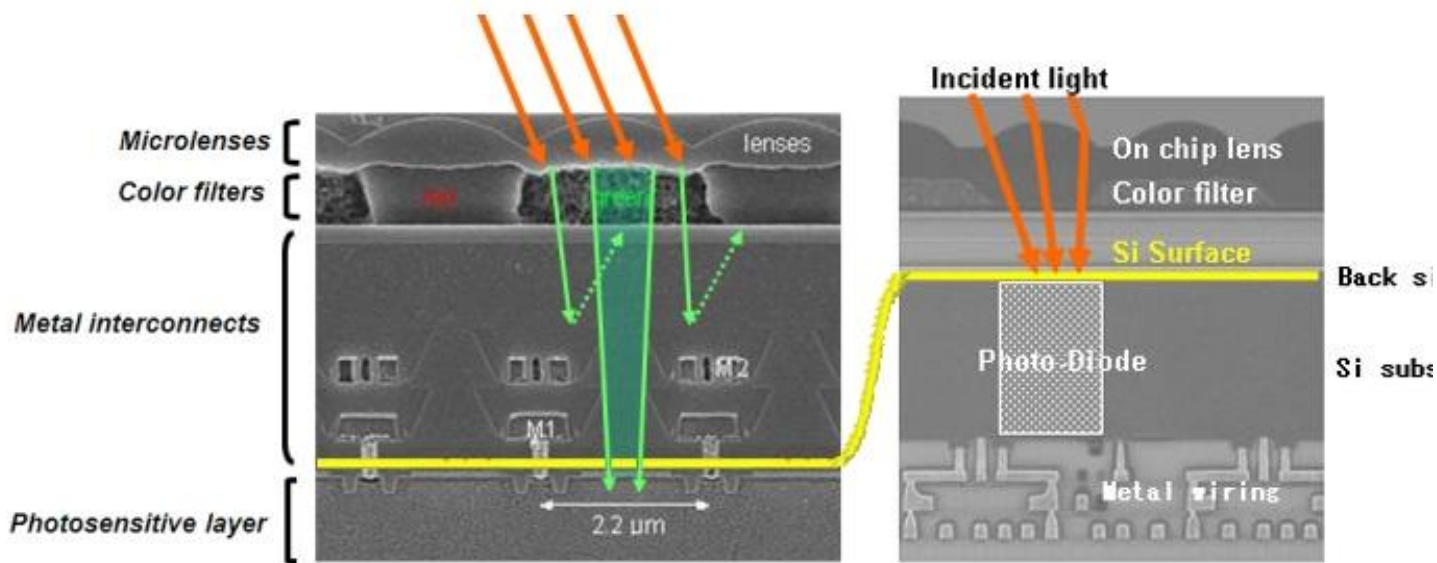
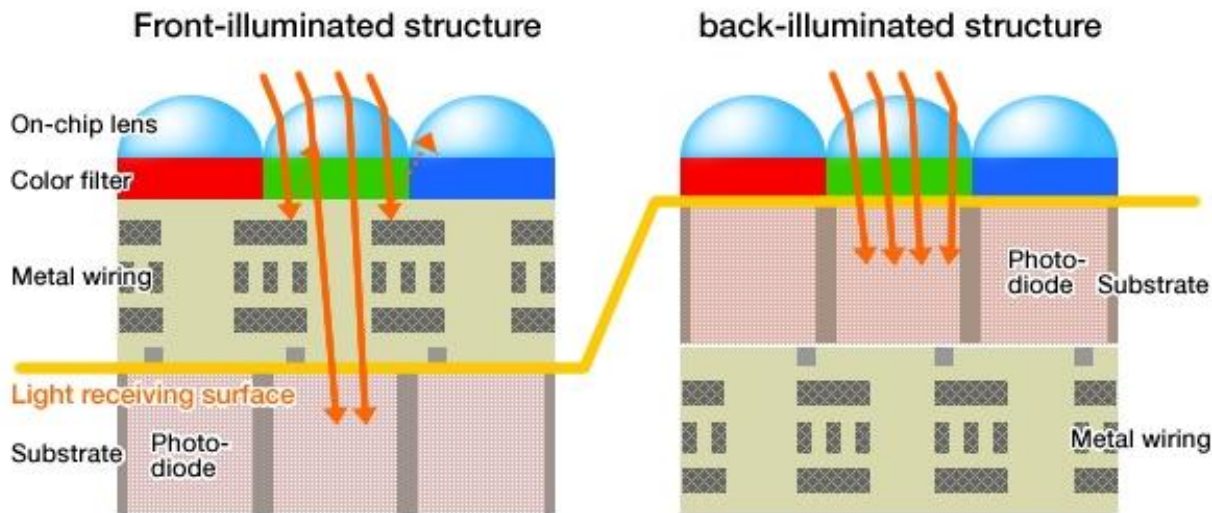




<http://indico.cern.ch/conferenceTimeTable.py?confId=170595#20120917>

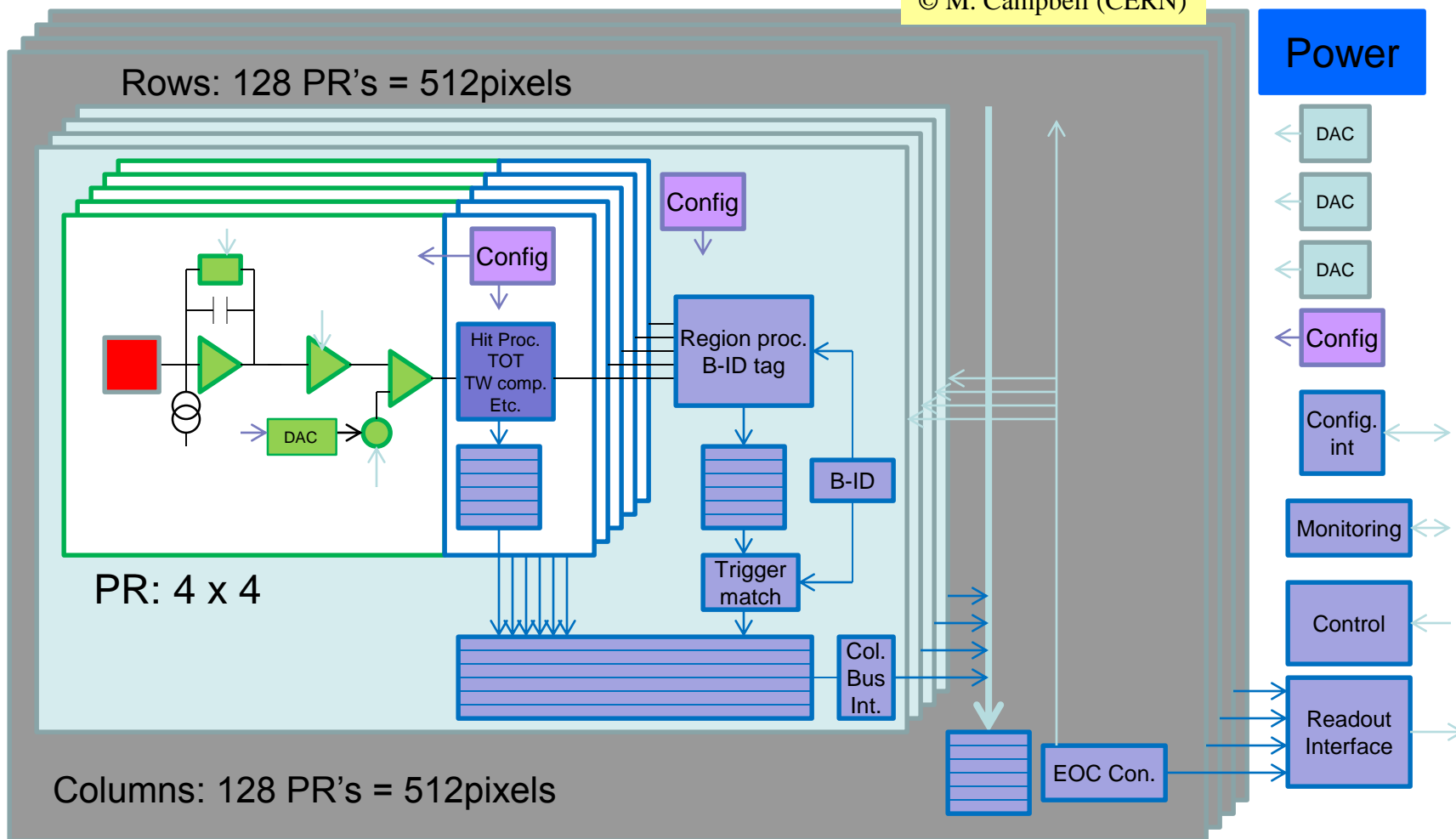
Pinned photodiode:

- 1/10 dark current
- Integration capacitance is small (floating diffusion)
- Correlated-Double-Sampling -> no more kT/C
- Sharing of in-pixel electronics



- 65nm CMOS-CIS, Pinned photodiode:
- Pixel pitch <math><1.1\mu\text{m}</math>
- Global shutter, **DR>80dB**
- Extra pixel-level circuitry (8μm pitch)
- Rolling shutter, **DR>140dB**
- In-pixel Buried SF, High-Gain Column Amplifier and CMS:
- **PN$0.7e$**
- Special Column-level ADCs:UHDTV, **33Mpixel@120fps**

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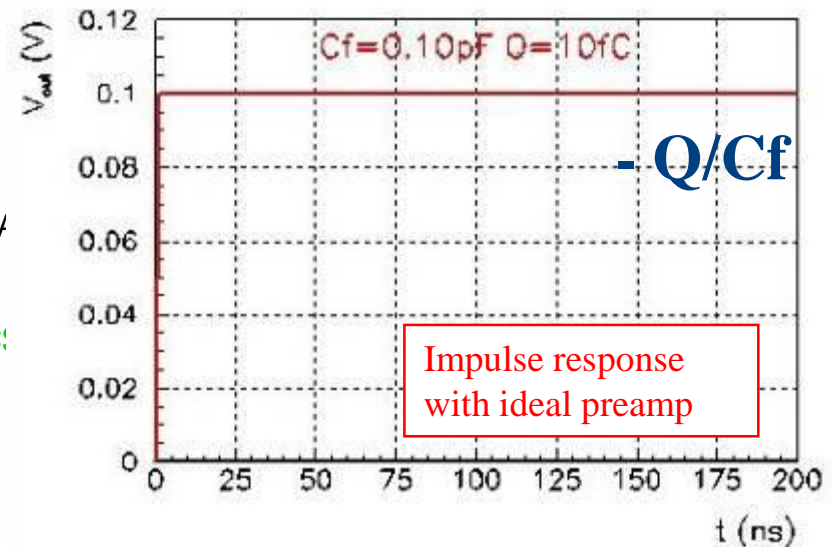
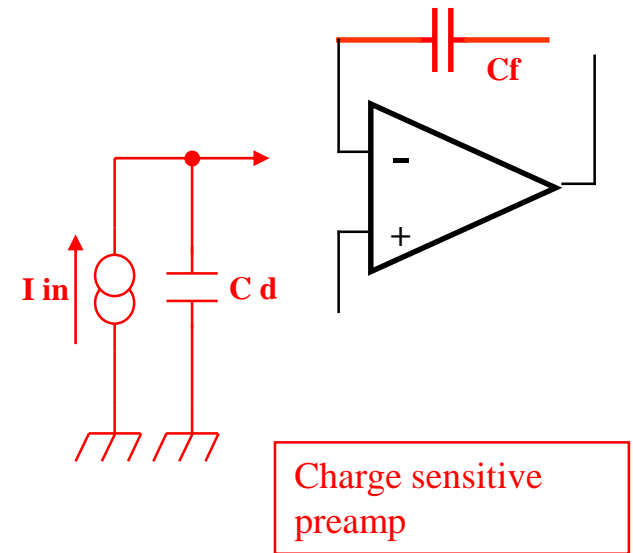
- Pixels: $4 \times 4 \times \sim 128 \times \sim 128 = \sim 256k$ (262144)
- Chip size = $\sim 50\mu m \times 4 \times 128 = \sim 2.6cm \times \sim 3cm$ (Yield maximization required)
- Obviously resembles LHCb/ALICE, FEI4, LHCb Velopix and other high rate pixels
 - And any other data driven (HEP) chip/system: System on a chip

Ideal charge preamplifier

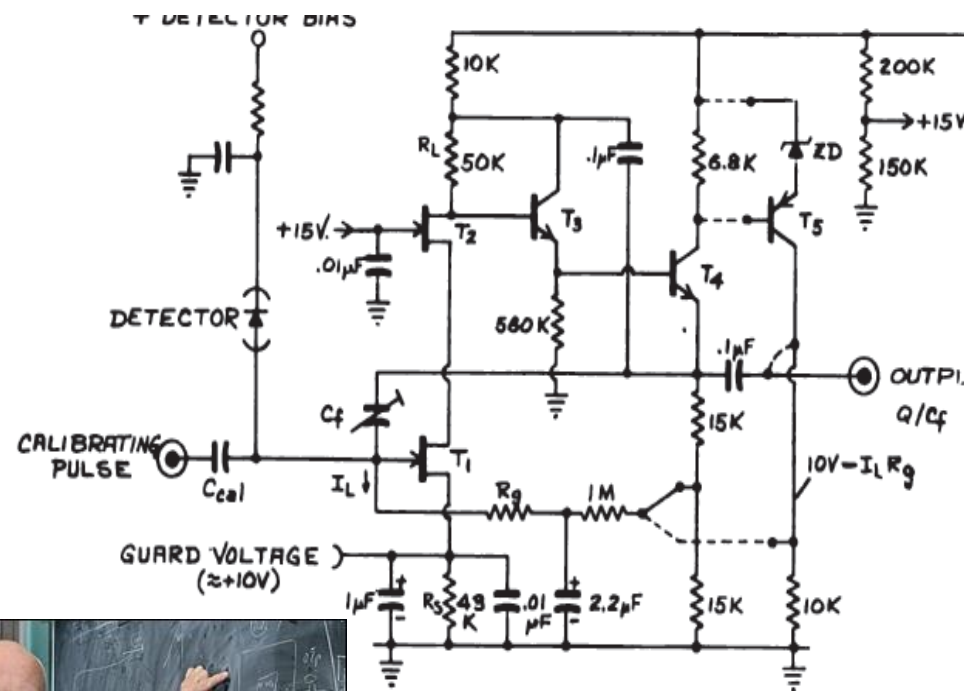
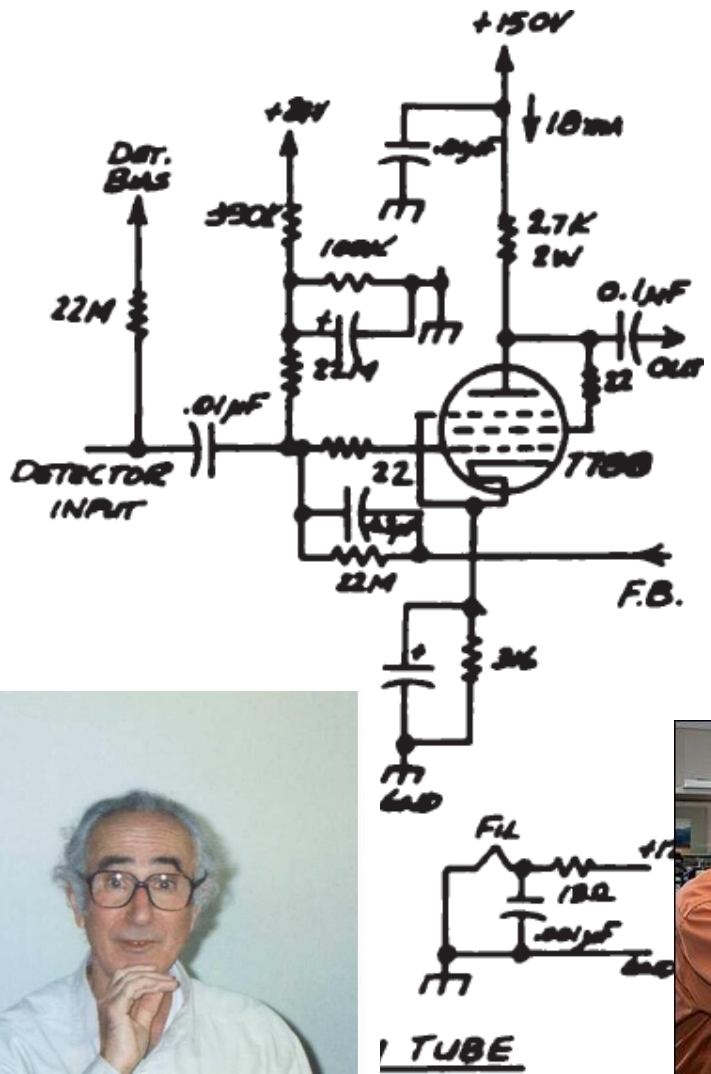
- ideal opamp in transimpedance
 - Shunt-shunt feedback
 - transimpedance : v_{out}/i_{in}
 - $V_{in-}=0 \Rightarrow V_{out}(\omega)/i_{in}(\omega) = -Z_f = -1/j\omega C_f$
 - **Integrator** : $v_{out}(t) = -1/C_f \int i_{in}(t)dt$

$$v_{out}(t) = -Q/C_f$$

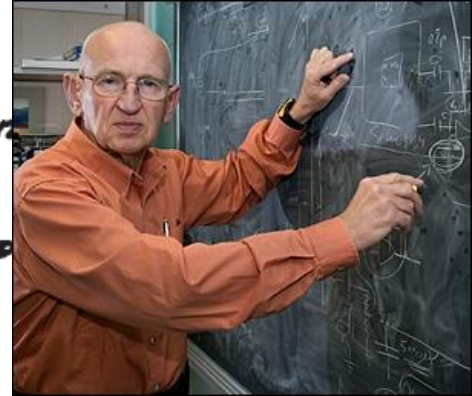
- Integration on C_f
 - Simple : $V = -Q/C_f$
 - Unsensitive to preamp capacitance $C_{P/}$
 - Turns a short signal into a long one
 - **The front-end of 90% of particle physic:**
 - **But always built with custom circuits...**



New developments in charge preamps (1963)



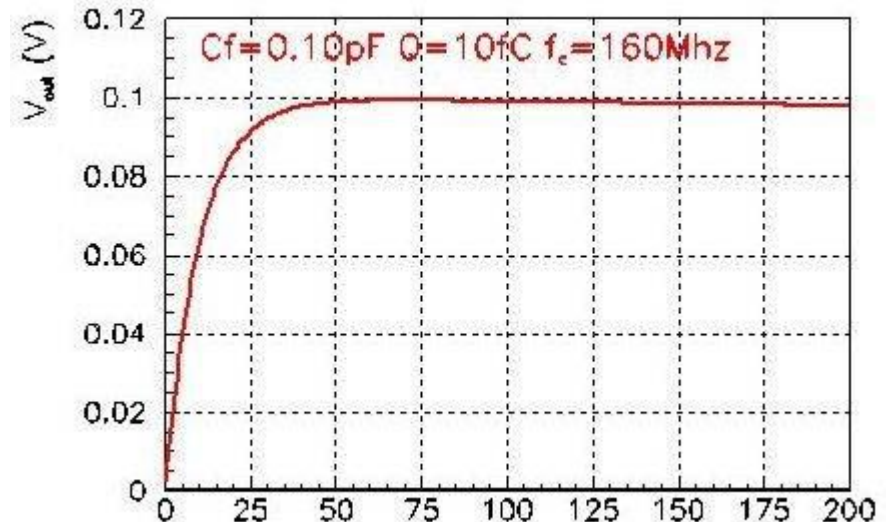
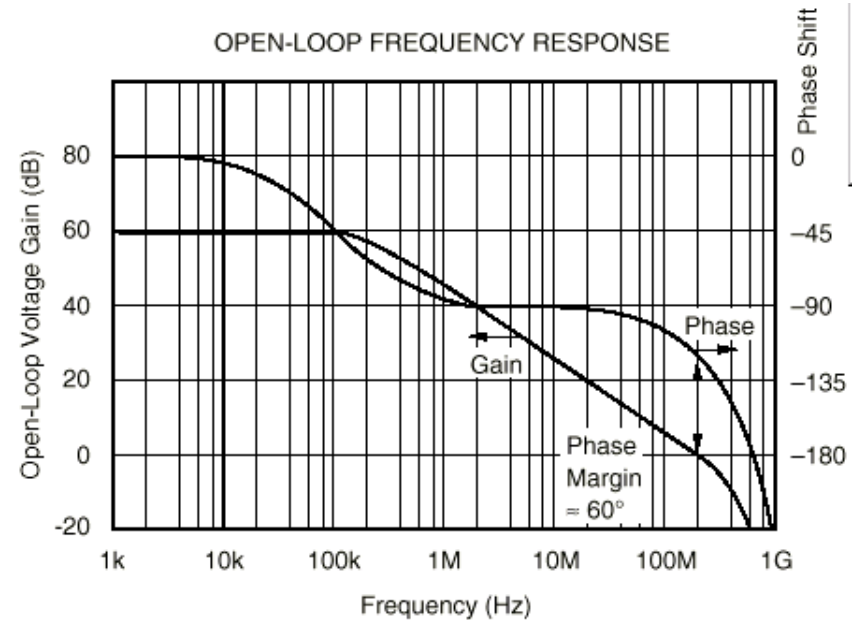
T₁, (T₂) N-CHANNEL FIELD-EFFECT TRANSISTORS FSP401
 (T₂), T₃, T₄ - 2N2252, OR 2N930, OR
 T₅ - 2N274
 ZD - 1N751



Radeka's preamp (Monterrey 63)

Non ideal charge preamp, preamp speed

- Finite opamp gain
 - $V_{out}(\omega)/i_{in}(\omega) = -Z_f / (1 + C_d / G_0 C_f)$
 - Small signal loss in $C_d/G_0 C_f \ll 1$ (ballistic deficit)
- Finite opamp bandwidth
 - First order open-loop gain
 - $G(\omega) = G_0 / (1 + j \omega / \omega_0)$
 - G_0 : low frequency gain
 - $G_0 \omega_0$: gain bandwidth product
- Preamp risetime
 - Due to gain variation with ω
 - Time constant : τ (tau)
 - $\tau = C_d / G_0 \omega_0 C_f$
 - Rise-time : $t_{10-90\%} = 2.2 \tau$
 - Rise-time optimised with w_C or C_f



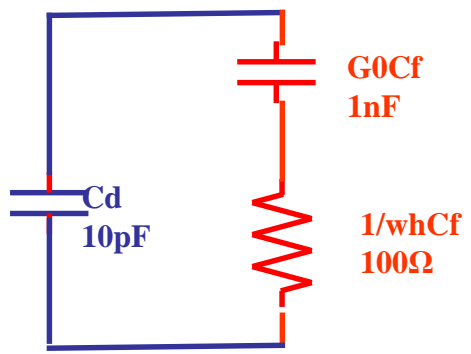
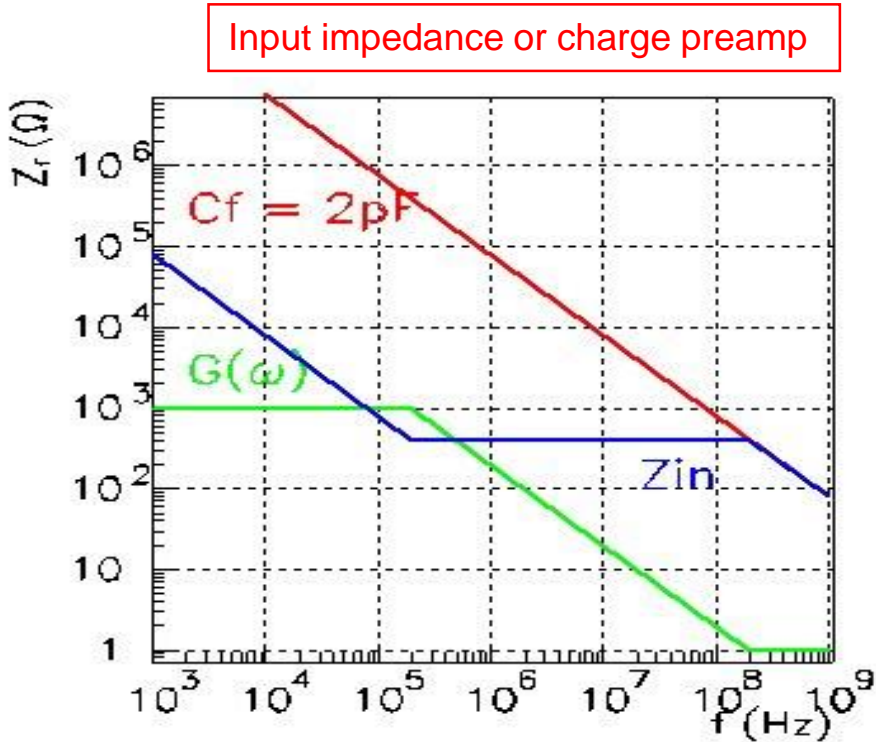
Impulse response with non-ideal preamp

Charge preamp seen from the input

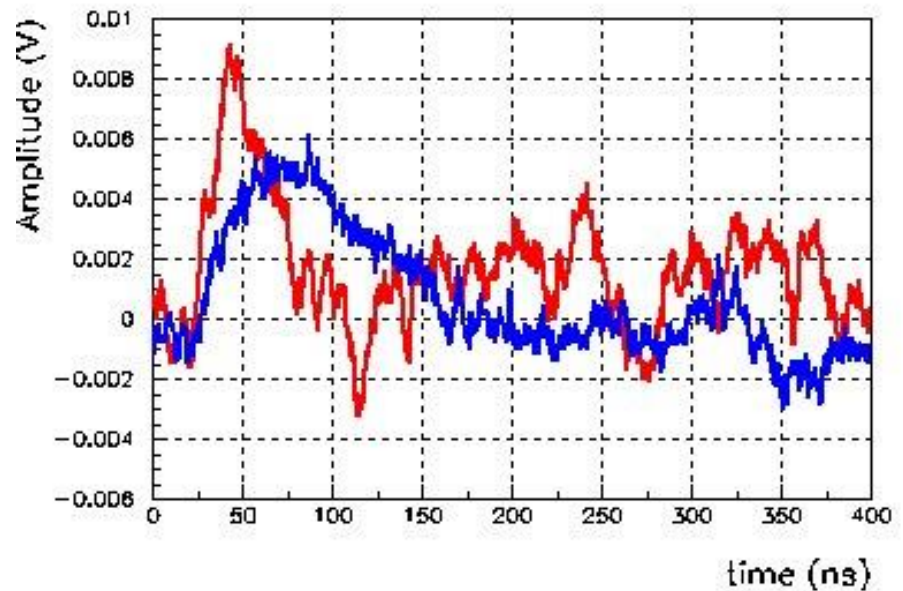


- Input impedance with ideal opamp
 - $Z_{in} = Z_f / G+1$
 - $Z_{in} \rightarrow 0$ for ideal opamp
 - « Virtual ground » : $V_{in} = 0$
 - Minimizes sensitivity to detector impedance
 - Minimizes crosstalk

- Input impedance with real opamp
 - $Z_{in} = 1/j\omega G_0 C_f + 1/ G_0 \omega_0 C_f$
 - Resistive term : $R_{in} = 1/ G_0 \omega_0 C_f$
 - Exemple : $\omega_C = 10^{10}$ rad/s $C_f = 1$ pF $\Rightarrow R_{in} \sim 100 \Omega$
 - Determines the input time constant : $t = R_{eq} C_d$
 - Good stability= (...!)
 - Equivalent circuit :

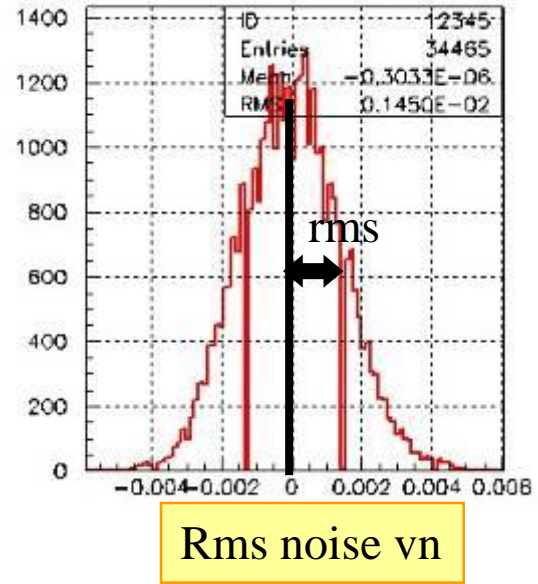
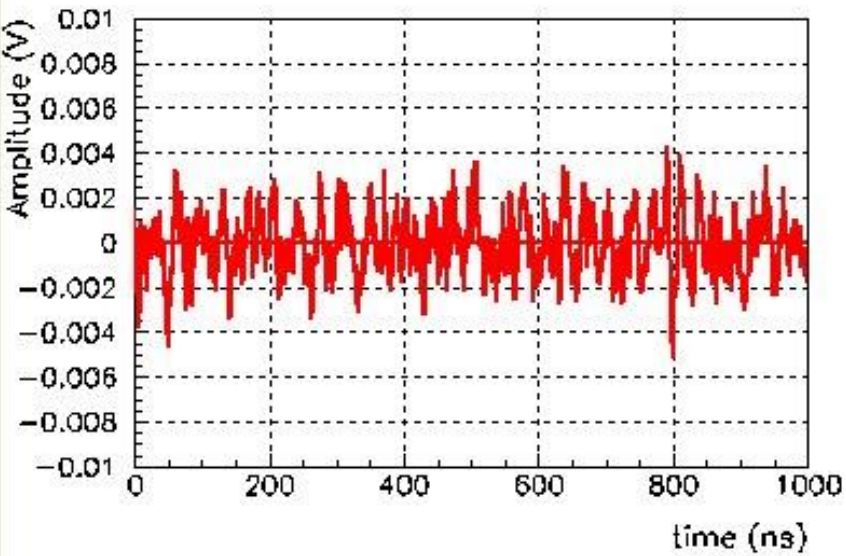
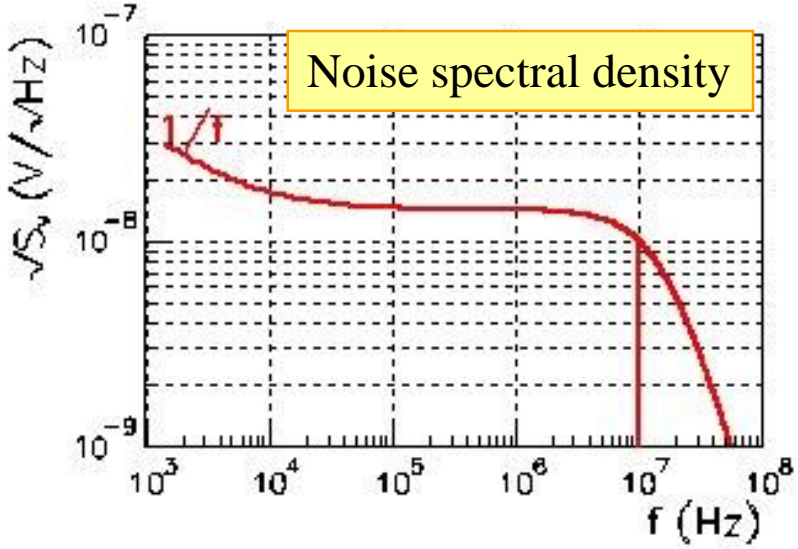


- Definition of Noise
 - Random fluctuation superposed to interesting signal
 - Statistical treatment
- Three types of noise
 - Fundamental noise (Thermal noise, shot noise)
 - Excess noise ($1/f$...)
 - Parasitics -> EMC/EMI (pickup noise, ground loops...)



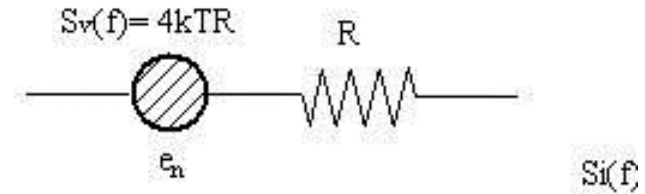
- Modelization
 - Noise generators : $e_n, i_n,$
 - Noise spectral density of e_n & i_n : $S_v(f)$
 - $S_v(f) = | F(e_n) |^2$ (V^2/Hz)

- Rms noise V_n
 - $V_n^2 = \int e_n^2(t) dt = \int S_v(f) df$
 - White noise (e_n) : $v_n = e_n \sqrt{\frac{1}{2}\pi f_{-3dB}}$

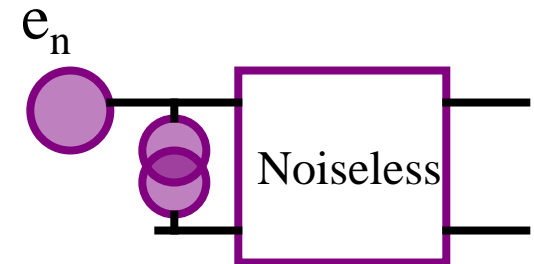
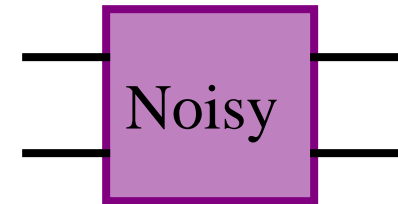


Calculating electronics noise

- Fundamental noise
 - Thermal noise (**resistors**) : $S_v(f) = 4kTR$
 - Shot noise (**junctions**) : $S_i(f) = 2qI$



- Noise referred to the input
 - All noise generators can be referred to the input as **2** noise generators :
 - A voltage one e_n in series : **series noise**
 - A current one i_n in parallel : **parallel noise**
 - Two generators : no more, no less...



■ **To take into account the Source impedance**

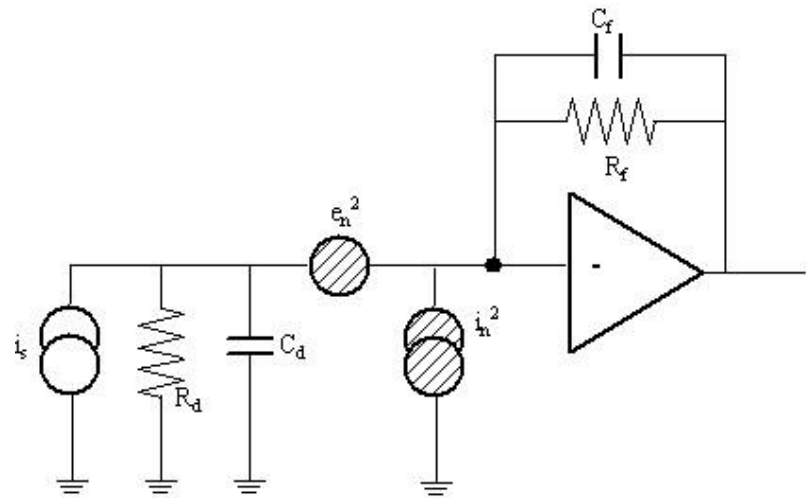
■ **Golden rule :**

- **Always calculate the signal before the noise**
what counts is the signal to noise ratio

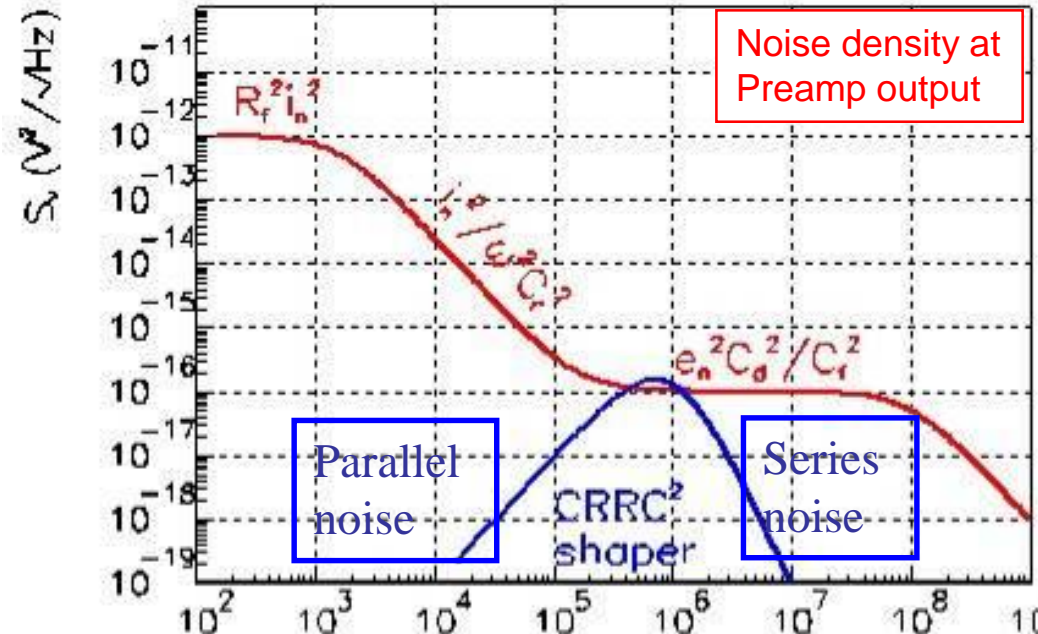
Noise generators referred to the input

Noise in transimpedance amplifiers

- 2 noise generators at the input
 - Parallel noise : (i_n^2) (leakage)
 - Series noise : (e_n^2) (preamp)
- Output noise spectral density :
 - $S_v(\omega) = (i_n^2 + e_n^2/|Z_d|^2) * |Z_f|^2$
- For charge preamps
 - $S_v(\omega) = i_n^2 / \omega^2 C_f^2 + e_n^2 C_d^2 / C_f^2$
 - Parallel noise in $1/\omega^2$
 - Series noise is flat, with a « noise gain » of C_d/C_f
- rms noise V_n
 - $V_n^2 = \int S_v(\omega) d\omega / 2\pi \rightarrow \infty$
 - Benefit of shaping ...



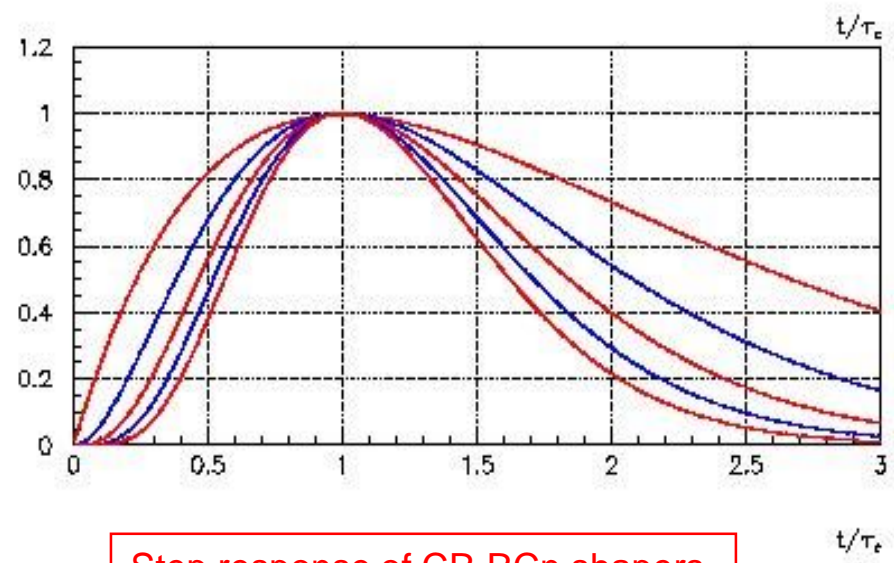
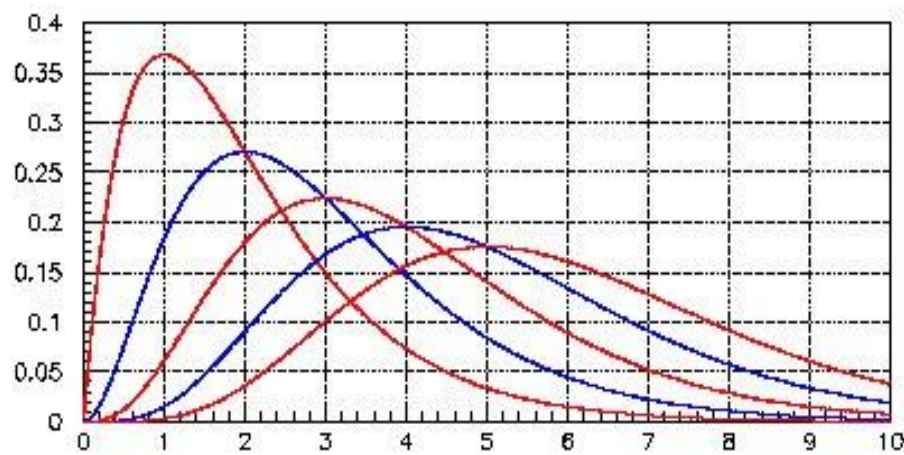
Noise generators in charge preamp



Noise density at Preamp output

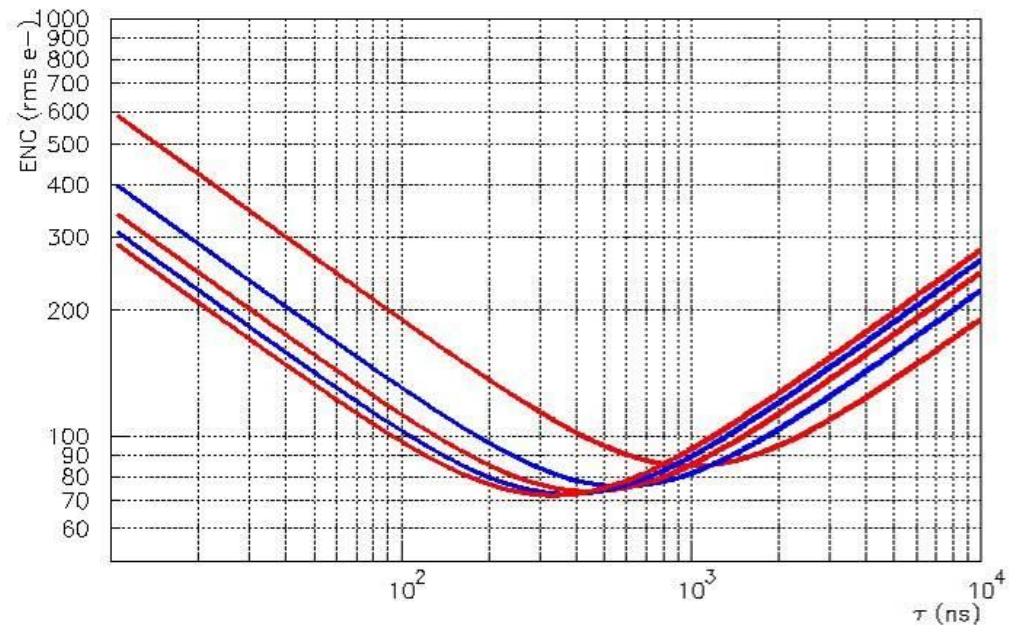
- Noise reduction by optimising useful bandwidth
 - Low-pass filters (**RCⁿ**) to cut-off high frequency noise
 - High-pass filter (**CR**) to cut-off parallel noise
 - -> pass-band filter **CRRCⁿ**

- Equivalent Noise Charge : **ENC**
 - Noise referred to the input in electrons
 - $ENC = I_a(n) e_n C_t \sqrt{T} \oplus I_b(n) i_n^* \sqrt{T}$
 - Series noise in $1/\sqrt{T}$
 - Parallel noise in \sqrt{T}
 - 1/f noise independant of T
 - Optimum shaping time $\tau_{opt} = \tau_c / \sqrt{2n-1}$



Step response of CR RCn shapers

- Peaking time t_p (5-100%)
 - ENC(t_p) independent of n
 - Also includes preamp risetime
- Complex shapers are **obsolete** :
 - Power of **digital filtering**
 - Analog filter = CRRC ou CRRC²
 - antialiasing



ENC vs tau for CR RCⁿ shapers

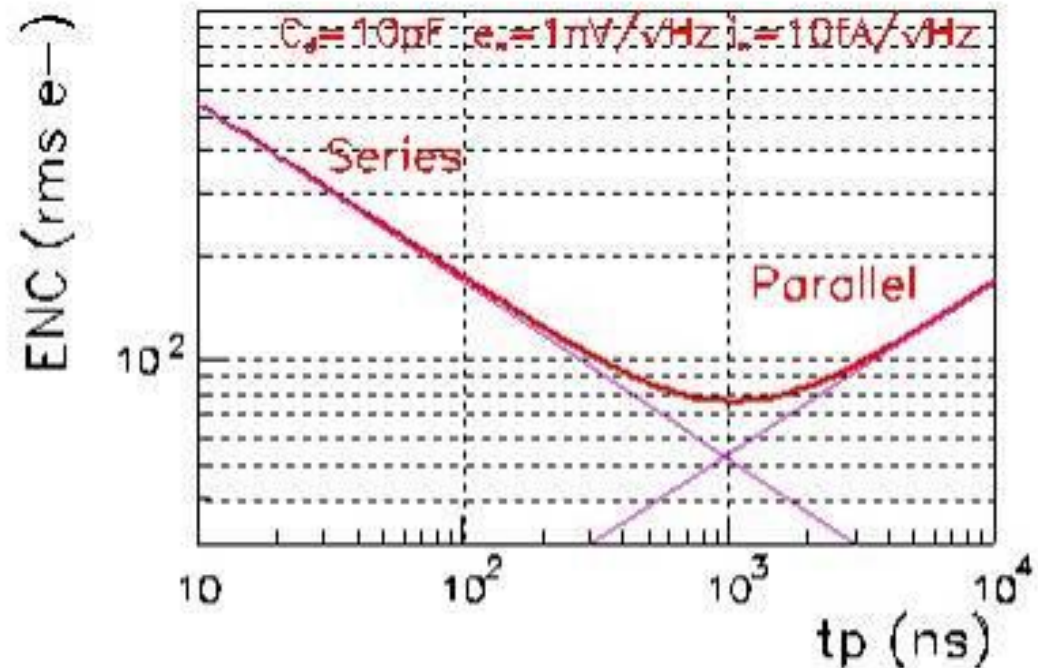
- A useful formula : **ENC (e⁻ rms) after a CRRC² shaper :**

$$\text{ENC} = 174 e_n C_{\text{tot}} / \sqrt{t_p} (\delta) \oplus 166 i_n \sqrt{t_p} (\delta)$$

- e_n in nV/ $\sqrt{\text{Hz}}$, i_n in pA/ $\sqrt{\text{Hz}}$ are the **preamp** noise spectral densities
- C_{tot} (in pF) is dominated by the detector (C_d) + input preamp capacitance (C_{PA})
- t_p (in ns) is the shaper peaking time (5-100%)

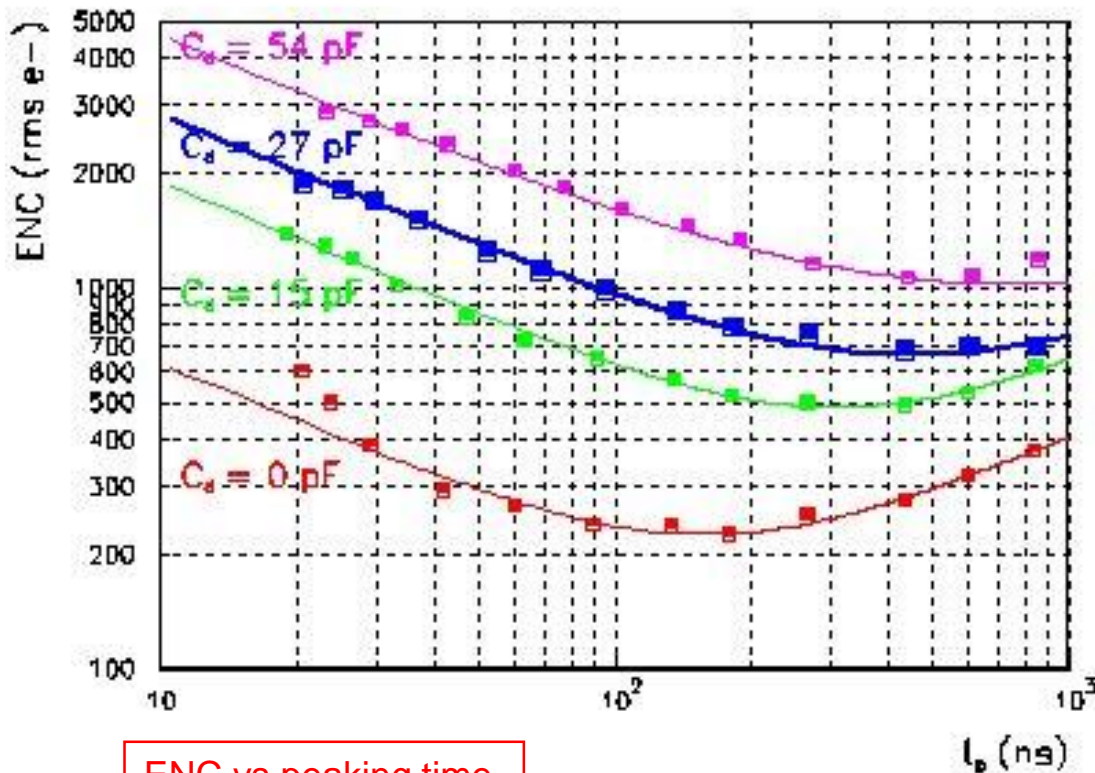
■ Noise minimization

- Minimize source capacitance
- Operate at optimum shaping time
- Preamp series noise (e_n) best with high transconductance (g_m) in input transistor
=> large current, optimal size

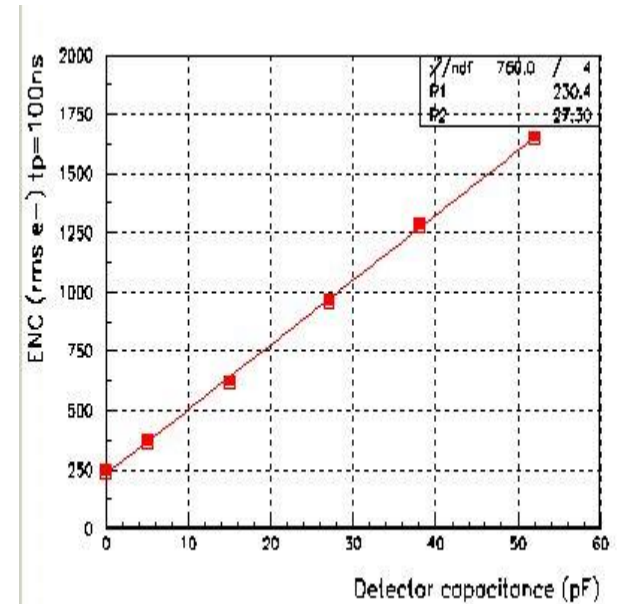


Example of ENC measurement

- 2000/0.35 PMOS 0.35 μ m SiGe $I_d=500 \mu$ A
 - Series : $e_n = 1.4 \text{ nV}/\sqrt{\text{Hz}}$, $C_{PA} = 7 \text{ pF}$
 - 1/f noise : 12 e-/pF
 - Parallel : $i_n = 40 \text{ fA}/\sqrt{\text{Hz}}$

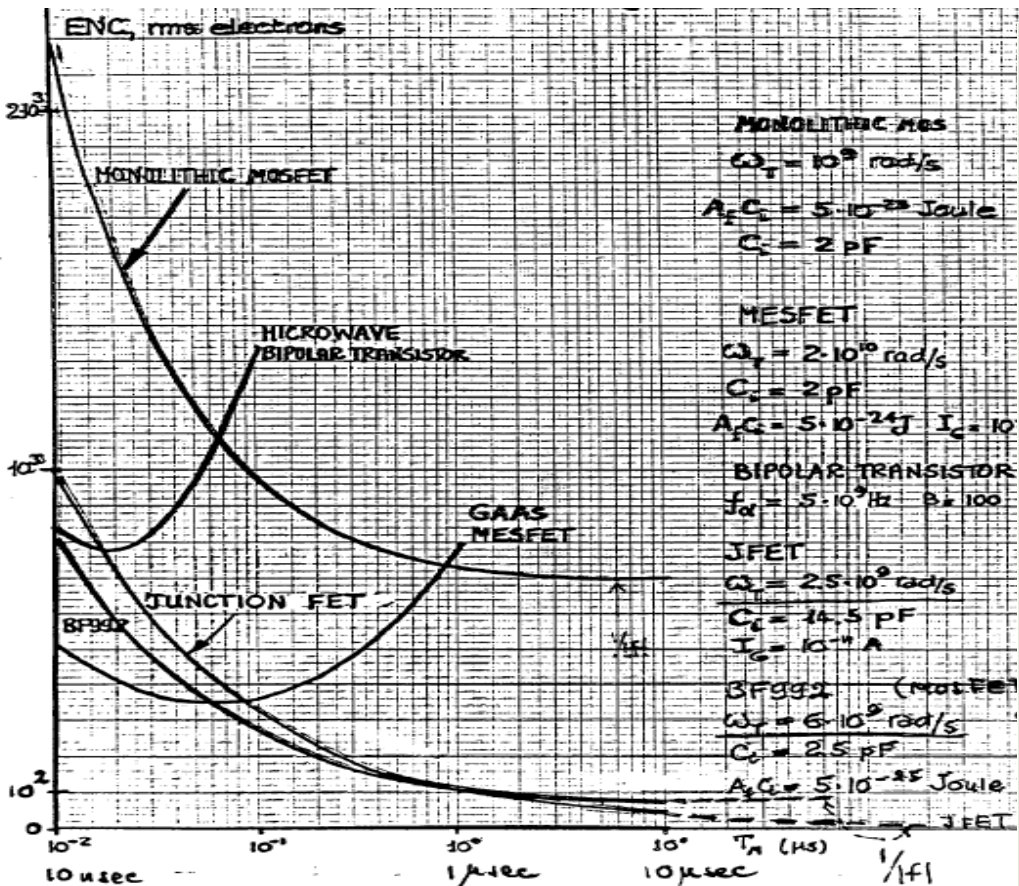


ENC vs peaking time



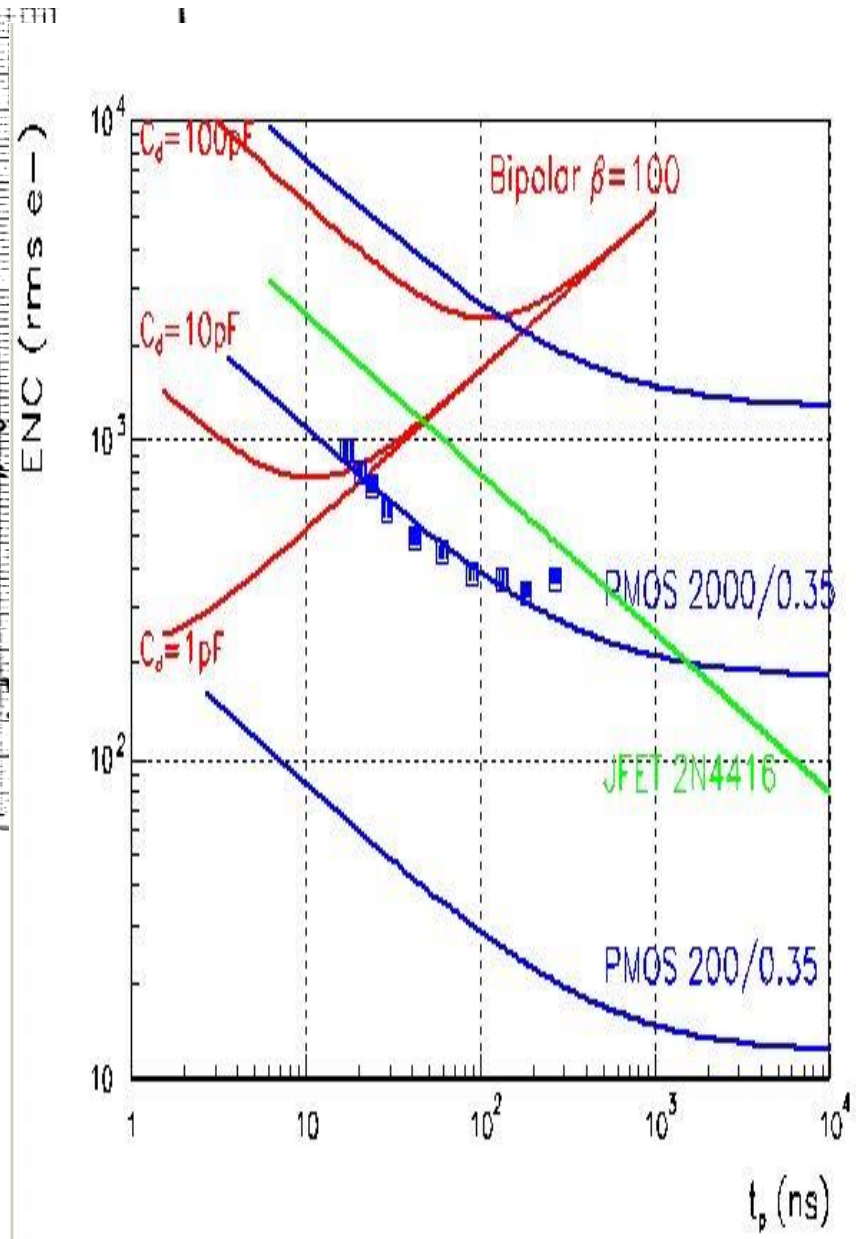
ENC vs Capacitance $t_p=100\text{ns}$

ENC for various technologies



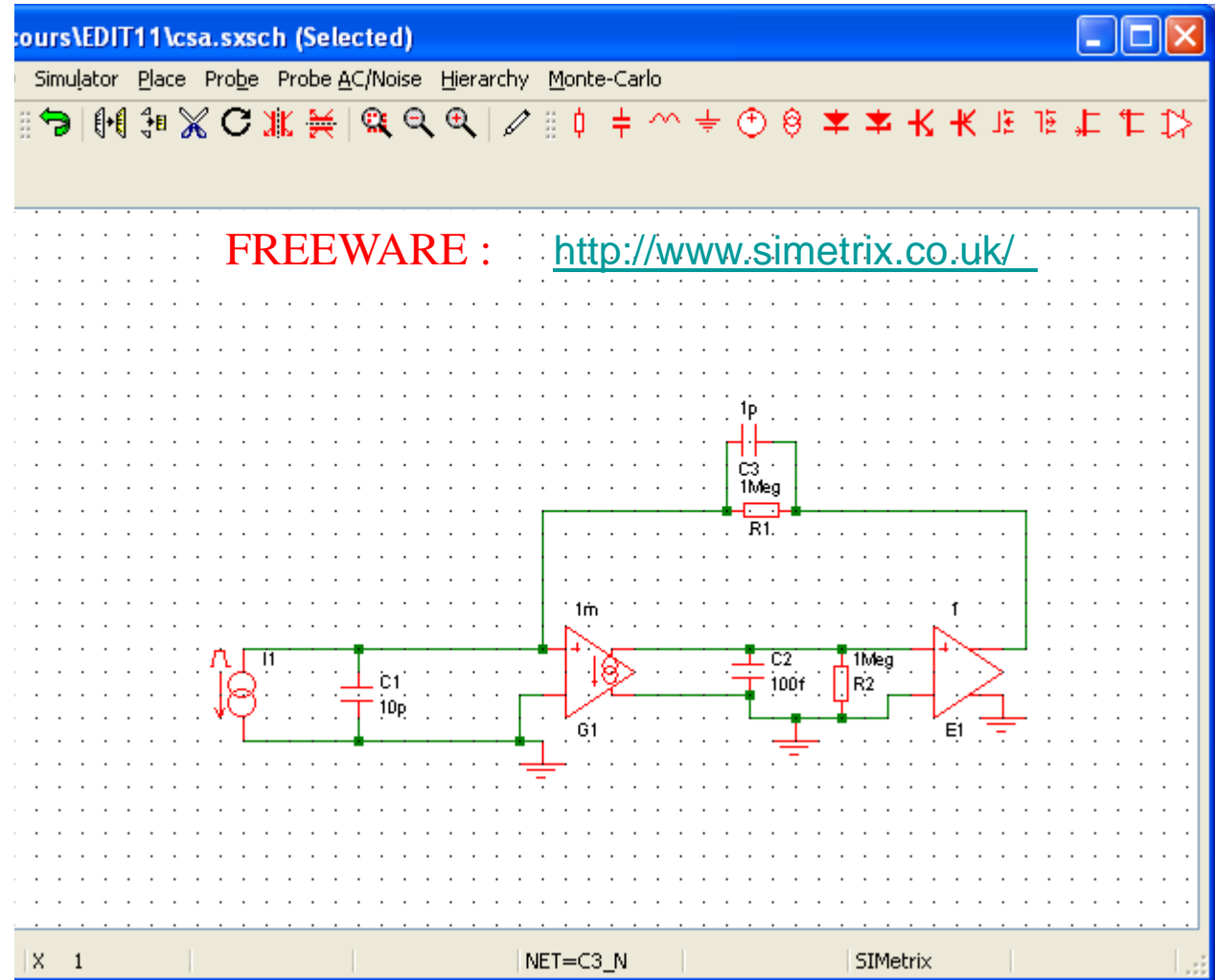
- 24 -

From:



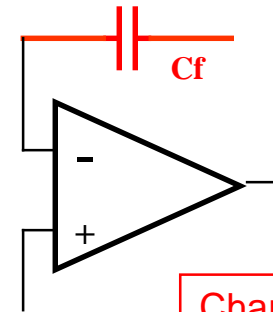
Example : bandwidth and EMC of simple charge preamp

- Simulate impulse response
- Frequency response
- Input impedance
- Ballistic deficit
- Effect of amplifier gain
- Effect of resistive feedback
- Test pulse injection
- Effect of input capacitance
- **Parasitic inductance**
- **Capacitive crosstalk**
- **Resistive/Inductive ground return**

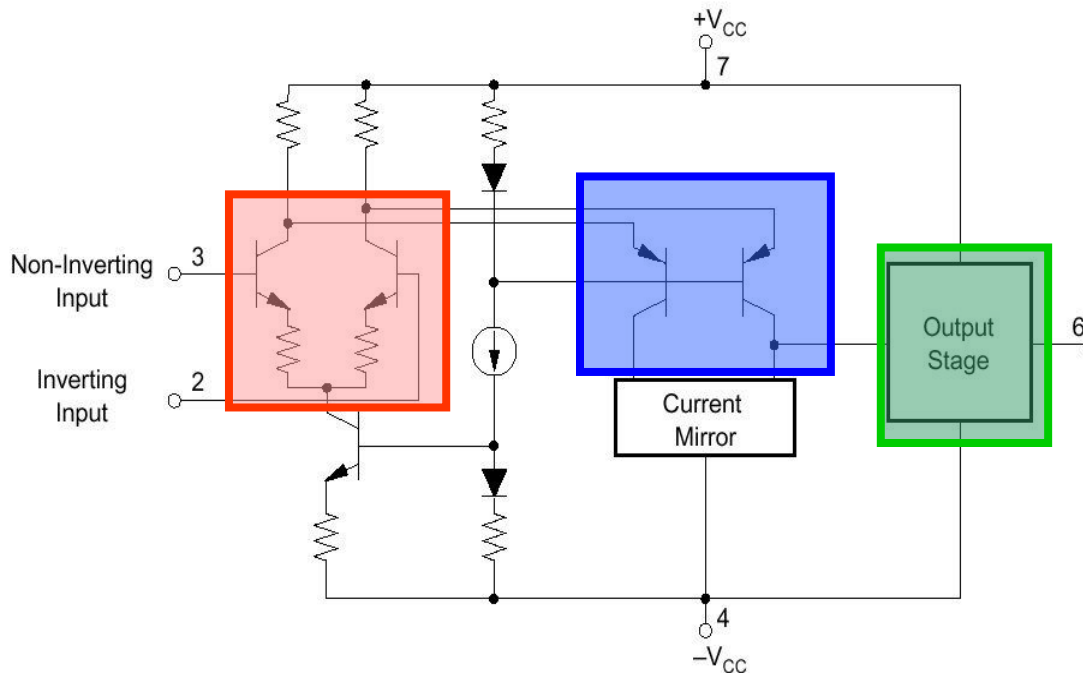


Designing a charge preamp...

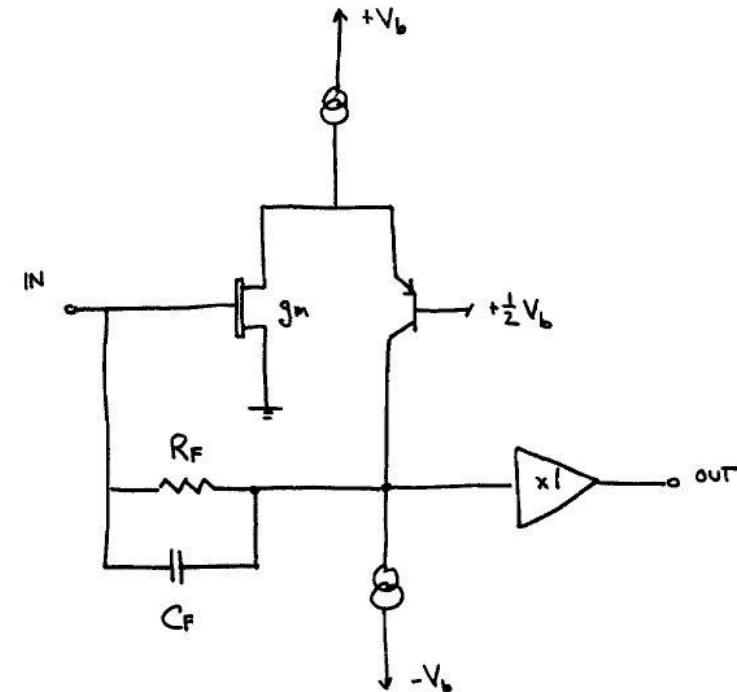
- From the schematic of principle
 - Using of a fast opamp (OP620)
 - Removing unnecessary components...
 - Similar to the traditional schematic «Radeka 68 »
 - Optimising transistors and currents



Charge preamp



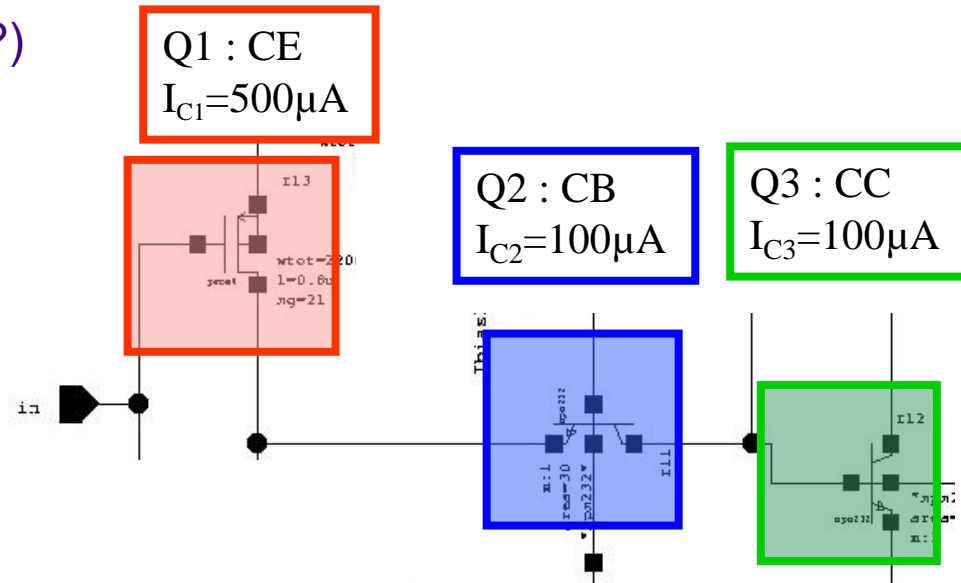
Schematic of a OP620 opamp ©BurrBrown



Charge preamp ©Radeka 68

Example : designing a charge preamp (2)

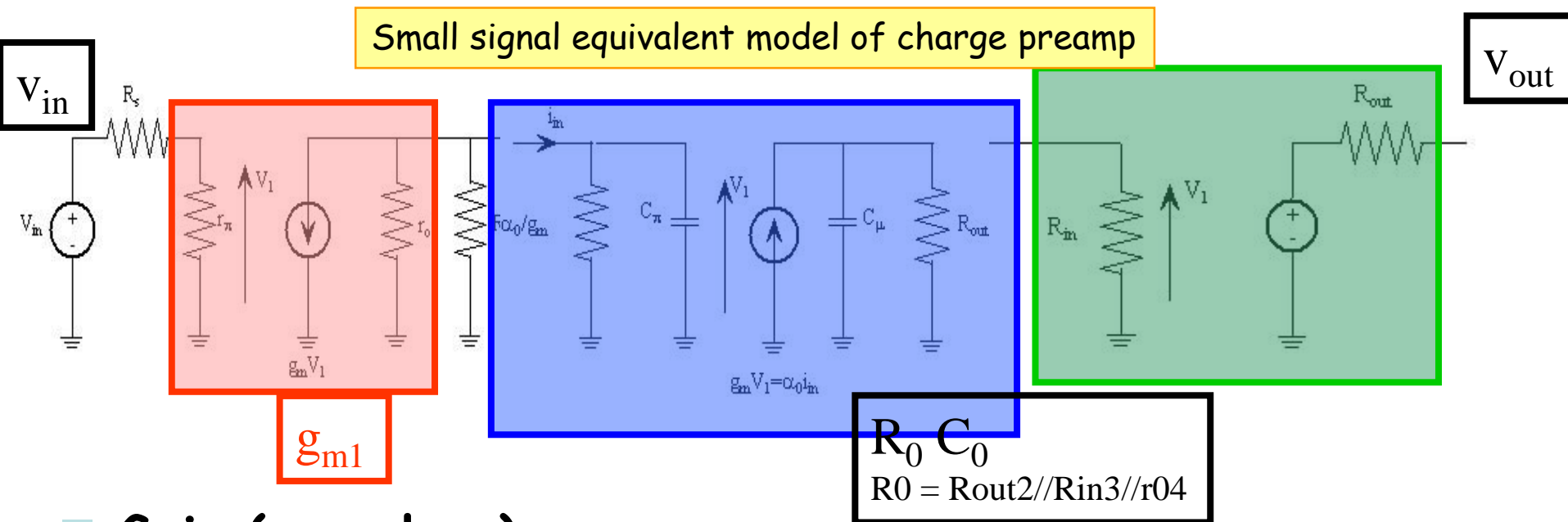
- Simplified schematic
- Optimising components
 - What transistors (PMOS, NPN ?)
 - What bias current ?
 - What transistor size ?
 - What is the noise contribution of each component ?
 - how to minimize it ?
 - What parameters determine the stability ?
 - What is the saturation behaviour
 - How vary signal and noise with input capacitance ?
 - How to maximise the output voltage swing ?
 - What is the sensitivity to power supplies, temperature...



Simplified schematic of Charge preamp

Example : designing a charge preamp (3)

- Small signal equivalent model
 - Transistors are replaced by hybrid π model
 - Allows to calculate open loop gain



■ Gain (open loop) :

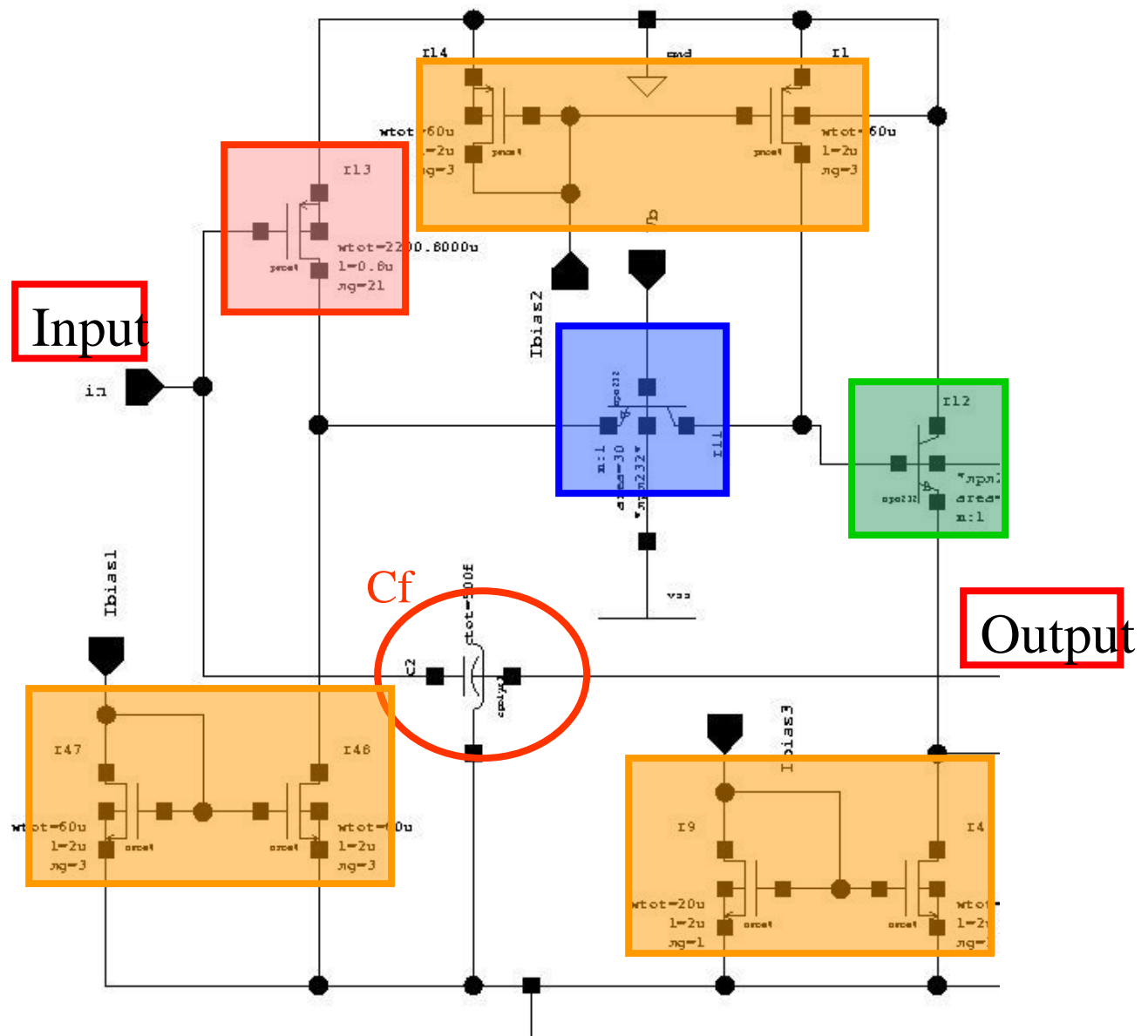
$$v_{out}/v_{in} = -g_{m1} R_0 / (1 + j\omega R_0 C_0)$$

- Ex : $g_{m1} = 20 \text{ mA/V}$, $R_0 = 500 \text{ k}\Omega$, $C_0 = 1 \text{ pF} \Rightarrow G_0 = 10^4$ $\omega_0 = 210^6$ $G_0 \omega_0 = 2 \cdot 10^{10} = 3 \text{ GHz}!$

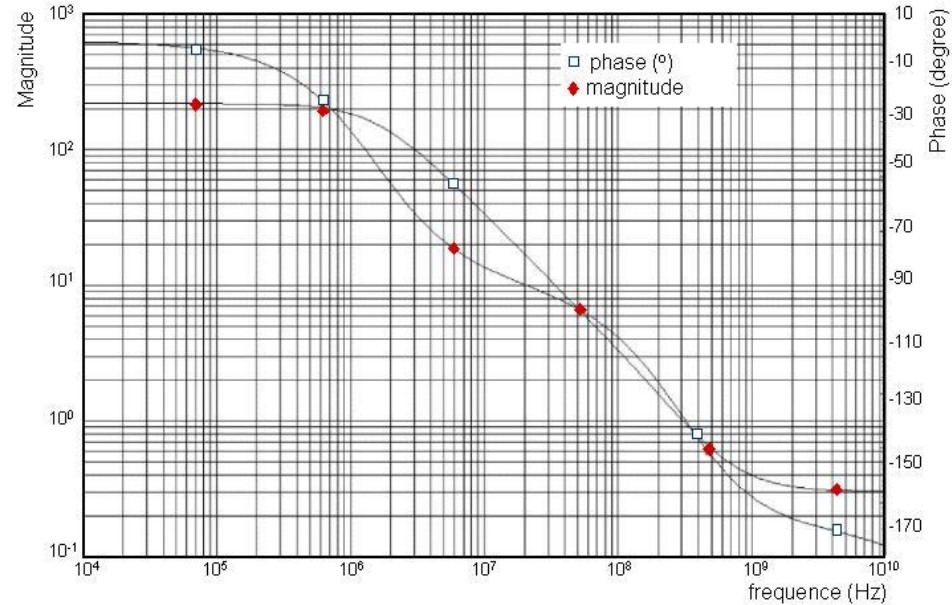
Example : designing a charge preamp (4)



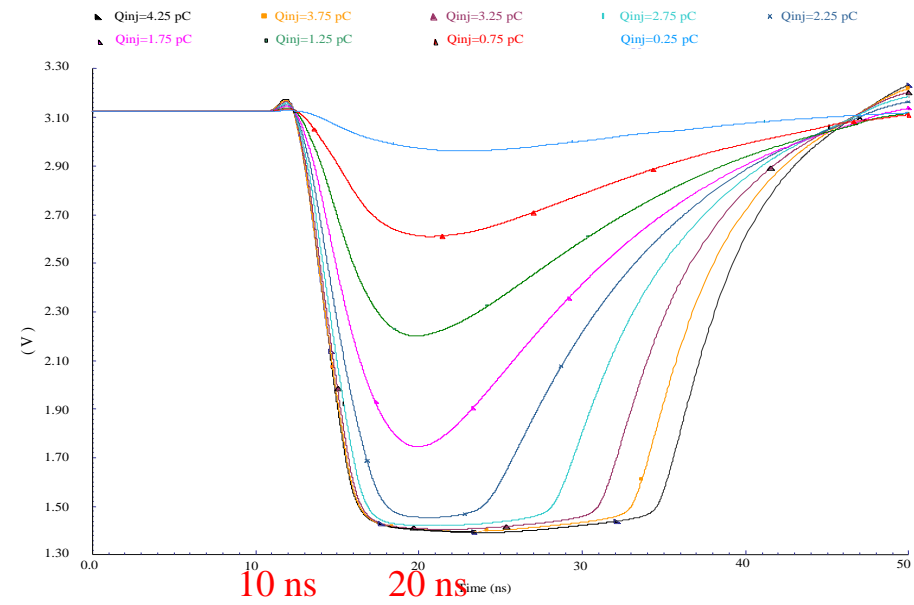
- Complete schematic
 - Adding bias elements



- Complete simulation
 - Checking hand calculations against 2nd order effects
 - Testing extreme process parameters (« corner simulations »)
 - Testing robustness (to power supplies, temperature...)

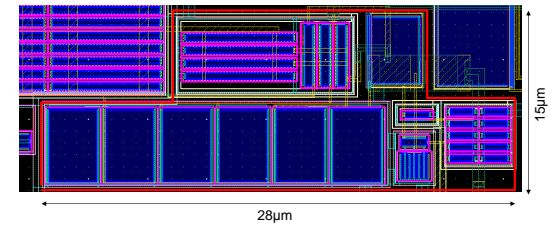


Simulated open loop gain

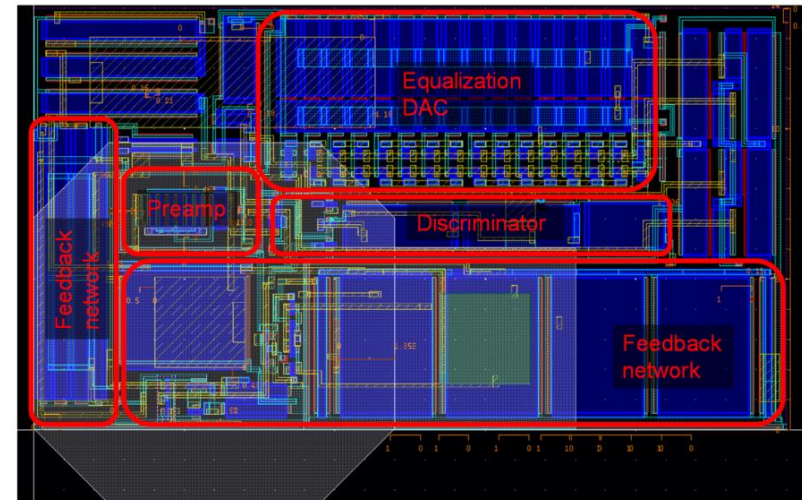


Saturation behaviour

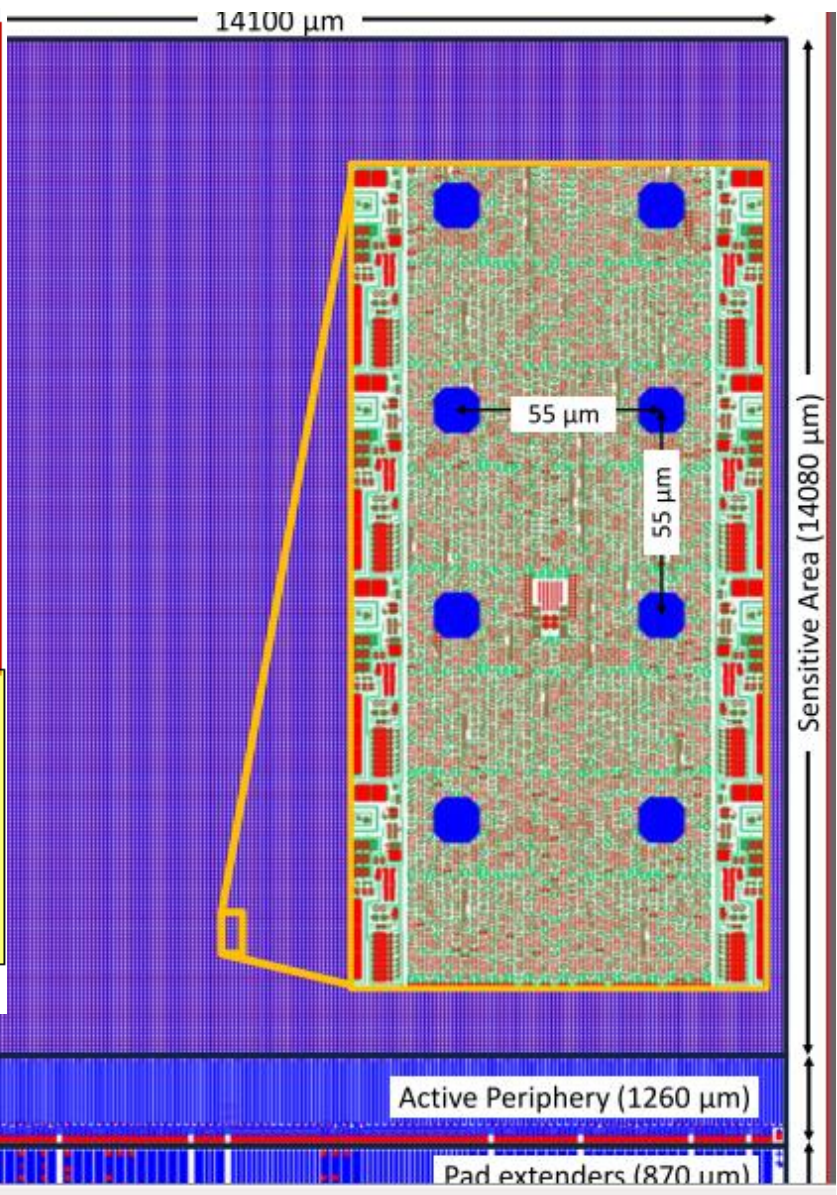
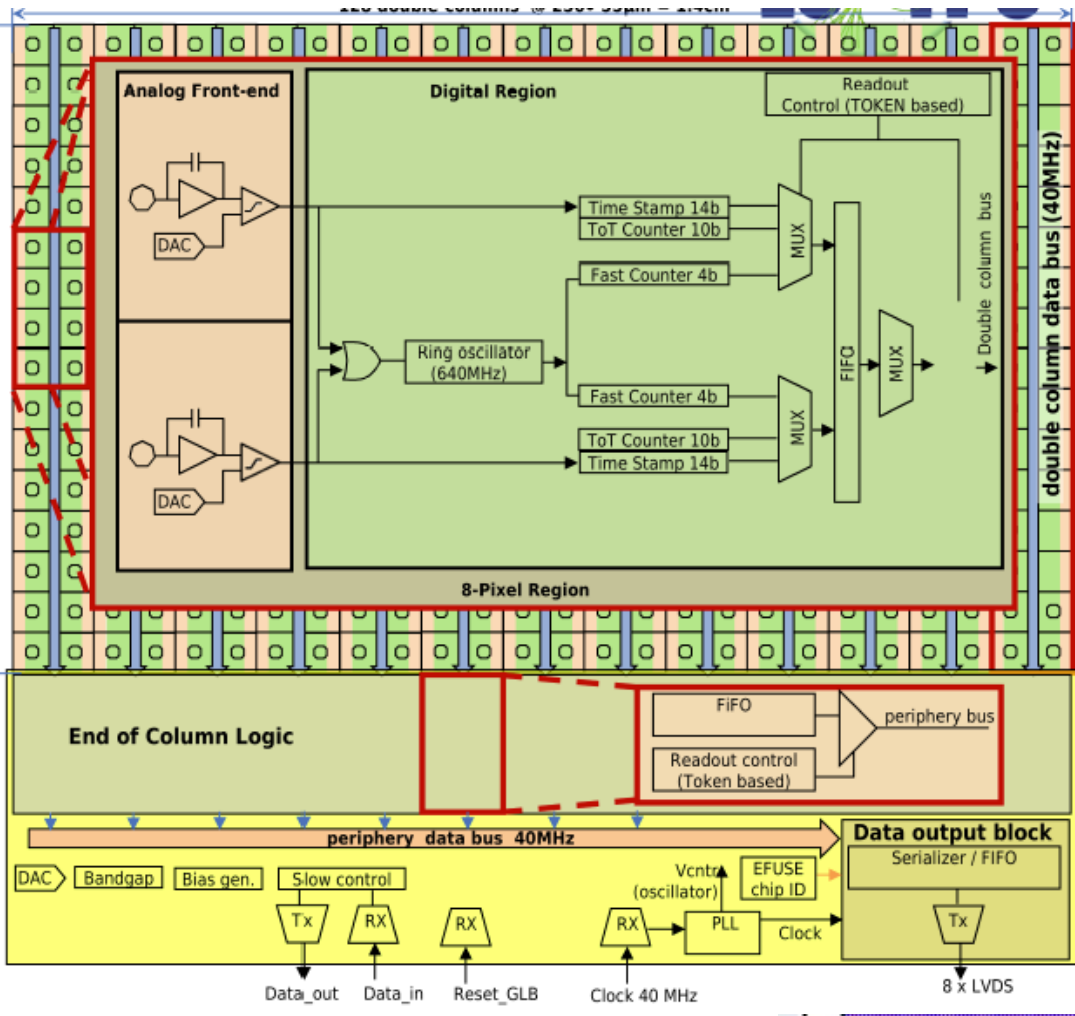
- Layout
 - Each component is drawn
 - They are interconnected by metal layers
- Checks
 - DRC : checking drawing rules (isolation, minimal dimensions...)
 - ERC : extracting the corresponding electrical schematic
 - LVS (layout vs schematic) : comparing extracted schematic and original design
 - Simulating extracted schematic with parasitic elements
- Generating GDS2 file
 - Fabrication masks : « reticule »



Charge preamp in 65nm
Clicpix P. Valerio (CERN 2013)



From preamp to chip : Timepix 3...



Medipix1 (1998)

*1 μ m SACMOS, 64x64 pixels, 170x170 μ m²
PC / Frame based readout*

Medipix2 (2001)

*0.25 μ m CMOS, 256x256 pixels, 55x55 μ m²
PC / Frame based readout*

Timepix (2006)

*0.25 μ m CMOS, 256x256 pixels, 55x55 μ m²
PC, ToT, ToA / Frame based readout*

Medipix3 (2009)

*0.13 μ m CMOS, 256x256 pixels, 55x55 μ m²
PC / Frame based readout
Event by event charge reconstruction and allocation*

Dosepix (2011)

*0.13 μ m CMOS, 16x16 pixels, 220x220 μ m²
ToT, PC / Rolling shutter (programmable column readout)
Event by event binning of energy spectra (16 digital thrs)*

Timepix3 (2013)

*0.13 μ m CMOS, 256x256 pixels, 55x55 μ m²
PC; ToT, ToA (simultaneous)/ Data driven readout*

Velopix

*0.13 μ m CMOS, 256x256 pixels, 55x55 μ m²,
ToA, Binary/ToT (TBD), Data driven readout*

Smallpix

*0.13 μ m CMOS, 512x512 pixels, 40x40 μ m² (TBD), TSV compatible
PC, iTOT; ToA, ToT1 (simultaneous)/ Frame based (ZC)*

Clicpix prototype (2013)

*65nm CMOS, 64x64 pixels, 25x25 μ m²
ToA, ToT1 (simultaneous)/ Frame based (ZC)*


```
process(Rstb, Clk)
begin
  if Rstb = '0' then
    Q <= '0';
  elsif rising_edge Clk then
    Q <= D;
  end if;
end process;
```

Architecture Design

High Level Synthesis

Synthesis

Verification

RTL

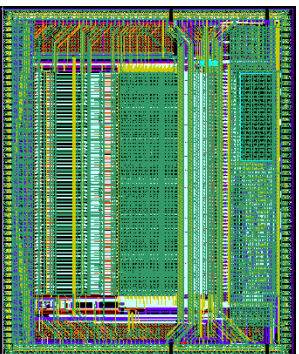
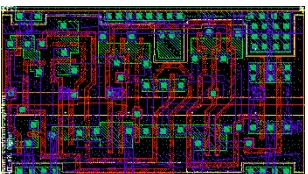
Placement

Extraction and Timing Verification

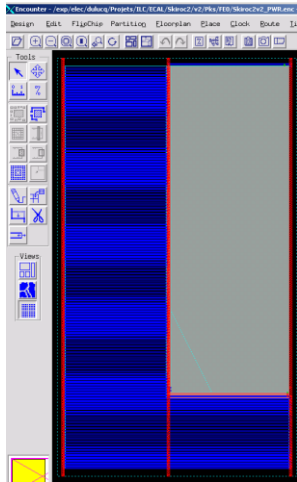
Routing

GDSII

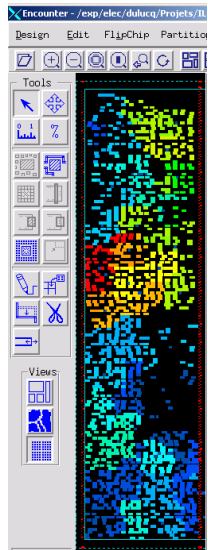
Manufacturing



Skiroc2 power planning



Skiroc2 clock tree



IO Pad Placement

Power planning
(Stripes & rings)

Global Placement

DFT (scan chains)

Clock Tree Synthesis

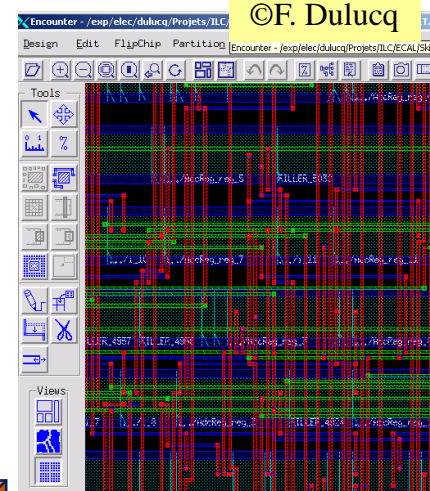
Global Routing

LVS / DRC
Specific Analysis (IR, Antennas)

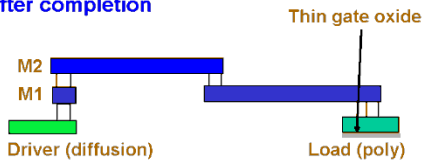
GDS2

(M1, M2, M3) =
(blue, red, green)

Extraction and
Delay Calc. Timing
Verification

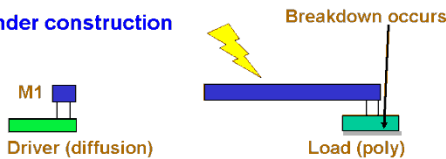


(a) After completion



Antennas fixing

(b) Under construction



Pentium4

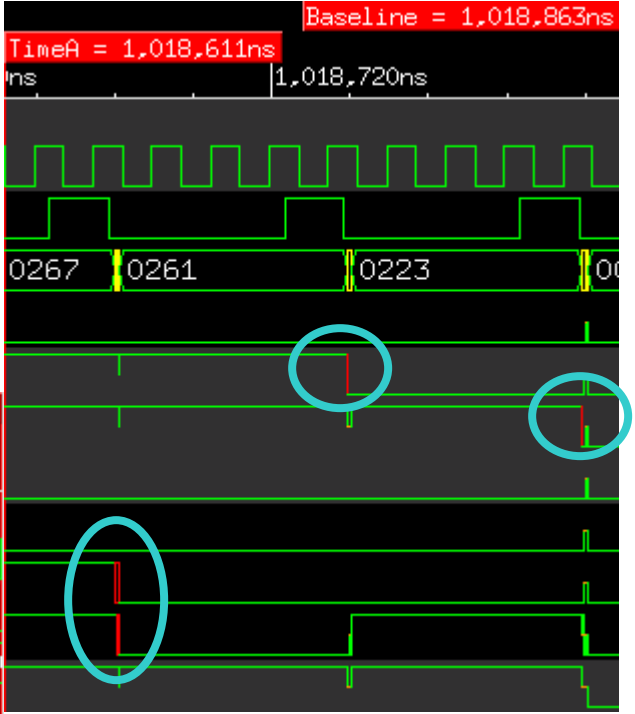
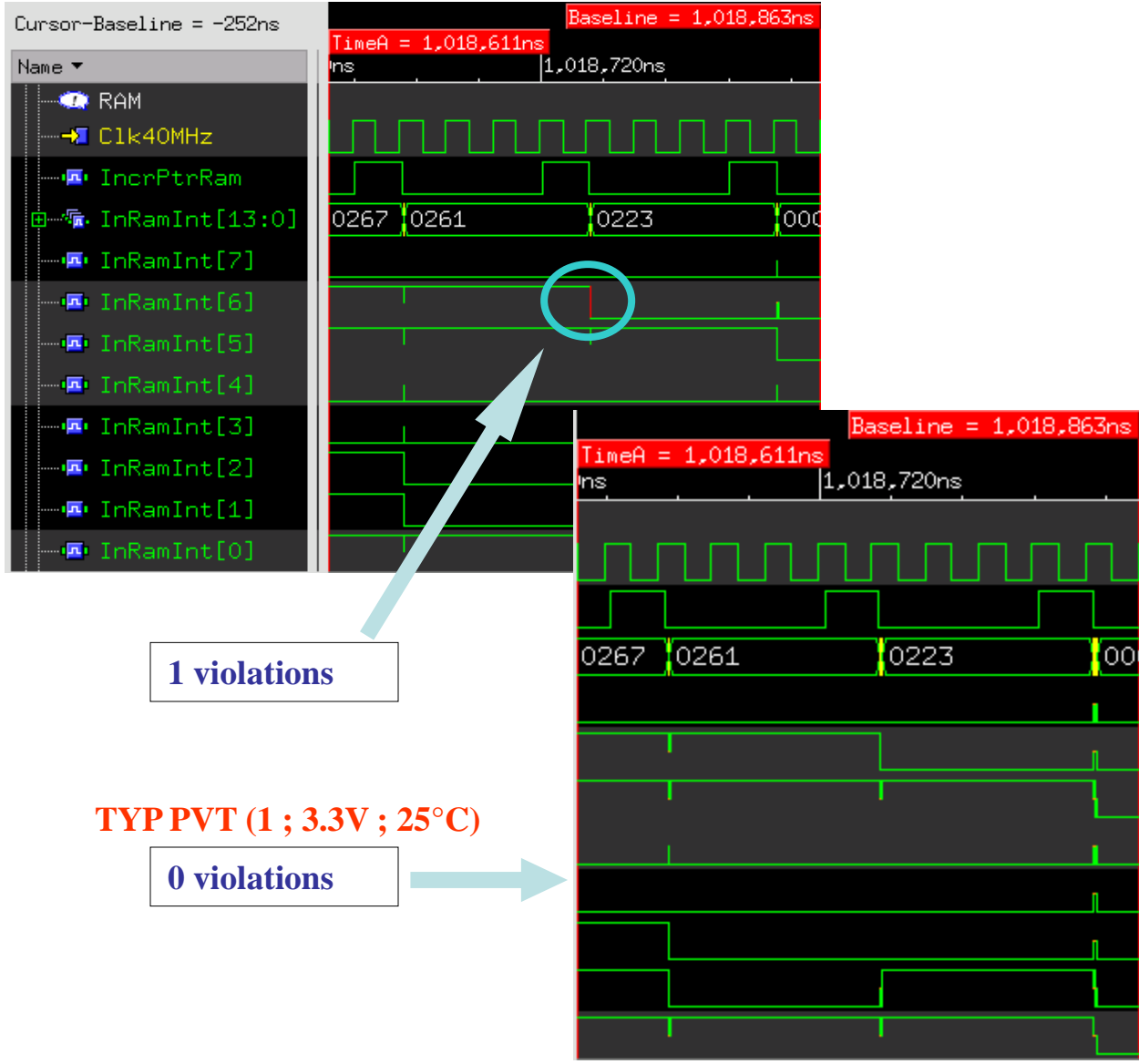
EDIT school

Parisroc2 IR drop Analysis
(red = drop > 5mV)



MIN PVT (1.6 ; 3.6V ; -50°C)

MAX PVT (1.4 ; 3V ; 125°C)



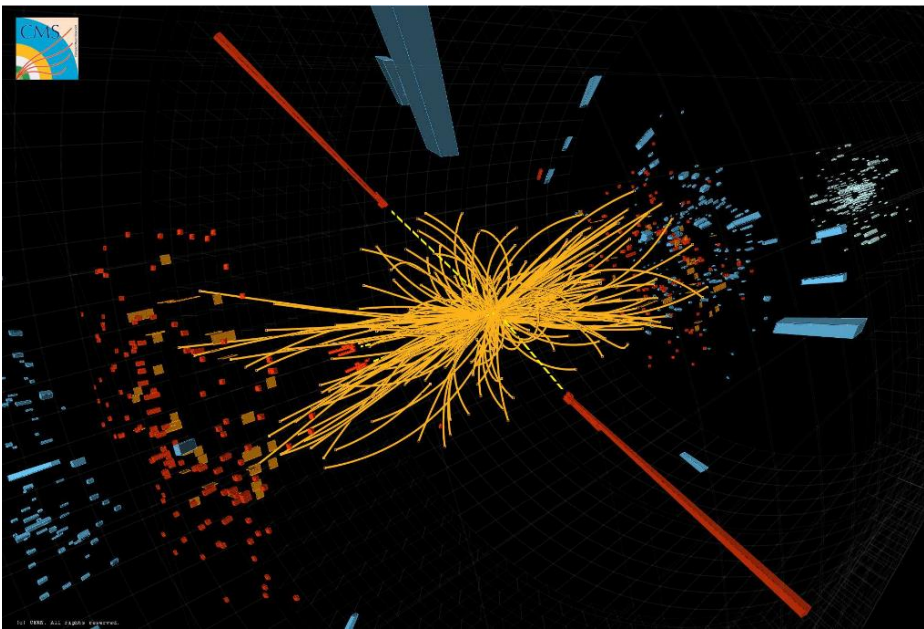
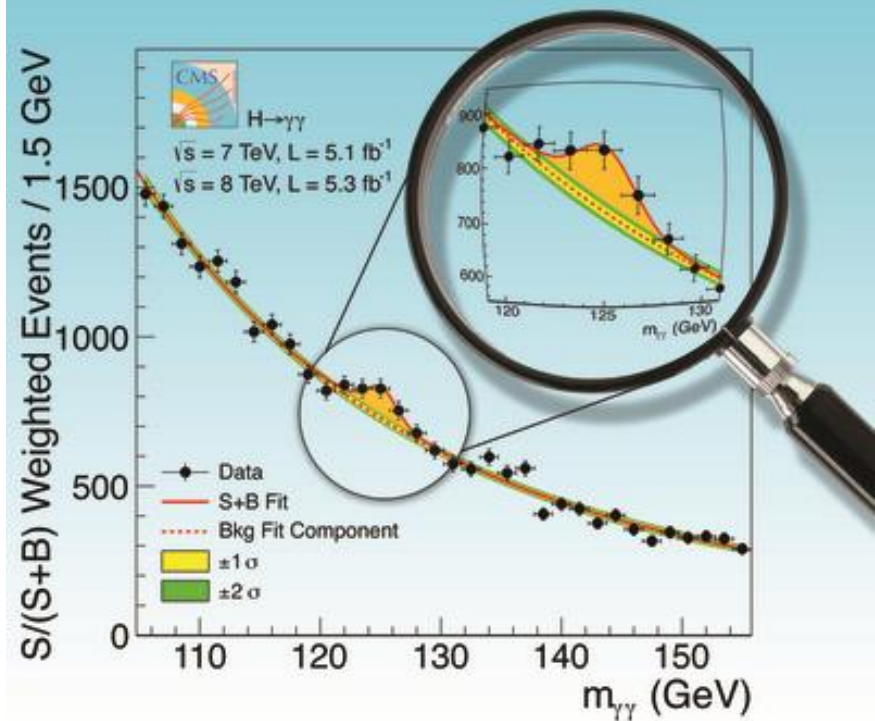
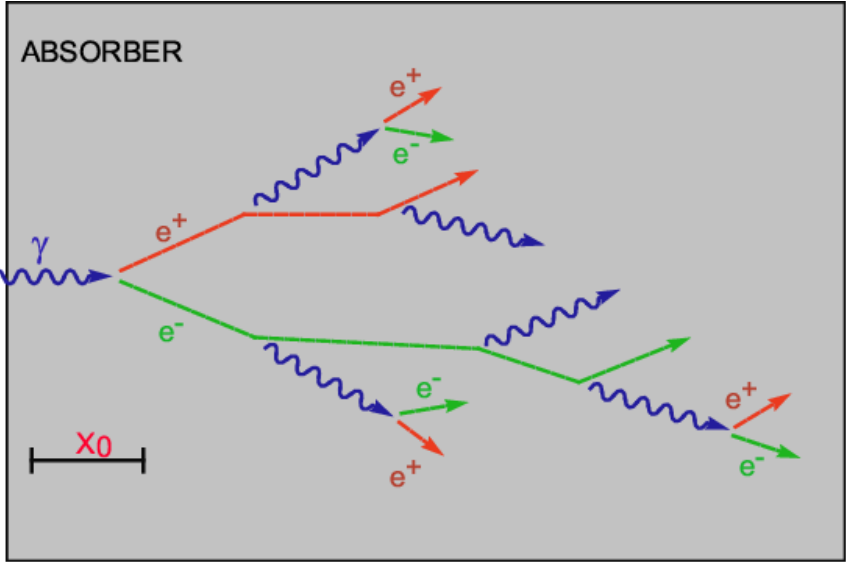
- Coexistence analog-digital
 - Capacitive, inductive and common-impedance couplings
 - A full lecture !
 - A good summary : there is no such thing as « ground », pay attention to current return



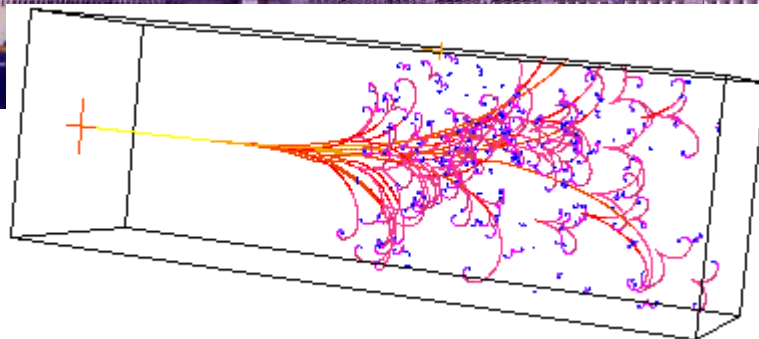
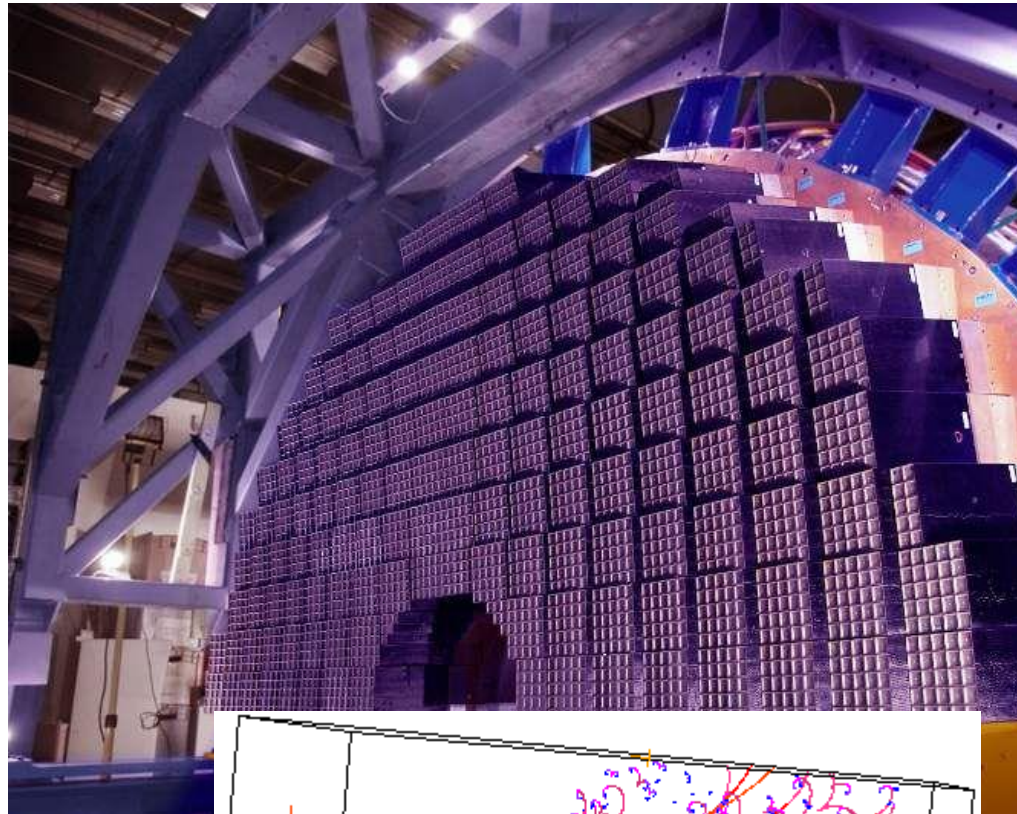
Calorimeters

- Large dynamic range (10^4 - 10^5)
- High Precision $\sim 1\%$
 - Importance of low noise, uniformity, linearity...
 - Importance of calibration

H \rightarrow $\gamma\gamma$ in CMS calorimeter



- 77000 PbWO₄ crystals -> scintillation light
 - 9 pe/MeV : APD photosensor

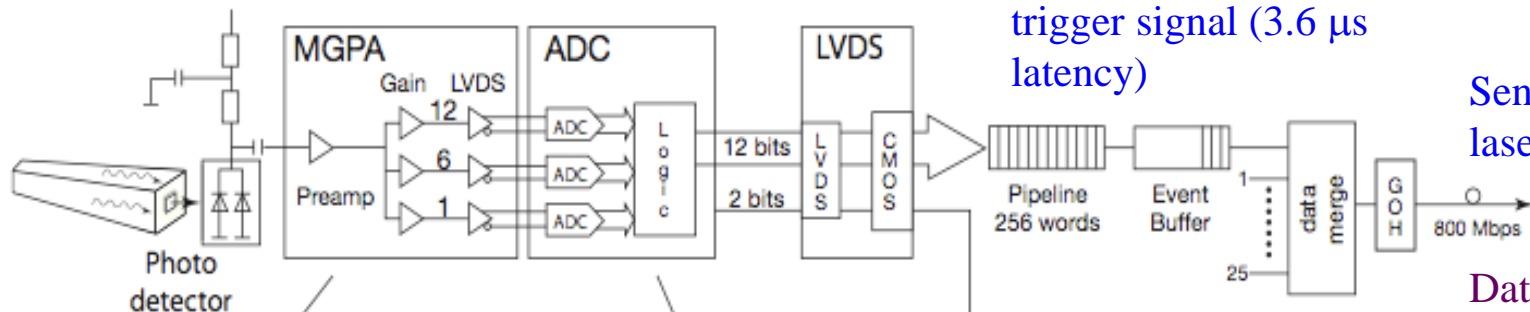


Overall the on-detector electronics is made by ~ 21,000 custom made boards,
2.3 W/ch => 180kW total

MGPA: Multi-Gain-Pre-Amplifier with 3 gains (1, 6 and 12)

ADC: 4 40-MHz 12 bit digitize the 3 outputs

The highest, non-saturated gain is selected and kept in memory waiting for a L1-trigger signal (3.6 μ s latency)



Sent off detector via laser fibers

Data information sent every L1

Trigger information sent every bunch crossing

Signal from the photodetector

Connectors to FE board

LVDSBUF

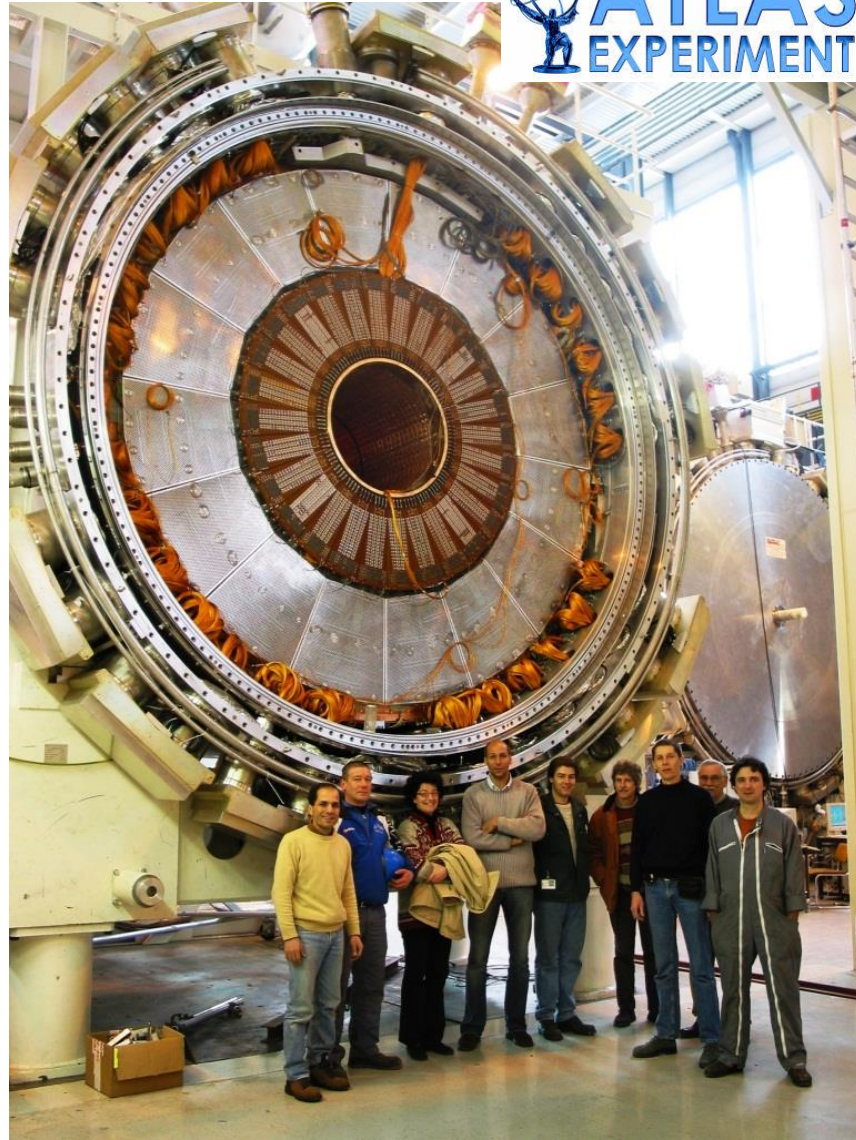
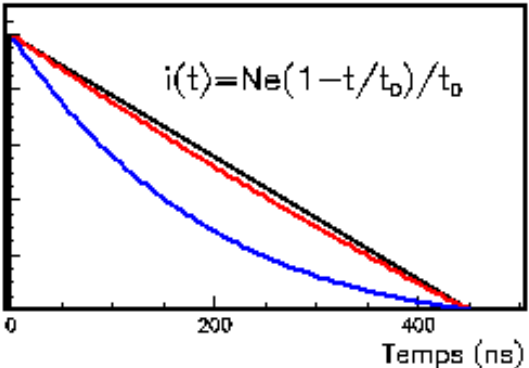
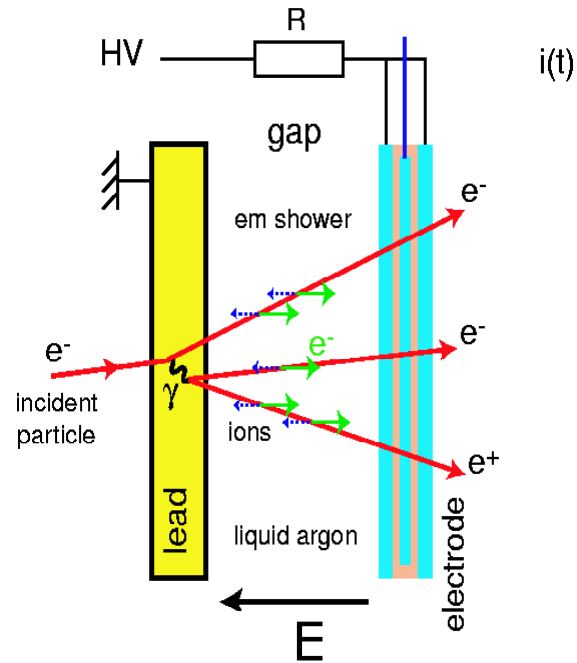
DCU on the back

ADC ADC ADC ADC ADC
MGPA MGPA MGPA MGPA MGPA

Connector to mother board

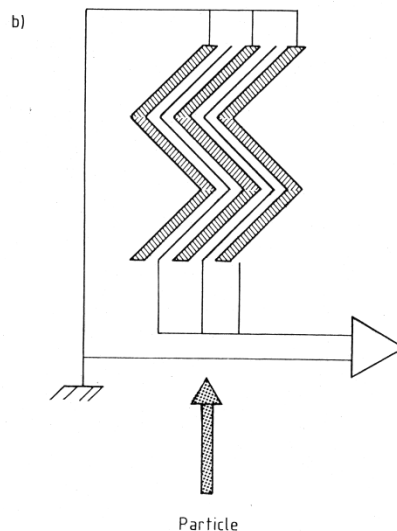
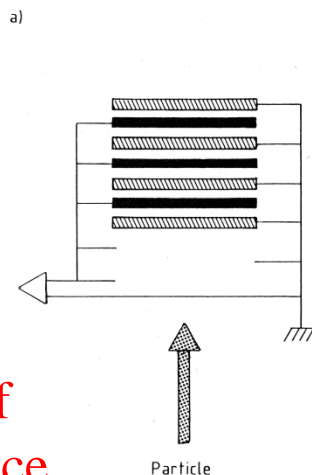
ATLAS : liquid argon calorimeter

- Liquid argon (87K) is a dense ionizing medium
 - Signal : 3 $\mu\text{A}/\text{GeV}$

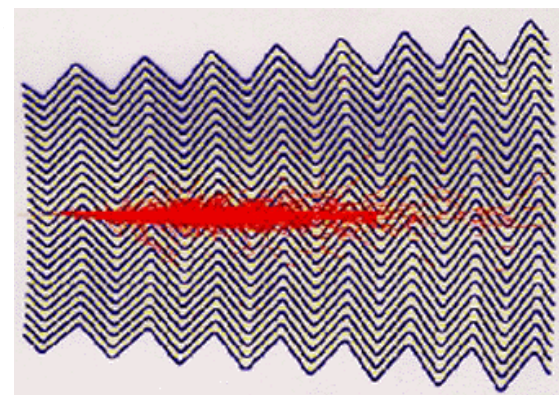




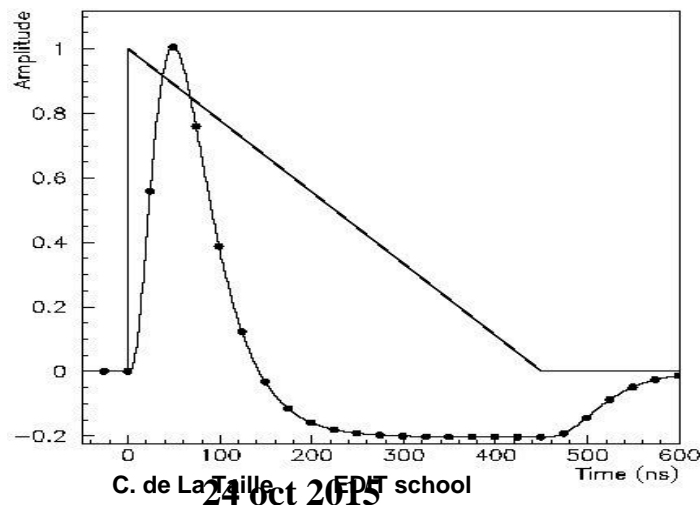
Slow because of parasitic inductance



Fast because behaves as a transmission line



Charge sensitive
=>
Current sensitive preamps

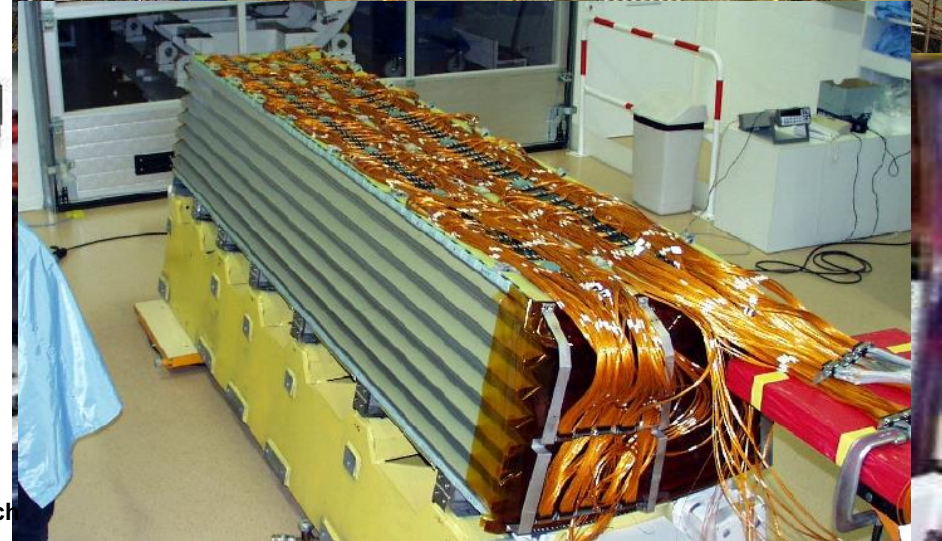
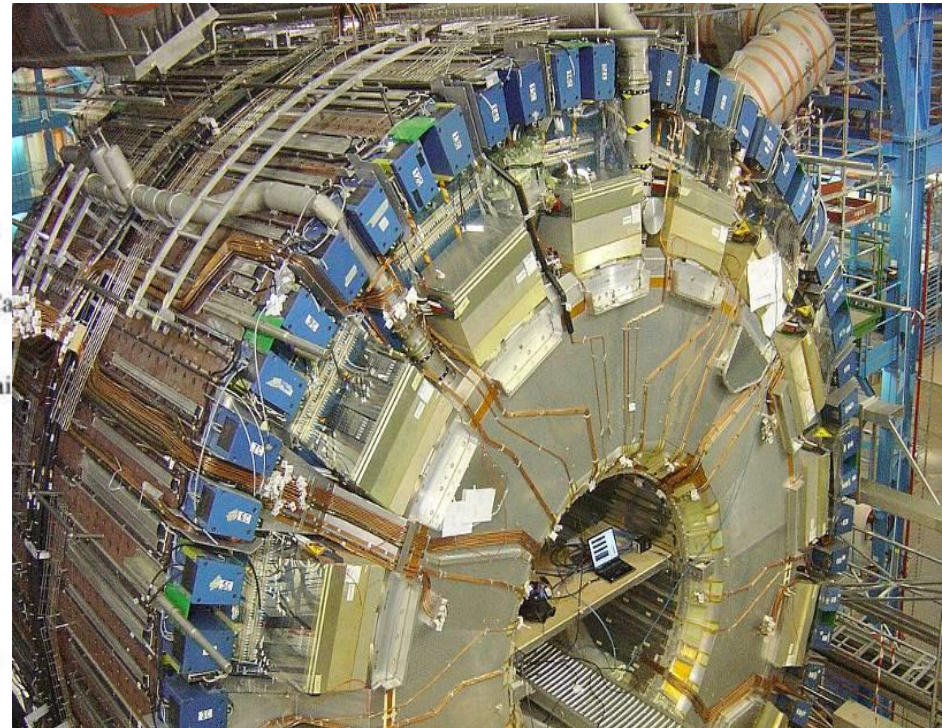
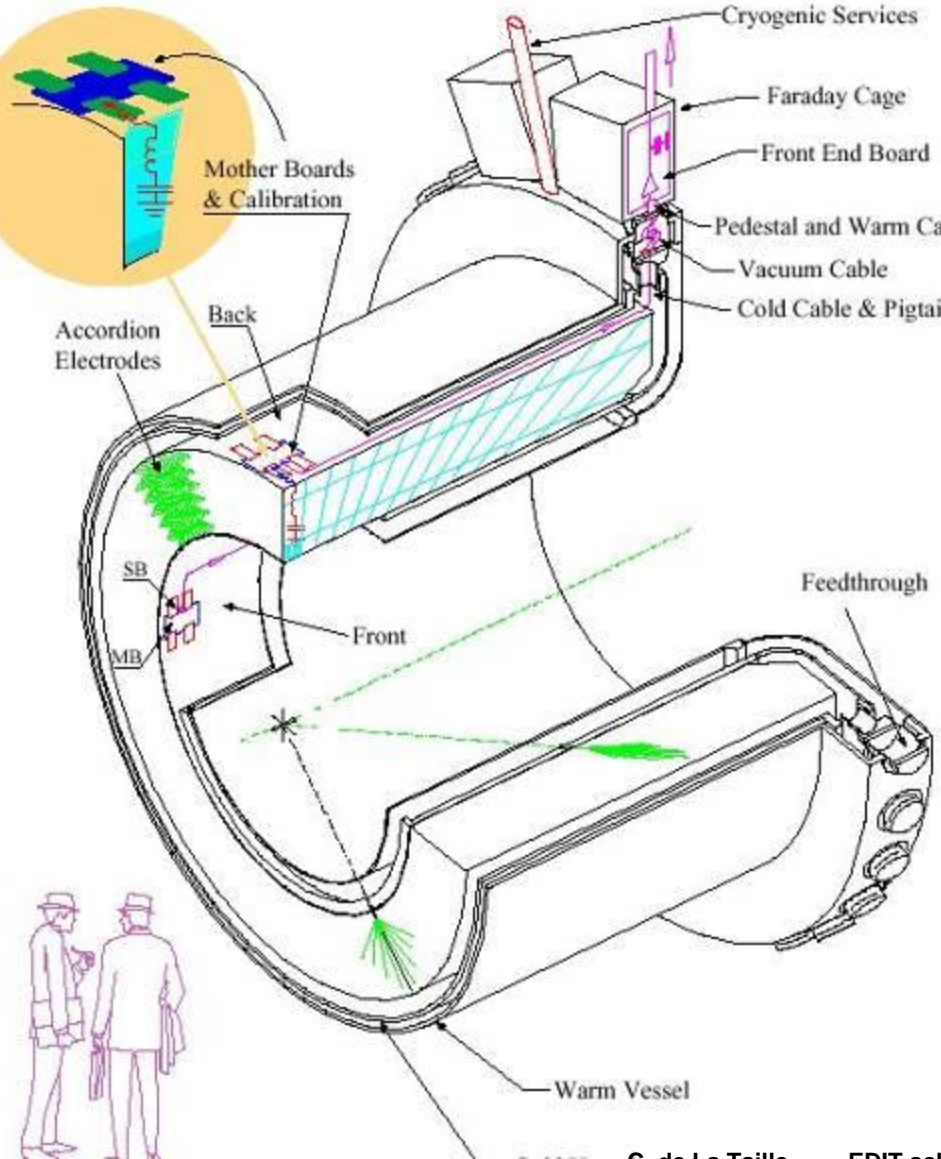


Long signal
=>
Fast shaping



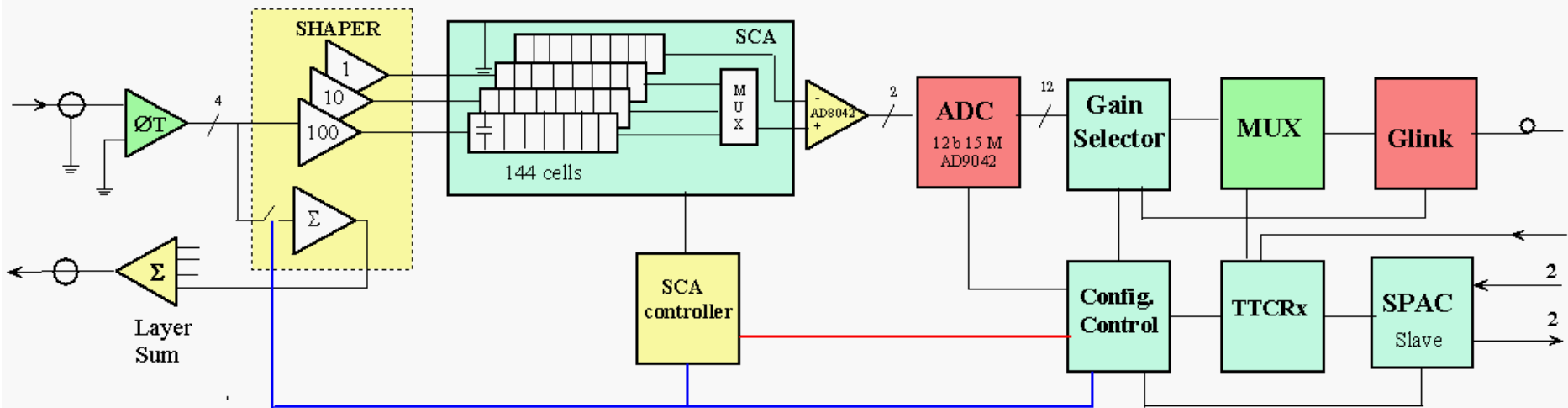
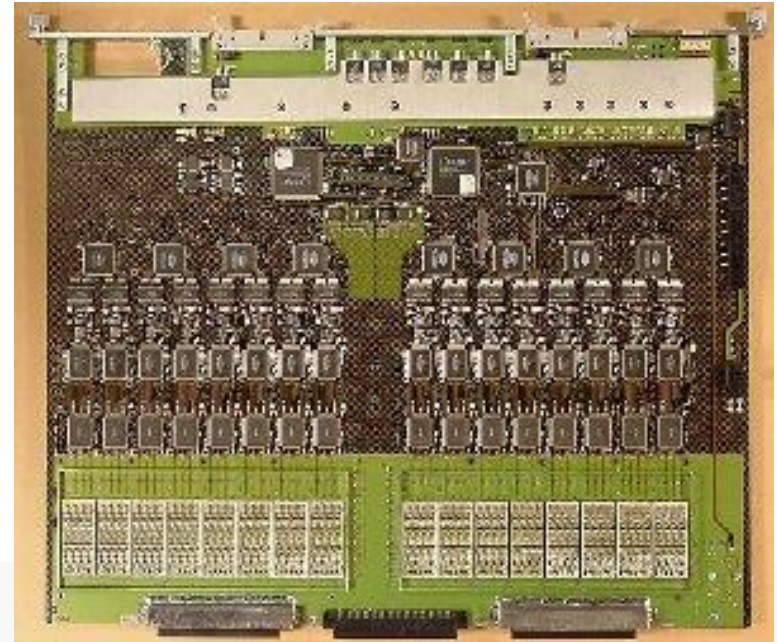
ATLAS calorimeter

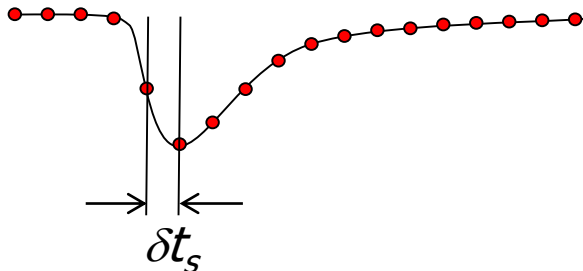
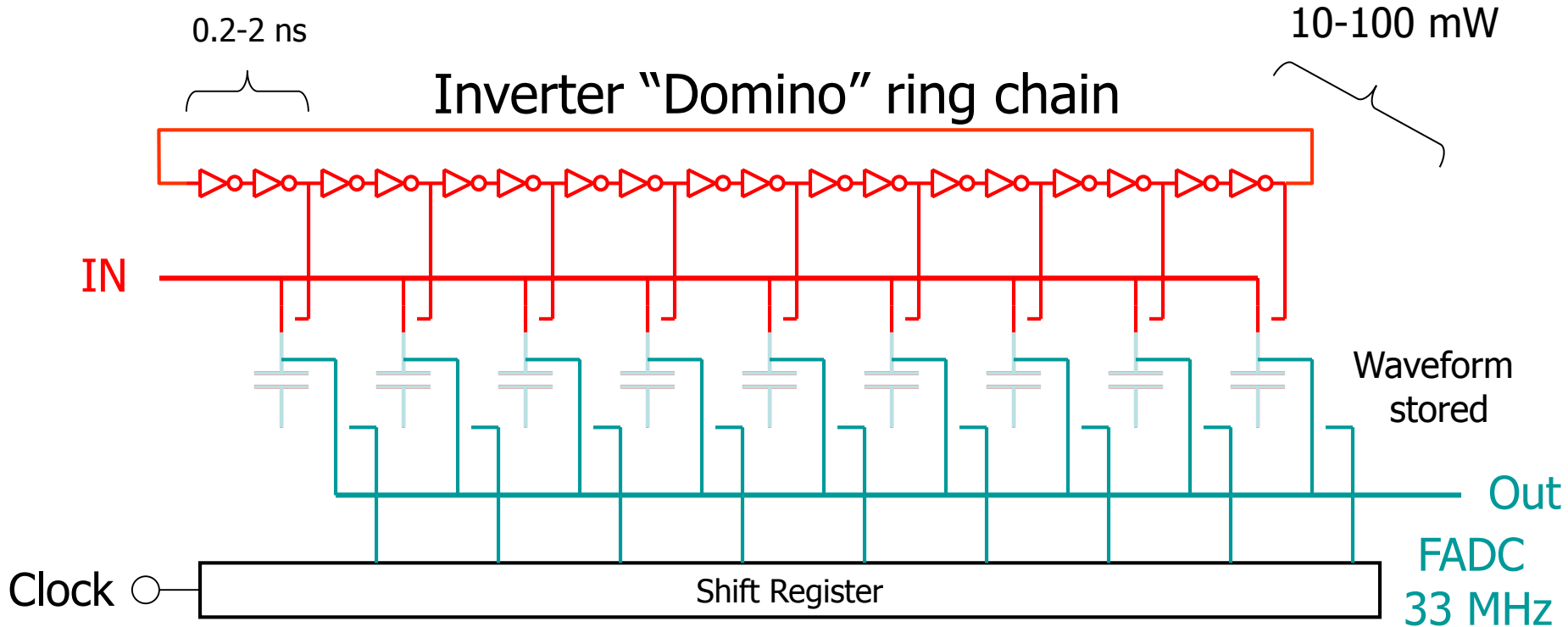
200 000 readout channels



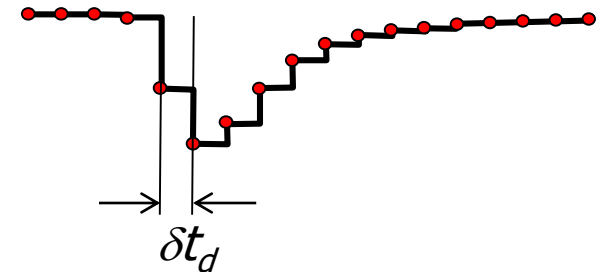


- Amplify, shape, store and digitize signals from detector
 - Line-terminating current sensitive preamplifiers (OT)
 - Tr-gain band pass shapers (1-10-100)
 - Analog memories 12 bits
 - 1 W/ch





"Time stretcher"
GHz \rightarrow MHz



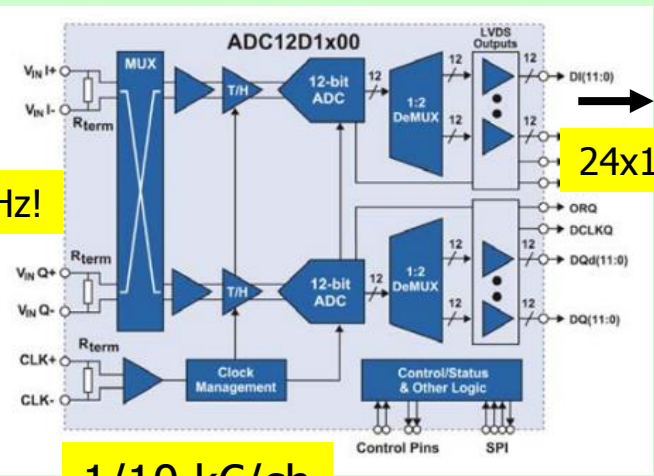
FADCs

- 8 bits – 3 GS/s – 1.9 W → 24 Gbits/s
- 10 bits – 3 GS/s – 3.6 W → 30 Gbits/s
- 12 bits – 3.6 GS/s – 3.9 W → 43.2 Gbits/s
- 14 bits – 0.4 GS/s – 2.5 W → 5.6 Gbits/s

1.8 GHz!

1/10 k€/ch

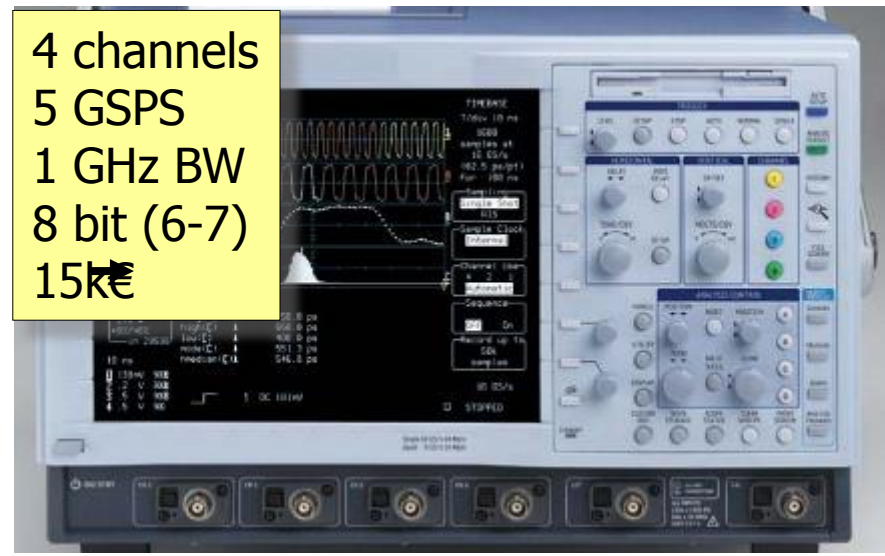
24x1.8 Gbits/s



PX1500-4:
2 Channel
3 GS/s
8 bits

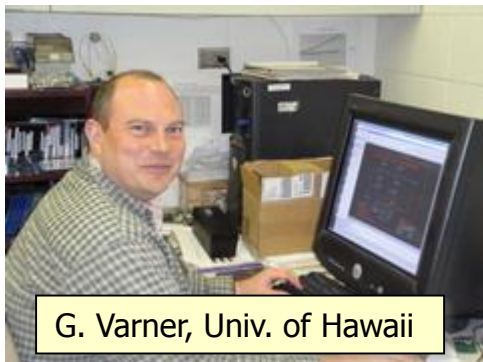


4 channels
5 GSPS
1 GHz BW
8 bit (6-7)
15k€



4 channels
5 GSPS
1 GHz BW
11.5 bits
900€
USB Power





G. Varner, Univ. of Hawaii

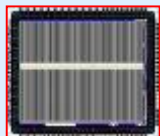


E. Delagnes
D. Breton
CEA Saclay



H. Frisch et al., Univ. Chicago

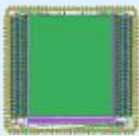
STRAW3 LABRADOR3 TARGET



- 0.25 μm TSMC
- Many chips for different projects (Belle, Anita, IceCube ...)

www.phys.hawaii.edu/~idlab/

AFTER SAM NECTARO



- 0.35 μm AMS
- T2K TPC, Antares, Hess2, CTA

matacq.free.fr

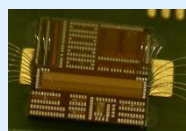


PSEC1 - PSEC4

- 0.13 μm IBM
- Large Area Picosecond Photo-Detectors Project (LAPPD)

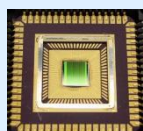
psec.uchicago.edu

DRS1



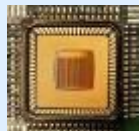
2002

DRS2



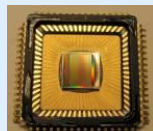
2004

DRS3



2007

DRS4



2008

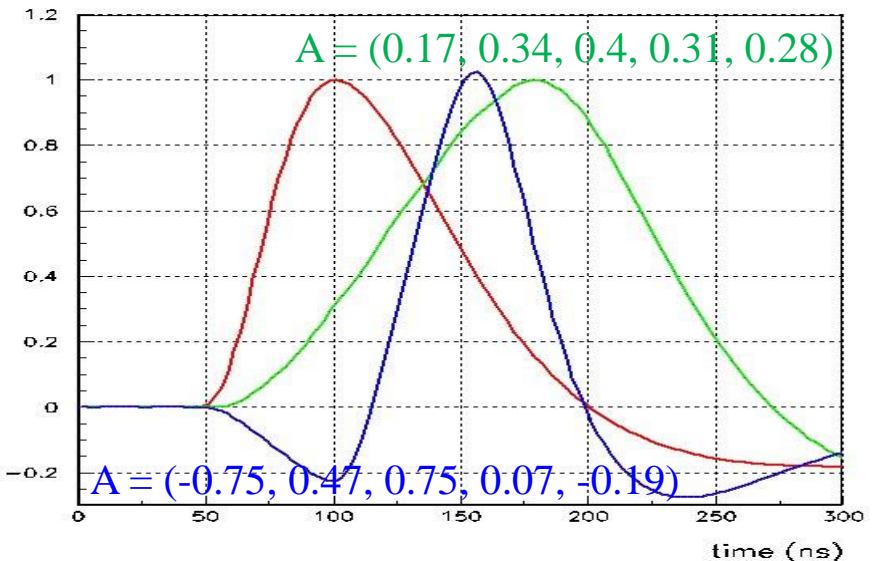
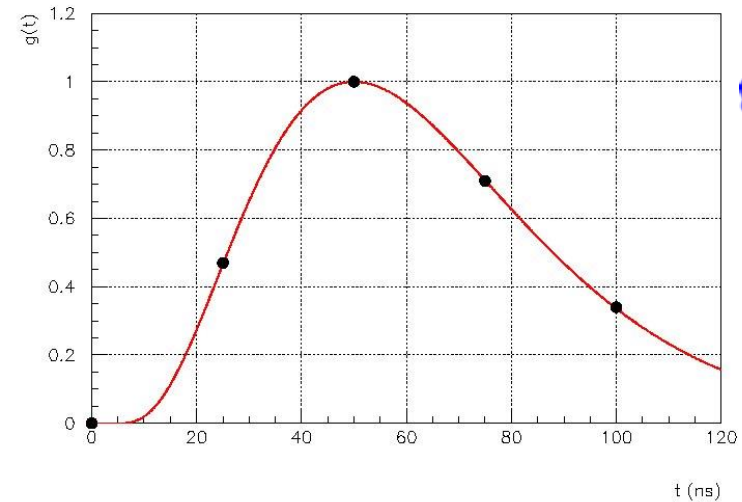
- 0.25 μm UMC
- Universal chip for many applications
- MEG experiment, MAGIC, Veritas, TOF-PET



Stefan Ritt
R. Dinapoli
PSI, Switzerland

drs.web.psi.ch

- Linear sums on sampled signal $g(t)$
 - Finite Impulse Response (FIR)
- Filter : weighed sum $\sum a_i s_i$
 - $a_i = \sum R^{-1}_{ij} g_j$
 - R = autocorrelation function
 - g_j = signal shape
 - Output Signal : $S = \sum a_i s_i$
- Slow down or accelerate signal
 - Reduction of electronics noise
 - Reduction of pileup noise
 - Adaptive filter
 - How does-it compare to an analog filter ?
 - How many samples are needed ?
 - What accuracy is needed on the waveform and on the autocorrelation ?
 - What analog shaping time is needed ?
 - Is the analog filter really useful ?



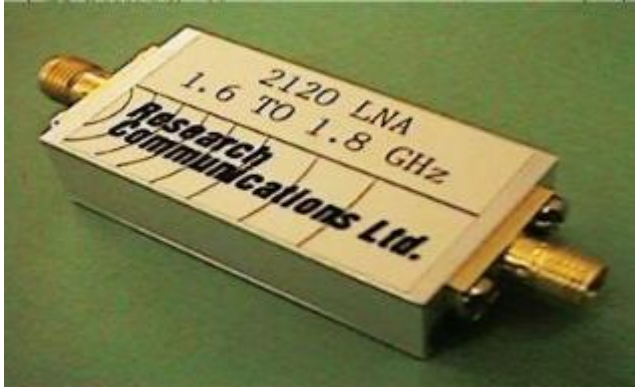
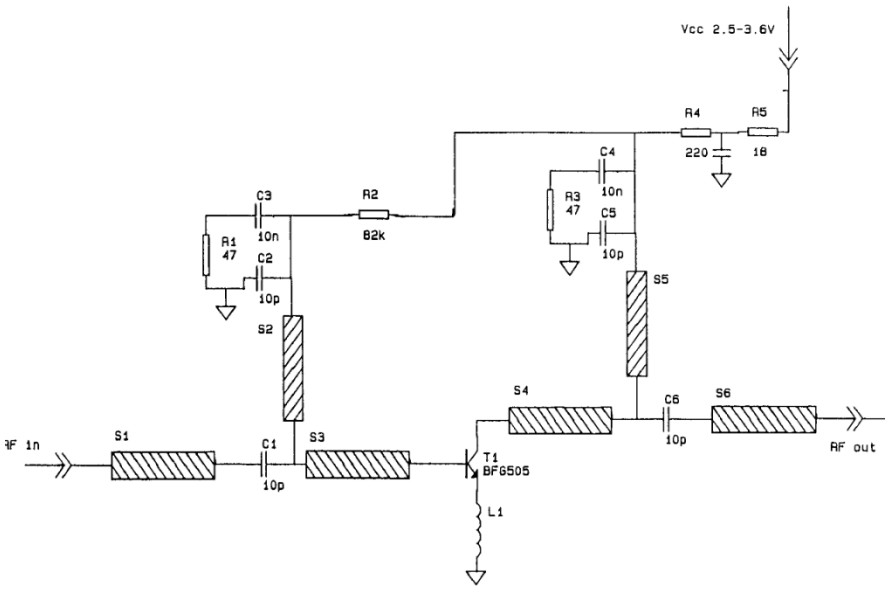
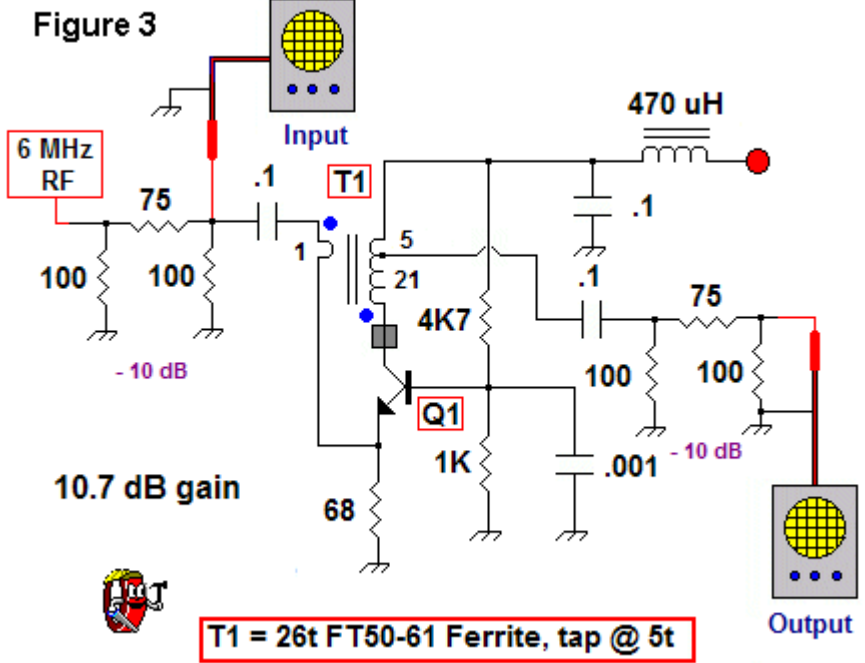


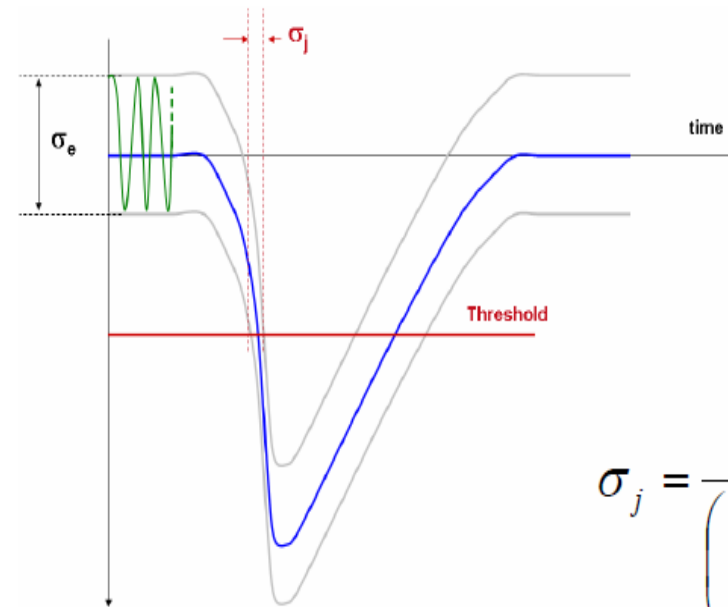
Figure 3



- Electronics noise dominated by series noise e_n
 - Large detector capacitance
 - For voltage preamp and load resistor R_L ,
 - Output rms noise $V_n^2 = (e_n^2 + 4kTR_s) G^2 \pi/2 * BW_{-3dB}$
 - Typical values : $R_s = 50 \Omega$, $e_n = 1 \text{ nV}/\sqrt{\text{Hz}}$ $V_n = 1 \text{ mV}$ for $G = 10$, $BW = 1 \text{ GHz}$
 - For current sensitive preamps, possible noise peaking due to C_d

- Jitter

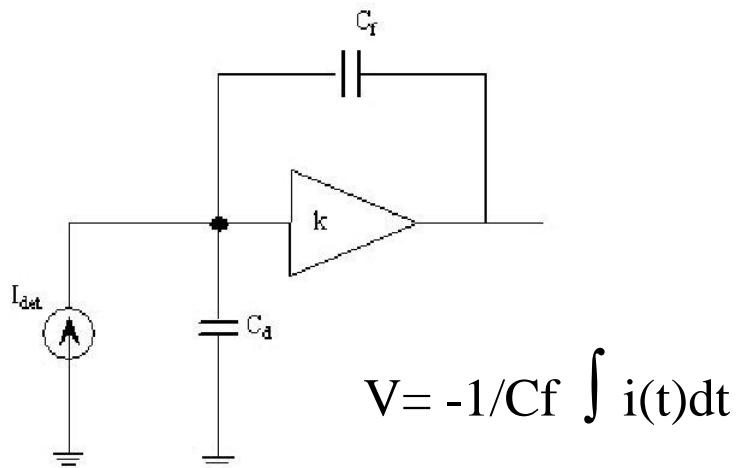
- Part due to electronics noise :
- $\sigma_t = \sigma_v / (dV/dt)$
- Minimized by increasing BW



$$\sigma_j = \frac{\sigma_e}{\left(\frac{dV}{dt}\right)_{\text{threshold}}}$$

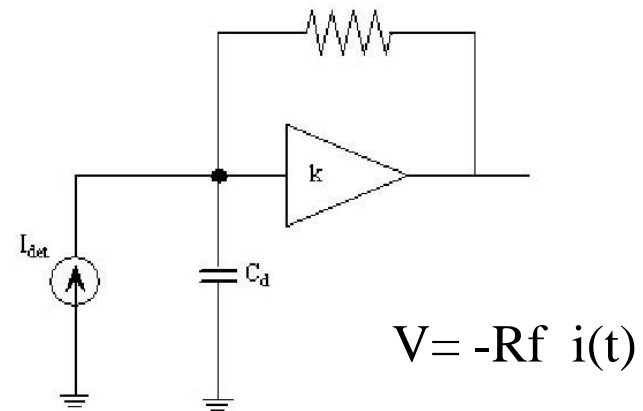
- **Charge preamp**

- Capacitive feedback C_f
- $V_{out}/I_{in} = -1/j\omega C_f$
- Perfect integrator : $v_{out} = -Q/C_f$
- Difficult to accommodate large SiPM signals (200 pC)
- Lowest noise configuration
- Need R_f to empty C_f



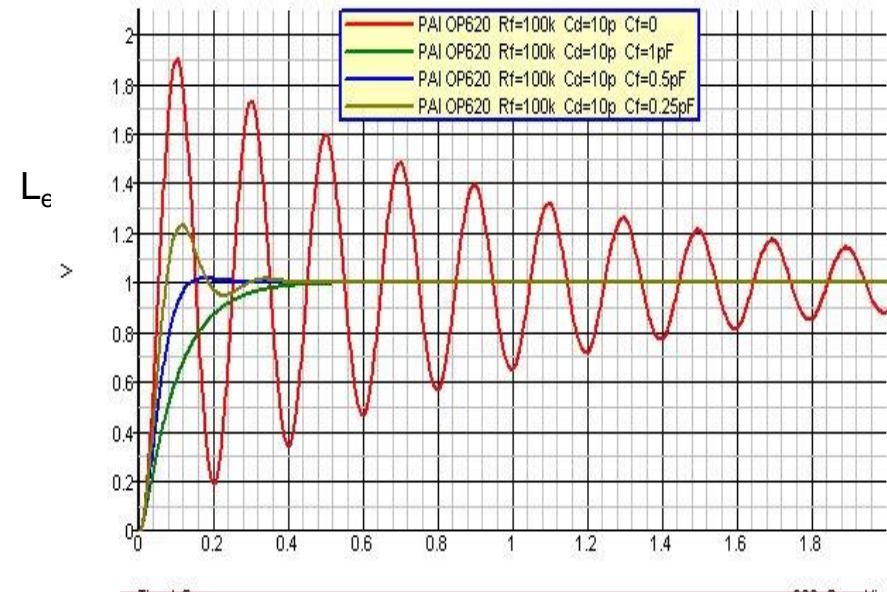
- **Current preamp**

- Resistive feedback R_f
- $V_{out}/I_{in} = -R_f$
- Keeps signal shape
- Need C_f for stability

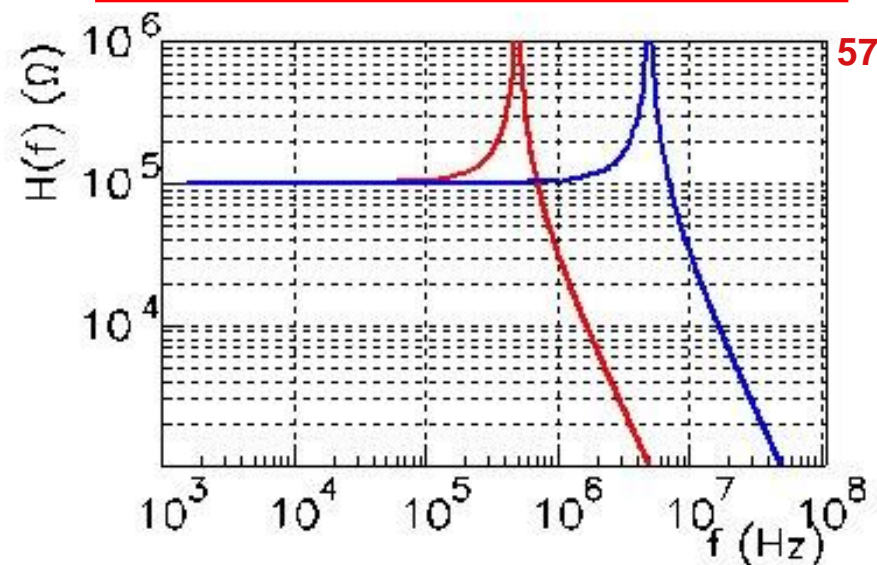


Current preamplifiers :

- Easily oscillatory
 - Unstable with capacitive detector
 - Inductive input impedance :
 $= R_f / \omega C_d$
 - Resonance at : $f_{res} = 1/2\pi \sqrt{L_{eq} C_d}$
 - Quality factor : $Q = R / \sqrt{L_{eq}/C_d}$
 - $Q > 1/2 \rightarrow$ ringing
 - Damping with capacitance C_f
 - $C_f = 2 \sqrt{(C_d/R_f G_0 \omega_0)}$
 - Easier with fast amplifiers
- In frequency domain
 - $H(j\omega) = -R_f / (1 + j\omega R_f C_d)$
 - $G(\omega) = G_0 / (1 + j\omega/\omega_0)$
 - $H = -R_f / (1 + j\omega R_f C_d / G_0 - \omega^2 R_f C_d / G_0 \omega_0)$



Step response of current sensitive preamp

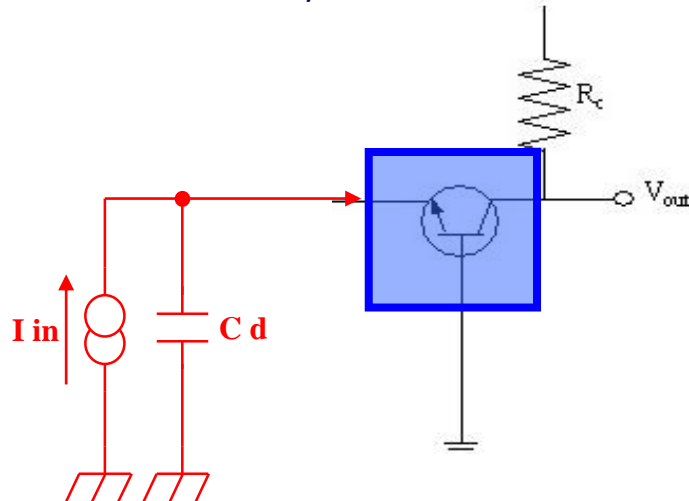


57

- Open loop configurations : current conveyors, RF amplifiers
- Usually designed at transistor level MOS or SiGe

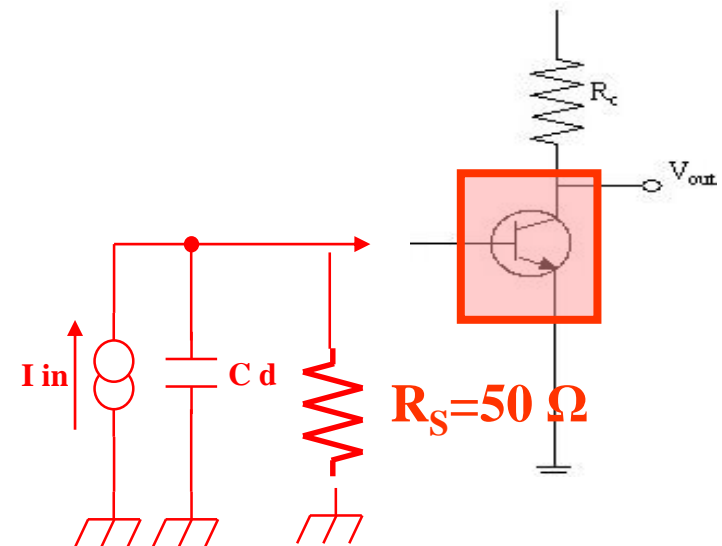
- **Current conveyors**

- **Small Z_{in}** : current sensitive input
- **Large Z_{out}** : current driven output
- Unity gain current conveyor
- E.g. : (super) common-base configuration
- Low input impedance : $R_{in} = 1/g_m$
- Transimpedance : R_c
- Bandwidth : $1/2\pi R_c C_d > 1 \text{ GHz}$



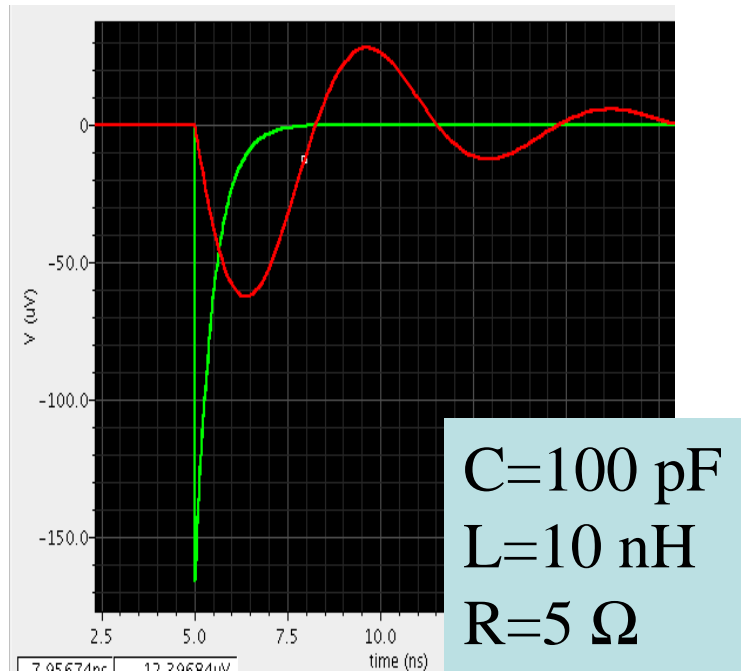
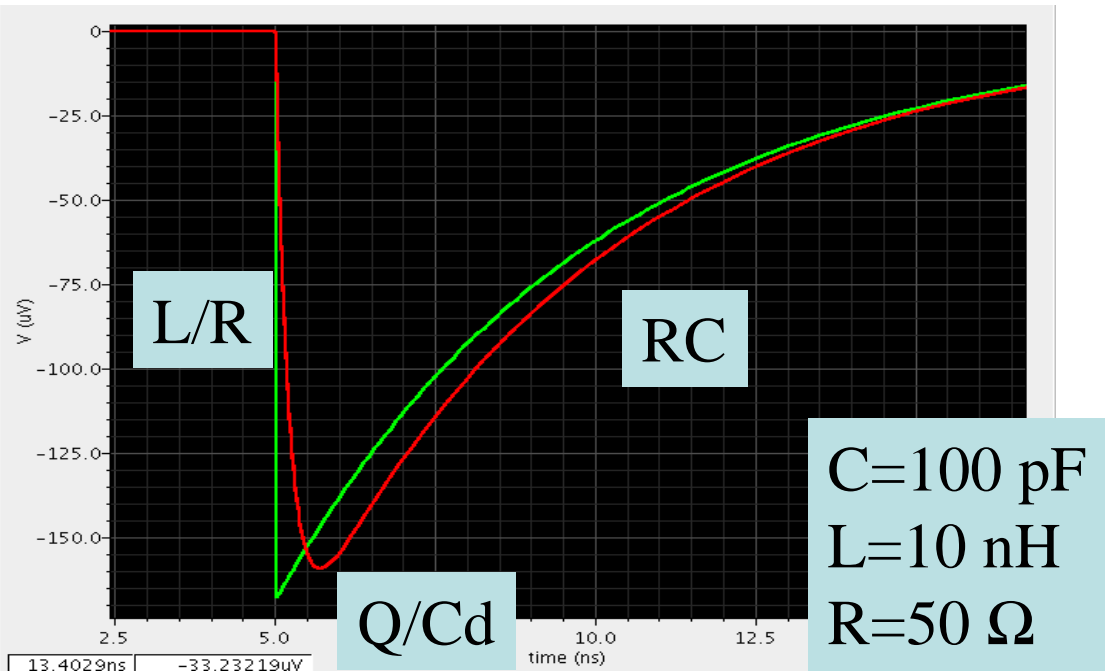
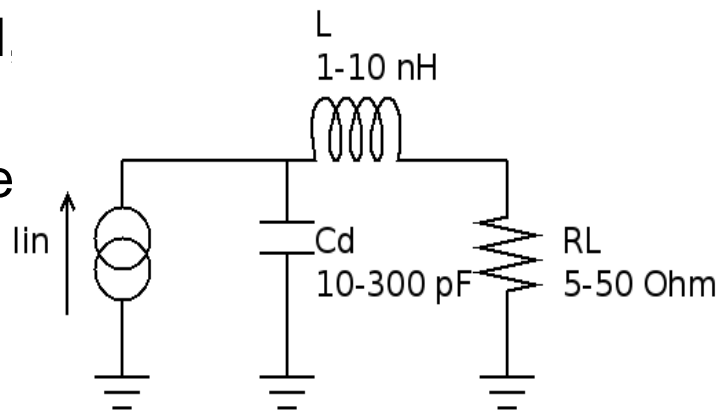
- **RF amplifiers**

- **Large Z_{in}** : voltage sensitive input
- **Large Z_{out}** : current driven output
- Current conversion with resistor R_S
- E.g. common-emitter configuration
- Transimpedance : $-g_m R_c R_S$
- Bandwidth : $1/2\pi R_S C_t$

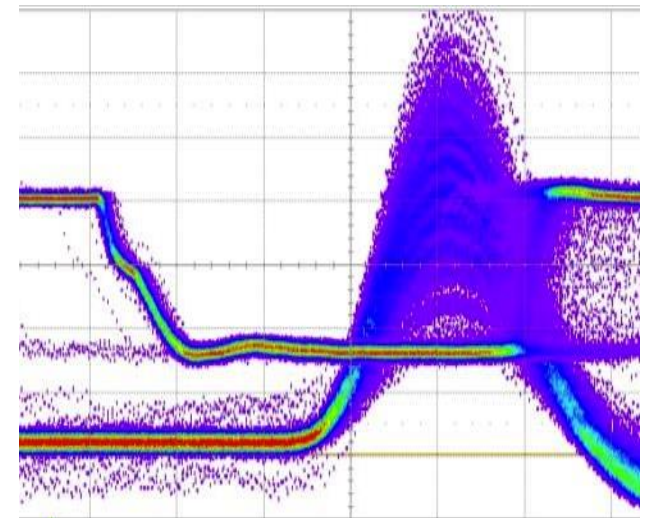
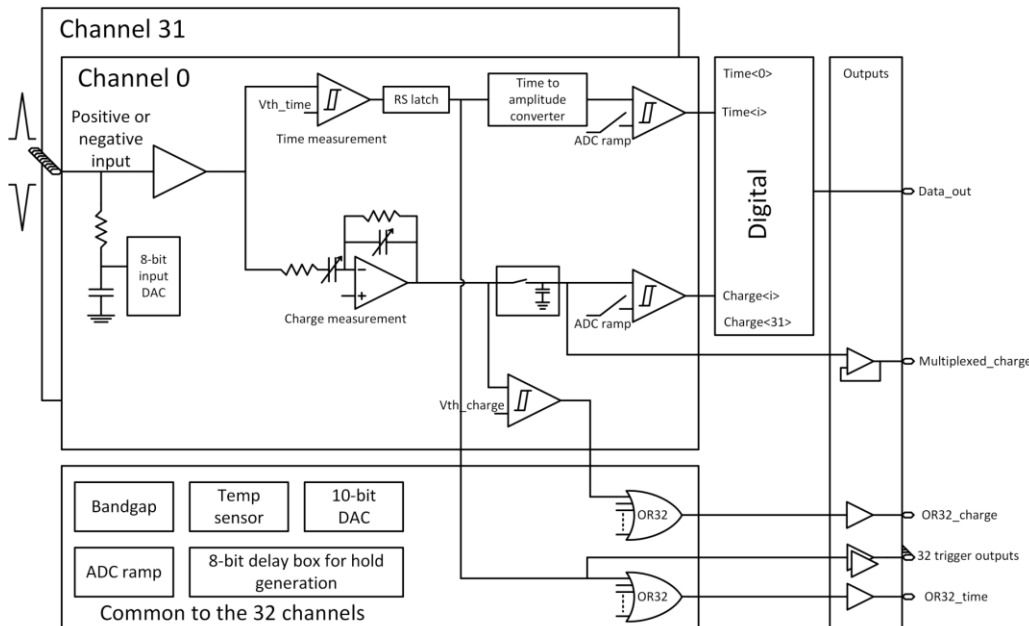
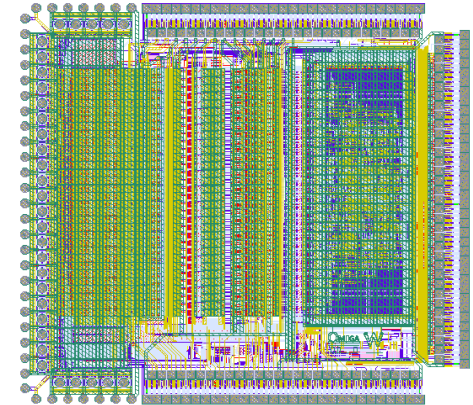


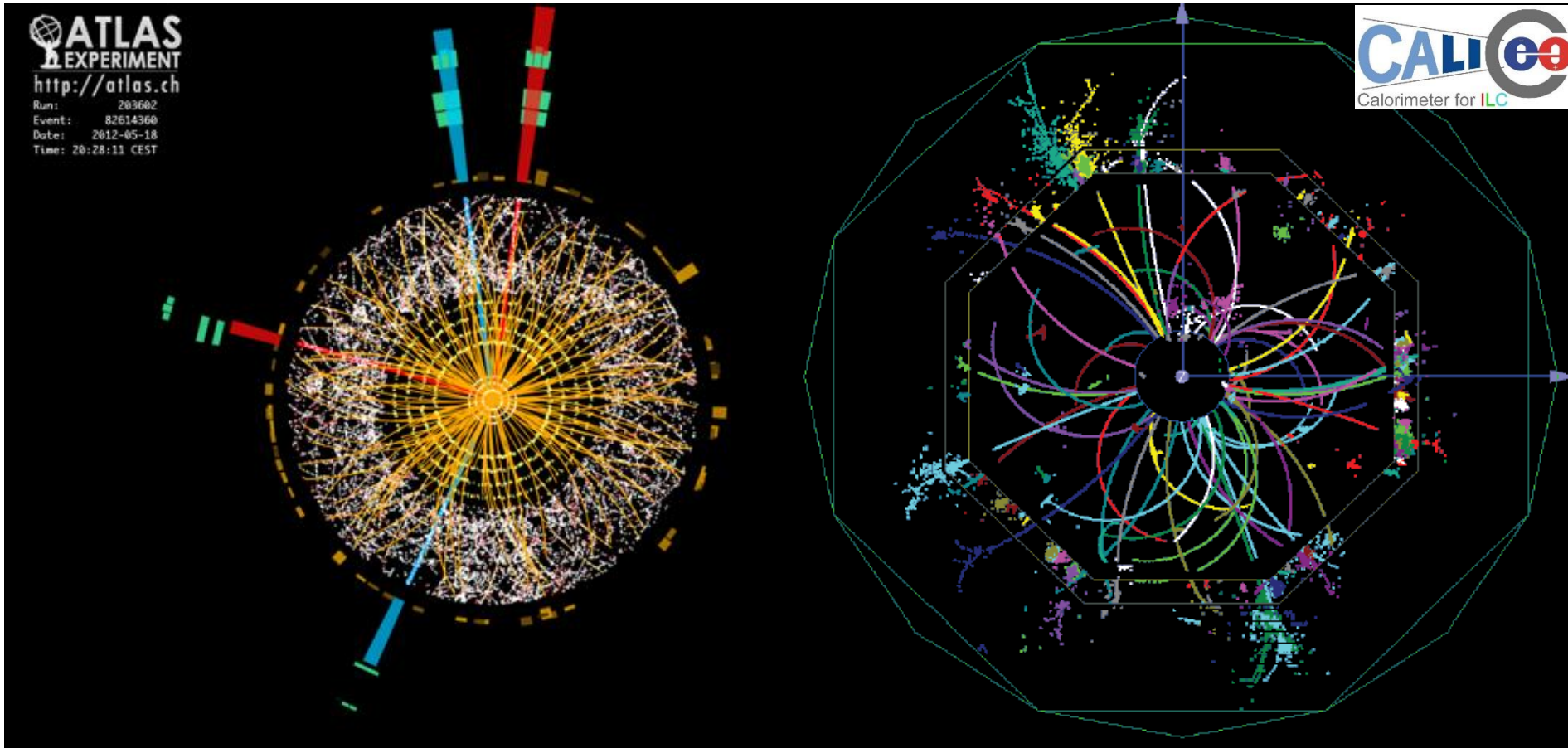
Examples of pulse shapes

- Short pulse : $Q=16 \text{ fC}$, $C_d=100 \text{ pF}$, $L=0-10 \text{ nH}$, $RL=5-50 \Omega$
- Smaller signals with SiPM (large C_d) $\sim \text{mV/p.e}$
- Sensitivity to parasitic inductance
- Choice of RL : decay time, stability
- Convolve with current shape... (here delta impulse)

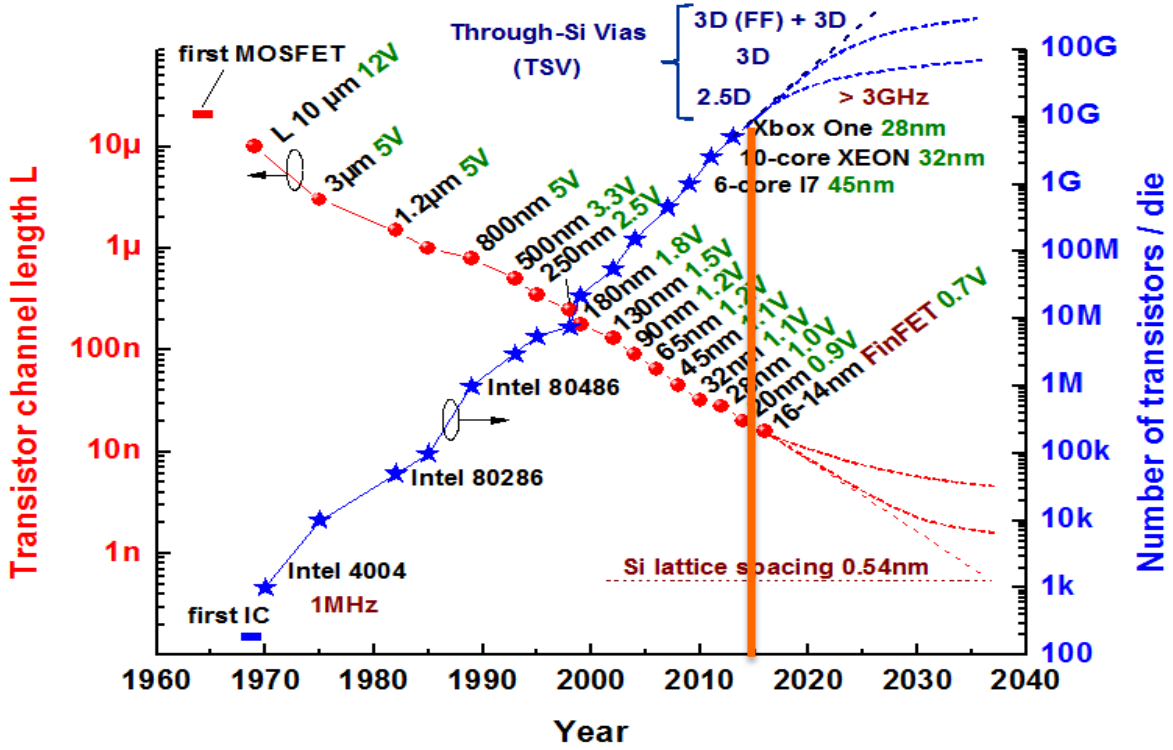


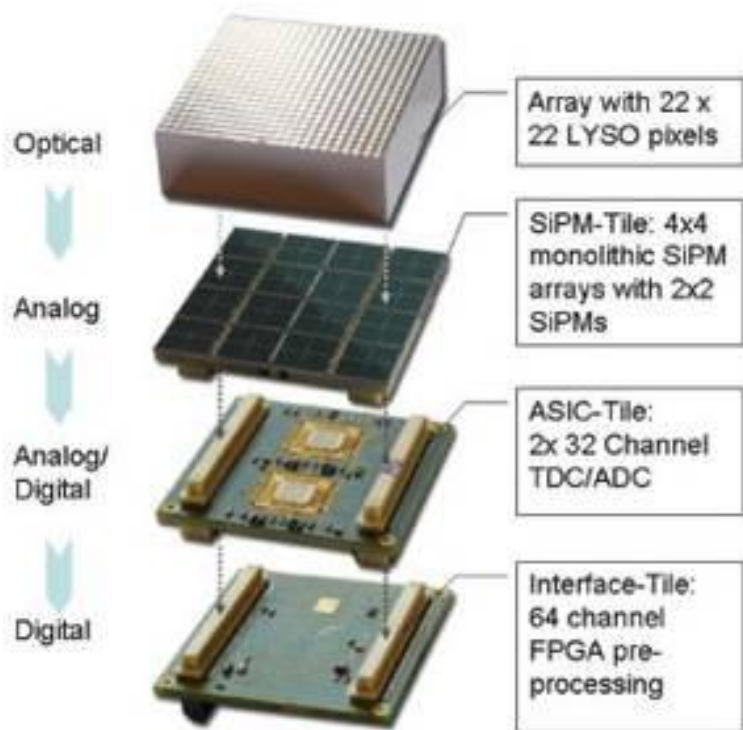
- 32 ch SiPM GHz readout ASIC, dual polarity, 100 fC-400 pC, 6 mW/ch
 - RF, common emitter SiGe fast amplifier, DC coupled to detector, **GBWP 10GHz@1mW**
 - Fast SiGe discriminator, **BW 1GHz @ 1.5mW**
- 32 trigger outputs and multiplexed data output
- Embedded 10 bit ADC and 50 ps TDC
- Dual threshold : first photons and energy



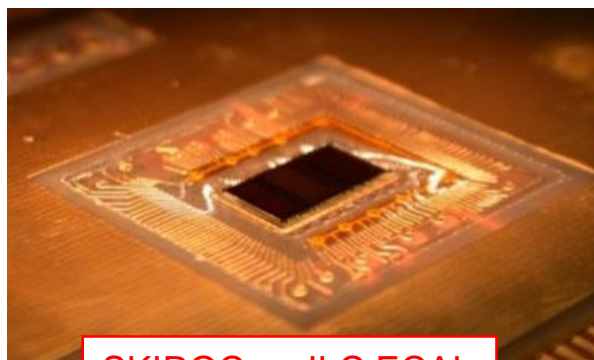


- More and more functions are integrated inside chips (ASICs)
- Evolution of technologies make them more and more performant but more and more complex
- Cost increases ...
 - MPW costs :
 - 350 nm : 1 k€/mm²
 - 130 nm : 2 k€/mm²
 - 65 nm : 6 k€/mm²
- Chip size also...
- CERN targets 65/130 nm
- SiGe in AIDA2020

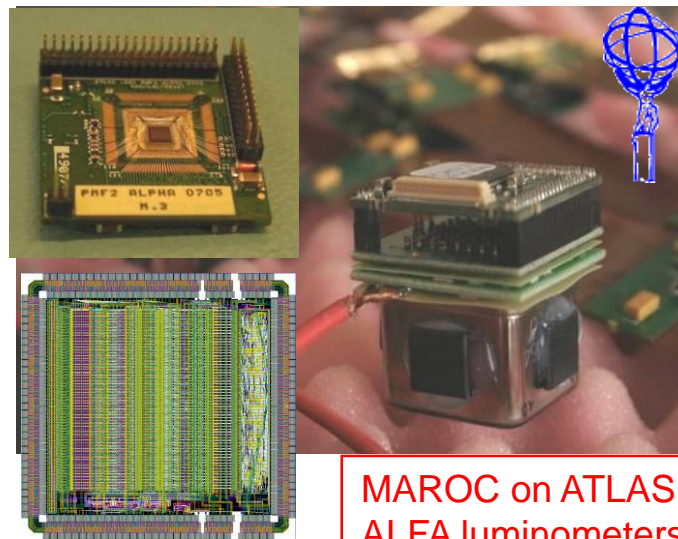




PET hyperimage project [P. Fisher]



SKIROC on ILC ECAL



MAROC on ATLAS ALFA luminometers

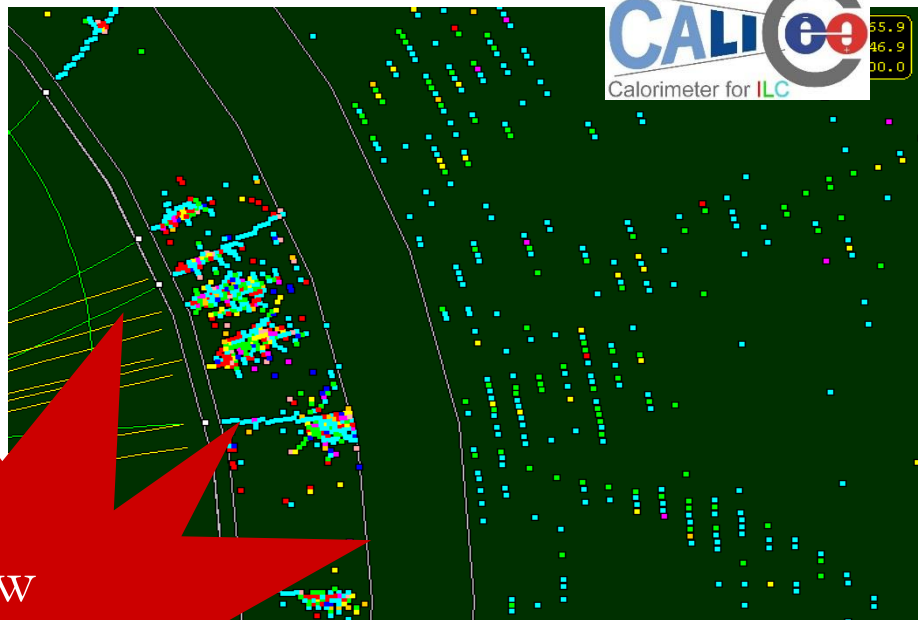


1m² RPC detector for ILC DHCAL [I. Laktineh]

« 5D calorimetry »

- Fine segmentation for shower reconstruction and particle flow algorithm
 - Position in 3D
 - Energy measurement
 - Picosecond time measurement

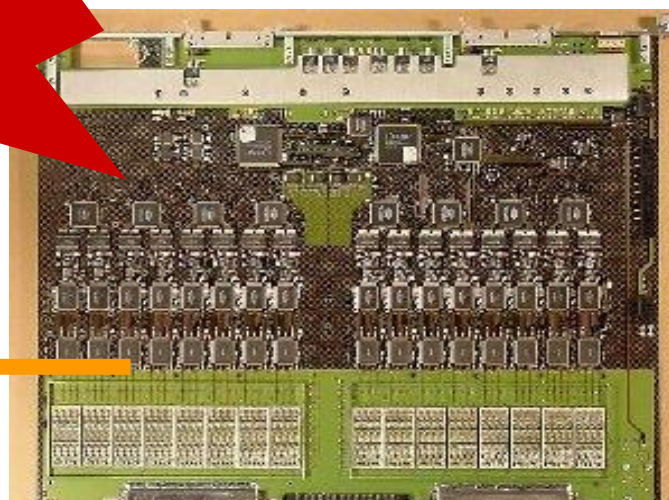
- Stringent requirements for FEE
 - Large dynamic range
 - Auto-triggering
 - Zero-suppress
 - On-detector electronics
 - **Ultra-low power : « 25 μW/ch »**
 - 100 Mchannels



Ultra-low
POWER
is the
KEY issue



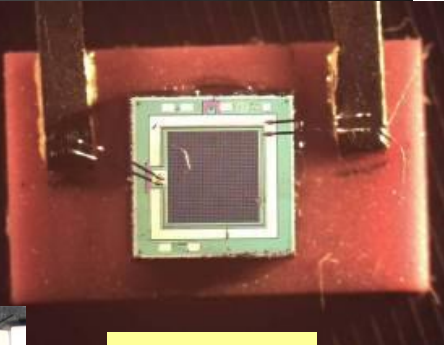
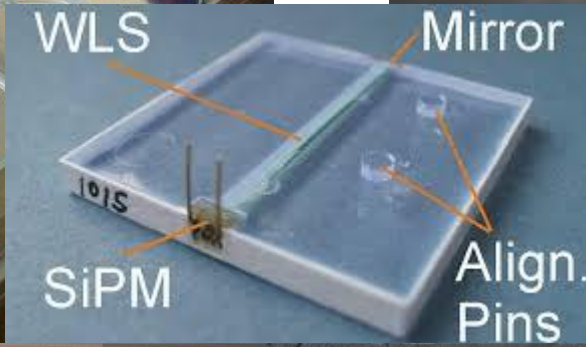
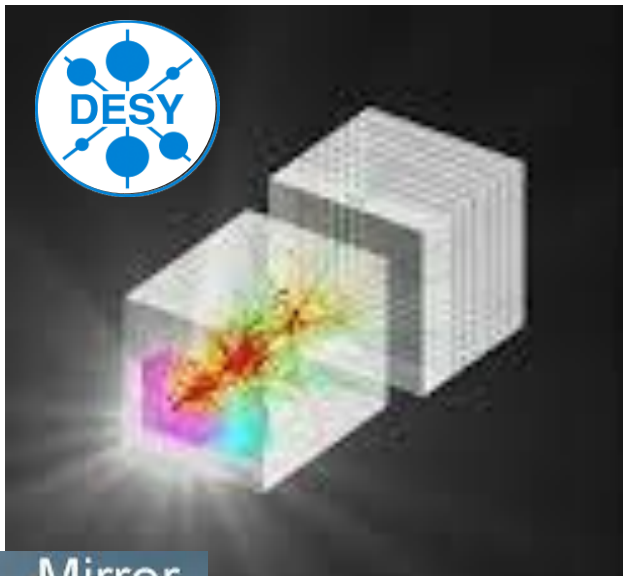
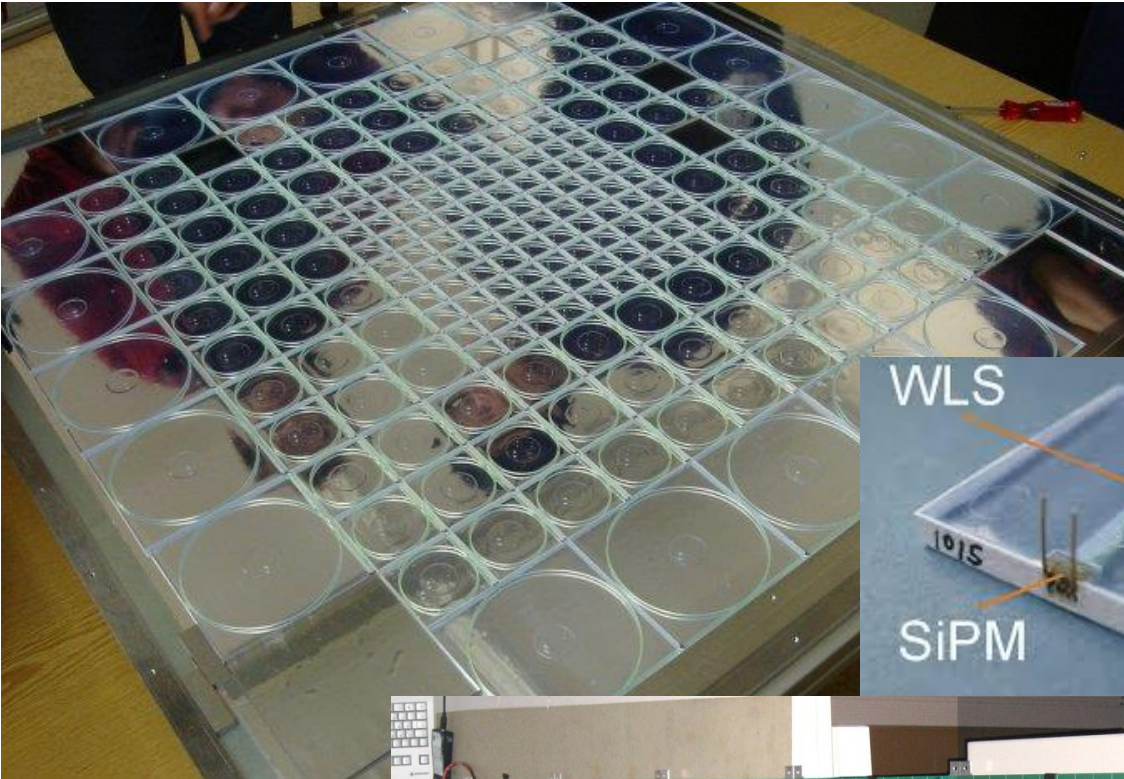
ILC : 25μW/ch



ATLAS LAr FEB 128ch 400*500mm 1 W/ch

Example : SiPM calorimeter

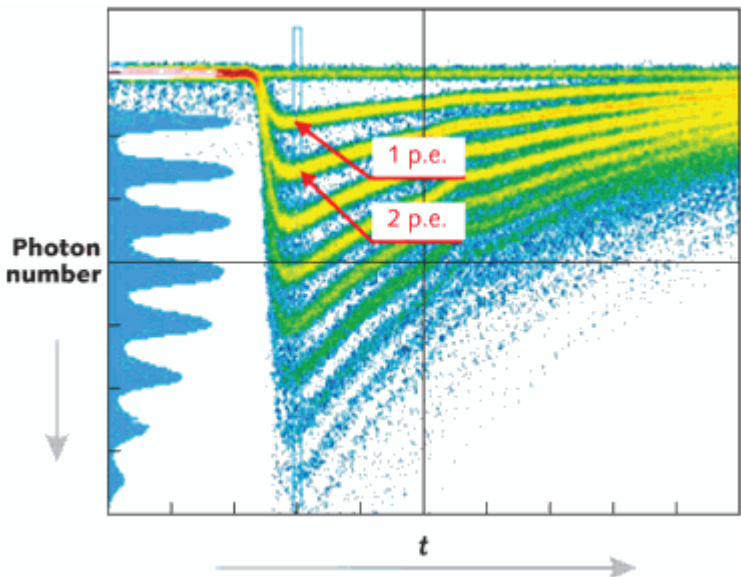
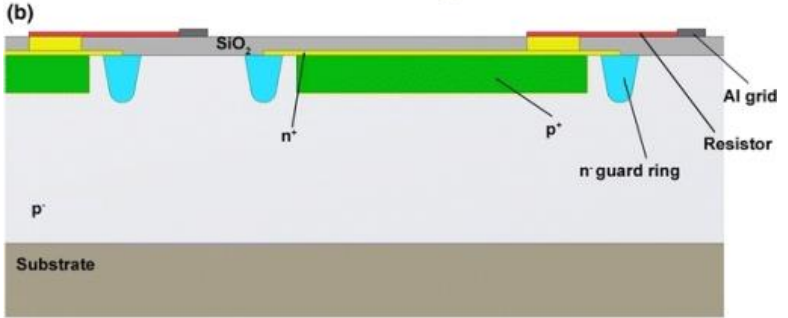
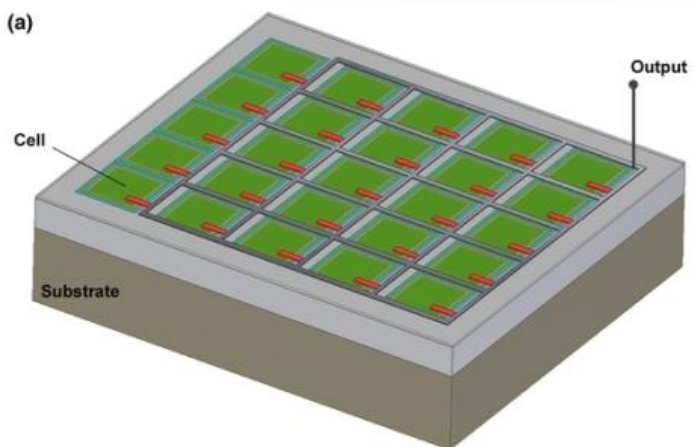
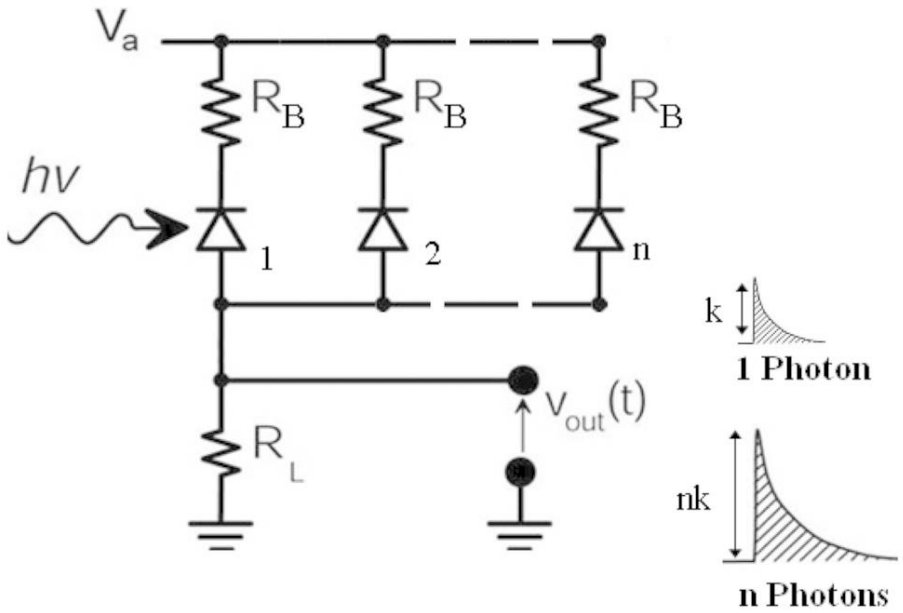
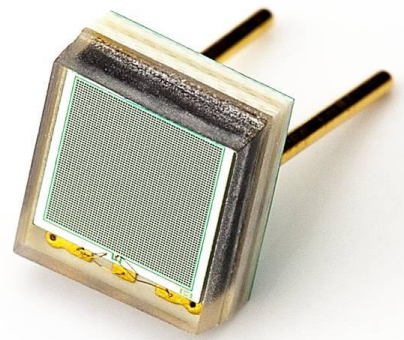
- Scintillating tiles
- SiPM readout

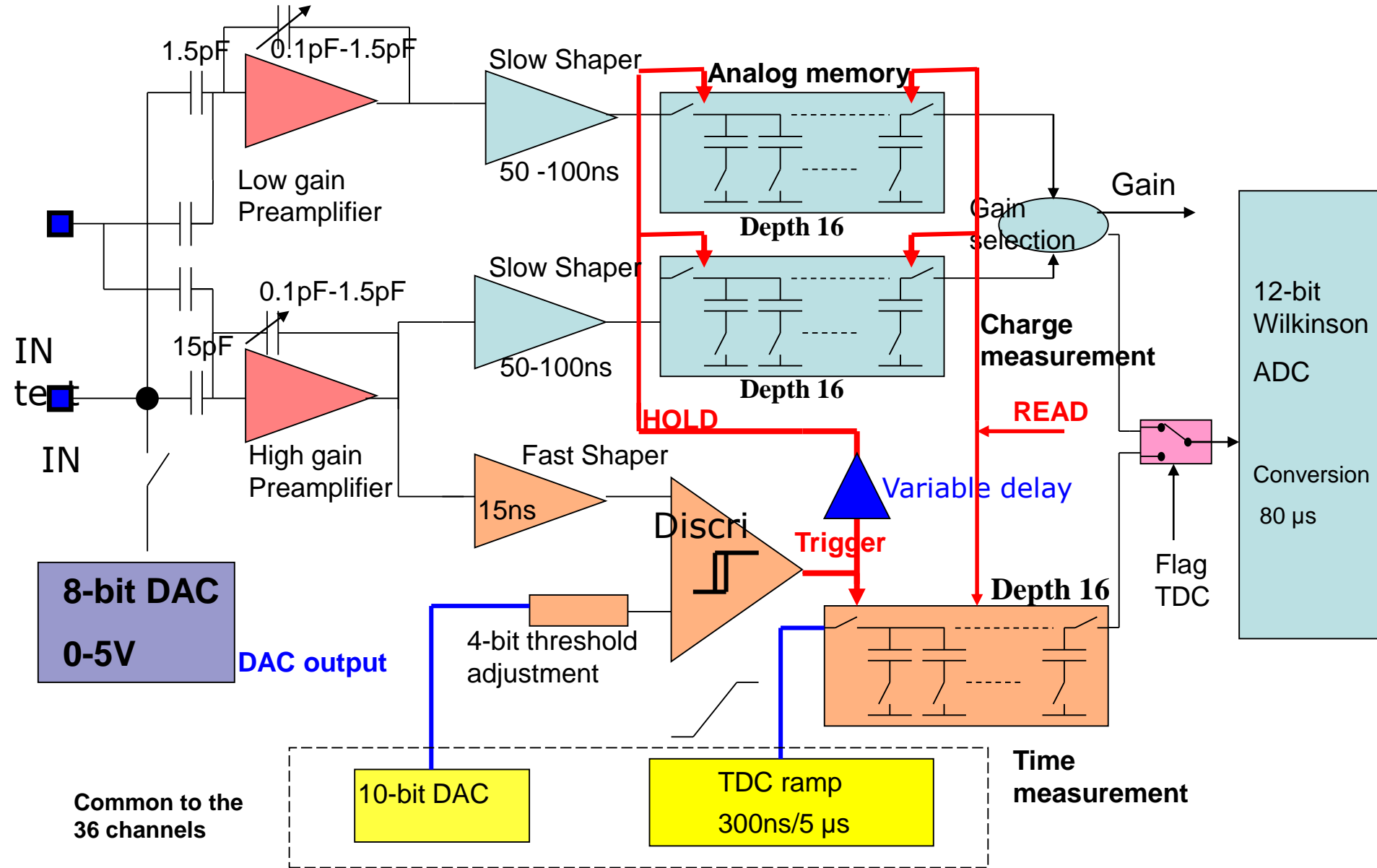


Mephy SiPM

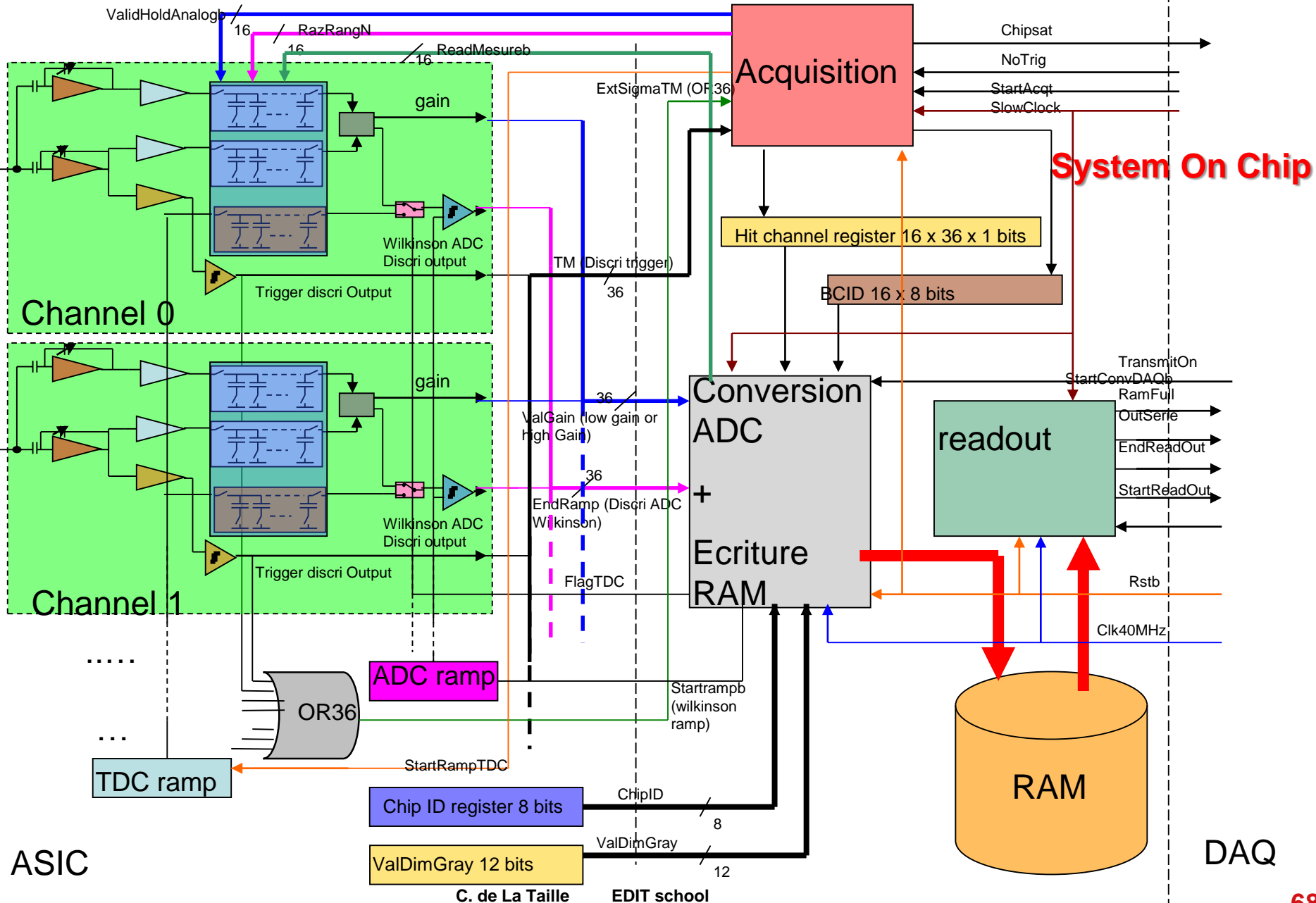


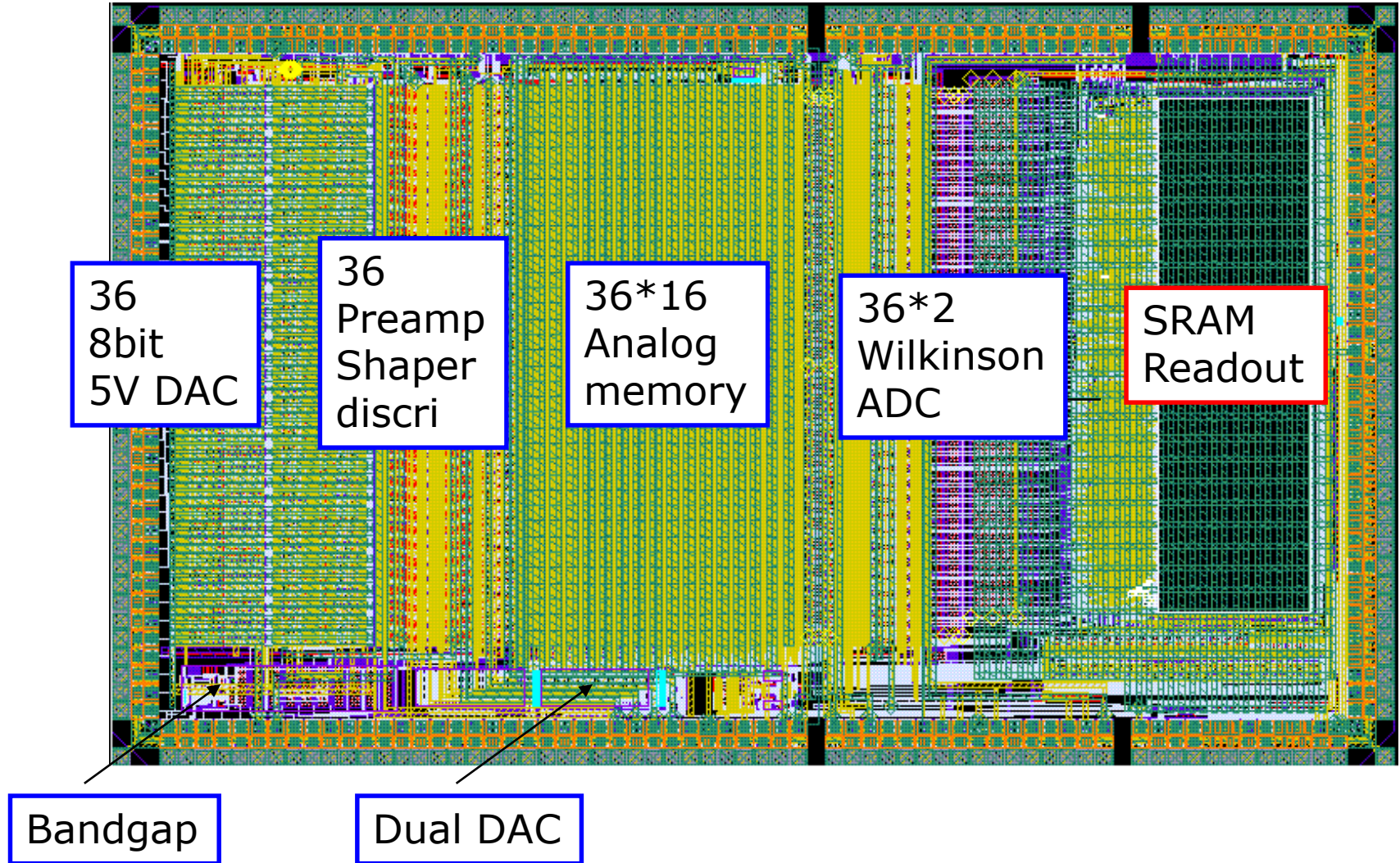
SiPM solid-state photomultiplier



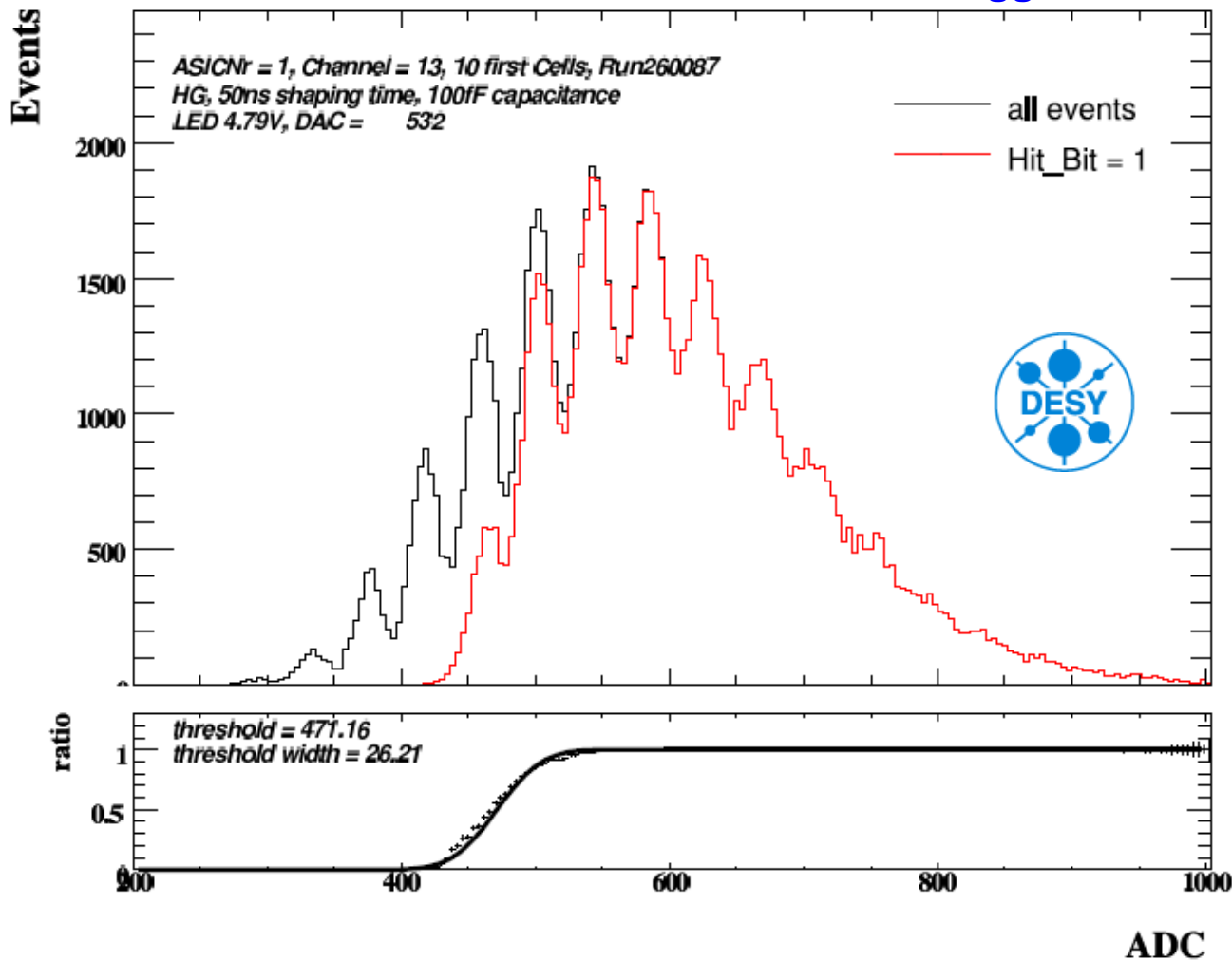


SPIROC : System On Chip





SiPM SPECTRUM with Autotrigger

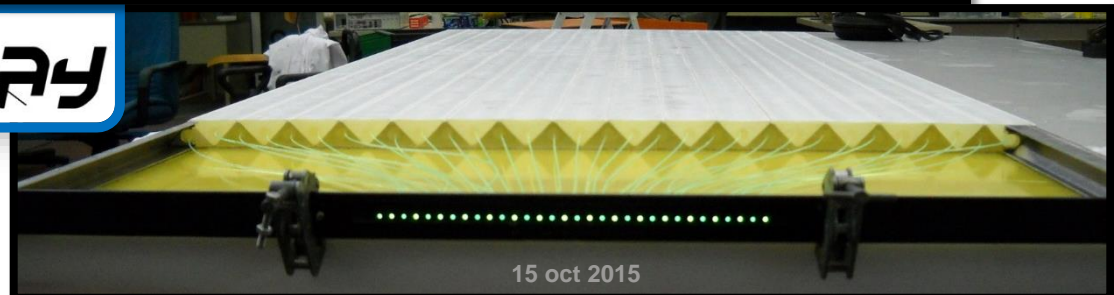
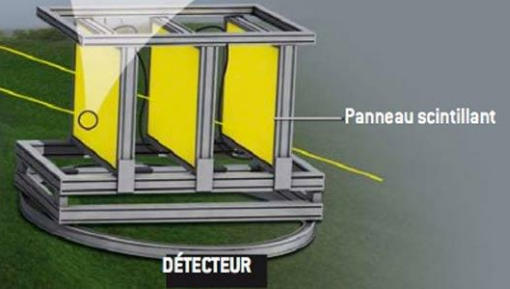
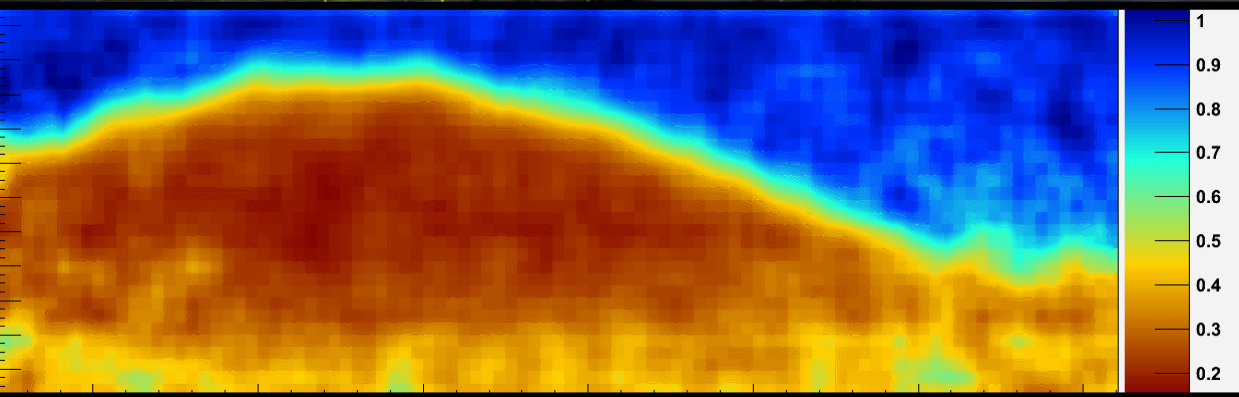
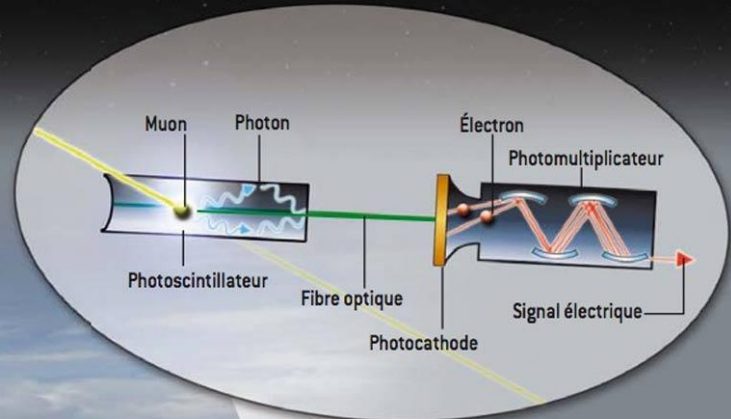


Applications : Muon tomography

Particule cosmique

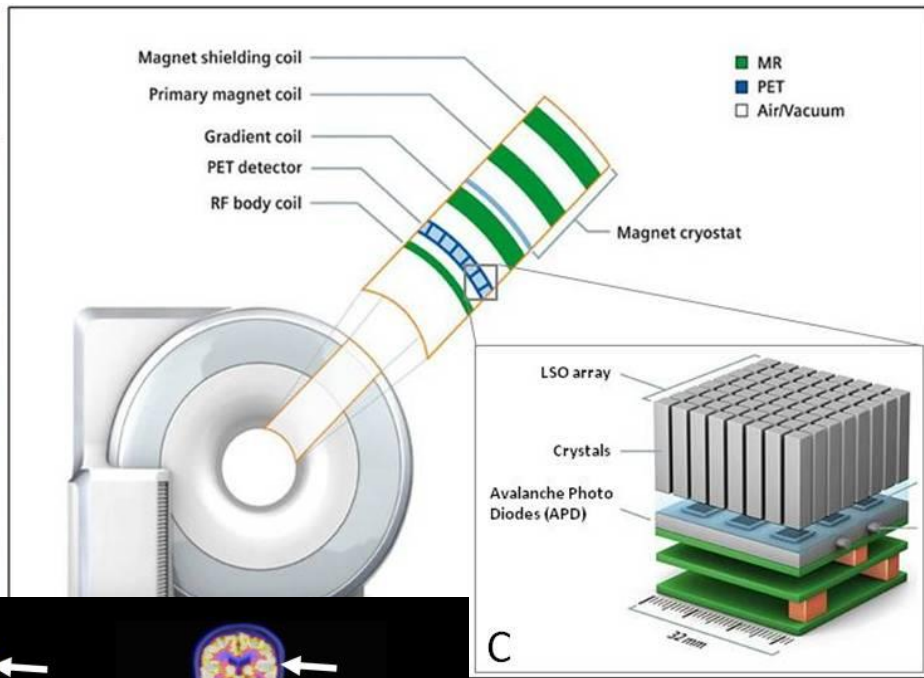
Les muons, des « électrons lourds » issus des gerbes cosmiques, ont des énergies telles qu'ils peuvent traverser la matière. Sur leur trajet dans un volcan, ils sont plus ou moins freinés, voire arrêtés, et ce d'autant plus que la quantité de matière traversée est importante. Par conséquent, le flux de muons recueillis au pied du volcan reflète l'opacité du volcan. En suivant l'évolution de ce flux en fonction du temps, on peut détecter des variations de densité.

Gerbe atmosphérique

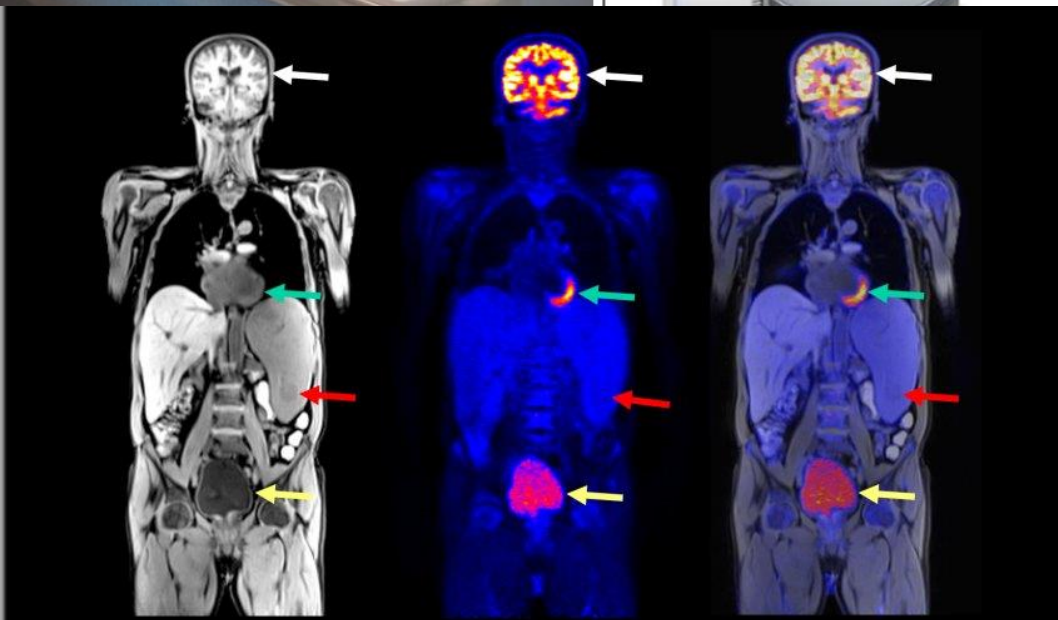




A



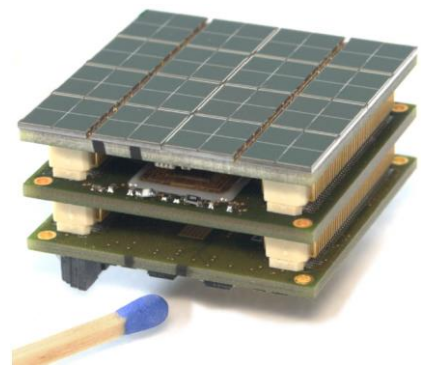
C



MRT (Struktur)

FDG-PET (Stoffwechsel)

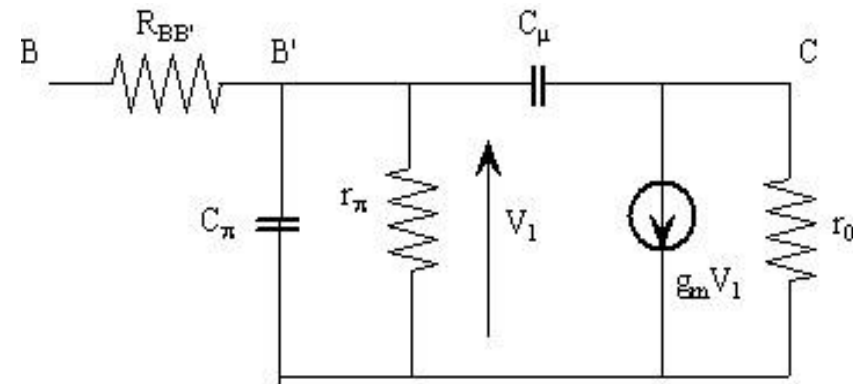
Fusion FDG-PET & MRT



- Importance of electronics in detector performance
- Fast evolution of technologies
- Readout electronics is more and more integrated on-detector.
 - Smaller, faster, lower power

Summary of transistor level design

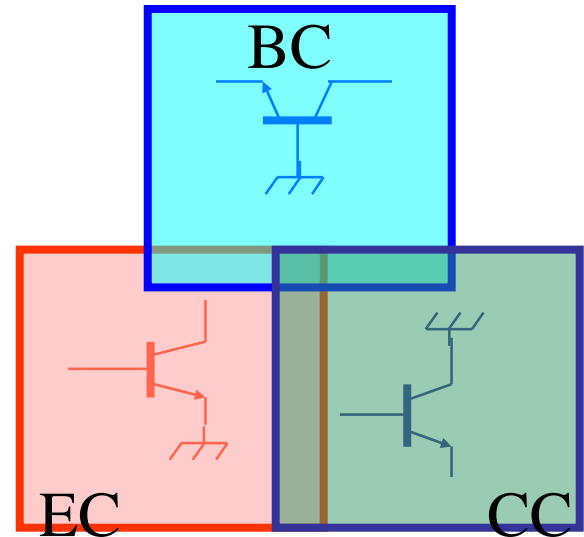
- Performant design is at transistor level
- Simple models
 - hybrid π model
 - Similar for bipolar and MOS
 - Essential for design



High frequency hybrid model of bipolar

■ Three basic configurations

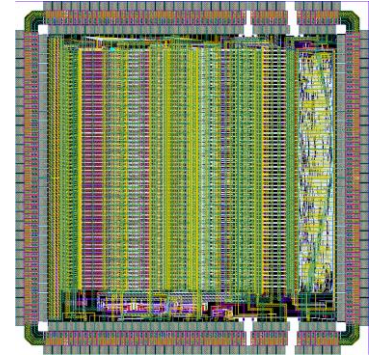
- Common emitter (CE) = V to I (transconductance)
- Common collector (CC) = V to V (voltage buffer)
- Common base (BC) = I to I (current conveyor)
- See backup slides



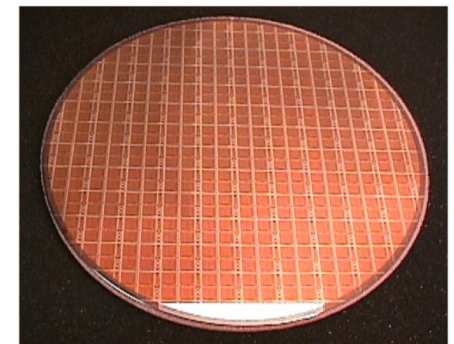
The *Art* of electronics design

- Numerous « composites »
 - Darlington, Paraphase, Cascode, Mirrors...

- ASICs : Application Specific Integrated Circuits
 - Access to foundries through **multiproject runs** (MPW)
 - Reduced development costs : 600-1000 €/mm² compared to dedicated runs (50-200 k€)
 - **Full custom layout, at transistor level**
 - mostly **CMOS & BiCMOS**
- Very widespread in high Energy Physics
 - High level of integration, limited essentially by power dissipation and parasitic couplings (EMC)
 - Better **performance** : reduction of parasitics
 - Better **reliability** (less connections)
 - But **longer developpement time**
- **Trends** :
 - Evolution of technologies (see next slides)
 - Low power design



MAROC : 64ch
MaPMT readout chip



300 mm wafer

- From Sand to ICs...

RETICLE
(Pattern with 0.7 micron apertures ie 4 X 0.18)

Lithography.

UV Light

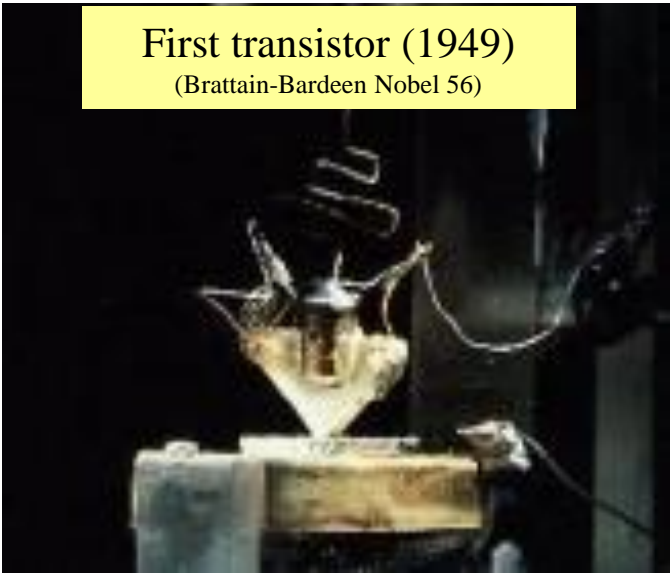
Silicon Wafer

Light Sensitive Coating.

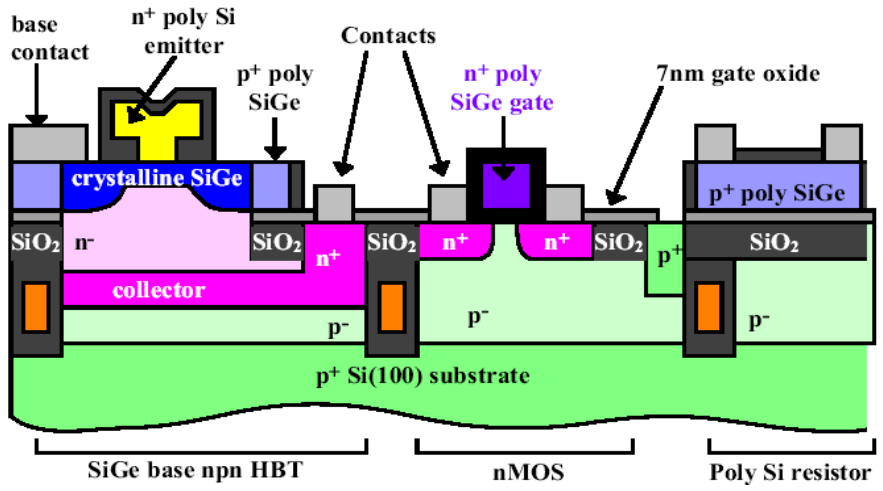
Multiple Layers.
>350 process steps.

CREATING > 125 million TRANSISTORS ON EACH MICROPROCESSOR;
WITH FEATURES 1/2000th THE WIDTH OF A HUMAN HAIR.

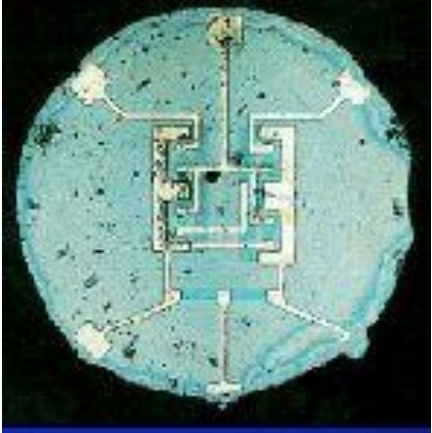
The diagram illustrates the lithography process. It starts with a Silicon Wafer (black circle) which is coated with a Light Sensitive Coating (green oval). A Reticle (a patterned mask) is used to project UV Light (represented by a lightbulb) through the coating. This process is repeated for multiple layers, involving more than 350 process steps. The final result is a microprocessor with a grid of transistors (yellow oval with small squares). An inset photo shows a technician in a cleanroom environment handling a large, circular silicon wafer.



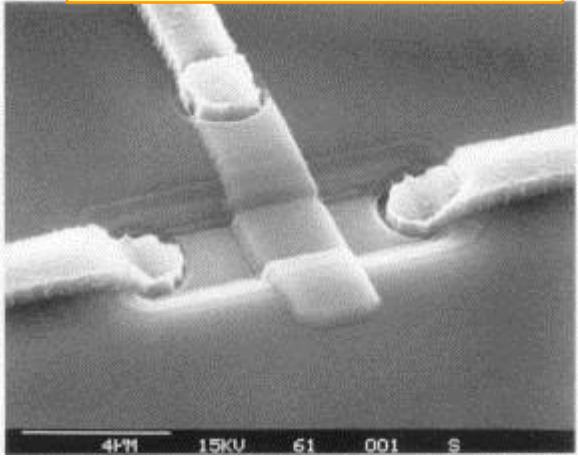
SiGe Bipolar in 0.35µm monolithic process



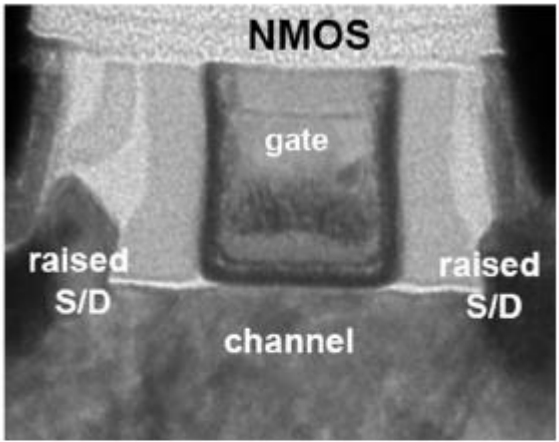
First planar IC (1961)



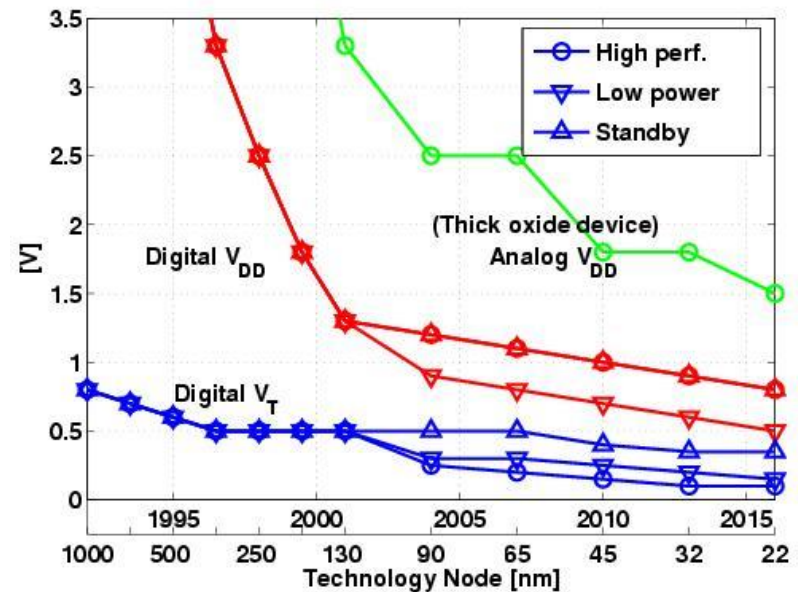
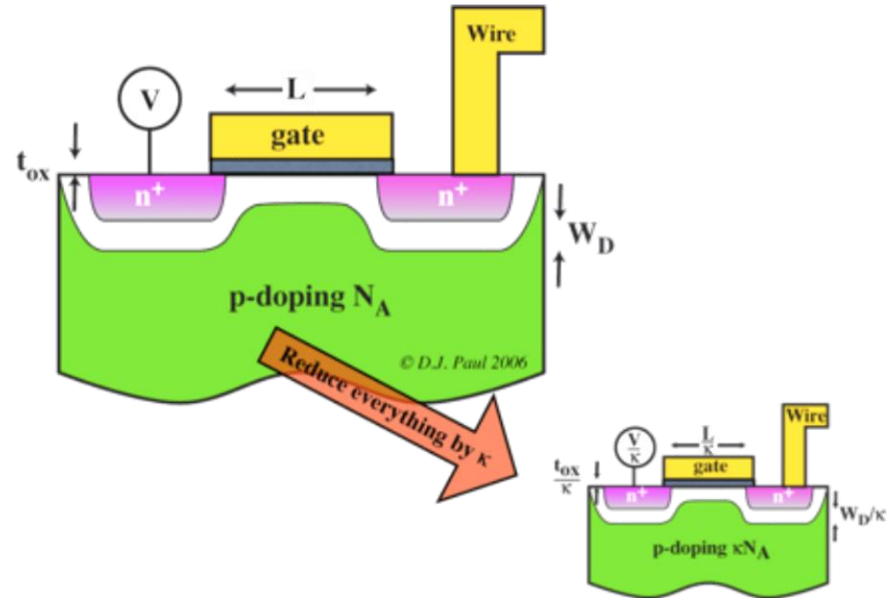
5 µm MOSFET (1985)



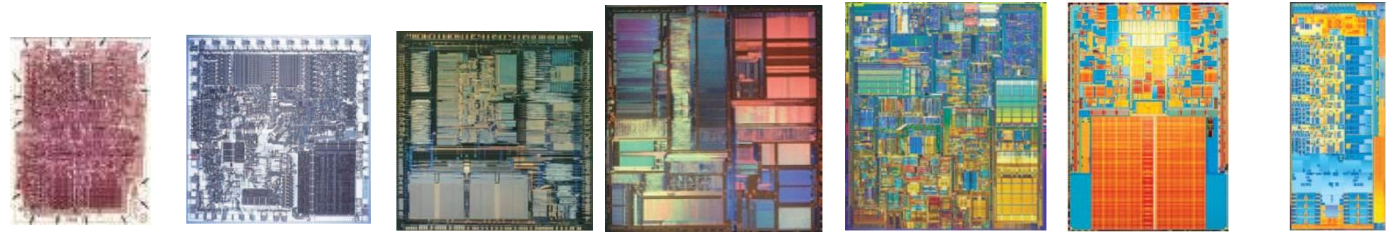
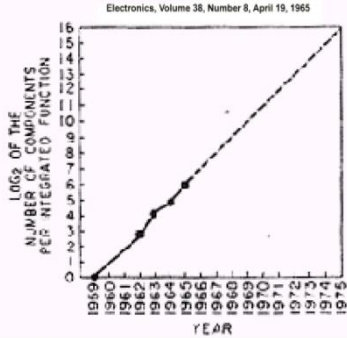
32 nm MOSFET (2010)



- Reduction of dimensions
 - « Quasi-constant voltage scaling »
 - Decrease of W, L, t_{ox}
 - (partial) decrease of V_{DD} et V_{Th}
- Improvement of speed as $1/L^2$
 - Improvement of transconductance as W/L and reduction of capacitance as WL
- Power increases as k and power density even worse
 - V_{DD} does not scale as L

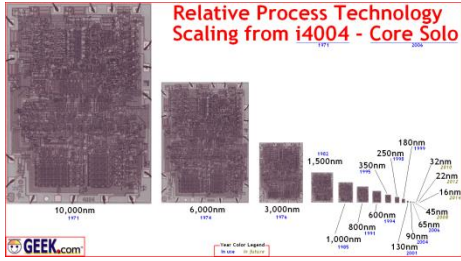


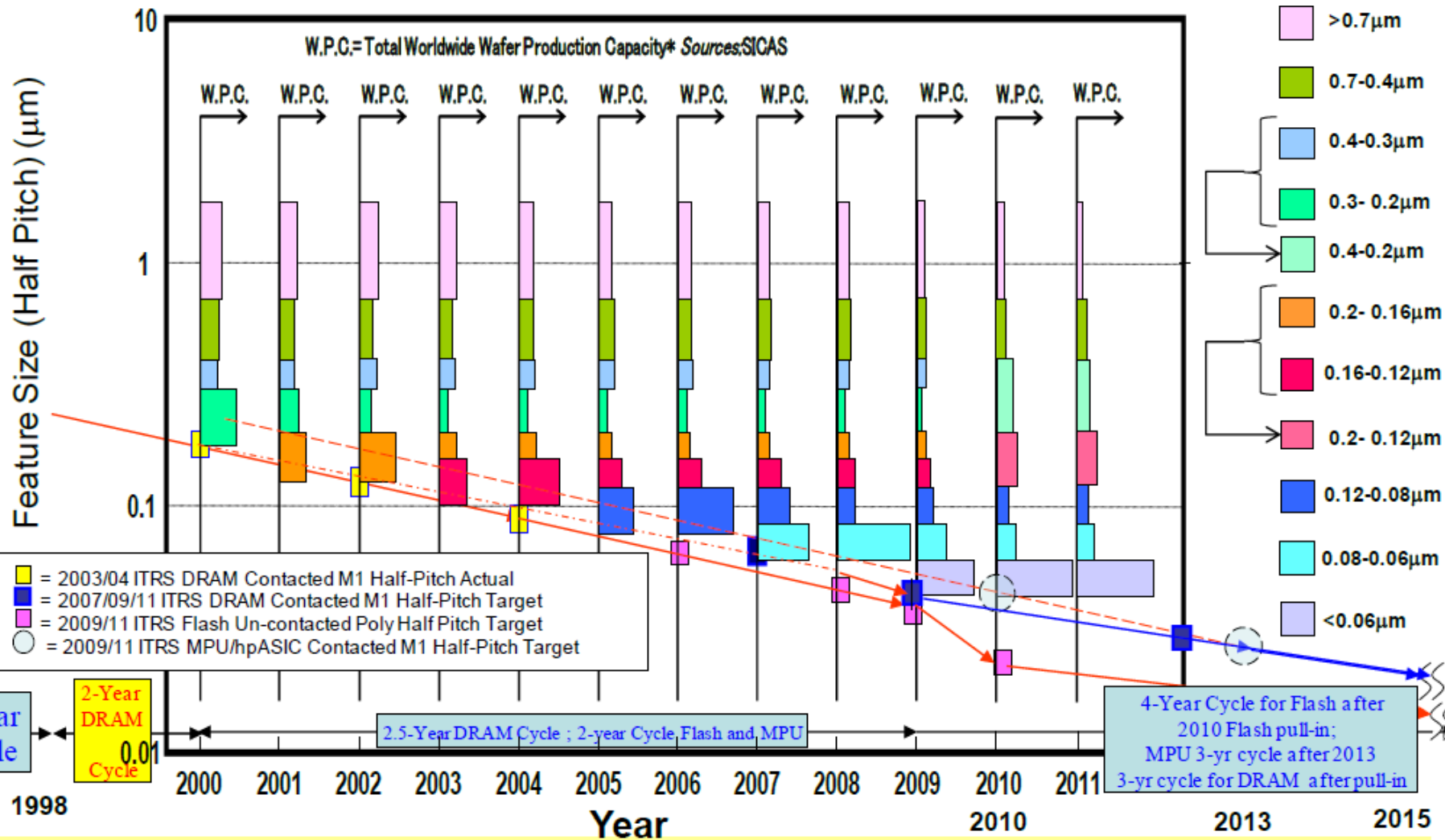
- Moore's law : number of transistors doubling every ~2 years
- Technology nodes (gate length) *0.7 every 2 years



Processor	4004	8086	i386	Pentium	Pentium 4	Core2	3G Core7
Year	1971	1978	1985	1993	2000	2007	2012
Clock	108 kHz	10 MHz	16 MHz	66 MHz	1.5 GHz	2.4 GHz	2.9 GHz
Technology	10 μm	3 μm	1.5 μm	0.8 μm	0.18 μm	65 nm	22 nm
Nb transistors	2300	29000	275000	3.1M	42M	291M	1.4G

<http://www.intel.com/content/www/us/en/history>





* Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 1Q data for 2011. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.

<http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf>



Example of prices, prototyping



© K. Troki (CMP)

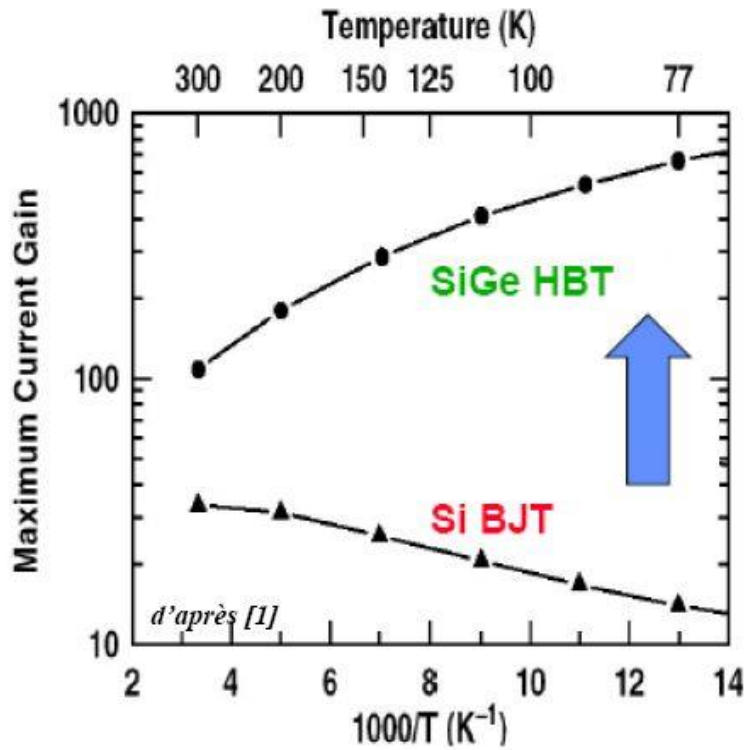
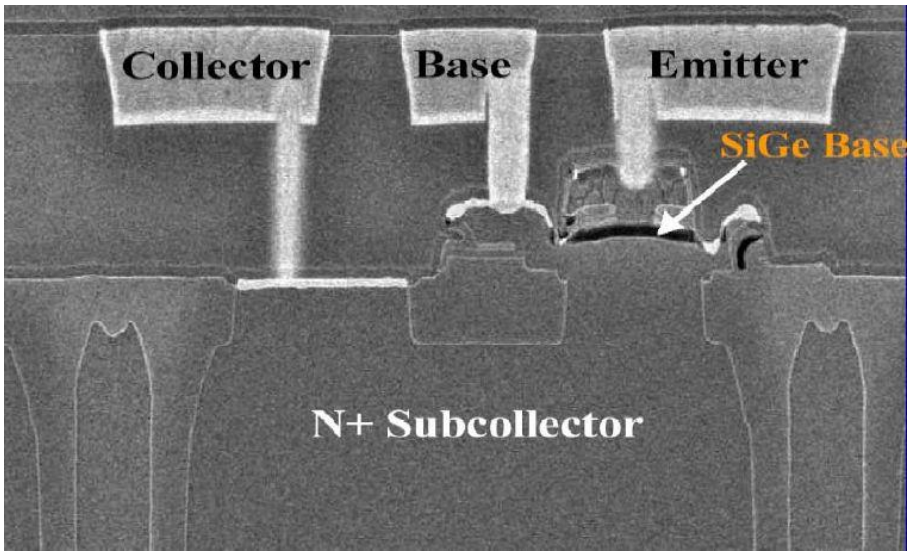
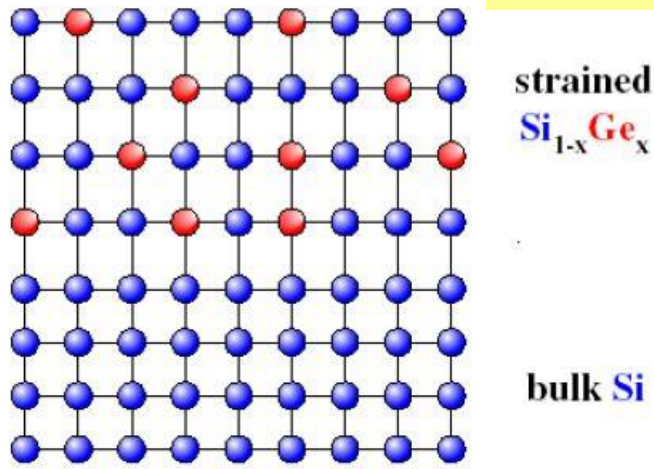
CMOS	.35 μ	AMS	650 €/mm ²
CMOS opto	.35 μ	AMS	810 €/mm ²
CMOS HV	.35 μ	AMS	1000 €/mm ²
CMOS	130nm	ST	2200 €/mm ²
CMOS	65 nm	ST	7500 €/mm ²
CMOS	40 nm	ST	15000 €/mm ²
SiGe BiCMOS	.35 μ	AMS	890 €/mm ²
SiGe:C BiCMOS	130nm	ST	3500 €/mm ²
SOI	130nm	ST	4000 €/mm ²
SOI	65nm	ST	9500 €/mm ²
Poly-SOI-Metal	MUMPS	MEMSCAP	3700 €/cm ²

CMP annual users meeting, January 20th 2011, PARIS

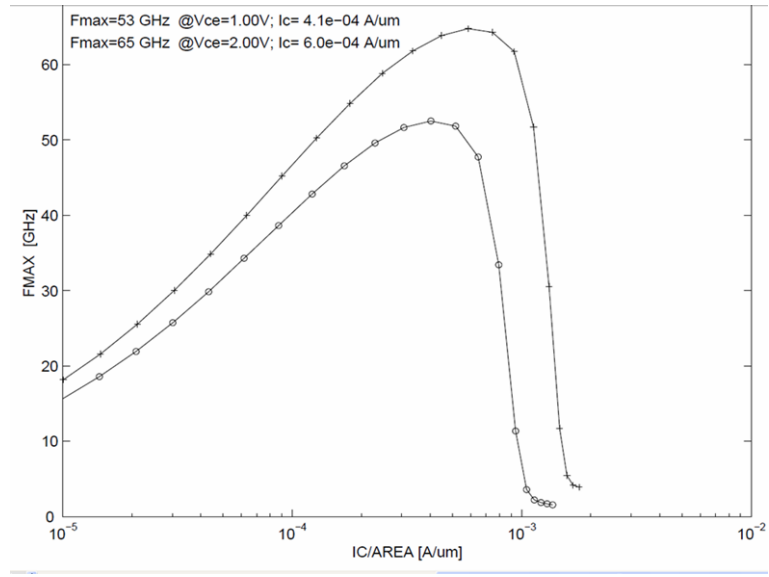
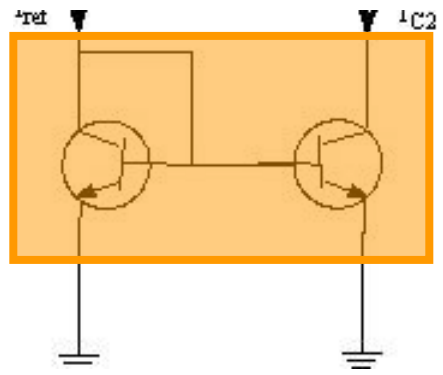
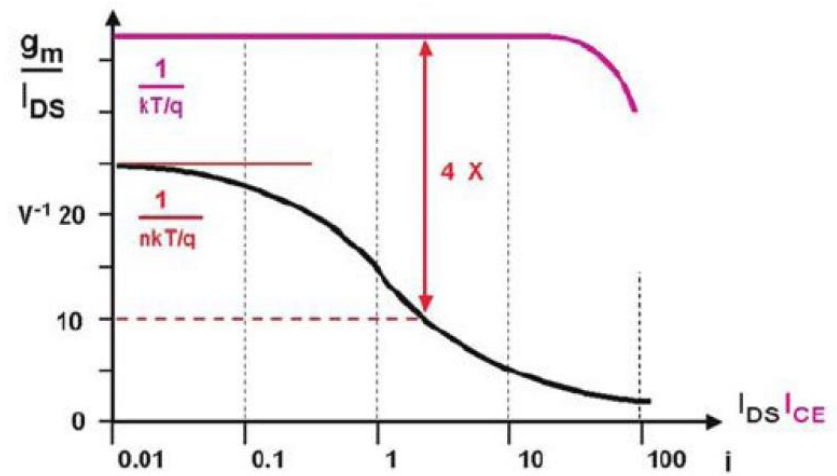
http://cmp.imag.fr/aboutus/slides/Slides2011/02_Runs_2011.pdf

© R. Hermel

- Faster bipolar transistors for RF telecom
 - Better mobility and FT
 - Better current gain (beta)
 - Better Early voltage
 - Interesting improvement at low T
 - Compact CMOS (0.25 or 0.35µm) for mixe



- BJT : best g_m/I ratio ($1/U_T$)
 - Large transconductance with small devices
- Speed goes as $F_T = g_m/2\pi C$
 - $C \sim 10$ fF g_m typ mA/V
 - $F_T \sim 60$ GHz for SiGe $0.35\mu\text{m}$
 - Interesting for fast preamps
- Not forgetting 100V Early voltage and **matching** performance ($A \sim \text{mV} \cdot \mu\text{m}$)
- $V_{BE} = V_T \ln(I_C/I_S)$
- Large swing : $V_{CEsat} \sim 3 U_T$



Intel CMOS Transistor Architecture Evolution in the Last Decade

.13 um and before

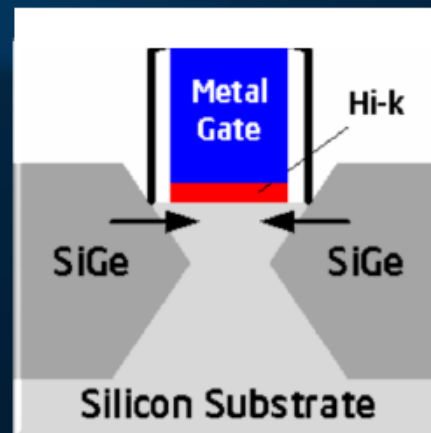
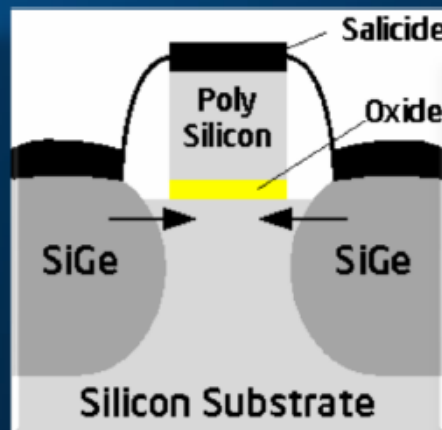
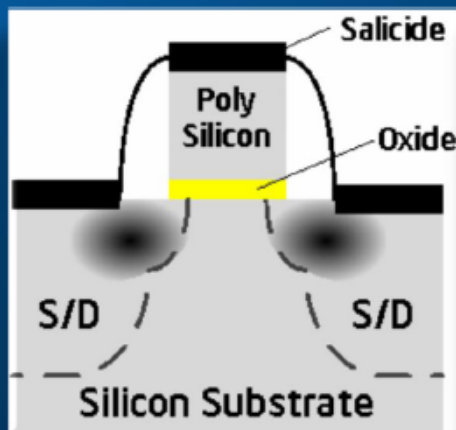
90nm/65 nm

45 nm/32 nm

Traditional

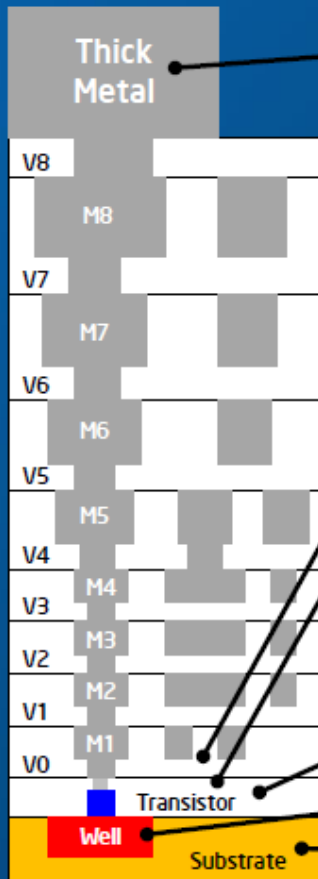
Strained Silicon

High k/Metal Gate +
Strained Silicon

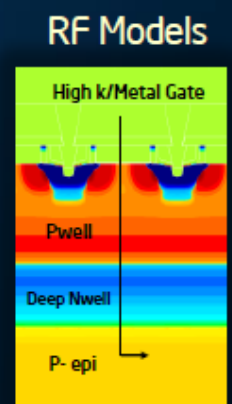
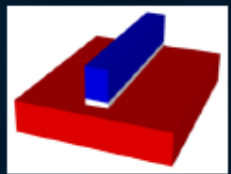
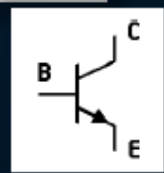
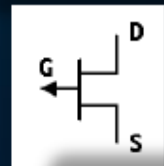
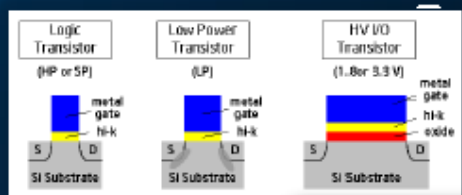
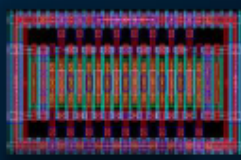


CMOS scaling has evolved from classical dimensional scaling to modern scaling with innovations in structures and materials

32 nm RF CMOS Technology

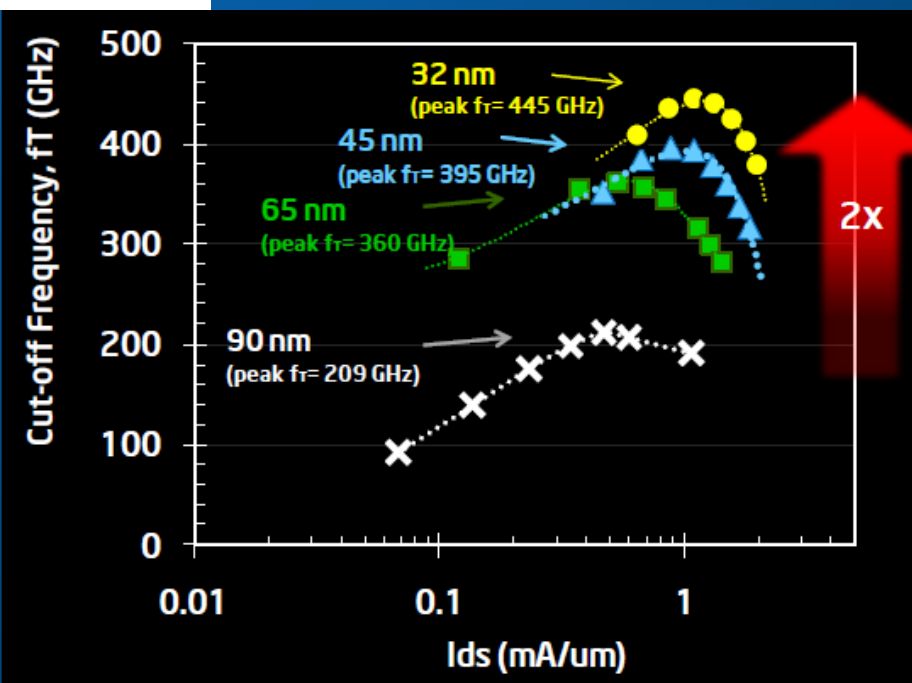


- **TM1 Inductor:** high Q and density
- **Passives:**
 - Precision Resistor
 - High Q Inductor
 - High Density Decap
- **HV PA Transistor**
- **RF Transistor:** Templates/Modeling
- **Transistor:**
 - Logic, low power, I/O
 - JFET, BJT
- **Well:** Triple Well/Deep Nwell
- **Substrate:** High Resistivity



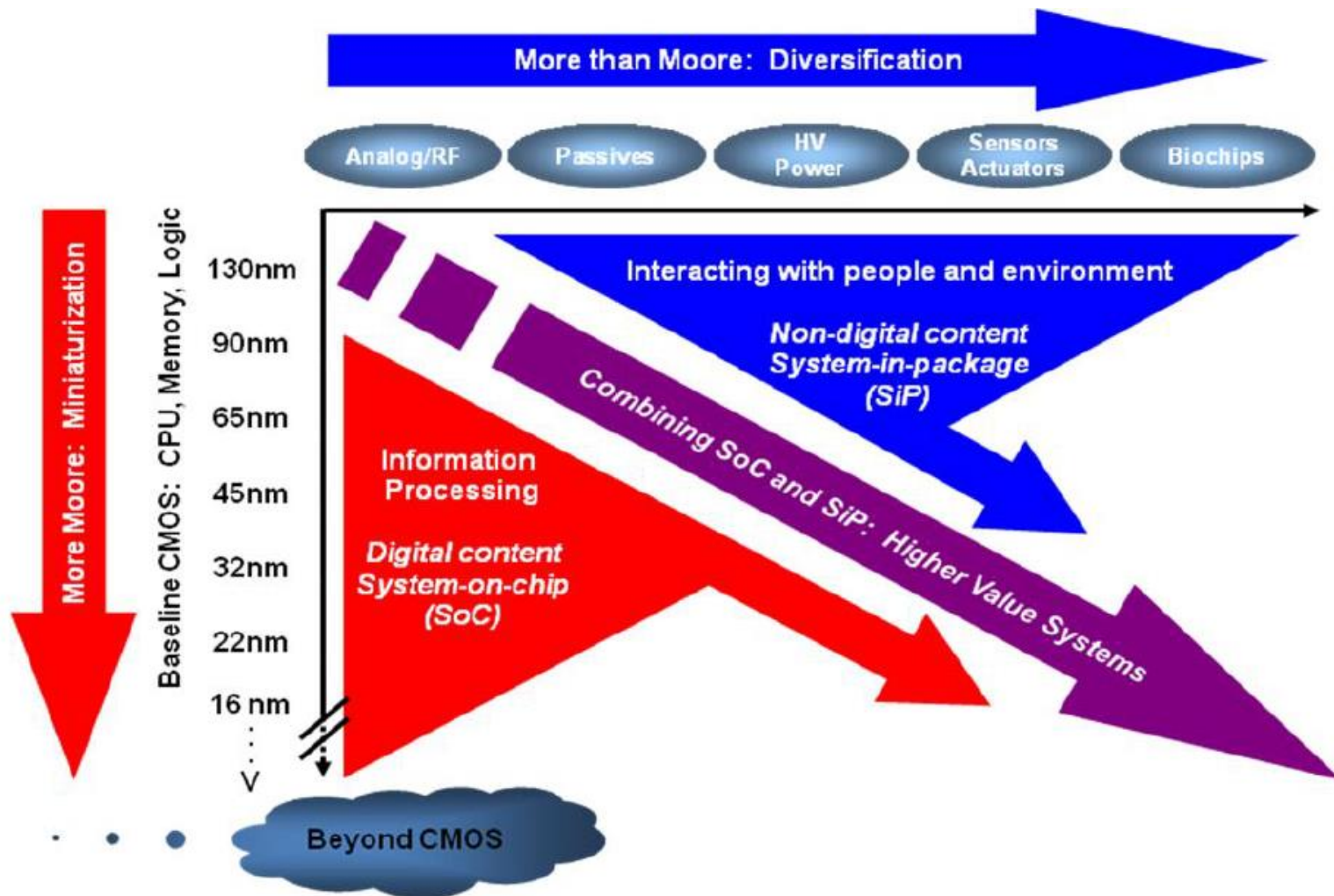
Basic 32 nm CMOS technology is expanded with many more mixed signals/RF features to meet RF SoC requirements

RF CMOS Technology Performance Metrics



RF Devices	RF Circuits	Key Device Characteristics
Logic Transistor	MAC/BB, ADC, DAC	I_{dsat} , I_{dlin} , V_t , I_{off}
Analog Transistor	ADC, DAC, MAC/BB	G_m , R_{out} , Matching, Linearity, Noise, NF_{min}
RF Transistor	PA, Mixer, T/R Switch	f_T , f_{max} , $1/f$ Noise, NF_{min}
PA Transistors	PA	R_{on} , Linearity, f_T , f_{MAX} , Efficiency, Breakdown V ,
Precision Resistors	ADC, DAC, BB Filter, others	R , $\sigma R/R$, Matching
Linear Capacitors	PLL, VCO	C , Q , Matching
Varactors	PLL, VCO	Tuning Ratio, Q , KV_{CO} ,
Inductor/Transformer/Balun	PA, LNA, Mixer	L , Q

What are the impacts of CMOS scaling on these metrics ?



Generic MOSFET scaling trends

Novel materials and architectures



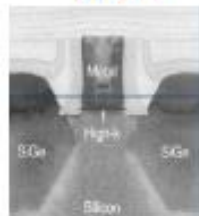
http://www.sematech.org/meetings/archives/symposia/9027/pres/Session%202/Jammy_Raj.pdf

New Mat'l/Structure



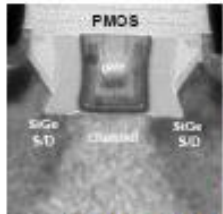
High-K
MG

45nm
2007



(Production)
Intel IEDM 2007

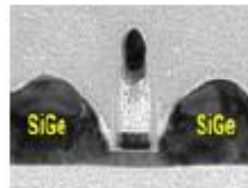
32nm
2009



(Production)
Intel IEDM 2009

planar

22nm
2011+



IBM, IEDM 2009

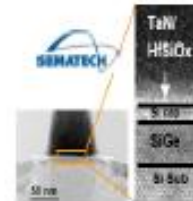
16nm (?)
2013+



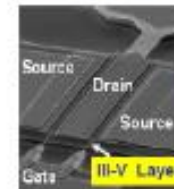
6nm Length
B. Doris IEDM 2002

12 nm + (2015+)

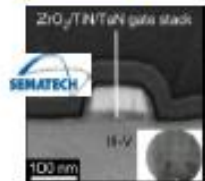
Si-Ge Device



III-V Device



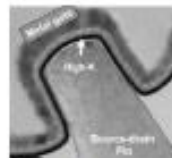
Intel,
IEDM 2007,9



T-FET



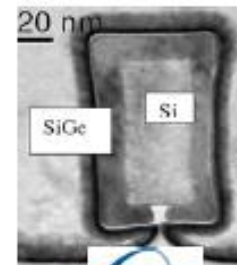
Non-planar



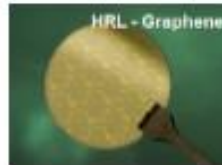
Intel Tri-Gate,
VLSI 2006



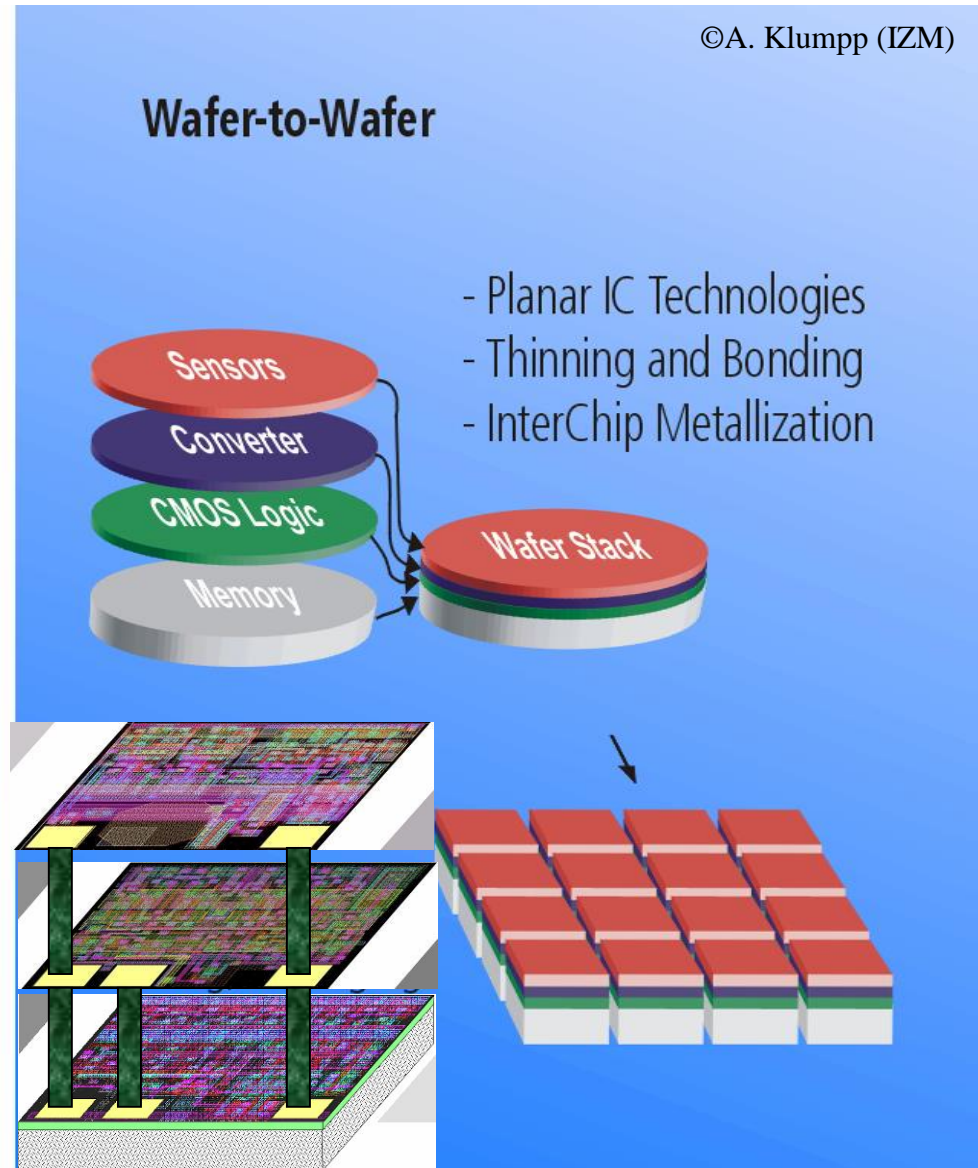
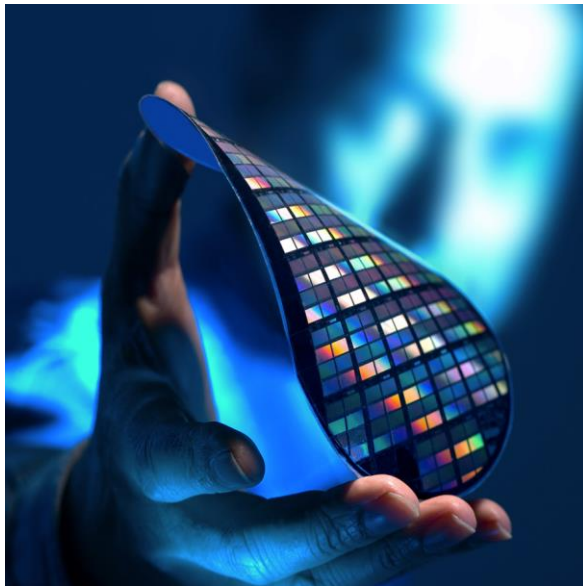
NXP FINFET, VLSI 2007



Nano-wire (LETI IEDM'08)

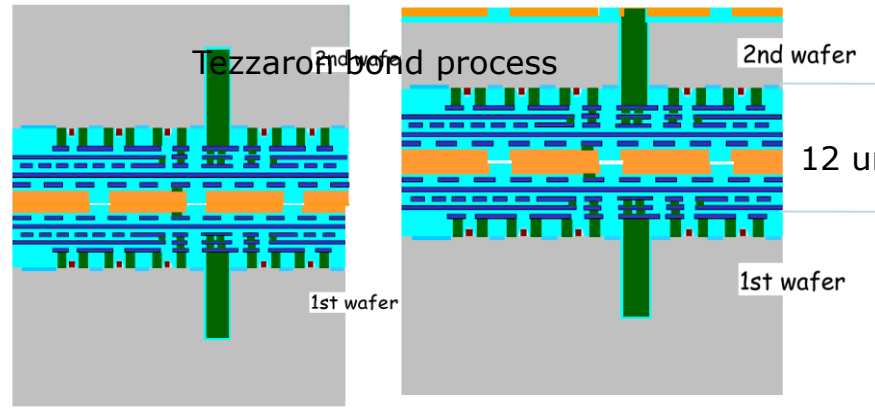
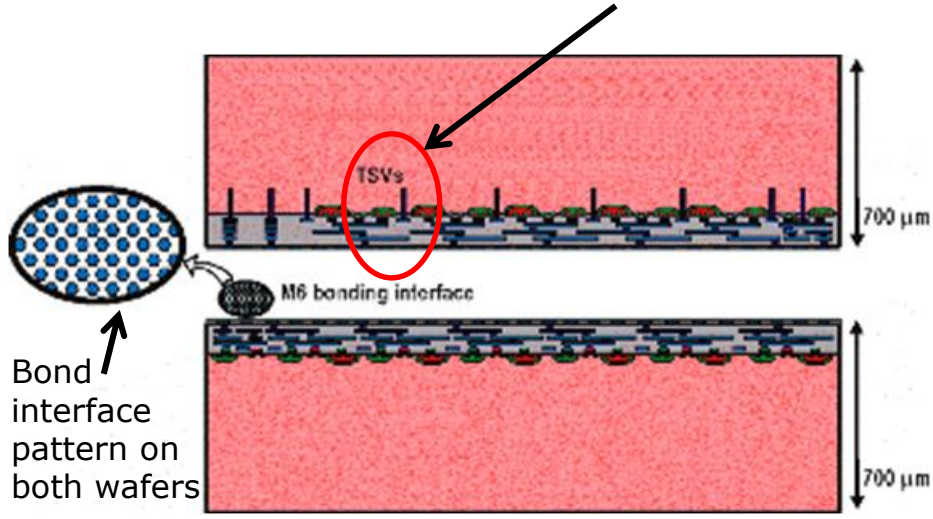
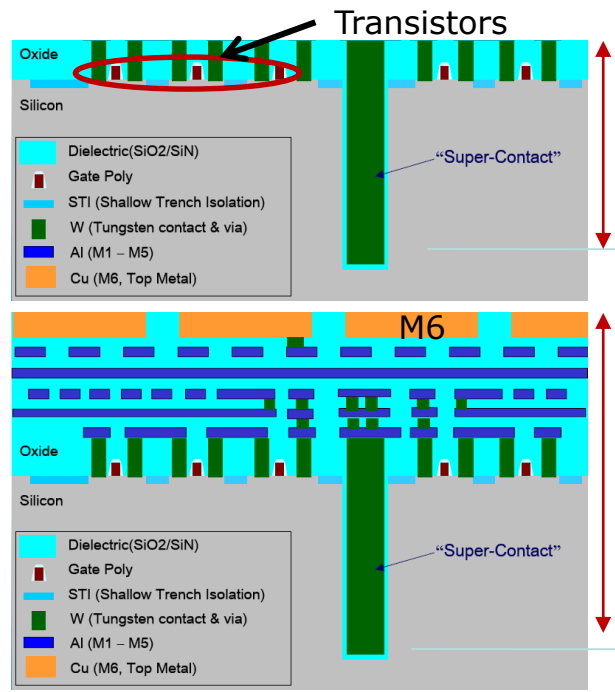


- Increasing integration density, mixing technologies
- Wafer thinning to $<50\ \mu\text{m}$
- Minimization of interconnects
- Large industrial market
 - Processors, image sensors...



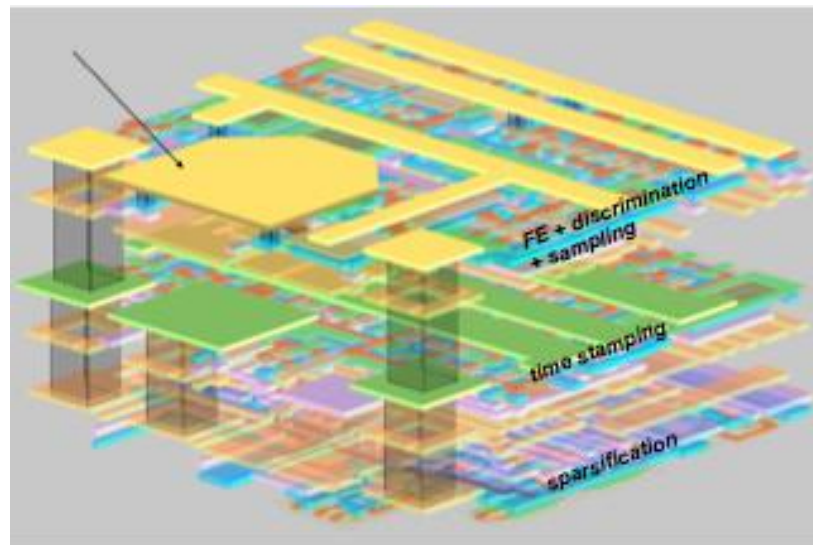
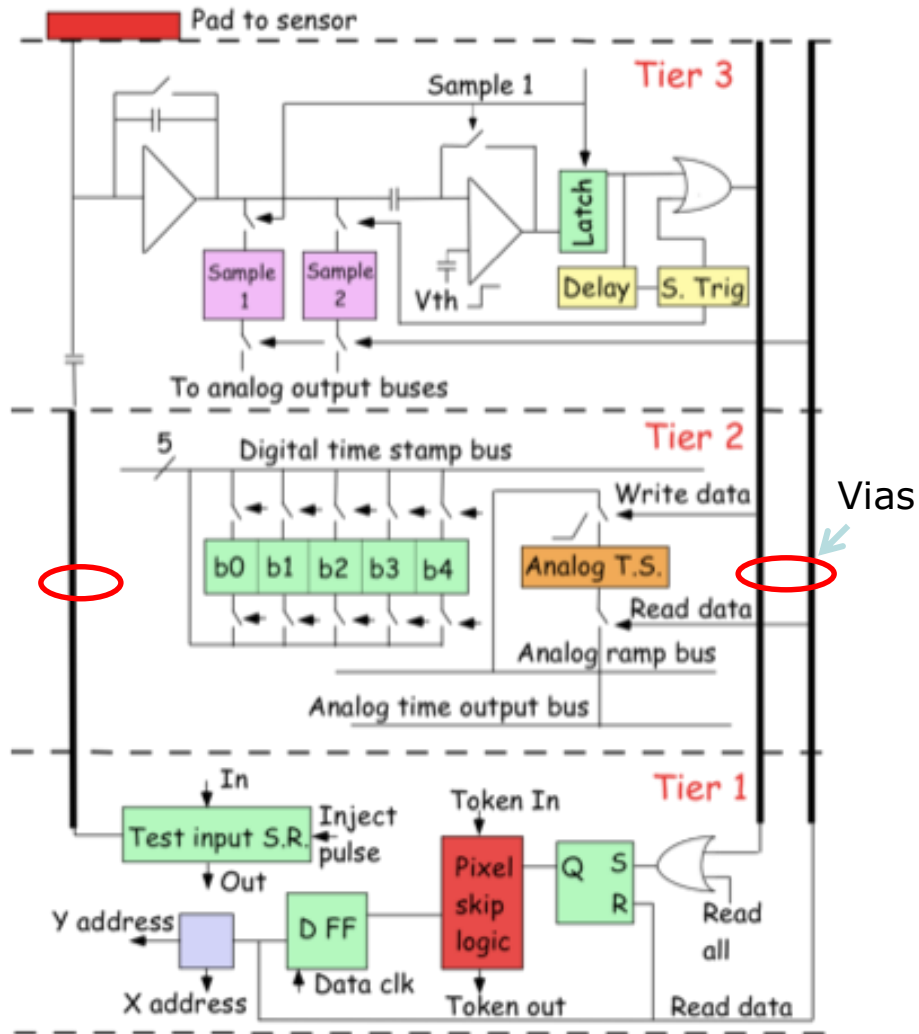
© R. Yarema (FNAL)

- Access to 3D via Tezzaron
 - 130 nm Global foundry wafers
 - 1μm vias (Via middle process)
 - Cu-Cu bonding face to face

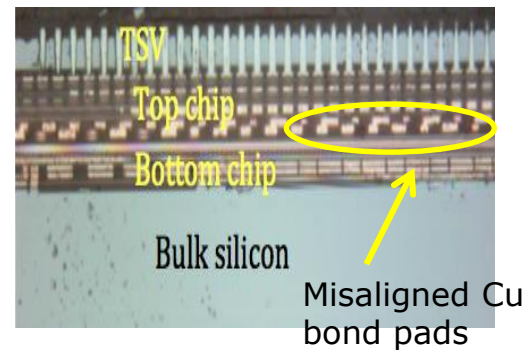


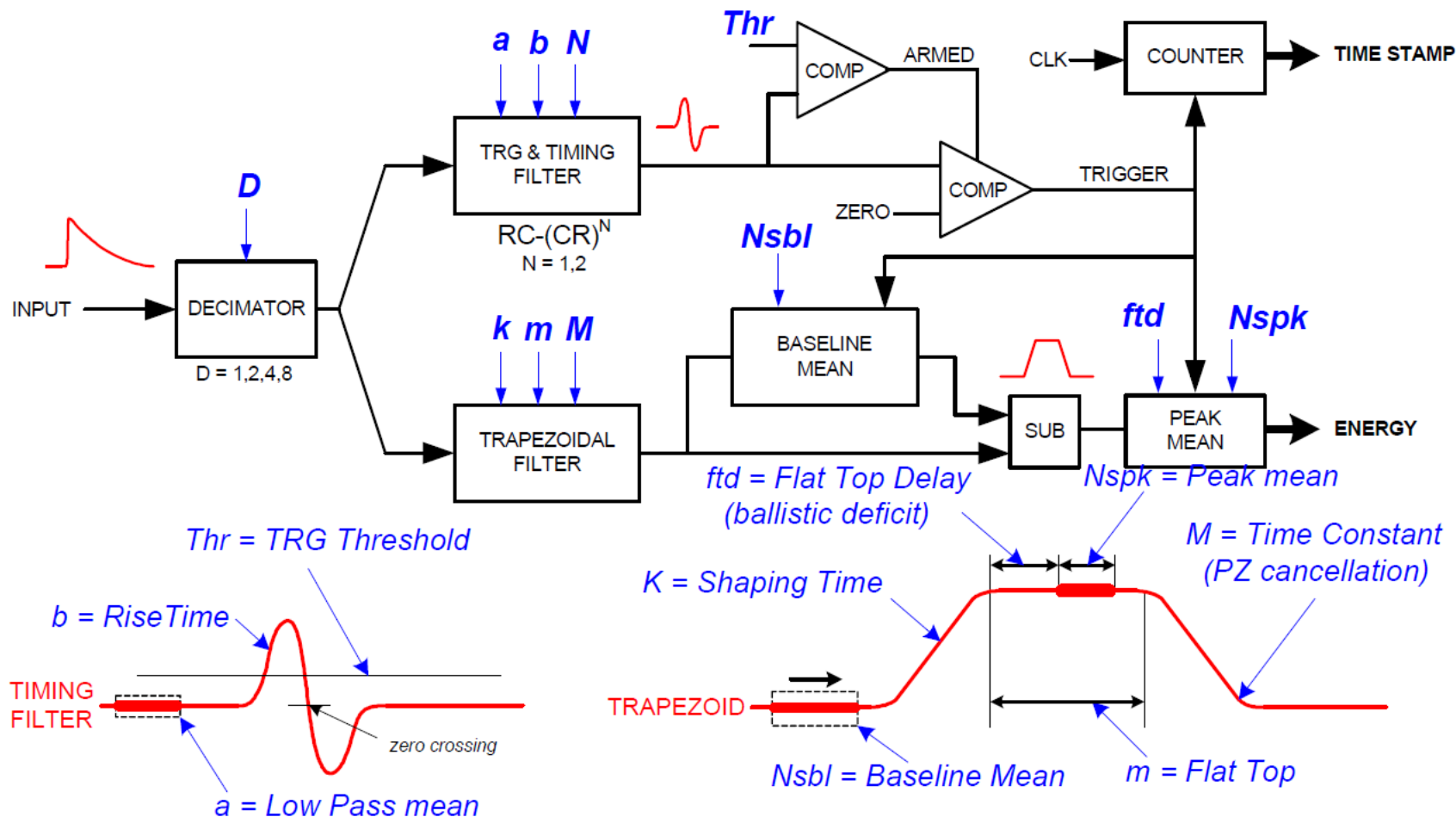
Exampe of realization at FNAL

© R. Yarema (FNAL)



VIP1 3D chip by FNAL





C. Tintori (CAEN)
 V. Jordanov *et al.*, NIM **A353**, 261 (1994)

Example of SoC : OMEGA « ROC chips »

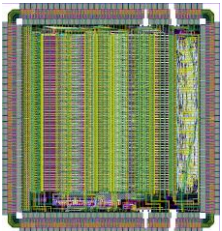


- Use of Silicon Germanium 0.35 μm BiCMOS technology since 2004
- Readout for MaPMT and SiPM for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)

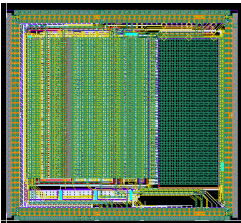
<http://omega.in2p3.fr>

Chip	detector	ch	DR (C)
MAROC	PMT	64	2f-50p
SPIROC	SiPM	36	10f-200p
SKIROC	Si	64	0.3f-10p
HARDROC	RPC	64	2f-10p
PARISROC	PM	16	5f-50p
SPACIROC	PMT	64	5f-15p
MICROROC	μMegas	64	0.2f-0.5p
PETIROC	SiPM	32	10f-200p

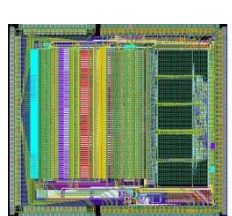
MAROC3



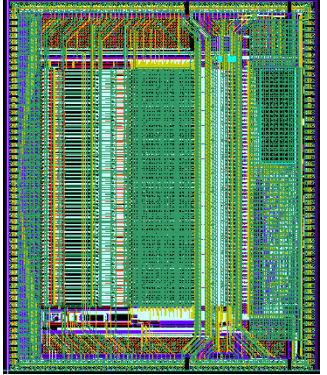
HARDROC2



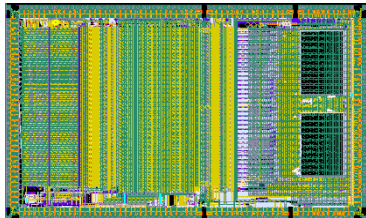
MICROROC1



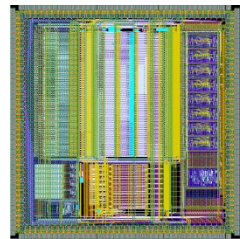
SKIROC2



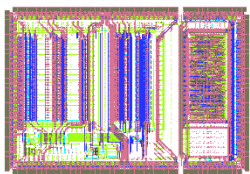
SPIROC2



SPACIROC

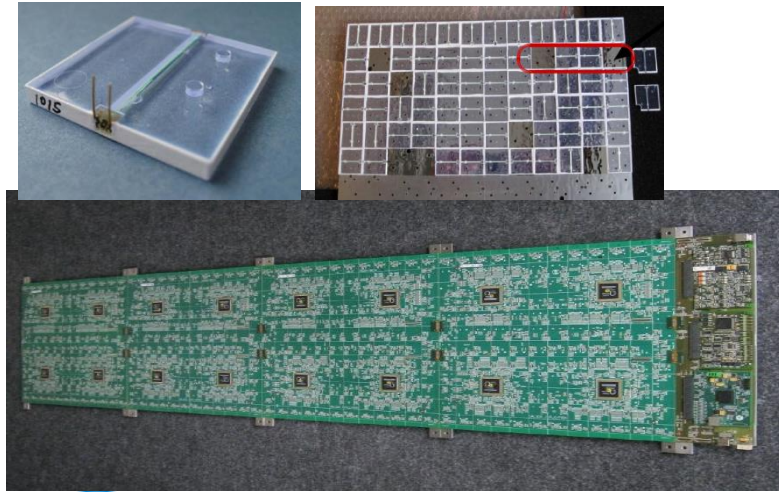


PARISROC2

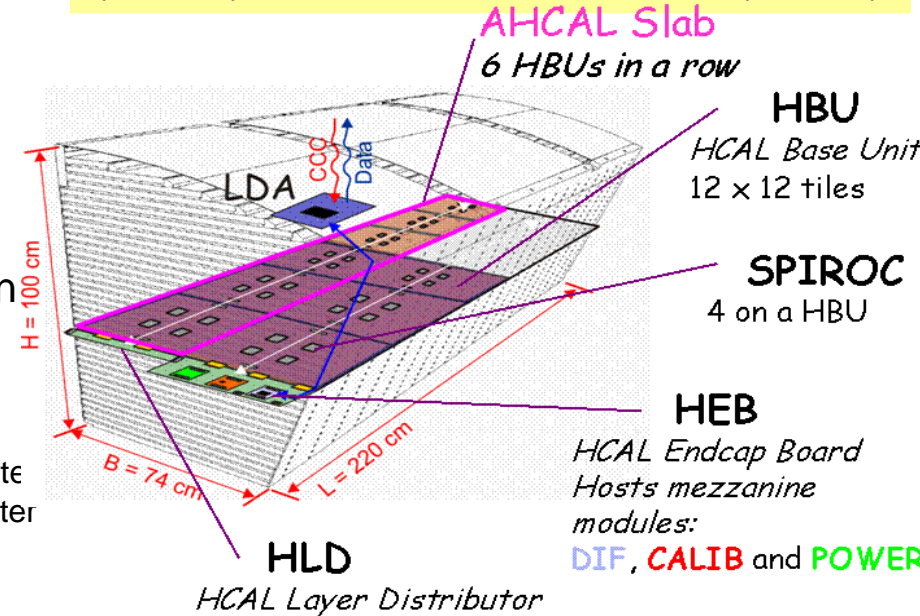


Example : SPIROC for SiPM

- SPIROC : Silicon Photomultiplier Integrated Readout Chip to read out the analog hadronic calorimeter for CALICE (ILC)
- **Ultra low-power 36-Channel ASIC**
- **Internal input 8-bit DAC** (0-5V) for individual SiPM gain adjustment
- **Energy measurement : 14 bits, 1 pe to 2000 pe**
 - pe/noise ratio : ~11
- **Auto-trigger on MIP or on single photo-electron**
 - Auto-Trigger on 1/3 pe (50fC)
- **Time measurement :**
 - 12-bit Bunch Crossing ID (coarse time)
 - 12-bit step~1 ns TDC->TAC (fine time)
 - Analog memory for time and charge measurement : depth = 16
 - **Low consumption** : ~25 μ W per channel (in power pulsing mode)
 - **4kbytes internal memory and daisy chain readout**

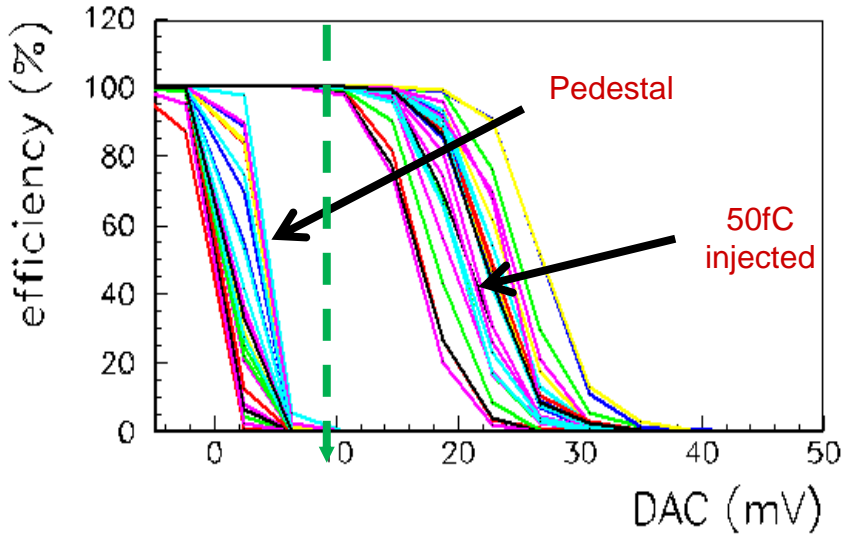


(0.36m)² Tiles + SiPM + SPIROC (144ch)

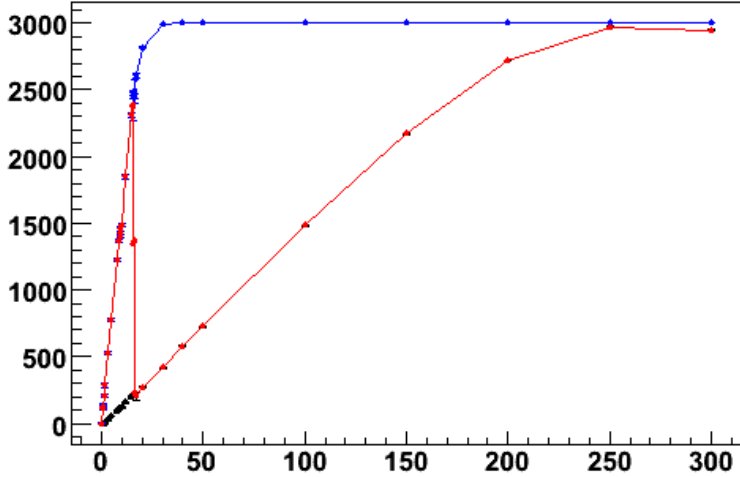


M. Bouchel et al. "SPIROC (SiPM integrated read-out chip): Dedicated very front-end electronics for an ILC prototype hadronic calorimeter with SiPM read-out," JINST, C01098 (2011).

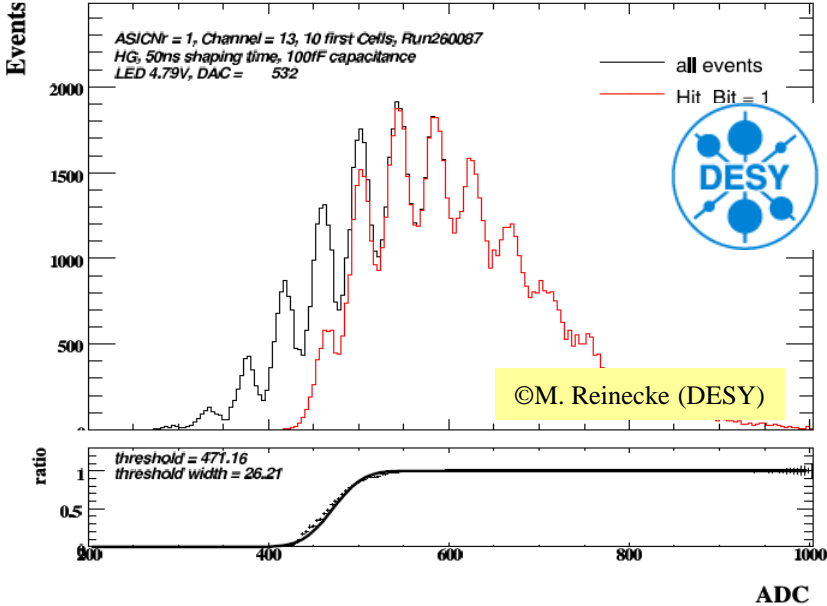
36-channel S-curves: trigger efficiency versus threshold (1 LSB = 2 mV)



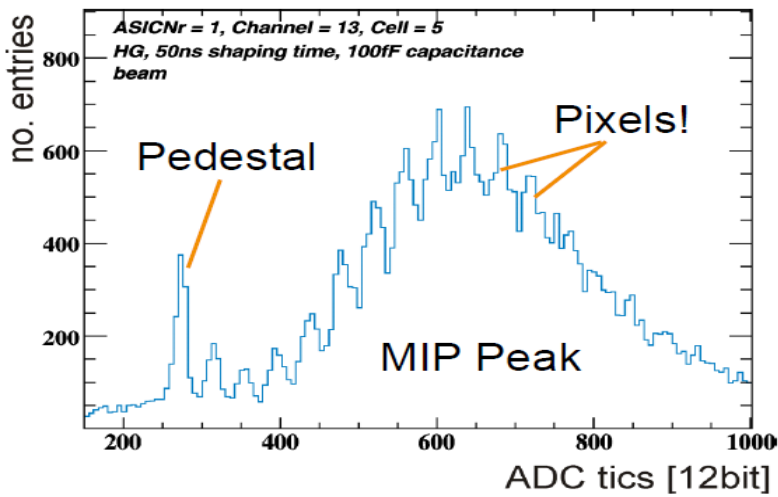
linearity using the auto gain mode and internal ADC



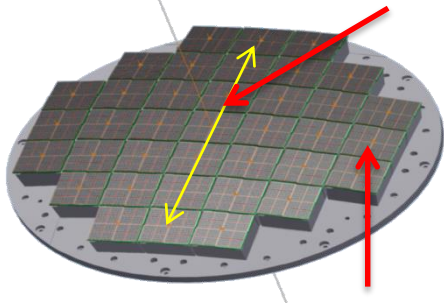
SiPM SPECTRUM with Autotrigger



MIP response in DESY 6 GeV electron testbeam

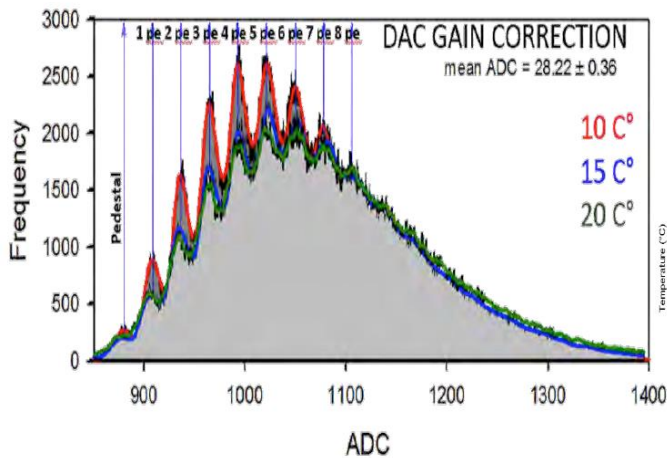


FOV = 9.6°
Ø = 350mm

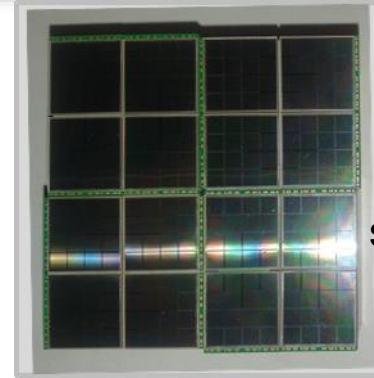
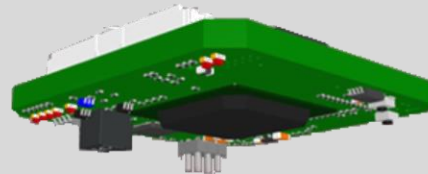
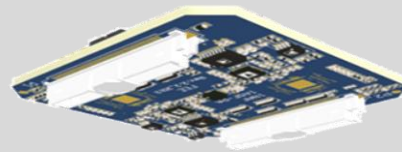
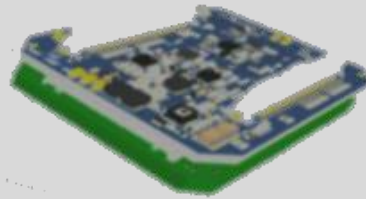
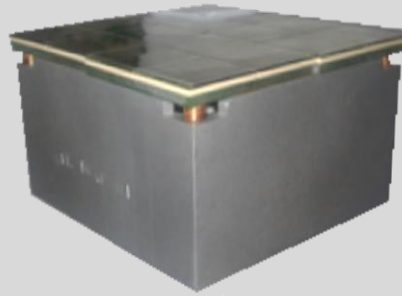


Photon Detection Module (PDM)
Pixel = 0.17° → 6.2 x 6.2 mm

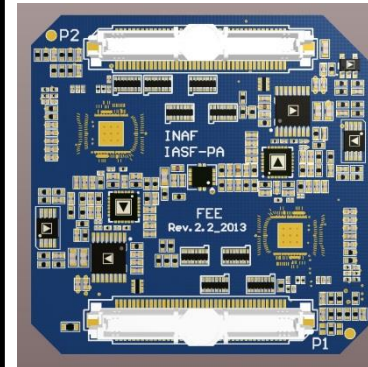
© O. Cataneo INAF Palermo



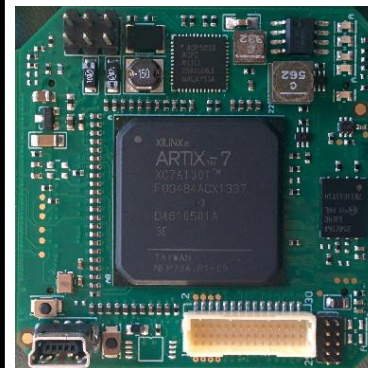
ASSEMBLING



SiPM board
(9 +1 temperature
sensors embedded)

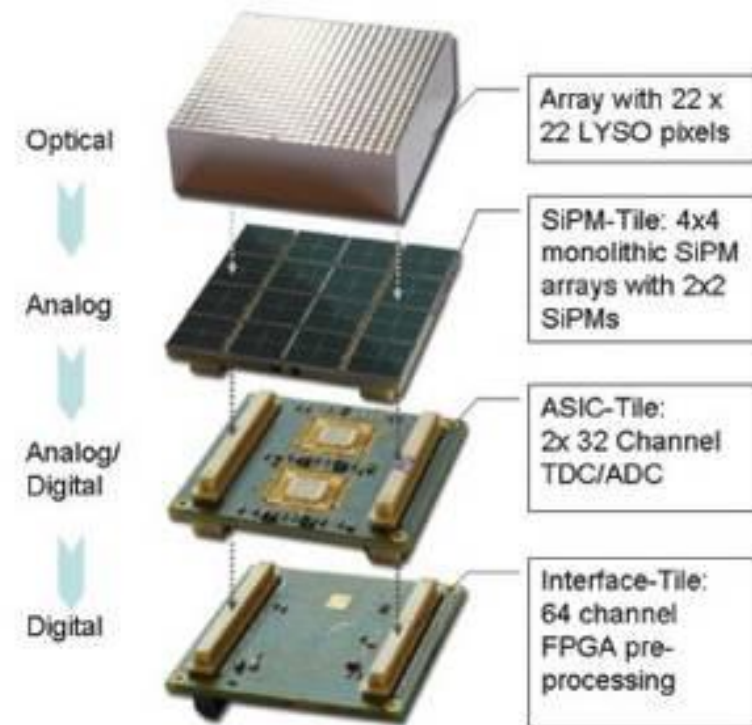
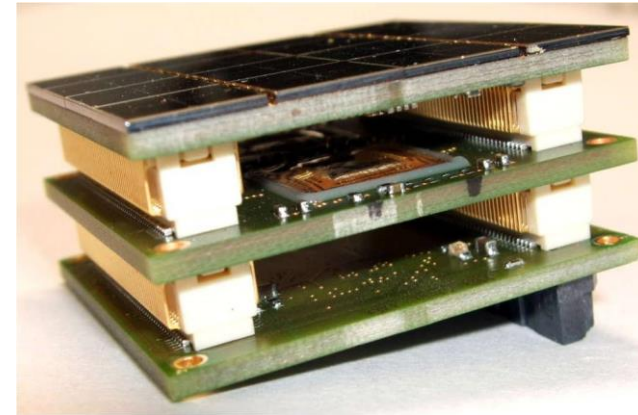


Front-End board
(2 CITIROC
ASIC)



PDM FPGA Board
(XILINX ARTIX 7)

- PET/MRI projekt
 - P. Fischer et al. Heidelberg, Philips, Aachen, FBK Trento
- 40-channel system on chip for readout of the detectors that generate low voltage (several mV) signals
- Combined high precision time (~ 14 ps) and energy measurements (signal integral = energy)
- Time of flight measurements with energy discrimination
- Particle recognition, by mass measurement
- Medical imaging (SiPM based PET)
- [M. Ritzert...: “Compact SiPM based Detector Module for Time-of-Flight PET/MR” on IEE NPS Real Time Conference



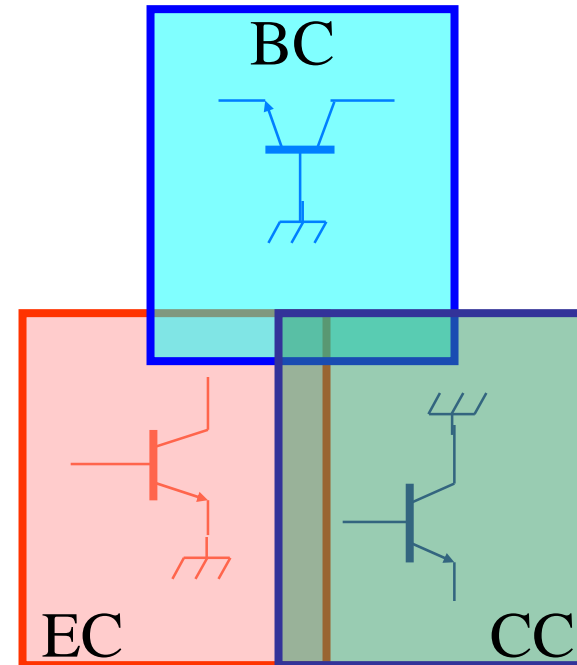
- Have fun designing electronics for future detectors !

44

Large collaborations... [V. Radeka]



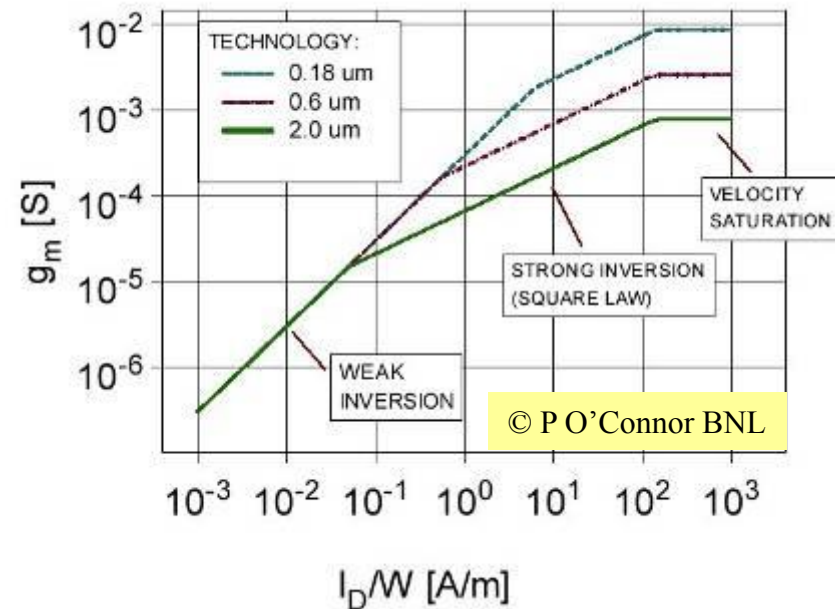
- Three basic bricks
 - Common emitter (CE)
 - Common collector (CC)
 - Common base (BC)
- Numerous composites
 - Darlington
 - Paraphase
 - Cascode...
- Simple models
 - hybrid π model
 - Similar for bipolar and MOS
 - Essential for design
- + Powerful simulation tools
 - Spice, Spectre, Eldo...



The Art of
electronics design

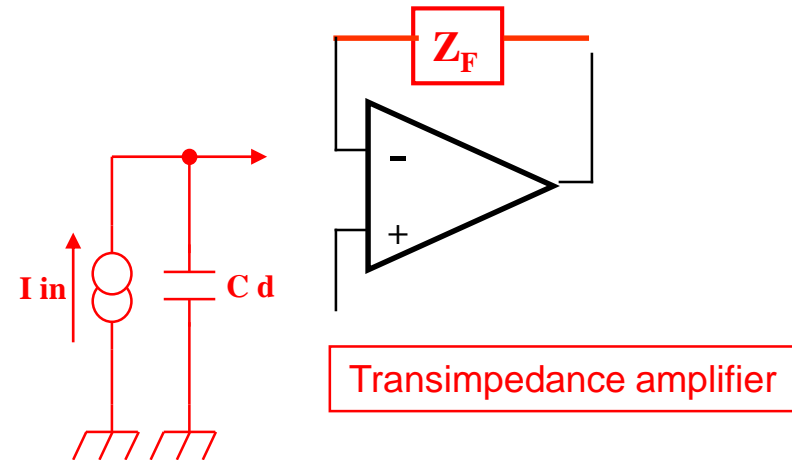
- Capacitive matching : strong inversion
 - g_m proportionnal to $W/L \sqrt{I_D}$
 - C_{GS} proportionnal to $W \cdot L$
 - ENC proportionnal to $(C_{det} + C_{GS}) / \sqrt{g_m}$
 - Optimum W/L : $C_{GS} = 1/3 C_{det}$
 - Large transistors are easily in moderate or weak inversion at small current

- Optimum size in weak inversion
 - g_m proportionnal to I_D (indep of W, L)
 - ENC minimal for C_{GS} minimal, provided the transistor remains in weak inversion



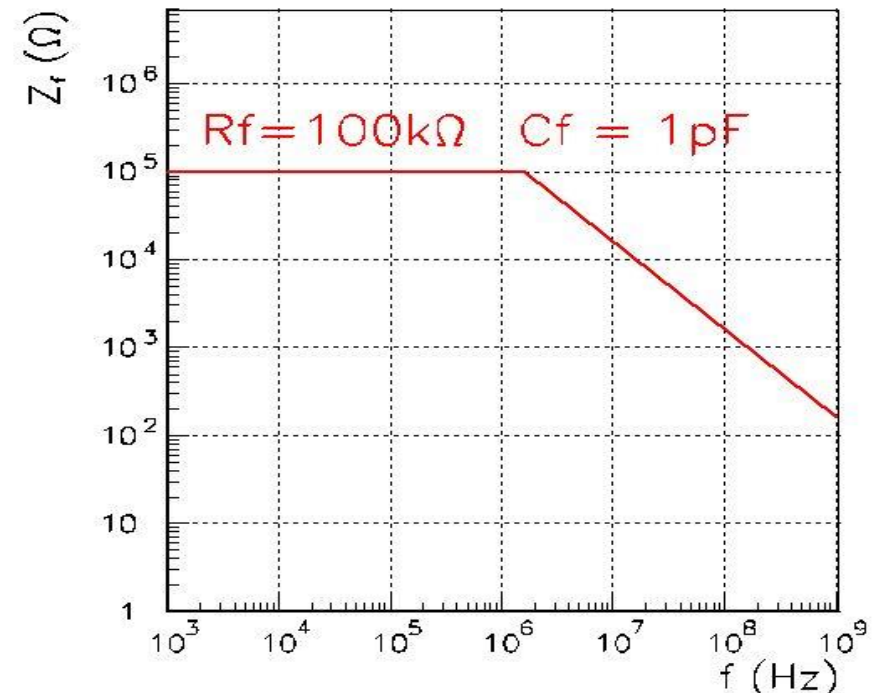
Transimpedance configuration

- Transfer function
 - Using a VFOA with gain G
 - $V_{out} - v_{in} = -Z_f i_f$
 - $V_{in} = Z_d (i_{in} - i_f) = -v_{out}/G$
 - $V_{out}(\omega)/i_{in}(\omega) = -Z_f / (1 + Z_f / GZ_d)$



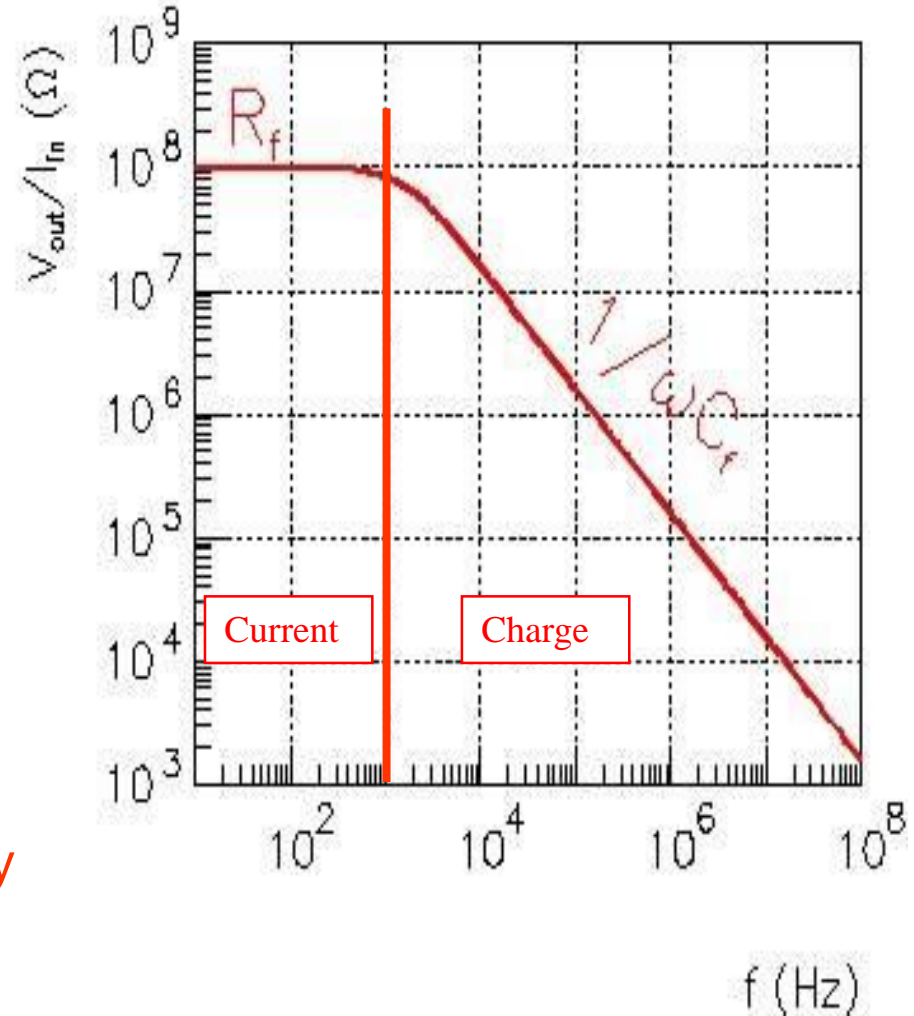
- $Z_f = R_f / (1 + j\omega R_f C_f)$
 - At $f \ll 1/2\pi R_f C_f$:
 $V_{out}(\omega)/i_{in}(\omega) = -R_f$
current preamp
 - At $f \gg 1/2\pi R_f C_f$:
 $V_{out}(\omega)/i_{in}(\omega) = -1/j\omega C_f$
charge preamp

- Ballistic deficit with charge preamp
 - Effect of finite gain : G_0
 - Output voltage «only» $Q C_d / G_0 C_f$



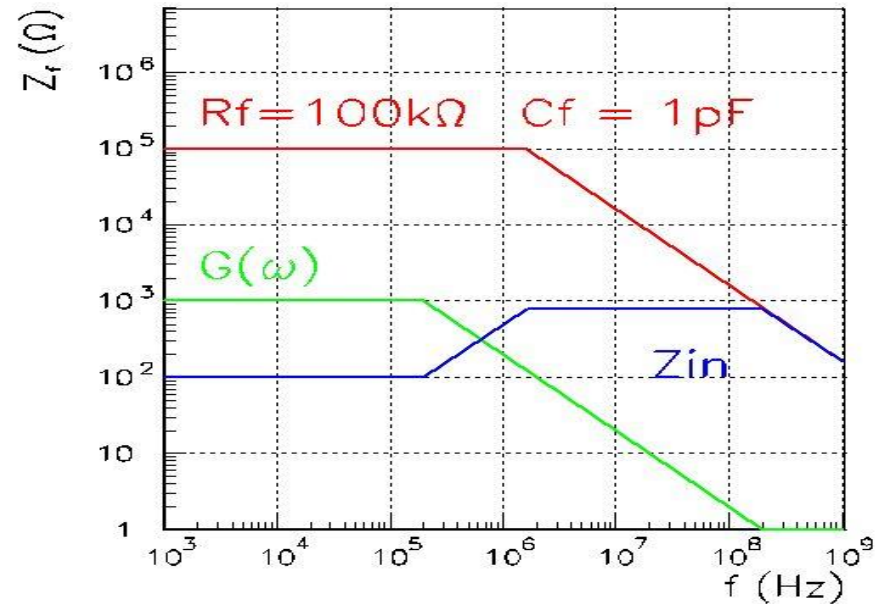
Transfer function

- Charge preamps
 - Best noise performance
 - Best with short signals
 - Best with small capacitance
- Current preamps
 - Best for long signals
 - Best for high counting rate
 - Significant parallel noise
- Charge preamps are not slow, they are long
- Current preamps are not faster, they are shorter (but easily unstable)

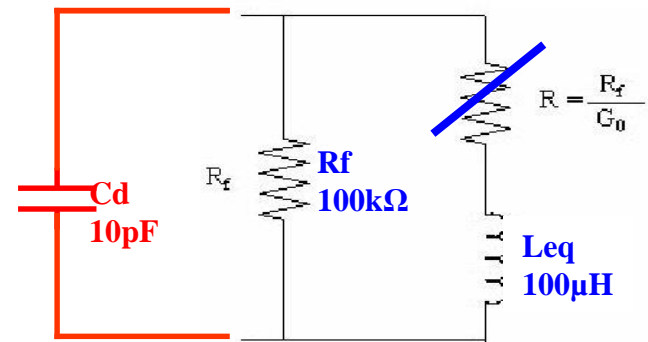


Input impedance

- Input impedance
 - $Z_{in} = Z_f / G+1$
 - $Z_{in} \rightarrow 0$ **virtual ground**
 - Minimizes sensitivity to detector impedance
 - Minimizes crosstalk
- Equivalent model
 - $G(\omega) = G_0 / (1 + j \omega / \omega_0)$
- Terms due to C_f
 - $Z_{in} = 1/j\omega G_0 C_f + 1/ G_0 \omega_0 C_f$
 - **Virtual resistance** : $R_{eq} = 1/ G_0 \omega_0 C_f$
- Terms due to R_f
 - $Z_{in} = R_f / G_0 + j \omega R_f / G_0 \omega_0$
 - **Virtual inductance** : $L_{eq} = R_f / G_0 \omega_0$
- Possible oscillatory behaviour with capacitive source



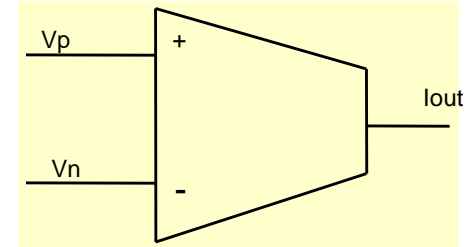
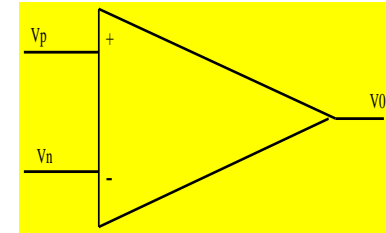
Input impedance or TZA



Equivalent circuit at the input

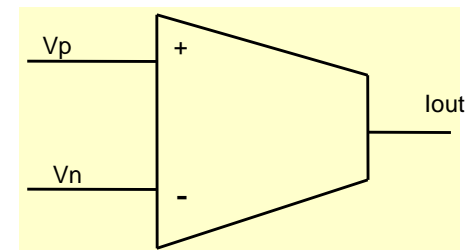
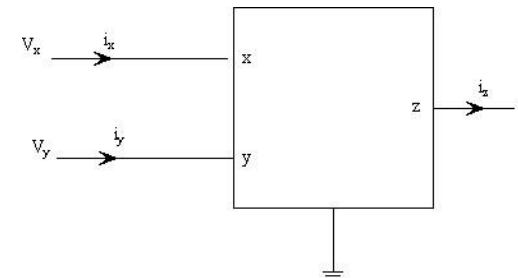
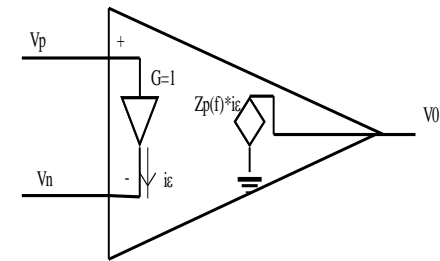
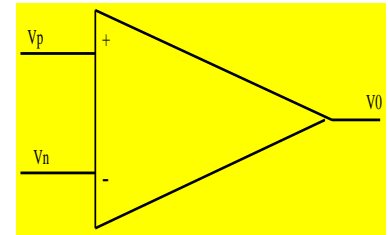
Amplifiers : a large zoo

- Voltage feedback operationnal amplifier (VFOA)
 - Voltage amplifiers, RF amplifiers (VA,LNA)
 - Current feedback operationnal amplifiers (CFOA)
 - Current conveyors (CCI, CCII +/-)
 - Current (pre)amplifiers (ISA,PAI)
 - Charge (pre)amplifiers (CPA,CSA,PAC)
 - Transconductance amplifiers (OTA)
 - Transimpedance amplifiers (TZA,OTZ)
- **Mixing up open loop (OL) and closed loop (CL) configurations !**



Only 4 open-loop configurations

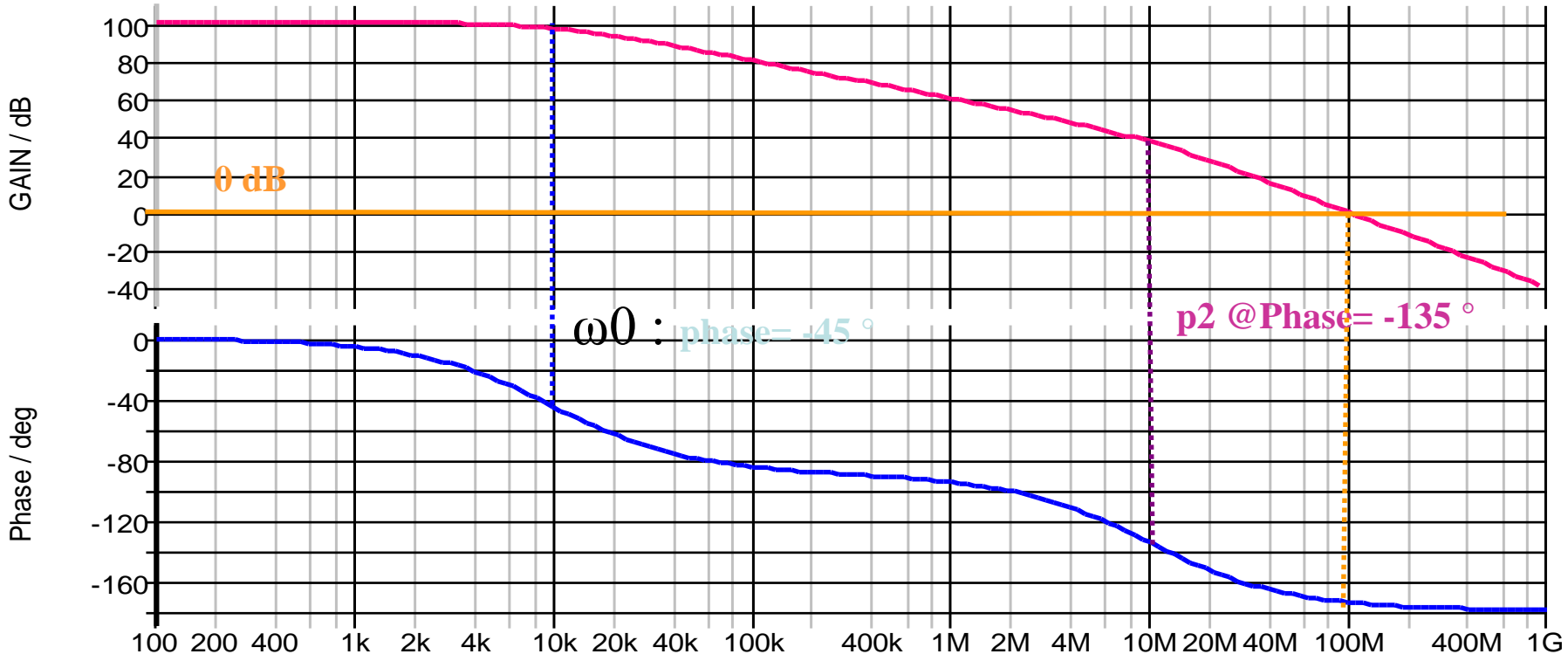
- Voltage operational amplifiers (OA, VFOA)
 - $V_{out} = G(\omega) V_{in\ diff}$
 - $Z_{in+} = Z_{in-} = \infty$ $Z_{out} = 0$
- Transimpedance operational amplifier (CFOA !)
 - $V_{out} = Z(\omega) i_{in}$
 - $Z_{in-} = 0$ $Z_{out} = 0$
- Current conveyor (CCI, CCII)
 - $i_{out} = G(\omega) i_{in}$
 - $Z_{in} = 0$ $Z_{out} = \infty$
- Transconductance amplifier (OTA)
 - $i_{out} = G_m(\omega) V_{in\ diff}$
 - $Z_{in+} = Z_{in-} = \infty$ $Z_{out} = \infty$



Open loop gain variation with frequency

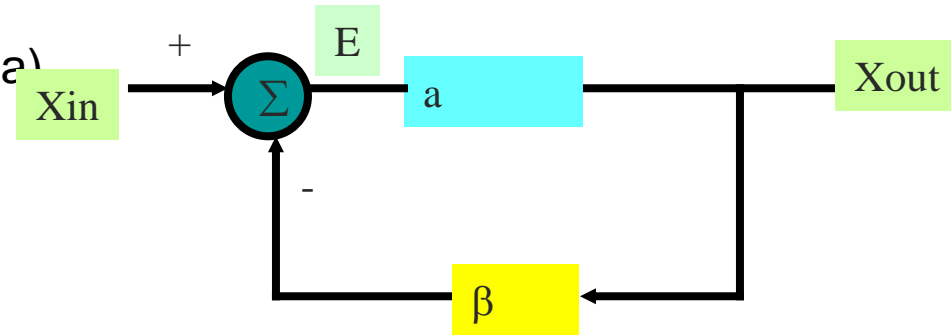


- Define exactly what is « gain » v_{out}/v_{in} , v_{out}/i_{in} ...
- « Gain » varies with frequency : $G(j\omega) = G_0/(1 + j \omega/\omega_0)$
 - G_0 low frequency gain
 - ω_0 dominant pole
 - $\omega_c = G_0 \omega_0$ Gain-Bandwidth product (sometimes referred to as unity gain frequency)

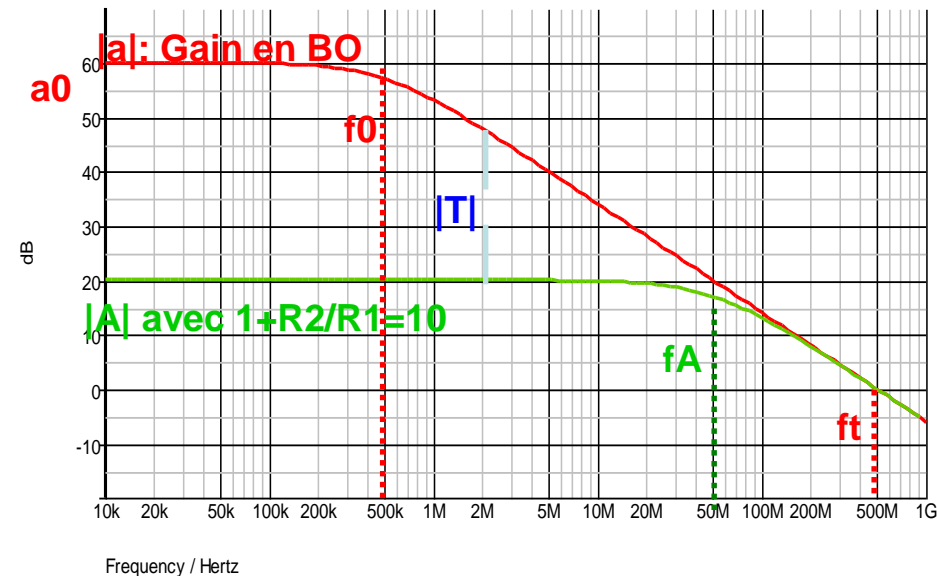


Feedback : an essential tool

- Improves gain performance
 - Less sensitivity to open loop gain (a)
 - Better linearity
- Essential in low power design
- Potentially unstable
- Feedback constant : $\beta = E/X_{out}$
- Open loop gain : $a = X_{out}/E$
- Closed loop gain : $X_{out}/X_{in} \rightarrow 1/\beta$
- Loop gain : $T = 1/a\beta$

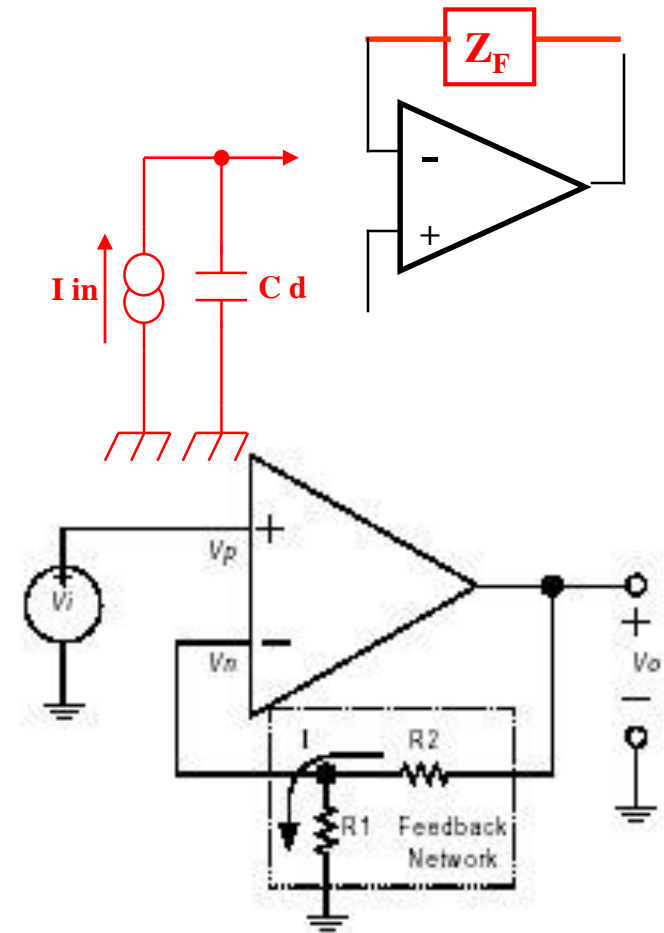


$$\frac{X_{out}}{X_{in}} = \frac{a}{1 + a\beta} = \frac{1/\beta}{1 + 1/a\beta}$$



Only 4 feedback configurations

- Shunt-shunt = transimpedance
 - Small Z_{in} ($= Z_{in}(OL)/T$) -> current input
 - small Z_{out} ($= Z_{out}(OL)/T$) -> voltage output
 - De-sensitizes transimpedance $= 1/\beta = Z_f$
- Series-shunt
 - Large Z_{in} ($= Z_{in}(OL)*T$) -> voltage input
 - Small Z_{out} ($= Z_{out}(OL)/T$) -> voltage output
 - Optimizes voltage gain ($= 1/\beta$)
- Shunt series
 - Small Z_{in} ($= Z_{in}(OL)/T$) -> current input
 - Large Z_{out} ($= Z_{out}(OL)*T$) -> current output
 - Current conveyor
- Series-series
 - Large Z_{in} ($= Z_{in}(OL)*T$) -> voltage input
 - Large Z_{out} ($= Z_{out}(OL)*T$) -> current output
 - Transconductance
 - Ex : common emitter with emitter degeneration



- Calculating $\beta = E/X_{out} = Z_d/(Z_d+Z_f)$

