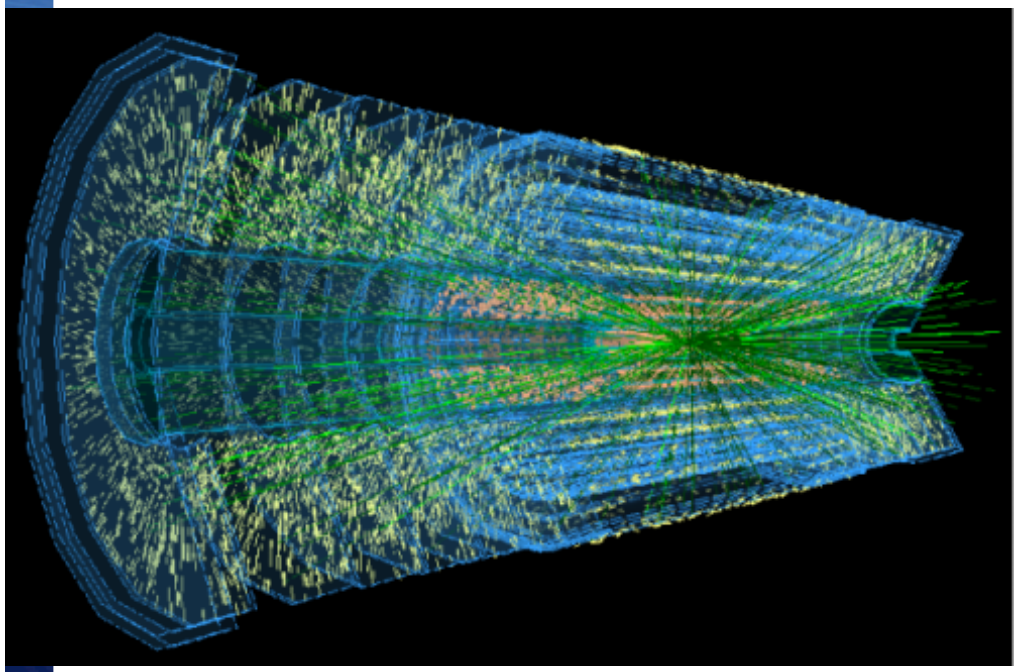
Track Triggers for HL-LHC

Alberto Annovi
On behalf of ATLAS, CMS and LHCb

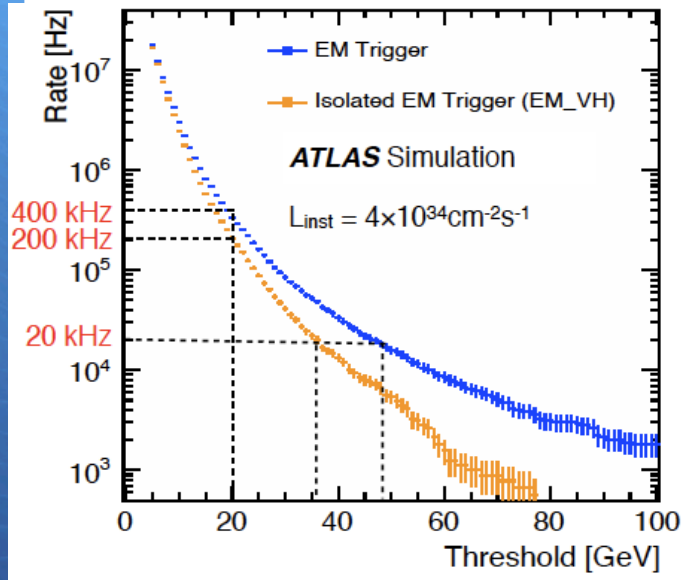
Challenges for HL-LHC

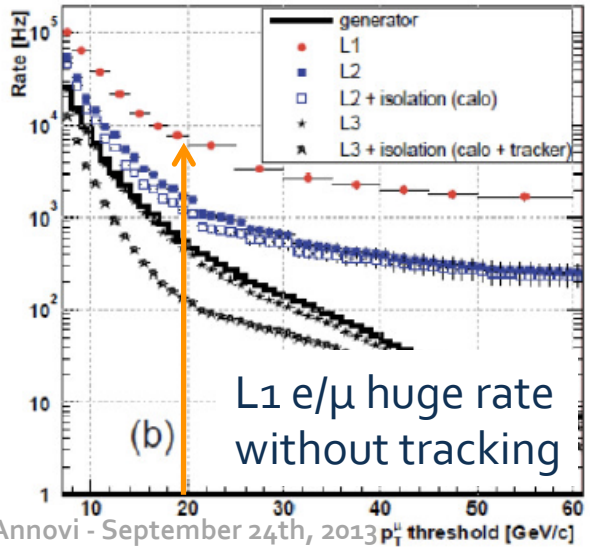
- High-Luminosity LHC
  - Goal 5E34Hz/cm2 (plan for 7E34)
  - 300 fb-1/anno → 3000 fb-1 total



- Higher occupancy
  - Pileup 140 (max 200)
  - Tracking more important!
- Increase trigger bandwidth
- Move part of High Level Trigger (HLT) to L1
  - Including tracking
  - Low latency tracking O(10μs)

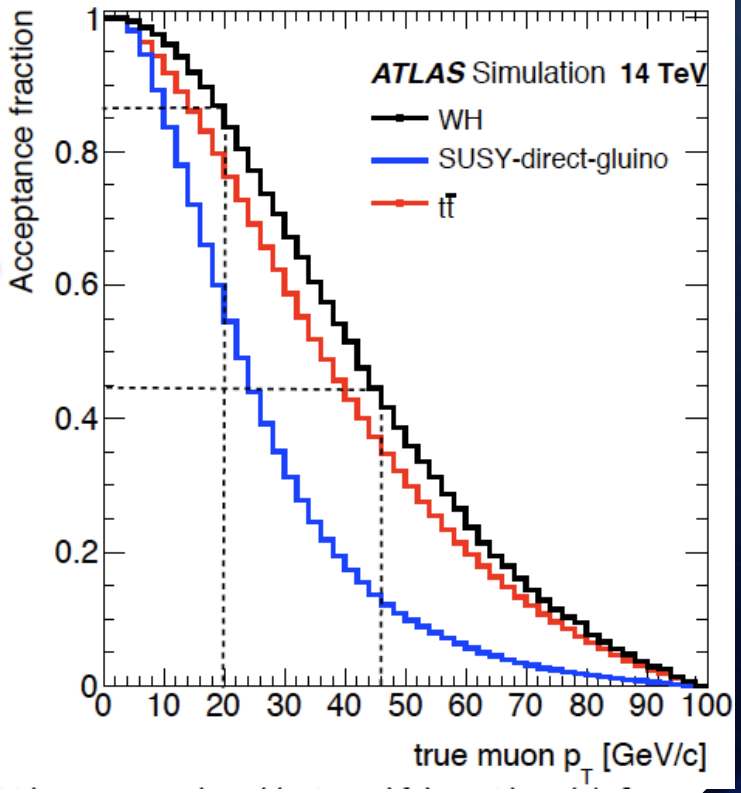
L1 Track for EWK pT leptons





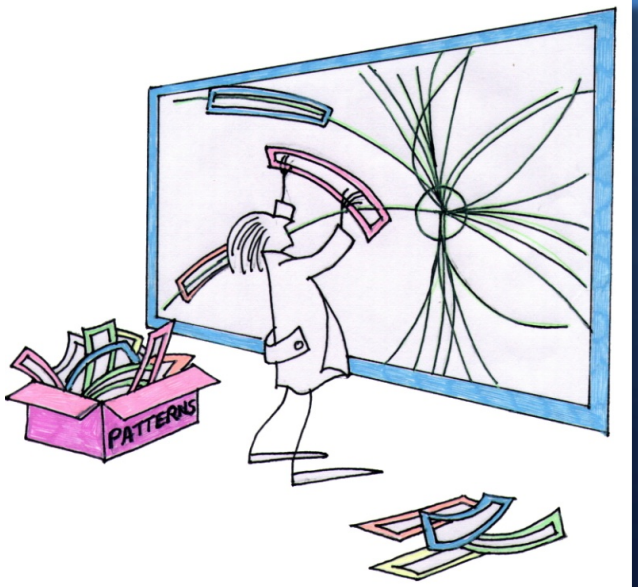
ATLAS and CMS L1 Track:
Need tracks at L1 in order to maintain O(20 GeV) single mu/e pT threshold

CMS 7TeV
10E34Hz/cm²



Strong interest for Track Triggers

- ATLAS L2 (FTK)
  - Full tracking at 100kHz, pT>1GeV, ~offline-quality
  - Start data taking in 2015, upgrade during LS3
- LHCb Track Processor
  - Recent studies on a "neural" track processor for LHC Phase-I
  - 40MHz, latency ~1μs. R&D for LHCb LS2
- ATLAS L1 (L1Track) installation LS3
  - Regional tracking at 0.5-1MHz, seeded by L-zero
  - 20μs latency, higher pT threshold 5-10 GeV
- CMS L1Track installation LS3
  - Self-seeded full tracking at 40MHz
  - Requires filtering of low pT clusters (pt~<2GeV)
  - Latency 5μs
- **3 projects with same time scale (LS3) → shared R&D**



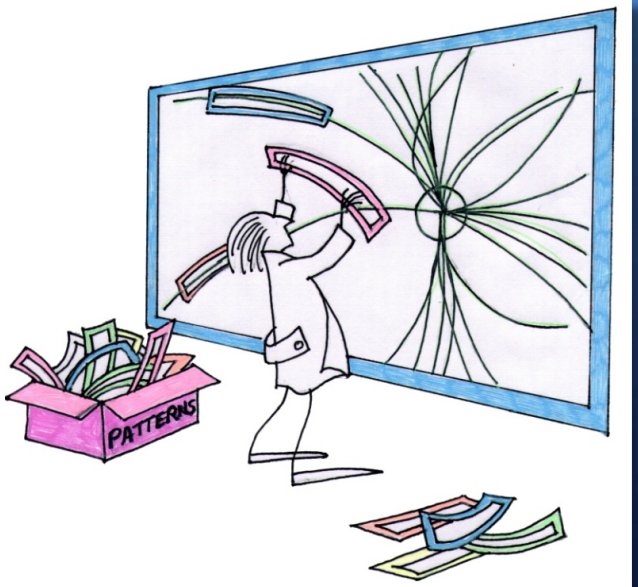
Strong interest for Track Triggers

- LHCb Track Processor
  - Recent studies on a "neural" track processor for LHC Phase-I
  - 40MHz, latency ~1us, R&D for LHCb LS2

- AM finds track candidates with enough Si hits
- FTK a total of O(10^9) patterns (8k AM chips)
- Patterns simultaneously see the silicon hits leaving the detector at full speed.
- Pattern recognition is complete as soon as all data is received! → very good fit with L1
- Based on the Associative Memory initially developed for CDF.
  L. Ristori, M. Dell'Orso NIM A **278**, 436 (1989)

  - Latency 10μs

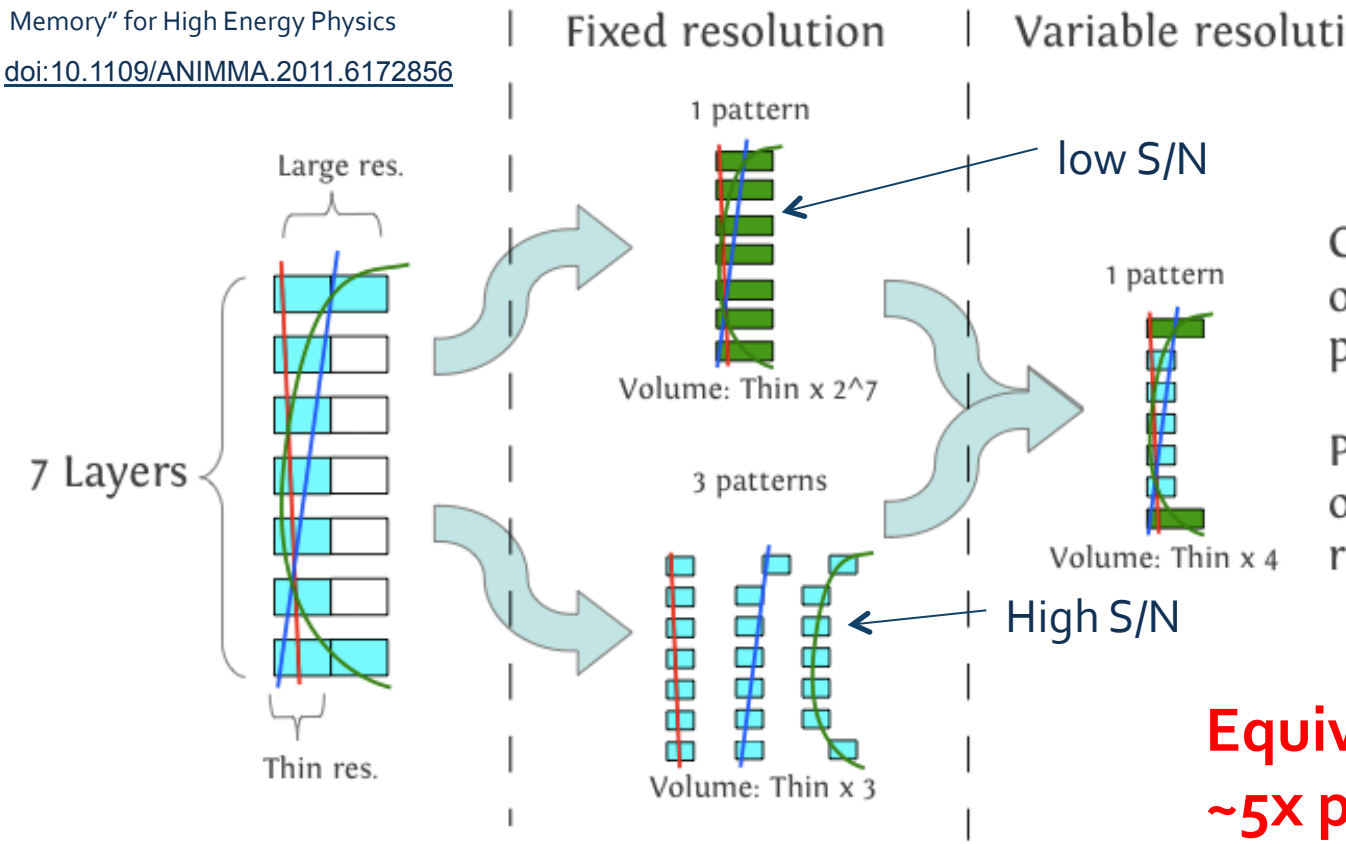
- **3 projects with same time scale → shared R&D**



AMCHIP04: VARIABLE RESOLUTION

A new "Variable Resolution Associative Memory" for High Energy Physics

doi:10.1109/ANIMMA.2011.6172856

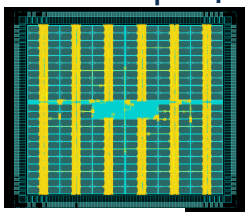


INFN Frascati

Good rejection and occupy only one pattern location.

Per-pattern choice of optimal resolution.

AMchip04



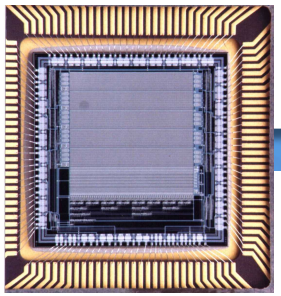
Equivalent to ~5x patterns → 1/5 HW size

Implementes the "don't care" feature: inspired by the Ternary CAMs

- Increases the width of a pattern only when needed (fully programmable)
- Wider patterns can be used in high occupancy regions, smaller patterns in low coverage regions (where the number of trajectories is low, thus reducing the fakes)
- The choice of wider or narrower width patterns is made layer by layer with simulation

AM technological evolution

SVT
AM chip



- (90's) **Full custom VLSI chip** - 0.7μm (INFN-Pisa)
- **128 patterns, 6x12bit words each, 30MHz**

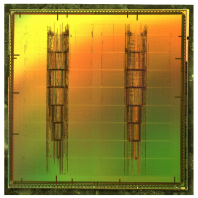
F. Morsani et al., IEEE Trans. on Nucl. Sci., vol. 39 **(1992)**

Alternative **FPGA** implementation of SVT AM chip

P. Giannetti et al., Nucl. Intsr. and Meth., vol. A413/2-3, **(1998)**

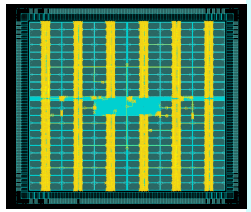
G Magazzù, 1st std cell project presented @ LHCC (1999)

SVT upgrade



Standard Cell 0.18 μm → 5000 pattern/AM chip
SVT upgrade total: 6M pattern, 40MHz
A. Annovi, L. Sartori et al., **IEEE TNS,** Vol 53, Issue 4, **2006**

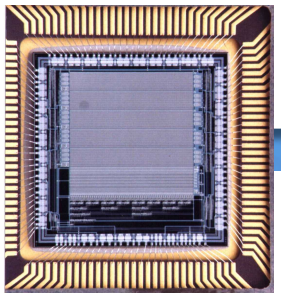
FTK R&D



AMchip04 –65nm technology, std cell & full custom, 100MHz
Power/pattern/MHz ~30 times less. Pattern density x12.
First variable resolution implementation!
F. Alberti *et al 2013 JINST* ***8 C01040,*** *doi:*10.1088/1748-0221/8/01/C01040

AM technological evolution

SVT AM chip



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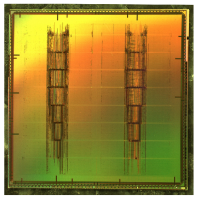
Alternative **FPGA** implementation of SVT AM chip

P. Giann

G Magaz

FTK R&D in progress:
AMchip05 prototype: switch to serialzed IO (11*2Gpbs)
submitted march 2014
AMchip06 FTK final: increase area goal 128k patterns/chip
submission later in 2014

SVT upgrade



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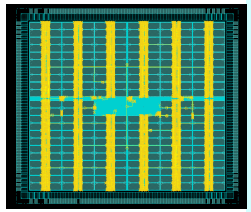

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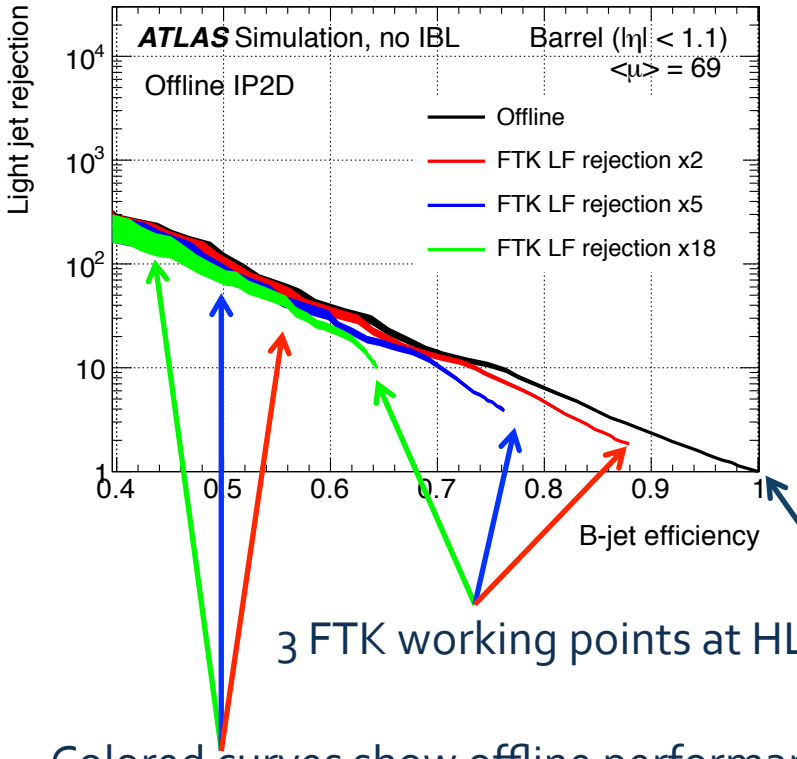
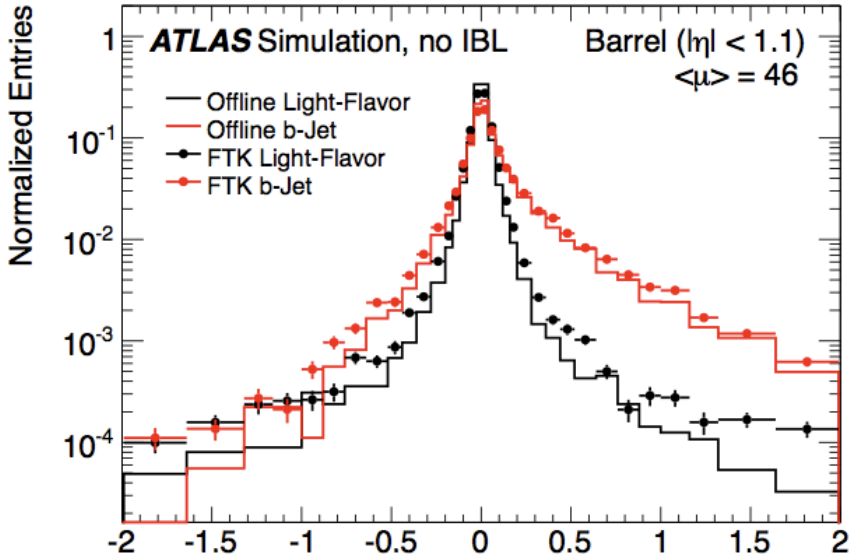
FTK example performance

Offline b-tagging (IP2D) applied to FTK (IP2D) selected samples.
Performance improvements in progress (adding IBL, better fit)



3 FTK working points at HLT

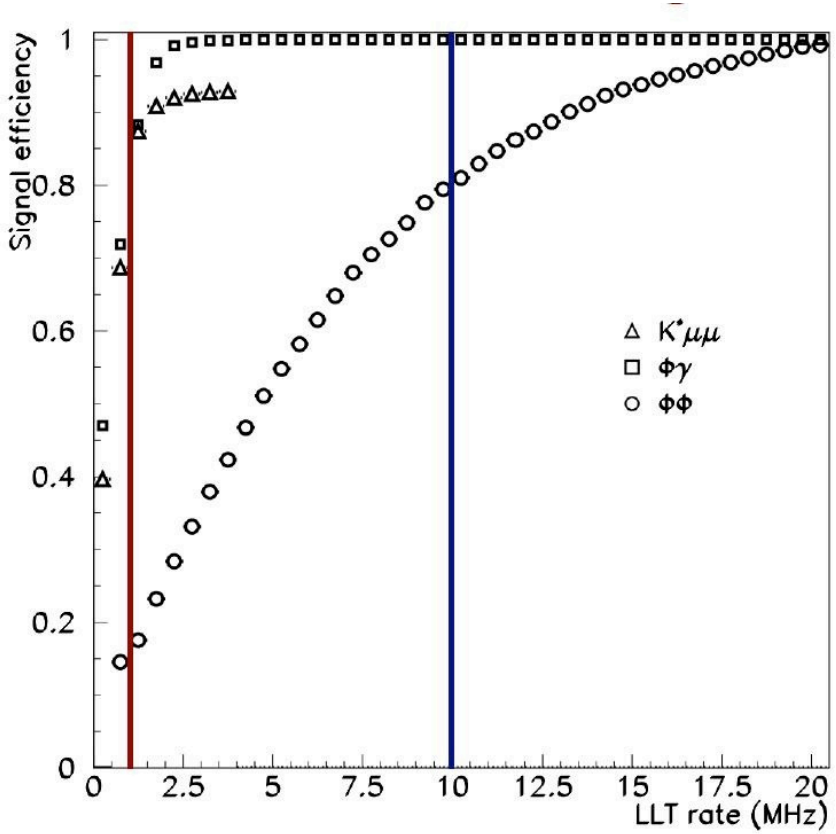
Colored curves show offline performance on FTK selected samples



do distributions FTK & offline

Offline performance no trigger

LHCb track trigger motivations



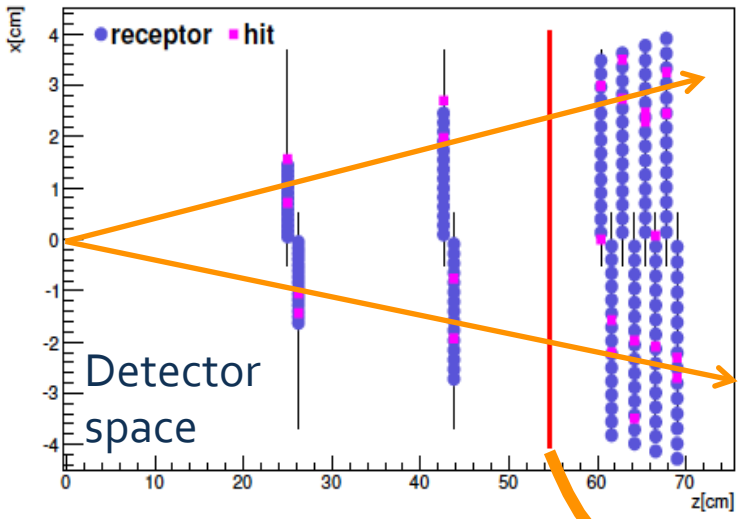
- Good efficiency for hadronic decays required track trigger at high-rate
- Plan is to collect data at full 30MHz and perform tracking

Neural processor: Tracks appear as clusters

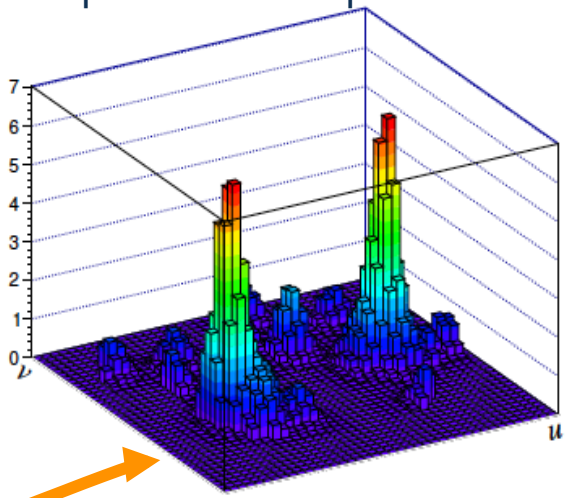
G. Punzi @ INSTR14: http://cern.ch/go/C6QS

Motivations: Tracking is essential for LHCb

Real tracks + noise



Space of track parameters



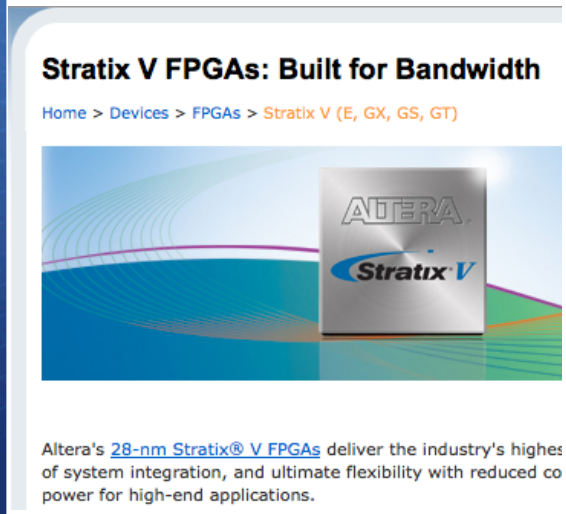
Track parameters estimated by cluster center interpolation

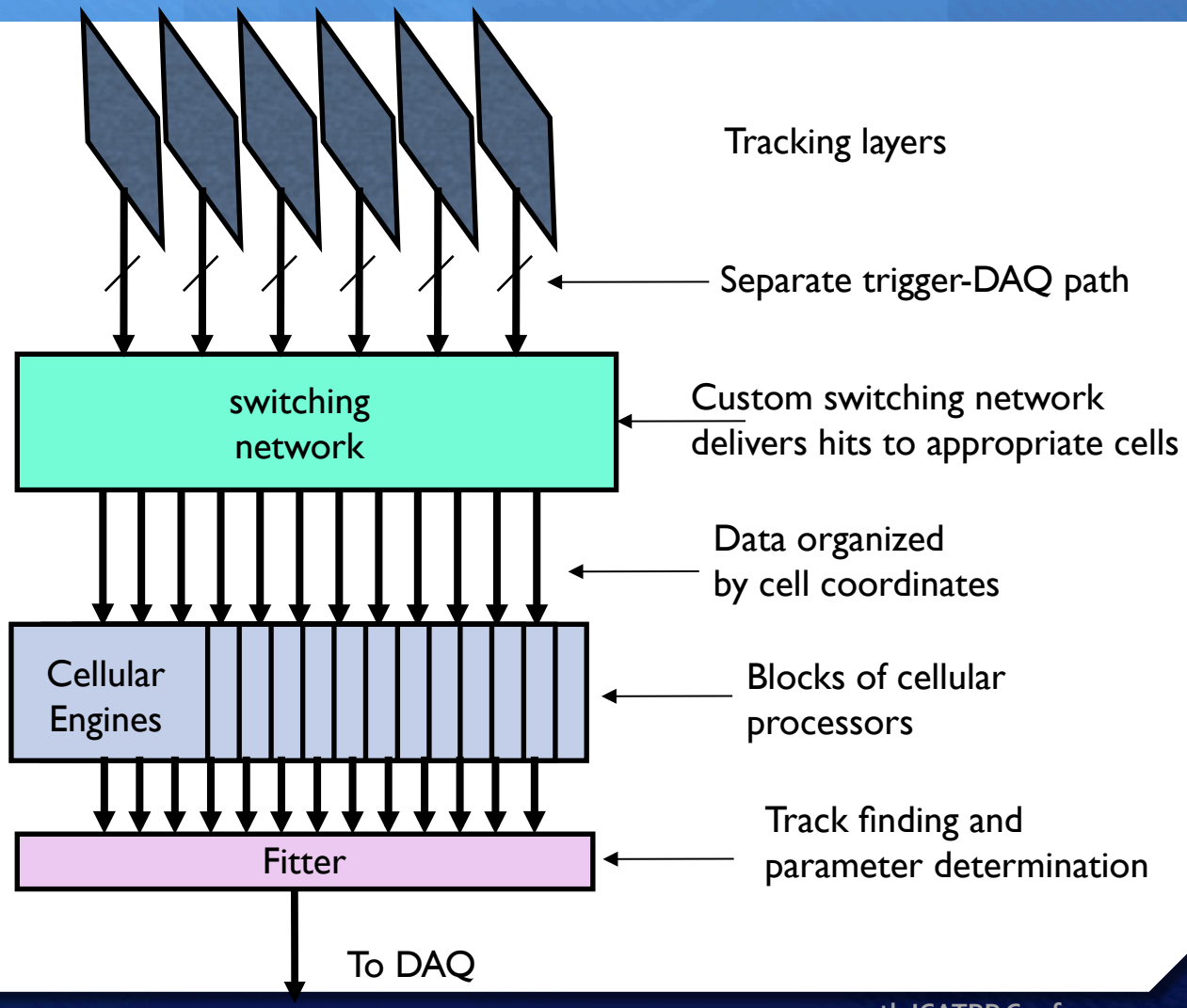
$$R_i = \sum_k e^{-s^2_{ir,k}/2\sigma^2}$$

$$s^2_{ir,k} = (x_i - x_r)^2_k + (y_i - y_r)^2_k$$

Distance of hit to nearby receptors

System Architecture

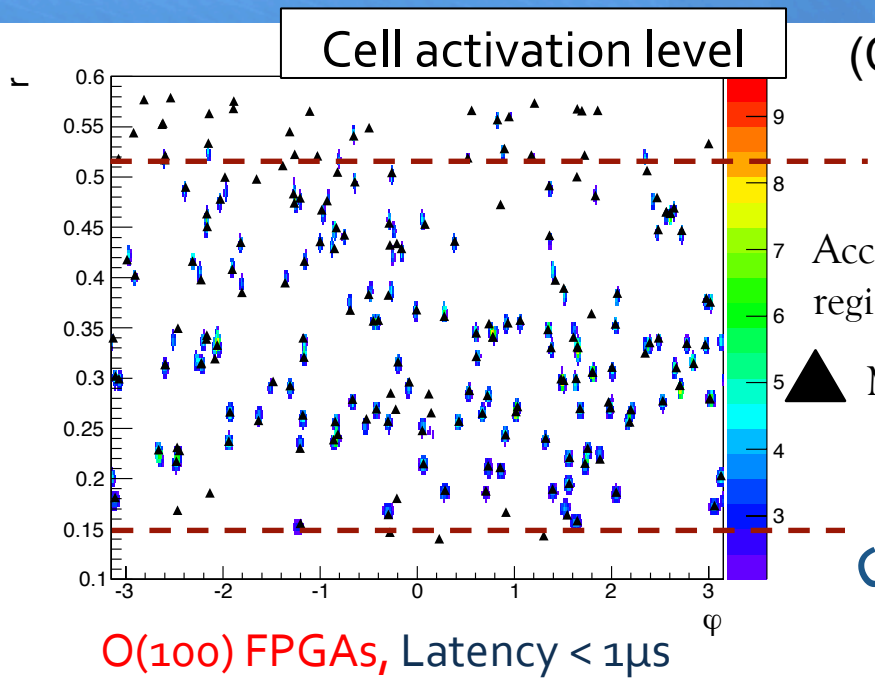




Further progress: R&D for LHCb phase-I

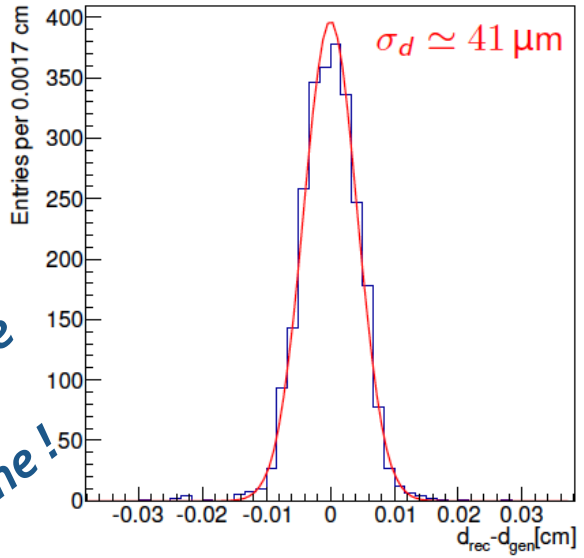
full-MC at phase-I upgrade luminosity

G. Punzi @ INSTR14: http://cern.ch/go/C6QS



O(100) FPGAs, Latency < 1μs

(Compare with offline-style fit: σ = 40μm)

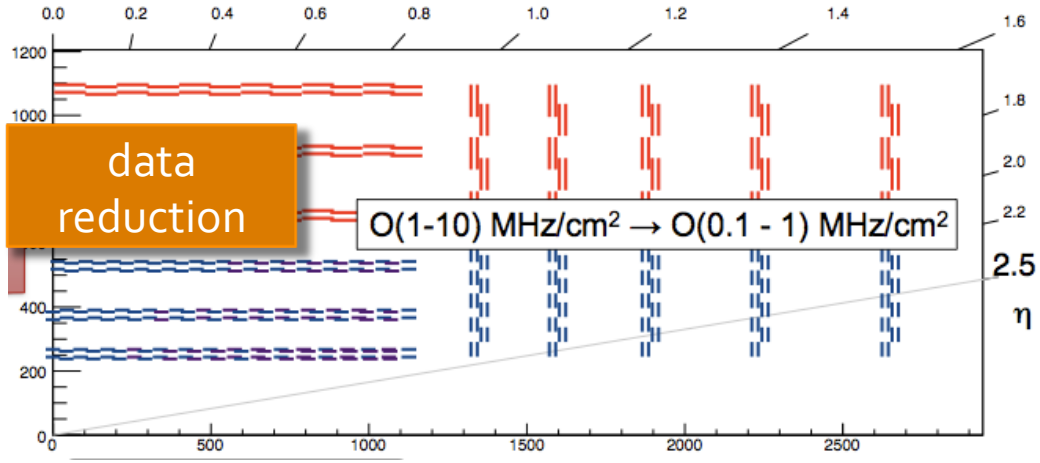


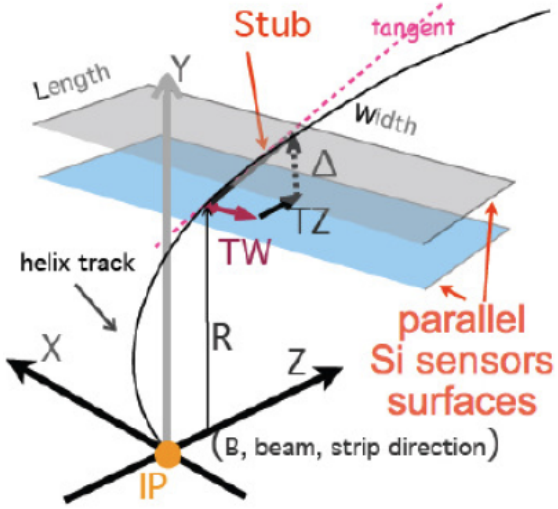
Comparable to offline !

- R&D on paper ~ completed
  - Demonstrator in 2014
  - Supported by INFN and SNS
- Input for future track triggers

CMS approach

- detector and readout discussed by F. Palla yesterday
- Selfseed trigger at 40MHz (strip & pixel-strip)
  - Readout data rate with pT>2GeV filtering (data reduction ~1/10)
  - Hard to solve tracking at 40MHz with single processor
    - Need time multiplexing over multiple processors
- (option if L1 latency at 20μs) pixel trigger seeded by the above



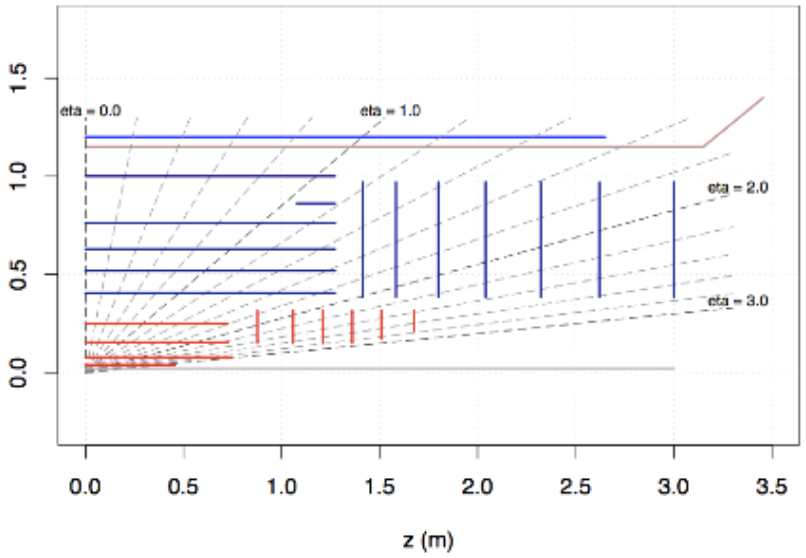


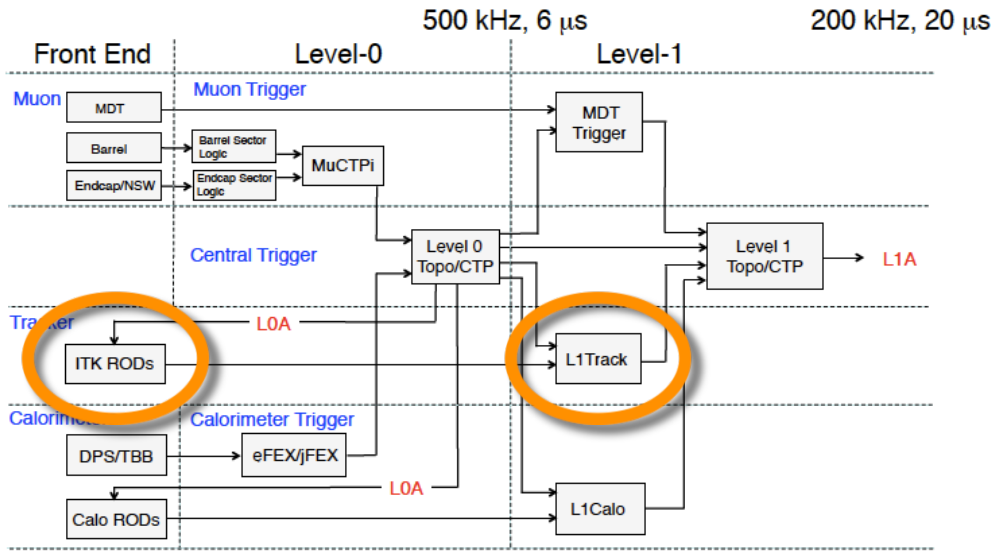
CMS challenges & solutions

- Data transfer at 40MHz → doable with pT filtering
- Pattern recognition
  - pT>2GeV filtering → lower detector occupancy (but 40MHz rate)
  - Main option based on AM (alternative full FPGA)
    - Grants low latency (benefit of faster AMchip clock)
  - Estimate: a few thousands future (LS3) AM chips
    - Considering a goal of 0.5-1M patterns / AMchip
- Track Fitting FPGA based several algorithms considered
  - Principal component, retina, Hough transform, tracklets
- L1 Track latency ~5μs (+ readout)
  - Total L1 latency 10μs (20μs?)

ATLAS approach

- detector and readout discussed by F. Palla yesterday
- Approach
  - Lo rate 500kHz (1MHz)
  - Regional readout request (R3) ~ 10% detector
  - Minimum pT ~5 GeV
  - Full pixel + strip tracking





ATLAS challenges & solutions

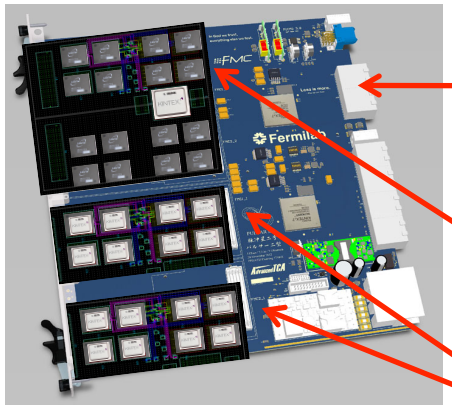
- Data transfer
  - Bandwidth ~ 10% * 1MHz ~ equivalent 100kHz full detector
  - But need to keep latency low <6 μs
- Pattern recognition
  - within regions of interest …
  - but very complicated: full 140 (max 200) pileup occupancy!!!
  - Main option based on AM
    - Grants low latency (benefit of faster AMchip clock)
  - (gues)stimate O(few thousands) future (LS3) AM chips (goal ~1M patterns / chip)
    - Simulations starting now
- Track Fitting FPGA based
- L1 Track latency 6μs (+ readout)

FTK miniaturization & speedup:

(1) ATCA power, (2) New Amchip (40 nm), (3) Multipackaging

(1) ATCA demonstrator

Up to 40Gbps board to board



FTK Data Formatter

2015-2016:
2 AM + FPGA mezzanines

2017-2018:
4 AMSIP mezzanines

- Exploit inter-board ATCA bandwidth and flexibility
- Allow to demonstrate full system potentiality
- Prepare a modular system architecture

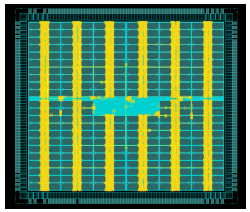
(2) New AMchip 40 nm (or 65nm)

Prepare NEW AM technology core of FTK Phase II and L1 Track

Goals: increase pattern density, low power, low latency, other applications

Mini asic & MPW 40nm (or 65nm) prototypes

AMchip06 FTK
Design ends in 2014



Full custom AM cell
R&D limited by FTK schedule

Miniasic 40nm
~3mm²
Cheap AM cell
R&D
2015-16

MPW 40nm
~12mm²
usable for ATCA
demonstrator
& system in
package
2016-17

New AMchip 40 nm (200+ MHz?, new functionalities for L1)

AMchip04 AMcell could work O(0.5GHz), but not a goal for FTK.

(3) FTK could become smaller and smaller
Multi-packaging FPGA & AMchip – mini FTK

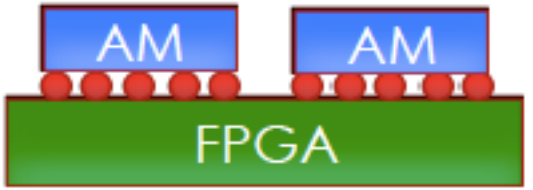
(1) We have a very interesting **quote** for FPGA **bare dies** to be packaged with AMchips

(2) IMEC support for feasibility studies

(3) FTK AMSIP (AM System In Package) becomes a real possibility

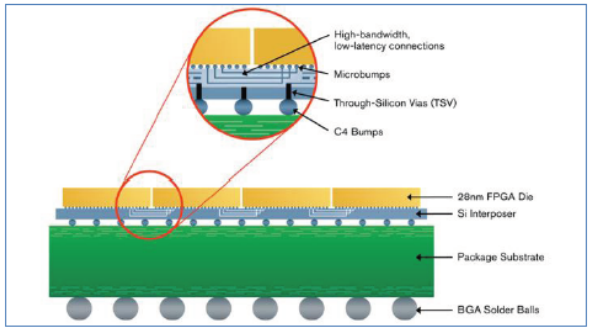
Dramatically increases AM to Track Fitter bandwidth

Full 3D technology not required!



(4) Full 3D explored by Fermilab

R&D coordinated with Fermilab



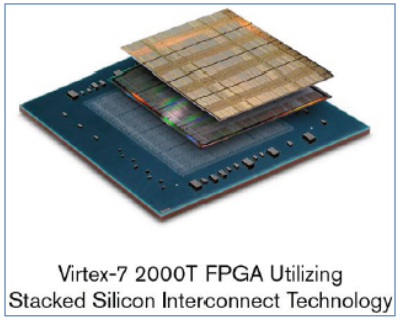


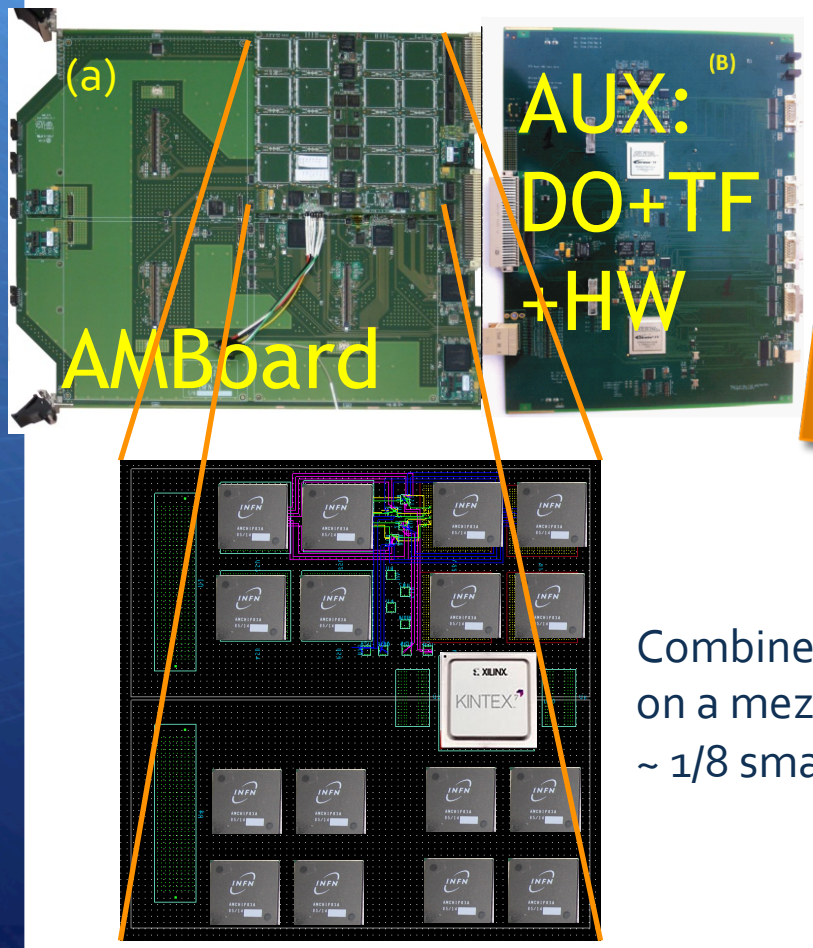
Fig. 1.1.7 Left and right - example of silicon interposer approach for Xilinx Virtex-7 FPGA; This approach will constitute the basis for the innovations that the NEURONS project will develop as described in the text.

- System-in-Package integration
  - Die-to-die stacking design
  - Optimize the packaging
  - Thermal power dissipation analysis
- Define a new trigger architecture
  - exploit higher AM-FPGA connectivity

1 AM chip
1 FPGA in the same package

(1-2-3) Compressing AM/FTK size

FTK: AM + Track Fitting (TF)

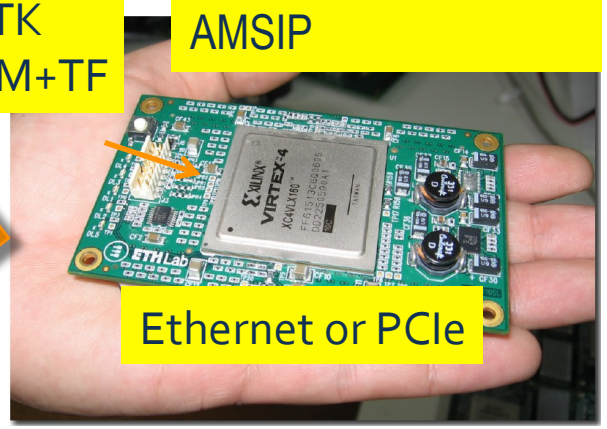


Combine AM & TF on a mezzanine ~ 1/8 smaller

Goal: build a Lamb that can fit in a PC or can be accessed by a PC.

FTK AM+TF

What about this size ? AMSIP



Both miniaturization steps:
- Reduce size
- Increase internal bandwidth
- ATCA compatible (ext bandwidth)

Possibility of interdisciplinary applications with a Ethernet or PCIe connector

R&D plan (being proposed to INFN)

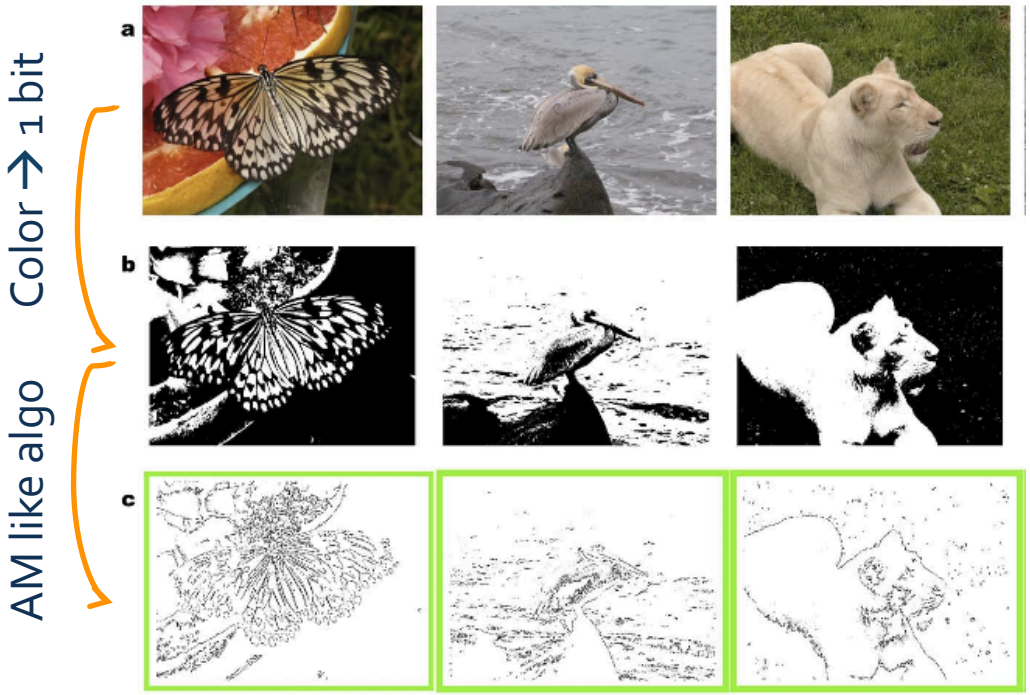
- The 3 R&D activities shown are of interest to INFN for ATLAS and CMS
  - CMS needs to start the ATCA demonstrator early 2015
- Time line 2014-2018
  - 2014 studies and start on ATCA demonstrator
  - 2015 studies, ATCA demo, start AM chip (miniasic) design
  - 2016 AM miniasic submission & test, start AM chip (MPW) design
  - 2017 test AM chip MPW, design & submission AM System in Package
  - 2018 test System in Package: standalone, onboard, on ATCA
- Goals & deliverables: demonstrate Phase–II compatible system
  - Interconnection bandwidth with ATCA
  - AM chip: patterns/mm^2, µW/pattern/MHz, bandwidth, latency
  - AM to Track Fitter I/O (System in Package)

Collaborazioni e progetti associati

- Collaborazioni in corso
  - AMchip: LPNHE, IMEC, Fermilab
  - AMSIP: LPNHE, IMEC
  - ATCA: Fermilab, Lione, Northwestern e Karlsruhe
  - Simulazione HW e fisica: INFN, LPNHE, Lione, Fermilab, Northwestern, Karlsruhe, UCLondon, Uppsala
- Progetti associati
  - FP7-PEOPLE-2012-IAPP: Fast Tracker for Hadron Collider Experiments (P. Giannetti)
  - PRIN: H-TEAM: Trigger, Elettronica Avanzata e Metodi innovativi per misure di precisione nel settore dell' Higgs ad LHC (G. Tonelli)
  - ANR: Development of a fast processing electronics for track triggering at Hadron Collider Experiments (LPNHE, IPNL Lione)
  - FP7-PEOPLE-ITN INFIERI (CMS)
- Next proposals
  - SIR, ERC, Pillar II (ICT-4), CSN5

Applicazioni interdisciplinari

- AM chip: a general processor for "data correlation searches"
- Image reconstruction in various field: e.g. smart cameras
- Example: imaging



AM like algorithm used to identify salient features of the images.

M. M. Del Viva, G. Punzi, D. Benedetti
DOI: 10.1371/journal.pone.0069154

Main focus of the article: which are the most meaningful patterns.

Conclusions

- To produce a modern-powerful system for
  - Level 1 @ ATLAS & CMS
  - Level 2 @ ATLAS & (L2 Pixel CMS?)
  - Interesting non HEP applications

BACKUP

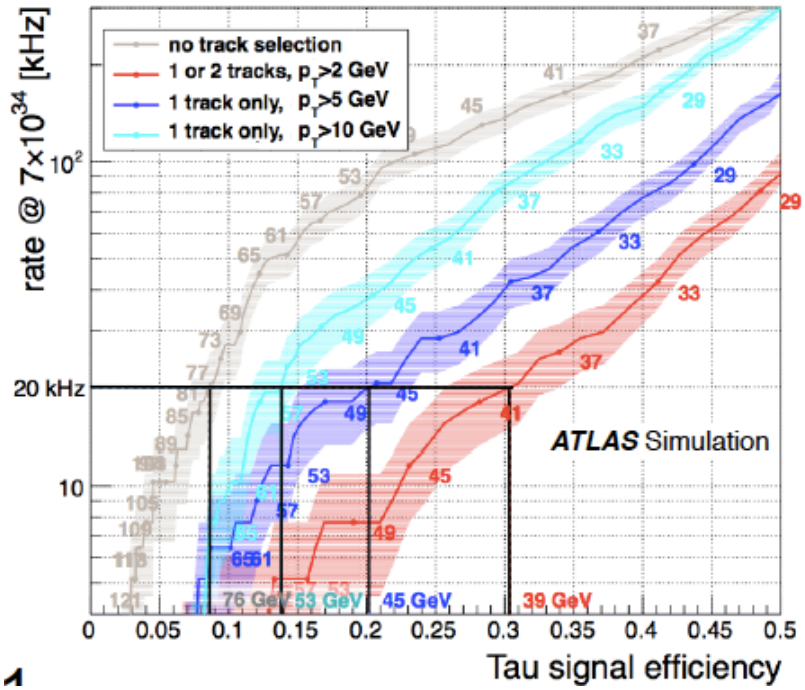
L1 Track

- Potential benefits have been studied for electrons, muons, taus and jets, single and multiple/combined object triggers using both smeared offline tracks, and smeared truth particles

- Even modest resolution tracking information (pT, η, ϕ) can provide sufficient rejection

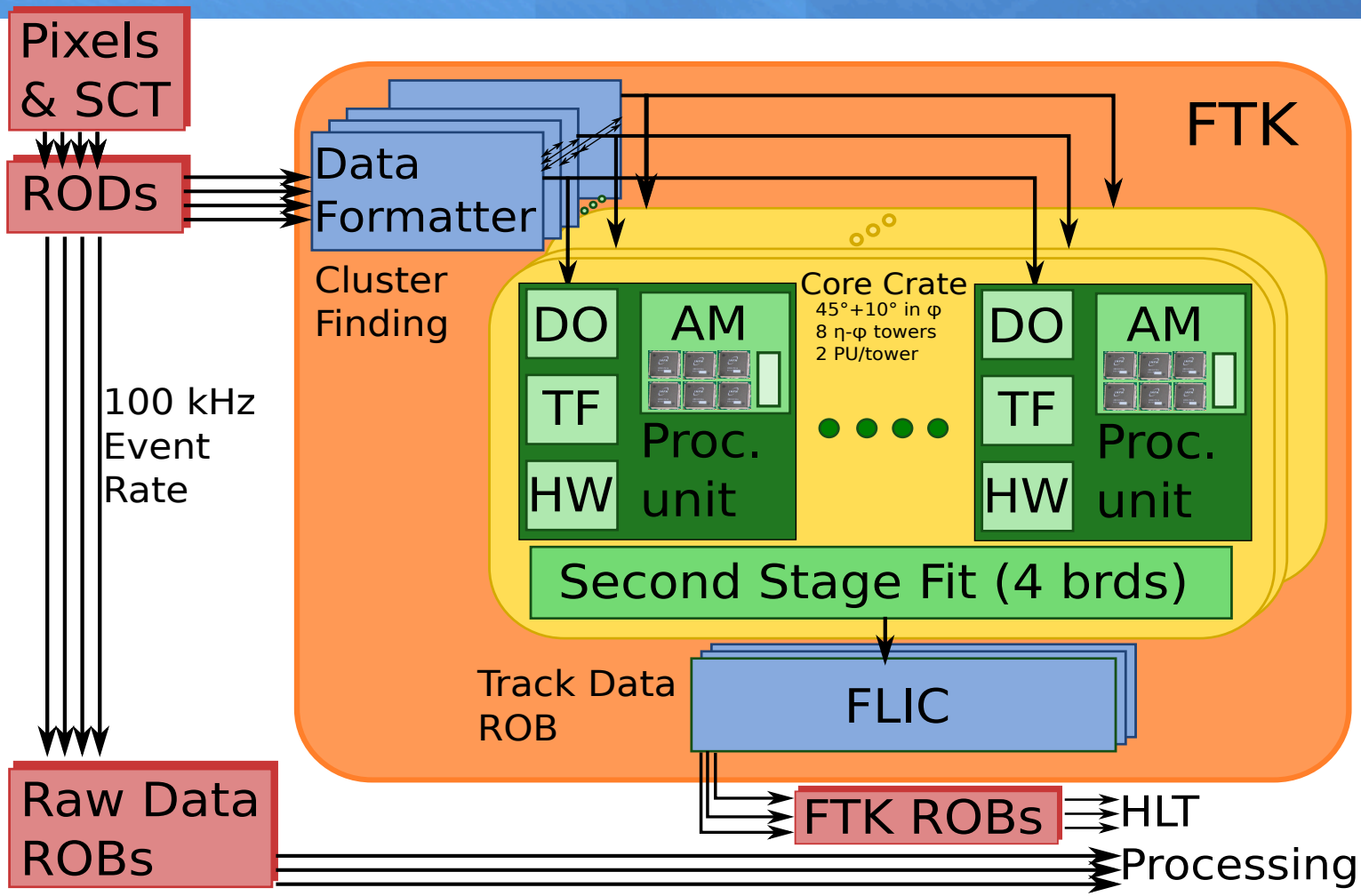
- Rejection factors of between 3 - 10 for muons and electrons respectively, with only small efficiency losses

Example 3x yield for taus signals

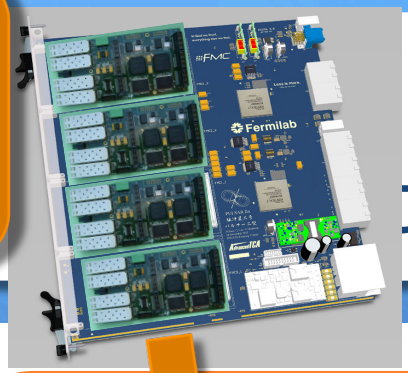


M Sutton - Tracking for the ATLAS Level 1 Trigger for the HL-LHC ICATPP, 24th September 2013 - Como

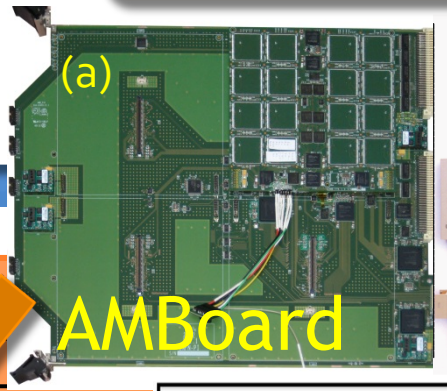
FTK in the TDAQ system

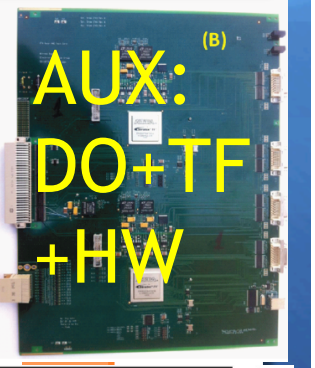


4 FTK_IM/DF do cluster finding. ATCA DF distributes clusters to 64 FTK η-φ towers.



128 PUs do pattern matching and the 1st stage track fitting.





Pixels & SCT

RODs

Data Formatter

Cluster Finding

DO

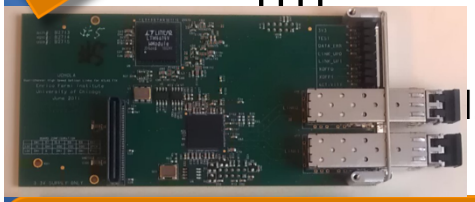
AM

TF

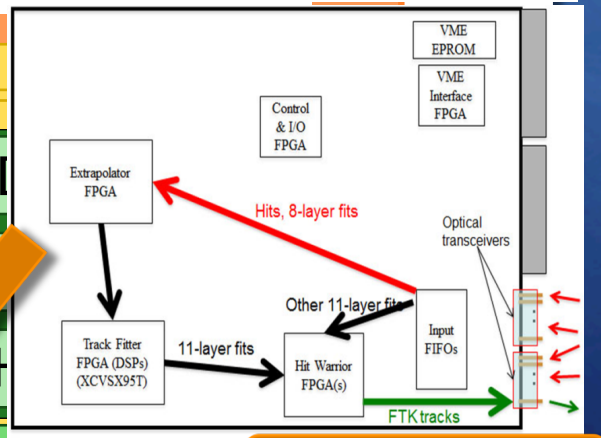
HW

Proc. unit

Core Crate
45°+10° in φ
8 η-φ towers
2 PU/tower

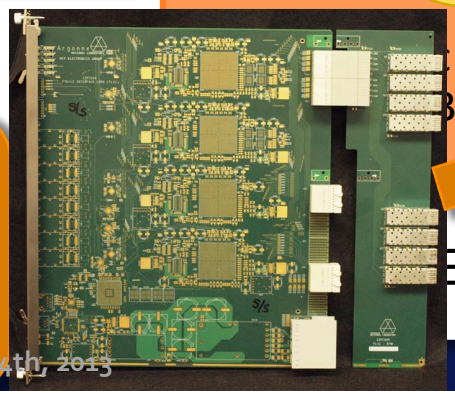


Sends SCT & pixel data to DAQ & FTK.



Second Stage Fit (4 brds)

Do full 12 layer fit



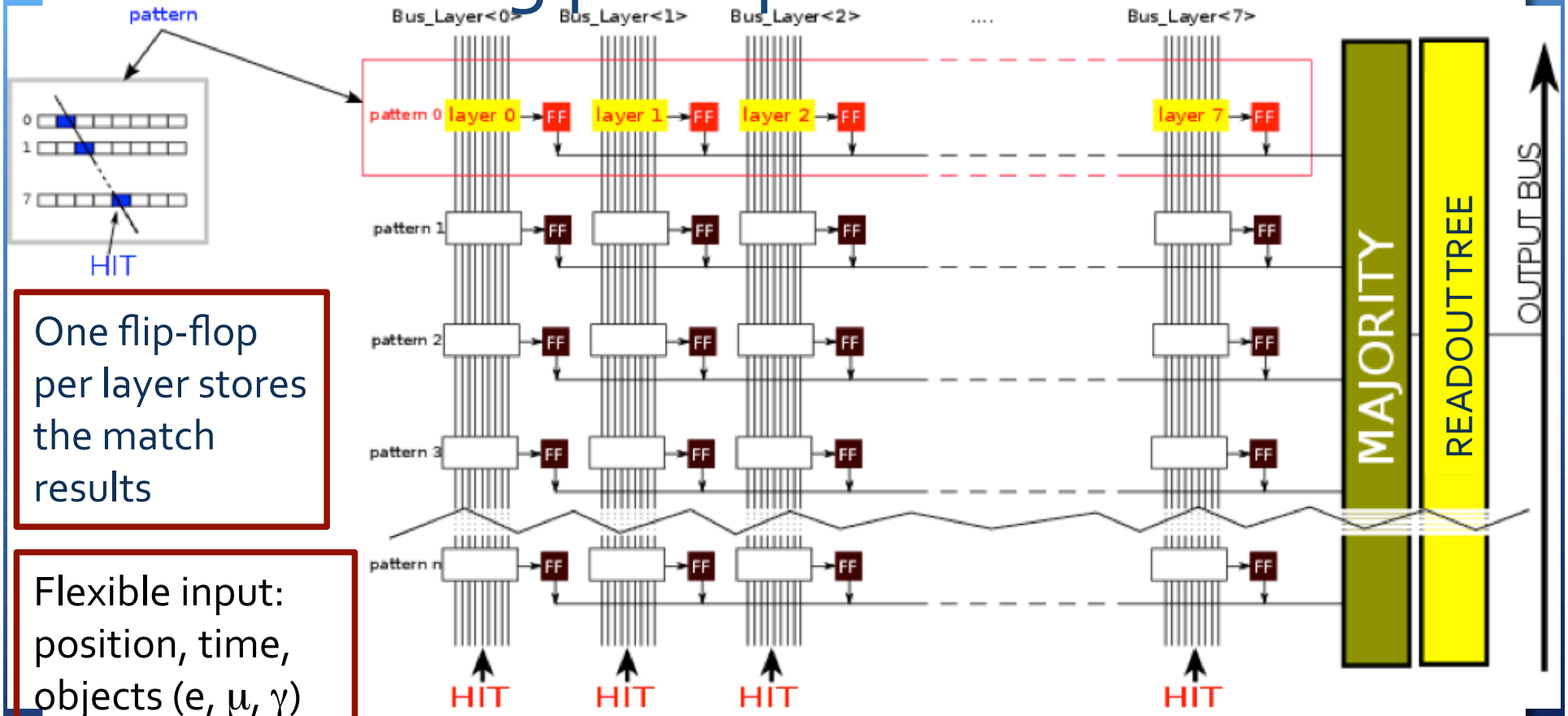
FLIC

FLIC sends tracks to ROS's. ATCA for global function TBD

FTK ROBs

HLT Processing

AM working principle



One flip-flop per layer stores the match results

Flexible input: position, time, objects (e, μ, γ)

Pattern matching is completed as soon as all hits are loaded.
Data arriving at different times is compared in parallel with all patterns.
Unique to AM chip: look for correlation of data received at different times.

AM chip scaling

Semiconductor manufacturing processes

10 μm – 1971
3 μm – 1975
1.5 μm – 1982
1 μm – 1985
800 nm – 1989
600 nm – 1994
350 nm – 1995
250 nm – 1997
180 nm – 1999
130 nm – 2002
90 nm – 2004
65 nm – 2006
45 nm – 2008
32 nm – 2010
22 nm – 2012
14 nm – 2014
10 nm – est. 2015
7 nm – est. 2017
5 nm – est. 2019

Half-nodes

V•T

- Scale effects
  - O(1000) medium size FPGAs are more expensive than AMchips
- The AM chip is a memory
  - There is a large degree of programmability

180nm in 2005 (5k patterns, 46kbits) AMchip03 (CDF)

65nm in 2014 (128k patterns, 18Mbits) AMchip06 (FTK planned)

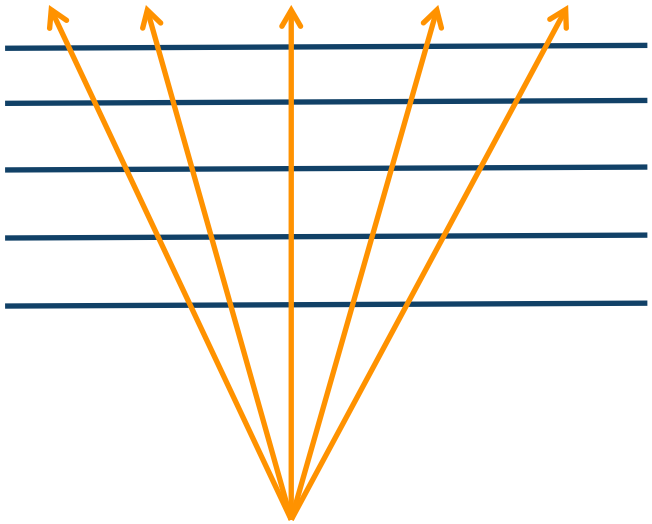
Scaled up by factor ~40 in 9 years!
Lot of design R&D beyond process size reduction!

There is always a pattern

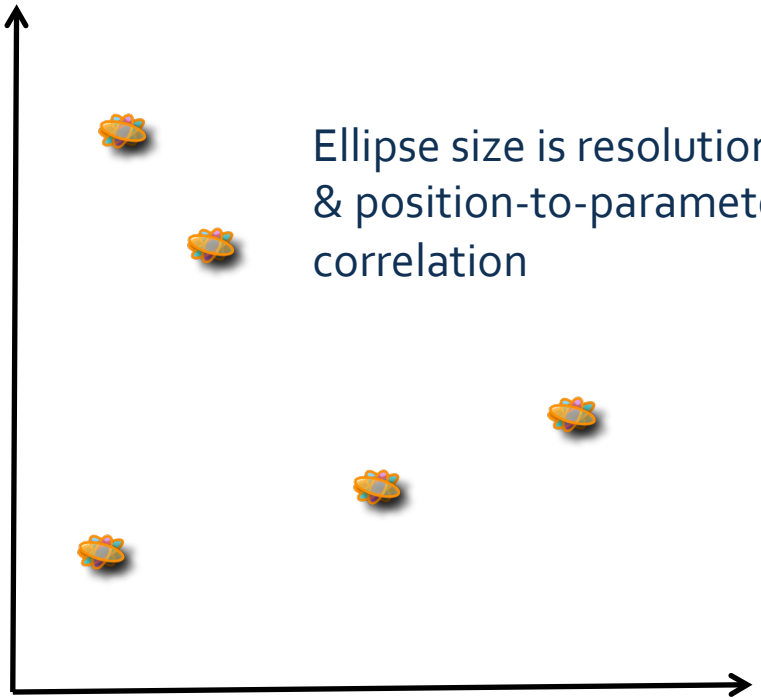
- Associative Memory (and similar algorithms)
  - define a pattern in the hit (measurement) space
    - a pattern is a dedicated piece of electronics
  - patterns are discrete
- Hough transform, other
  - define a "pattern" in the "track parameter" space
  - usually a "pattern" has its own logic
  - patterns can be discrete or contiguous

Easy most tracking

- Point like source
- Strait tracks only
  - 2 parameters
  - 1 hit (pix or stero-strips) determines the track



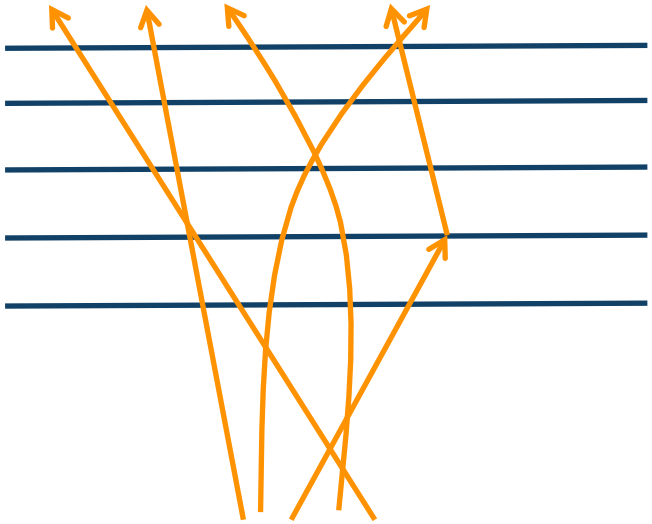
Track phase space



Ellipse size is resolution & position-to-parameters correlation

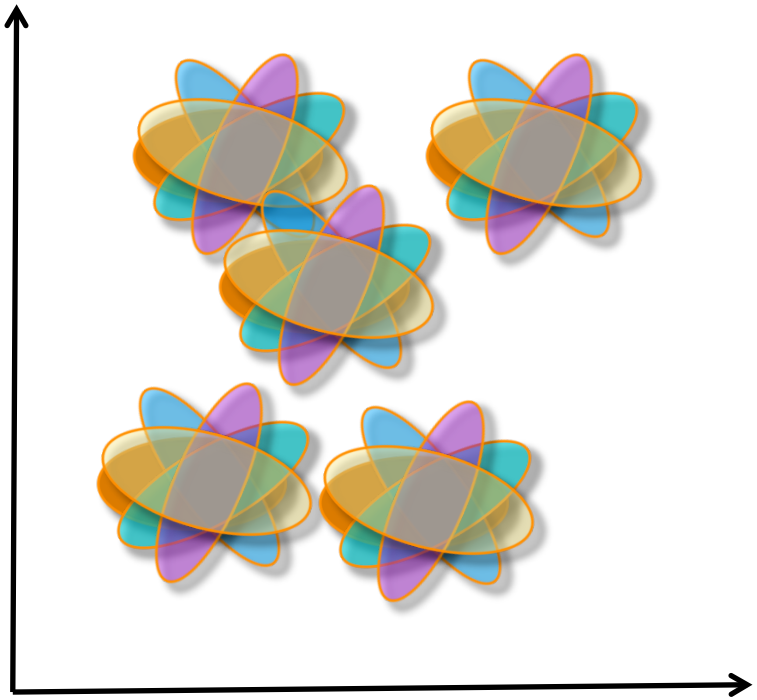
Adding more track parameters

- Adding curvature and significant multiple scattering
- Large source size (w.r.t. effect of curvature & M.S.)
- Tracking becomes highly non local



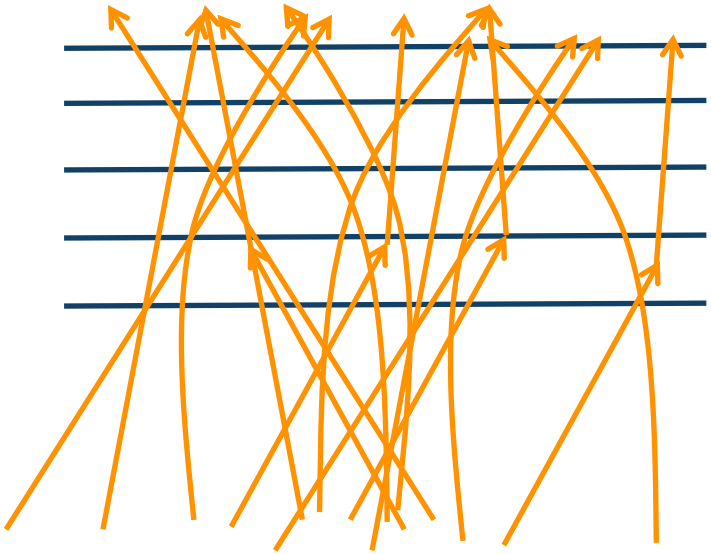
Large source region

Track phase space

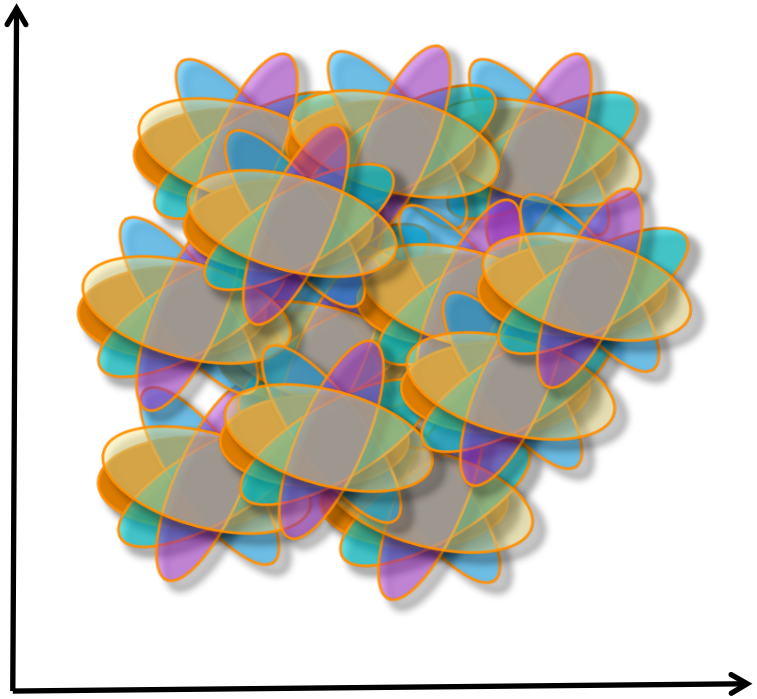


Increasing occupancy

- When occupancy high w.r.t. "hit size in track phase space"
- → tracking is tough



Track phase space

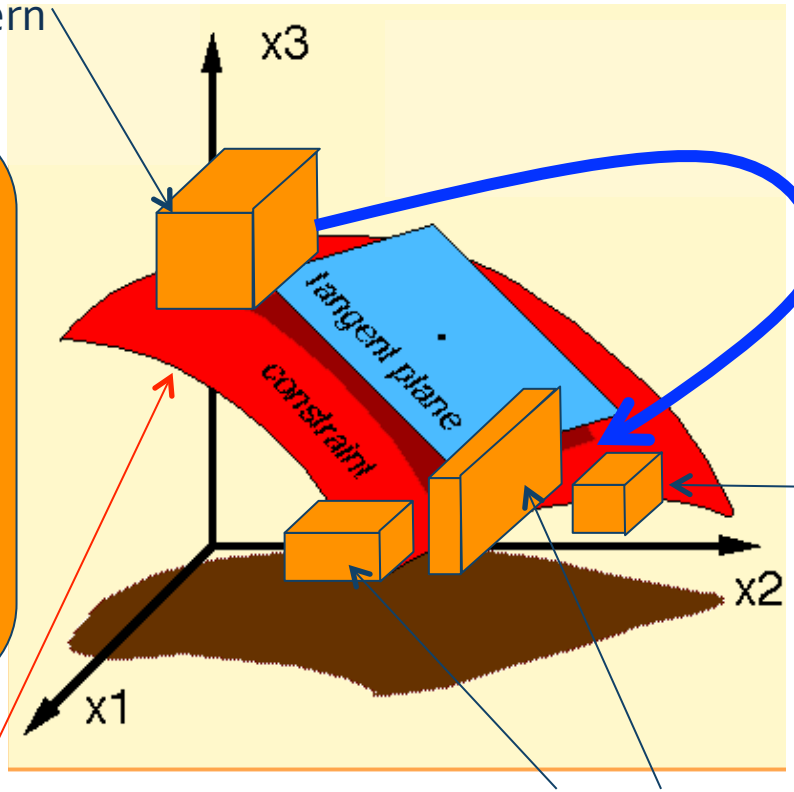


Variable resolution Associative Memory combines advantages of both hit space, and trk parameter space

The patterns: a different point of view

5 strip + 3 pixel layers
→11 coordinates
→11D hit coord. space

Large pattern



The pattern bank:
• covers the track manifold with patterns.
• covered space outside manifold → acceptance for fakes
• with variable resolution → dramatically improves S/N

For example: a factor of 2 better resolution on each coordinate
→ a factor 2^11 less matching volume

Thin pattern

Fixed resolution patterns → fixed aspect ratio

5D track manifold

Variable resolution patterns