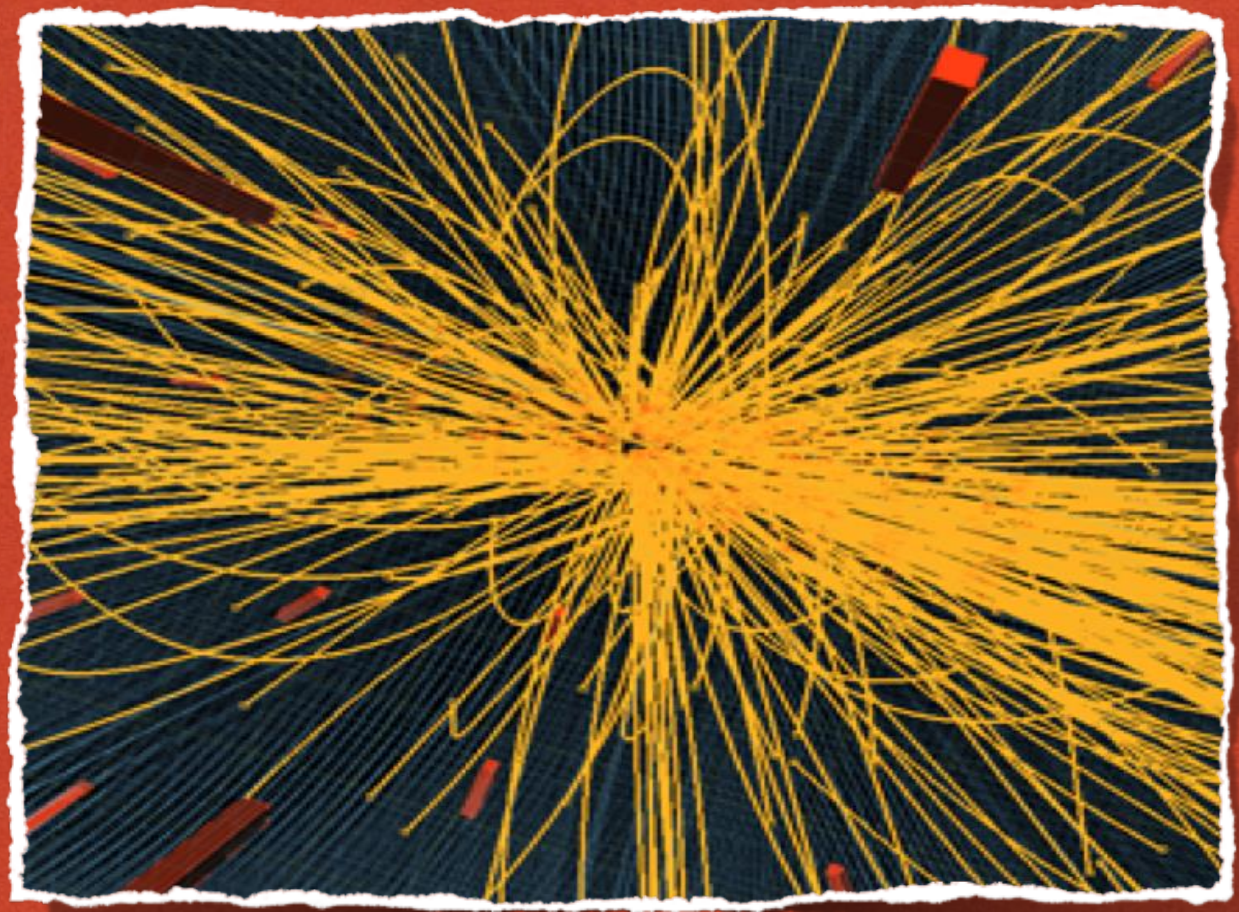


MUON ELECTRONICS R&D

TOWARDS LHC FORTHCOMING PHASES (WG3)

V.Bocci (RM1), R.Cardarelli (RM2), L.Guiducci (Bo), F.Loddo (Ba), L.Paolozzi (RM2), S.Veneziano(RM1), R.Vari(RM1), F.Montecassiano (Pd), S.Ventura (Pd), C.Cicalò (CA), A.Lai (CA), A.Cardini (CA)

(WG3 chair S.Ventura)

- Reasons to upgrade
- What's going on during Phase1
  - Alice
  - LHCb
- What's going on toward Phase2
  - Atlas
  - CMS
  - Multipurposes Front-ends
- Synergies

ELECTRONICS UPGRADE

Driving Motivations

Detector Upgrade

- increased channel count, better hermeticity, lower tracker mass
- Detector and its readout upgrade need an entangled R&D
- see talk WG2

Readout Requirements

- better timing resolution, higher trigger and data read-out rates and more flexible data processing
- trigger rate/latency/rules
- see WG1 and Trigger talks

Why?

Ageing/Longevity

- ten times higher radiation hardness
- give 10 more years to vintage >20 years old systems
- see talk WG4

Technical Concerns

- off detector relocation
- standard crates, power supplies, cooling system, ancillary modules

ELECTRONICS UPGRADE

What's to be done

General R&D Activities Coverage:

What?

- Deep sub-micron technologies (e.g. 130 nm and lower)
- High density, low mass interconnect and hybrid technologies
- Radiation hardness
- High reliability design and qualification
- Efficient power distribution systems and low power design techniques
- Low power, high speed electrical and optical links
- Modular electronics standards for high speed data back-end processing

ELECTRONICS UPGRADE

μ-trigger evolution towards HL-LHC

Different physics, different approaches:

ALICE , LHCb: μ from B-meson, J/ψ decays , ...
simpler Hardware-Trigger, if any
increase events processed by Software-trigger
→ **New readout electronics (by LS2)**

ATLAS , CMS : high-pT μ from heavy particles
increase purity of trigger events with sharper turn-on
Bring part of the present Software HLT to hardware
→ **More effort on new Trigger Hardware**

Ready by LS2

- Alice
- LHCb

While most of the upgrade for those experiments relates to Phase 1, some LS2 upgrade choices will define baseline options for the future

ALICE UPGRADE

The Muon Tracking System

After LS2 (2018):

- 50 kHz Pb-Pb interaction rate (↗ x 10) (---→→ 100 kHz ??)
- 2 MHz p-p

• Expected Muon Trigger maximal rates – ~ 5 kHz (---→→10 kHz ??) for p_T > 1 GeV/c

From Trigger mode to "continuous" read-out mode

(continuos sampling @ 10-40 MHz & R/O pipeline)

To run at f_{Trig} = 5-10 KHz all the electronics and read-out:

- New Readout cards (CROCUS): => $T_{RO} \approx 100$ μs
- FEE upgrade: ADC + analogic ...: => > $T_{RO} \sim 20$ μs
- All the links on the detectors (buses, bridges, translator) to be changed

ALICE UPGRADE

A common Alice Architecture

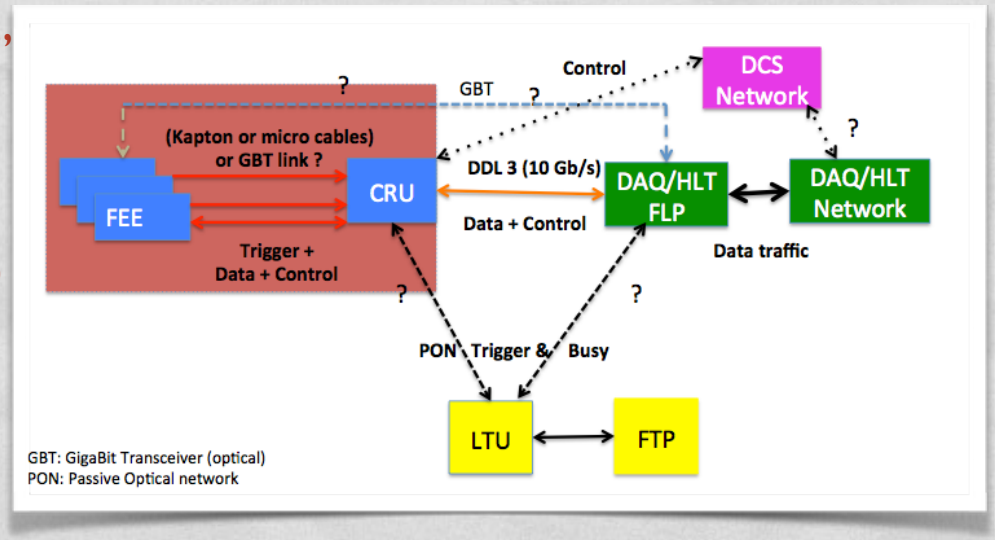
INFN Cagliari

- FEE chip "common" to TPC + MUON. SAMPA CHIP (Brazil)

more on backup slides

- gain and shaping time extension
- sampling and data readout run independently
- ASIC on TSMC 130nm

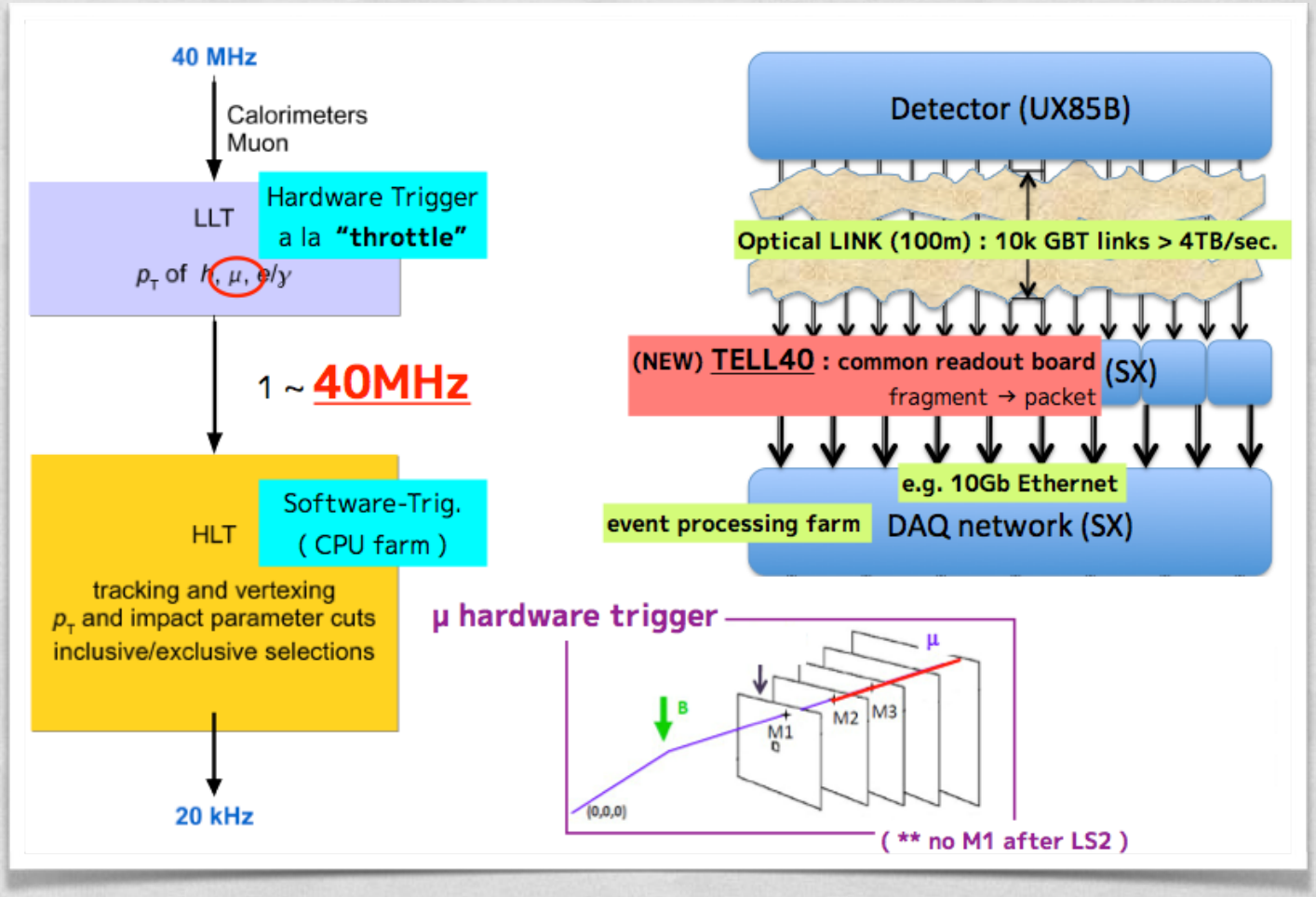
- CRU (Common Read-Out Unit) (Crocus) "common" to ITS, TPC, MUON +...
- Links FEE -> CRU :"common" types
- Common data link (DDL 3) between CRU and DAQ
- CRU in radioactive area
- Design at early stage:
  - architecture, components, mecha



LHCb UPGRADE
DAQ/Trigger Scheme

- No more Hardware Trigger
- Continuos readout @40MHz and software based event selection based on a computing farm (HLT)

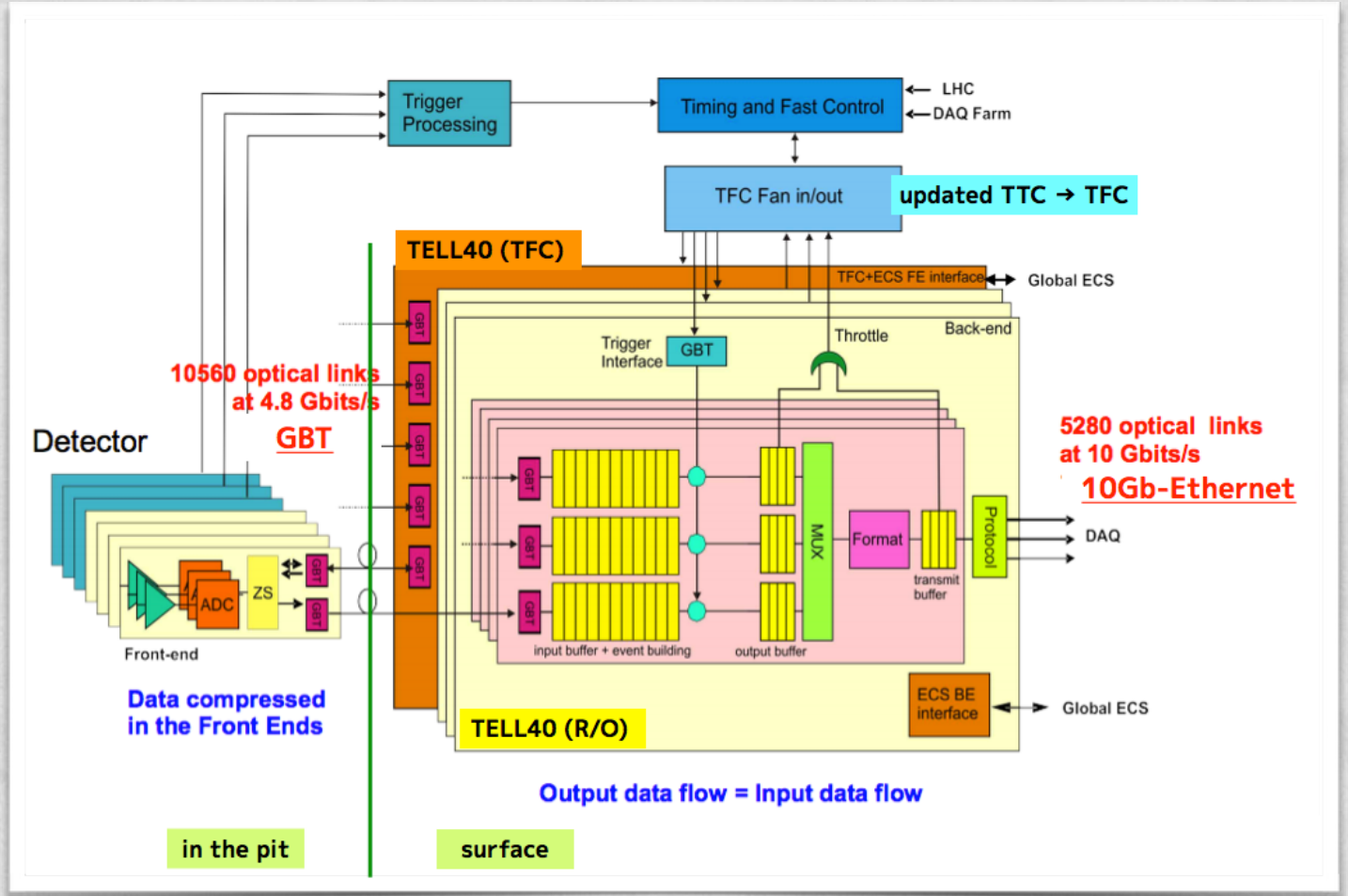
INFN Cagliari, Roma, Roma Tor Vergata, LNF



LHCb UPGRADE

Readout

- Data links based on 4.8Gbps GBT links
- All ODE (on detector) boards replaced (nODE)
- GBT also for Slow Controls and Clock/ Pulse distribution (nSB, nPDM)
- TELL40 boards to merge and interface to DAQ
- FPGA Microsemi Actel



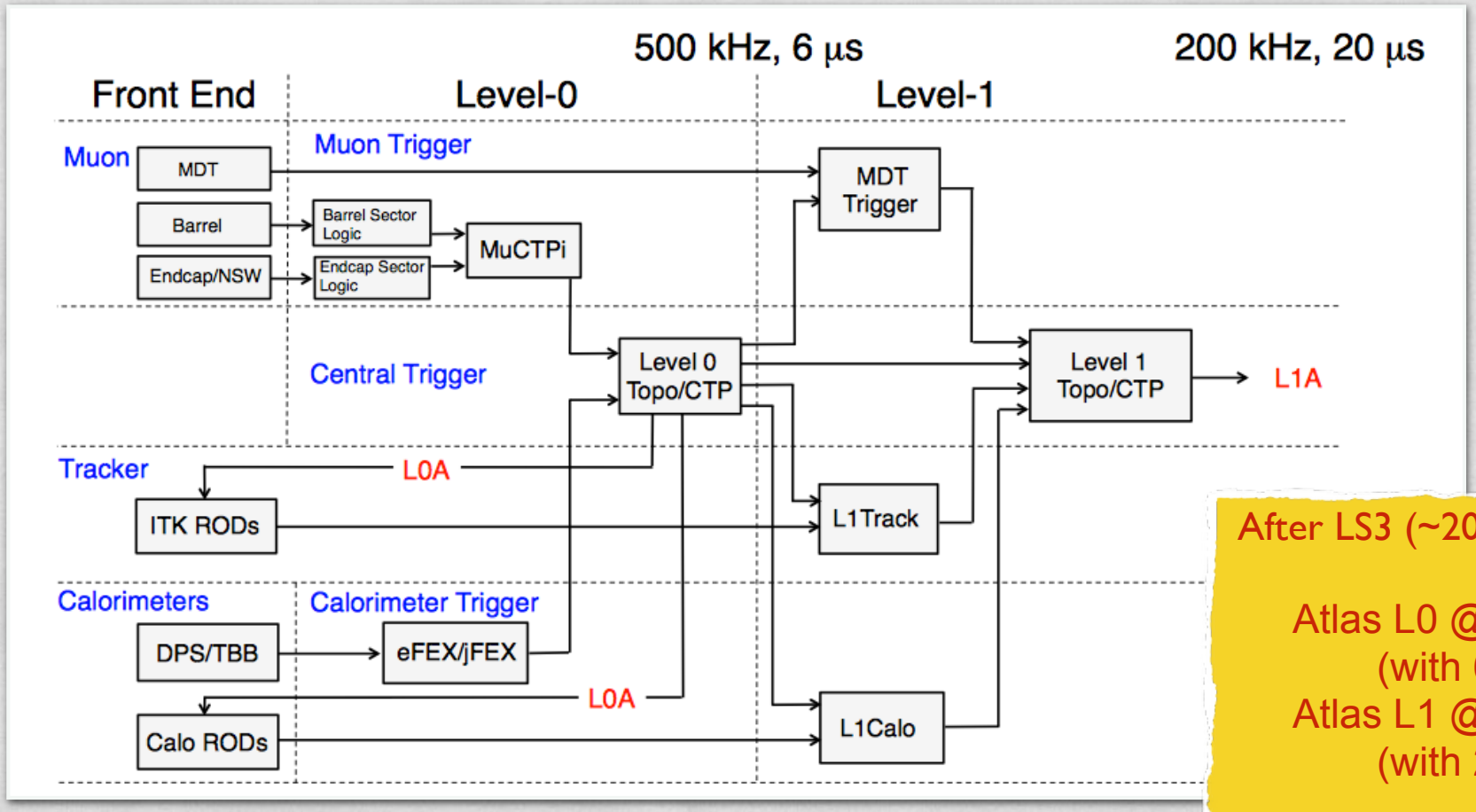
Phase2

- Atlas
- CMS

ATLAS UPGRADE

A split first level trigger layer

Tracking integration in L1 through ROI identification after L0



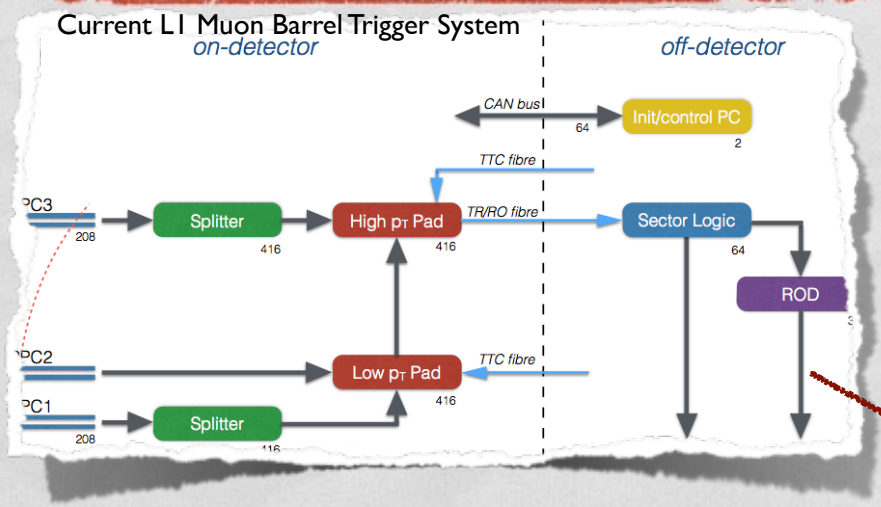
After LS3 (~2025)

Atlas L0 @ 500kHz
(with 6μs latency)
Atlas L1 @ 200kHz
(with 20μs latency)

RPC hit rate: ~1 kHz/cm2

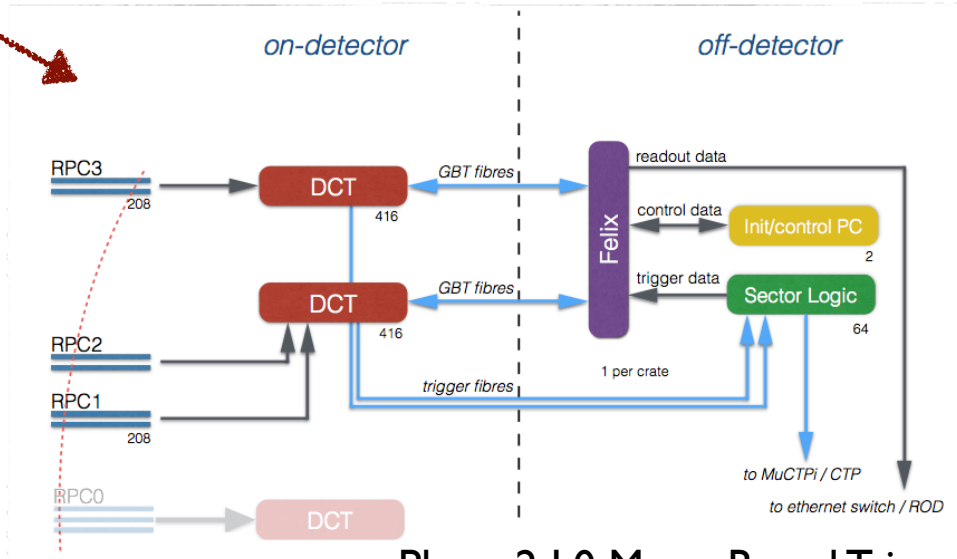
ATLAS UPGRADE
RPC

INFN
Bologna, Napoli, Roma,
Roma Tor Vergata



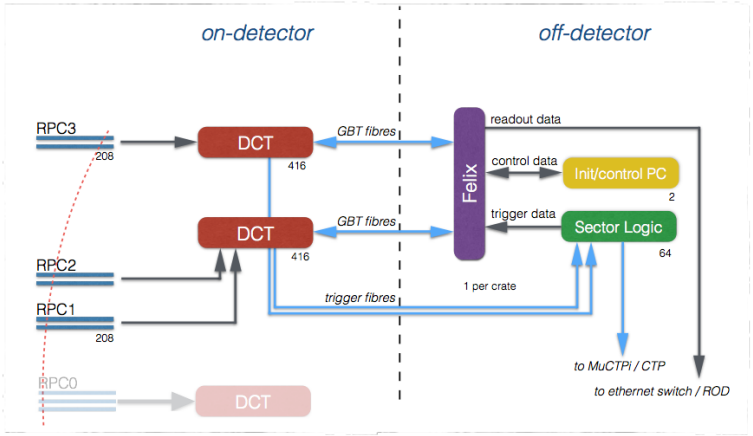
- Most of the trigger logic will be located off-detector

- The current RPC front-end cabling will not be replaced (costs and accessibility reasons).
- Splitter boxes will be possibly removed.
- Each Pad box will be replaced by a new DCT box.
- The DCT box will collect RPC front-end data, and perform some simple logic before sending the data off-detector



Phase 2 L0 Muon Barrel Trigger

ATLAS UPGRADE
RPC DCT



ITEM	Quantity	
DCT	832	
Trigger link	832	(+416)
RO link	832	
Sector Logic	64	
ROD	32	
Crates	8	

- The time of arrival of RPC hits (~2 ns time resolution) will be added to the hit data
- RPC signals Time-over-Threshold measurement is being considered to improve RPC spatial resolution
- one **GBT link** per DCT will send both trigger and readout data
- automatic noisy channel masking logic
- SEU recovery logic
- Possible data reduction logic to decrease the bandwidth on the fibre
- Use of **FPGAs** instead of ASICs for the on-detector electronics

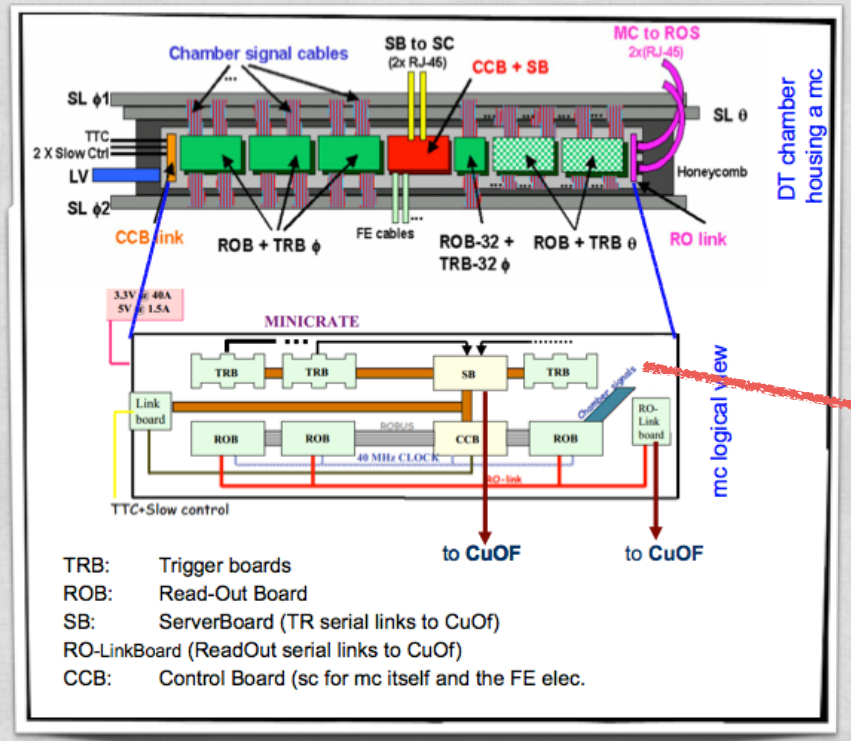
CMS UPGRADE

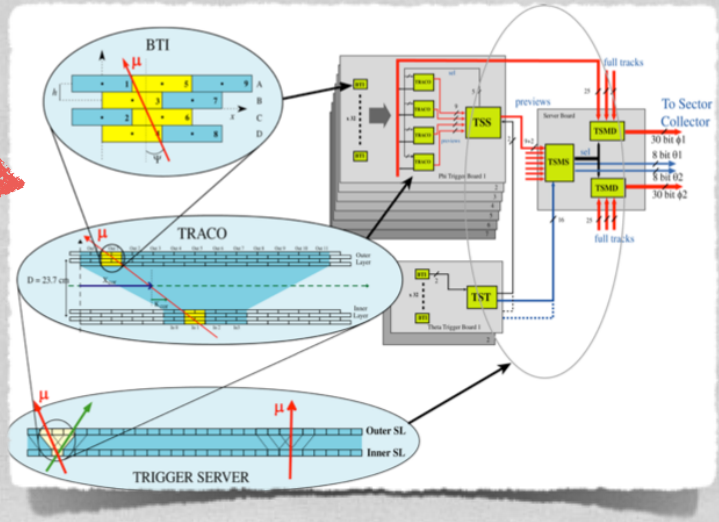
Muon Barrel Overview

After LS3 (2025)
CMS L1 @ 500kHz to 1MHz
(with 20μs latency)

- Trigger primitives are generated locally on the detector
- The readout architecture, also local, will not sustain Phase2 trigger requirements (latency and trigger rules)
- Some components obsolescence and radiation damages will anyway require a full detector, costly maintenance

DT chamber electronics (Minicrate)

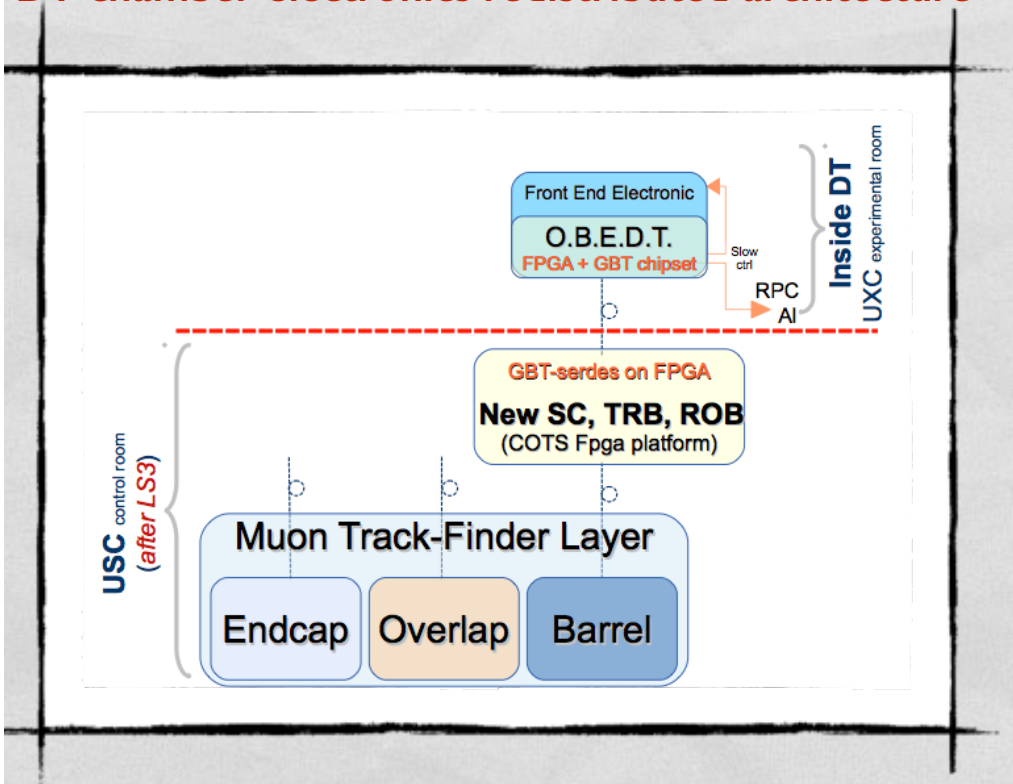




CMS UPGRADE

Muon Barrel Phase2 Minicrate Replacement

DT chamber electronics redistributed architecture

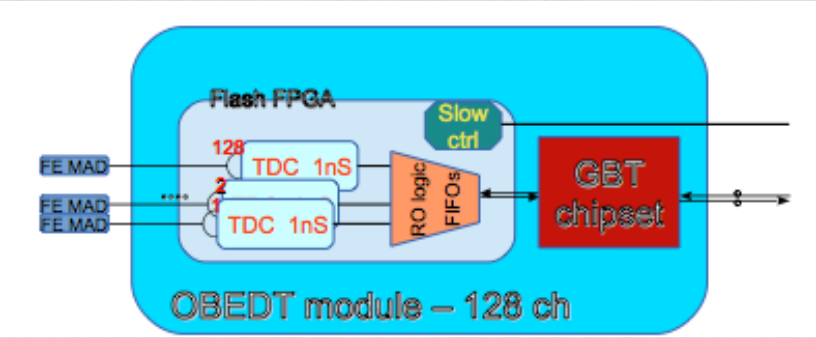


- Only legacy front-end and a new FPGA based Time Digitization electronics remains on the chambers (Minicrate)
- **GBT** based link transmission (2Gb/s throughput per link - max 7 links/ chamber)
- An estimate of ~20M equivalent asic logic gates to provide a whole DT Minicrate functionality in USC (~1 FPGA today)
- Trigger & Readout paths overlap
- Trigger primitives will be based on full time resolution
- UXC cavern power requirements halved

CMS UPGRADE

Muon Barrel Phase2 plans

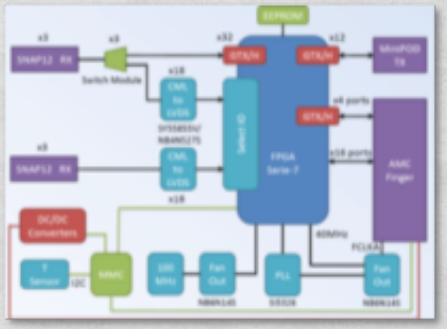
DT onboard module



INFN
Bologna, Padova,
Torino

Next step R&D

- Multichannel TDC implementation: on Flash **FPGA** (Microsemi IGLOO2 65nm)
  - TDC 5bit/~1ns
  - O(100)TDCs on the same FPGA IC
  - Radiation tolerance tests, according to HL-LHC doses
- Trigger logic algorithms porting on μTca FPGA boards (e.g. CMS Phase 1 L1 trigger processors)



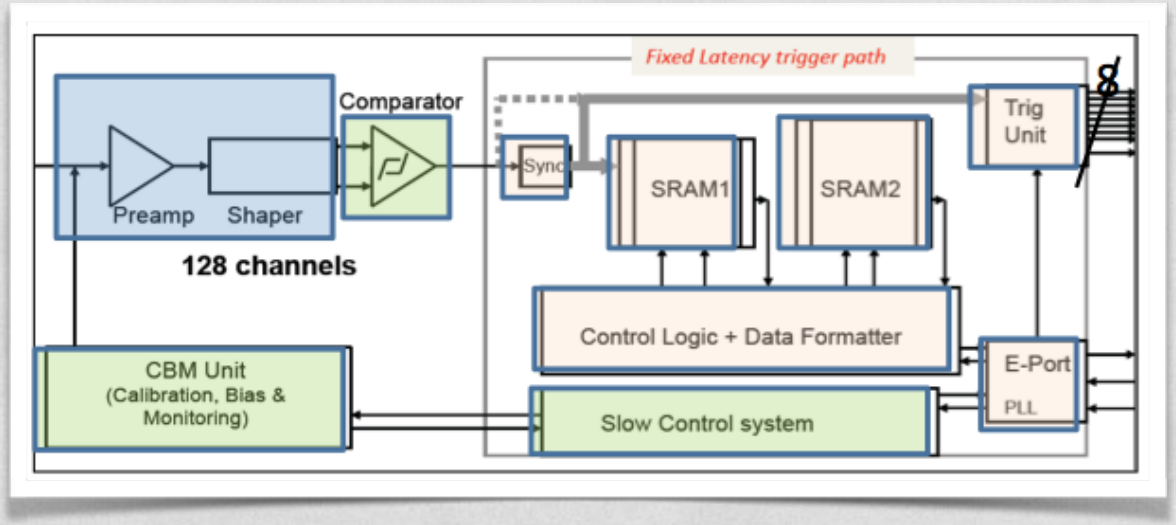
Multipurpose Front End Developments

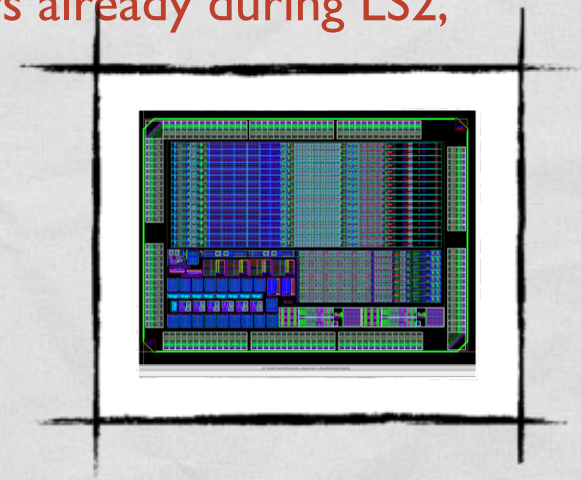
- CMS GEM Chip
- SiGe Preamplifier

FRONT END UPGRADES

VFAT3: a new Front-End chip for CMS GEM detectors

The VFAT3 chip based readout will equip the CMS GEM chambers already during LS2, but already suitable for Phase2 beam conditions.





The chip will be highly configurable and capable to satisfy the requirements of different detectors (detector capacitance, gain, peaking time)

Chip Status

- **Design of the block analog channel, the calibration & bias block and CFD is done**
- **Slow Control interface and the Readout section is under development**
- **On May.2014, the 1st prototype containing only the analog blocks (16 channels) and a simple slow control interface will be submitted to foundry**
- **Design of the first 128-channel VFAT3 started**

INFN Bari

CERN, INFN- Bari, CEA-Saclay, Brussel University (ULB) and Lappeenranta University of Technology

FRONT END UPGRADES

Ultra low-noise amplifiers R&D

INFN
Roma Tor Vergata

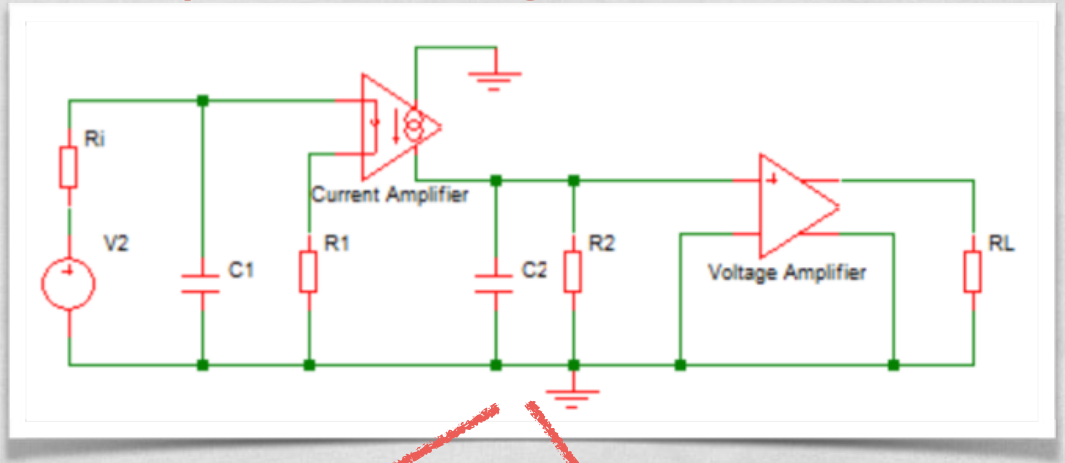
SiGe transistors technology:

- Low Power
- High Linearity
- Ultra Low Noise
- High speed of operation for RF, analog, memory and digital circuits
- Low cost

"One technology fits all":

- High Reliability
- Radiation hardness
- Easy integration
- An active developers community

Preamplifier Block diagram



Silicon technology

Voltage supply	3–5 Volt
Sensitivity	2–4 mV/fC
Noise (independent from detector)	4000 e^- RMS
Input impedance	100–50 Ohm
B.W.	10–100 MHz
Power consumption	10 mW/ch
Rise time $\delta(t)$ input	300–600 ps
Radiation hardness	1 Mrad, 10^{13} n cm^{-2}

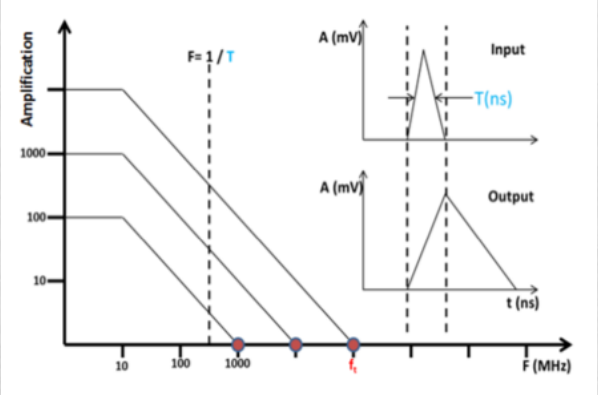
SiGe technology

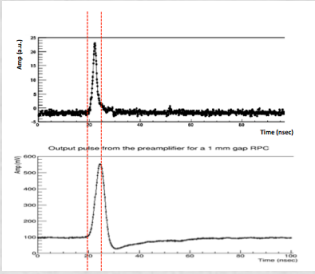
Voltage supply	2–3 Volt
Sensitivity	2–6 mV/fC
Noise (independent from detector)	500 e^- RMS
Input impedance	50–200 Ohm
B.W.	30–100 MHz
Power consumption	2 mW/ch
Rise time $\delta(t)$ input	100–300 ps
Radiation hardness [4]	50 Mrad, 10^{15} n cm^{-2}

FRONT END UPGRADES

RPC SiGe Front-end

Working Strategy

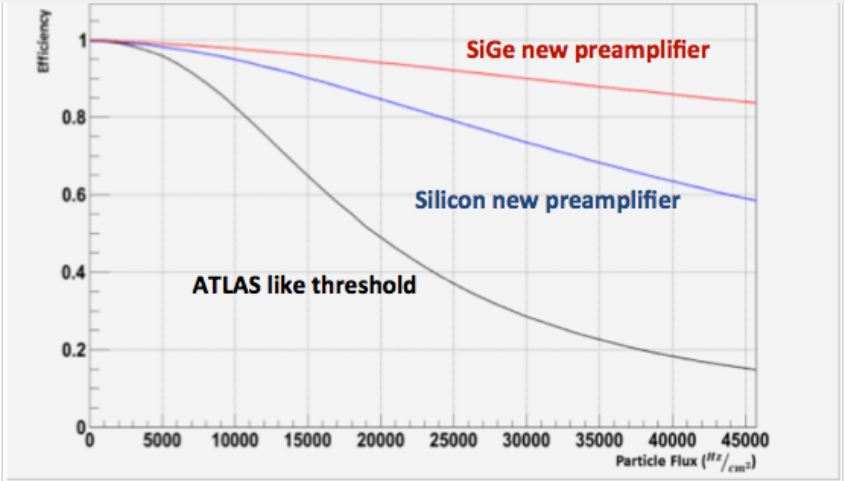




Actual Result for an RPC detector

- small integration time 10ns (pileup)
- fast rise time: 100 ps (uncorrelated bkgnd)
- low noise (500e^- RMS)
- low power (1.5V power supply)
- amplification transferred from the detector to the front end electronics
- suitable for large detector capacitance (up to 1nF)

Efficiency at different fluxes for 1mm gap RPC operated 200 V after efficiency knee (at cosmic ray rates)



Using a more sensitive front end allows to operate the detector at a lower gain, improving rate and in most cases reducing the ageing of the detector

CONCLUDING
Shared and Commons

Common concepts:

- Bring as much as possible off detector
- Use homogenous hardware among different subsystems

Shared Technologies and R&D:

- radiation hard Front-End Asics
- high-speed optical links (e.g. GBT)
- FPGA with high-density serial links & performance
- usage of FPGA in radiation areas
- ATCA or µTCA cards

As an effect of standardisation, although final choices for Phase2 might be due in three/four years from now, some LS2 scheduled upgrades will define a guideline for the whole LHC world.

BACKUP SLIDES

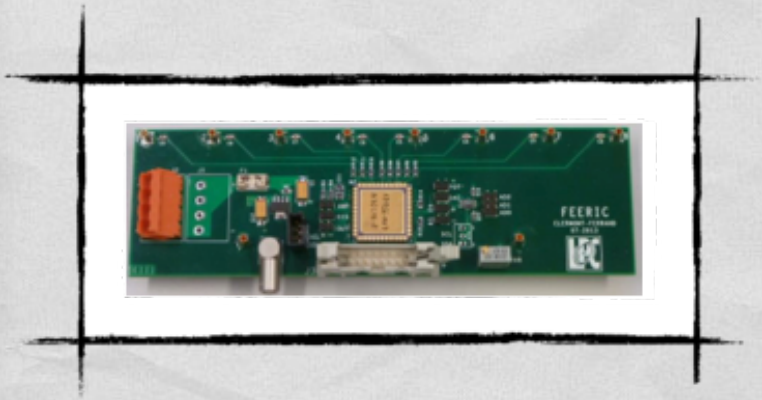
ALICE UPGRADE

The FEE SANPA CHIP

Muon Chamber FEE chip requirements

		MCH	
		Now	**Upgrade**
Polarity		Pos	Pos
Detector capacitance		40 – 80 pF	40 -80 pF
Peaking time		1200 ns	**~ 200 ns ? ?**
Shaping		2th order	**2** or 4th order
Sensitivity (mV/fC)		4	(5)
Gas gain		~2. 10^{4}	~2. 10^{4}
Noise (electrons)		640e-@0pF 1000-1800 e-	**≤ 1000 -2000 e-**
Linear Range (V)		~1,4V	
Linear Range (fC)		~ 650 fC (full range)	**400 fC** (full range) (with 200 ns Tp)
Signal coding		12 bits on 2,5V	11 bits (on 2 V) **10 bits** ?
Power consumption (per ch)		13mW (FEE board)	< 15 mW
Channel per chip		64 (per FEE board)	64 (per FEE board)
Chan per readout link		~50000/DDL	

- gain and shaping time extension
- sampling and data readout run independently

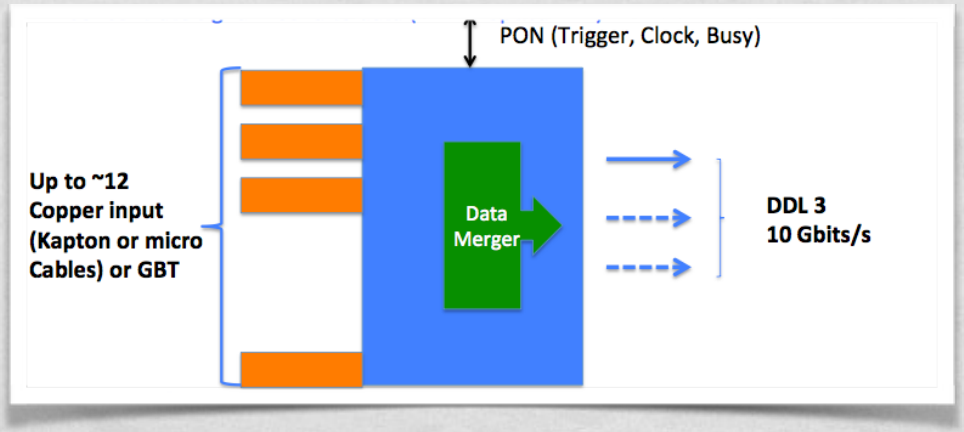


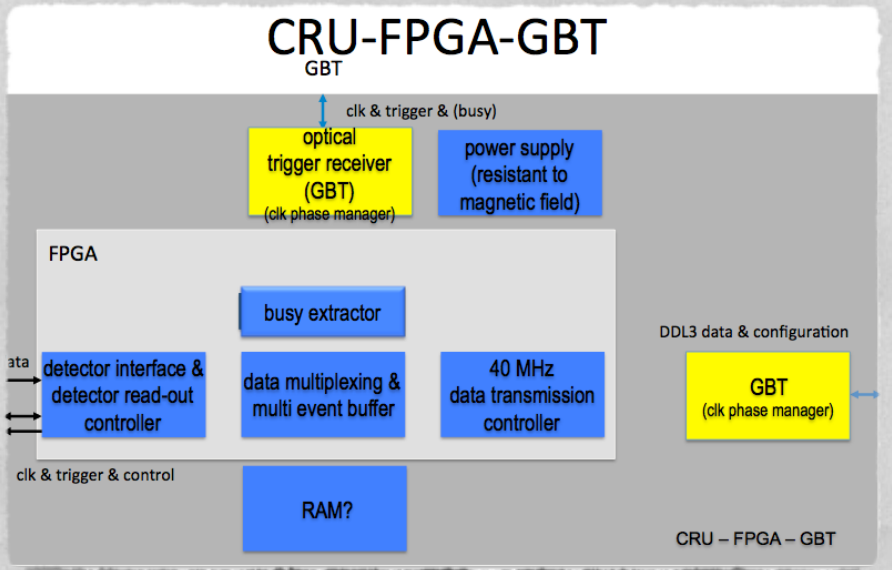
ASIC on TSMC 130nm

- In total 17,000FE cards (1 FE Chip = 32ch. , 1FE Card = 2FE chips)
- Power consumption : 15 to 20mW/ch. (x 1/4 w.r.t. the current chip)

ALICE UPGRADE
Common Readout Unit (CRU)

- Will replace CROCUS
- Common to TPC+MUON+ITS+…
  - common blocks but 2 kind of links/connectors (ITS / (TPC, MUON..))
- Concentrates and merge Data

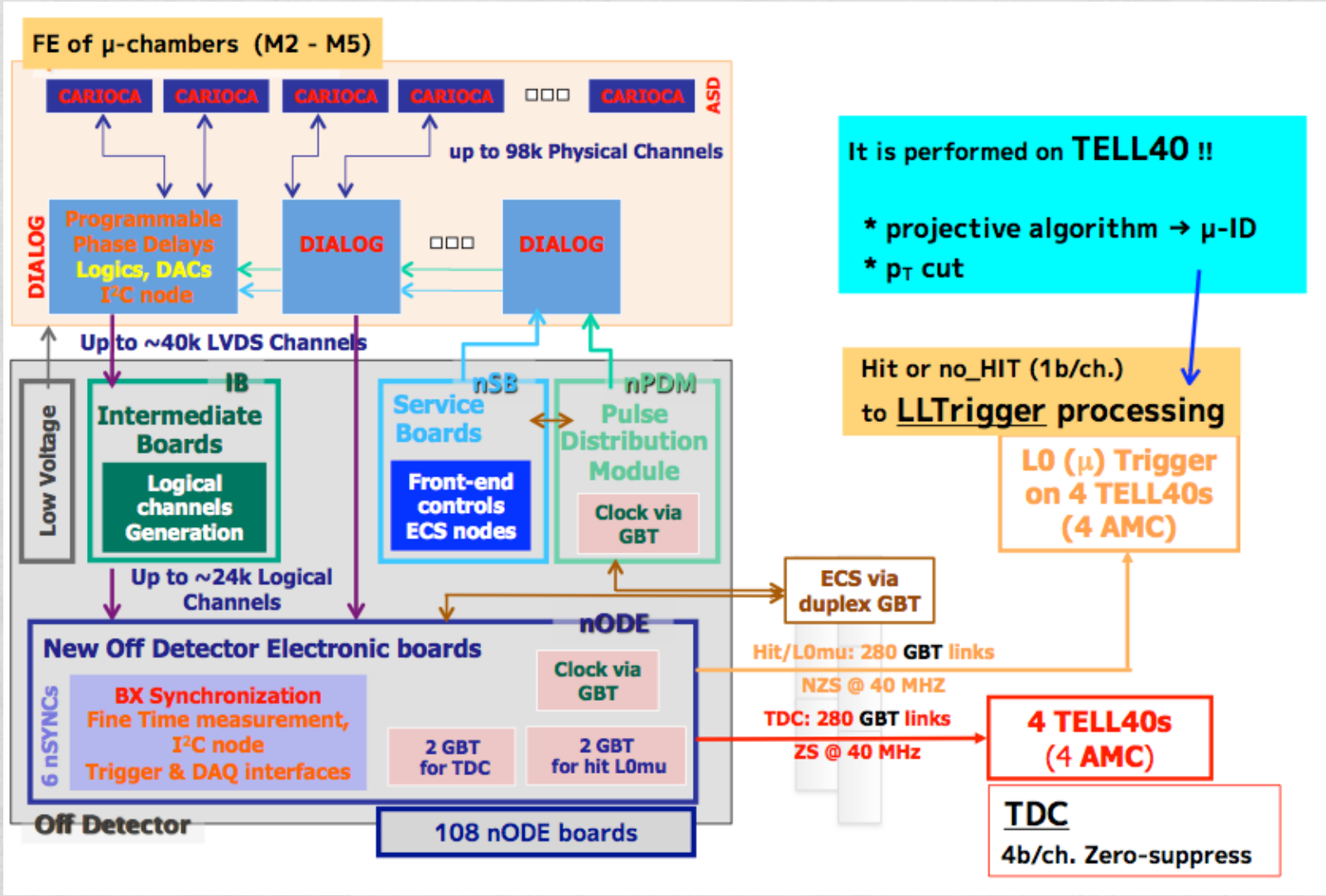




- CRU in radioactive area
- Design at early stage:
  - architecture, components, mechanics

LHCB UPGRADE

μ-Readout & μ-LLT



FRONT END UPGRADES

VFAT3: a new Front-End chip for CMS GEM detectors

Final **Specs**:

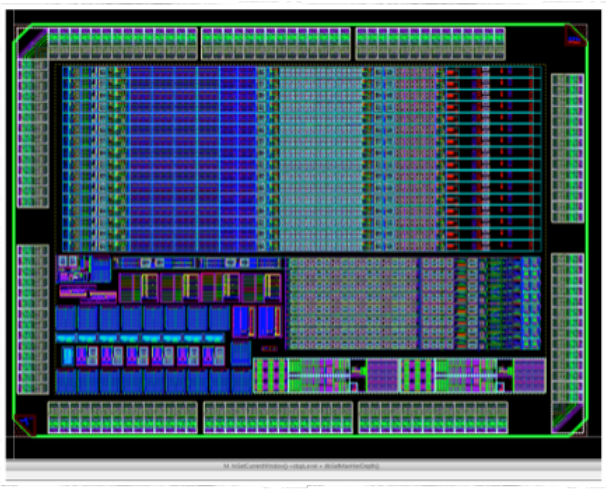
- 128 channels
- Technology: IBM 130 nm
- Input capacitance: from 1 pF to 80 pF
- Programmable peaking time: 25 ns, 50 ns, 75 ns, 100 ns, 200 ns, 400 ns
- Charge sensitivity: from 1.25 mV/fC to 50 mV/fC
- Noise: depends on the configuration

Example (Tpeak = 100 ns, Gain = 10 mV/fC)→ENC = 510 e^- + 13 e^-/pF

- Polarity: dual
- Constant fraction discriminator to decrease the amplitude time walk and not degrade the time resolution

- Fixed latency data path: 64 bits/BX synchronous with LHC 40 MHz clock for fast hit information

- Variable latency data path: full granularity via e-port (GBT)
  - Data are read upon LV1A arrival
  - SRAMs size according to LV1A max. latency (3.2 us→→20 us) and rate specification
  - Data are transmitted with timestamp to identify the BX



Chip Status

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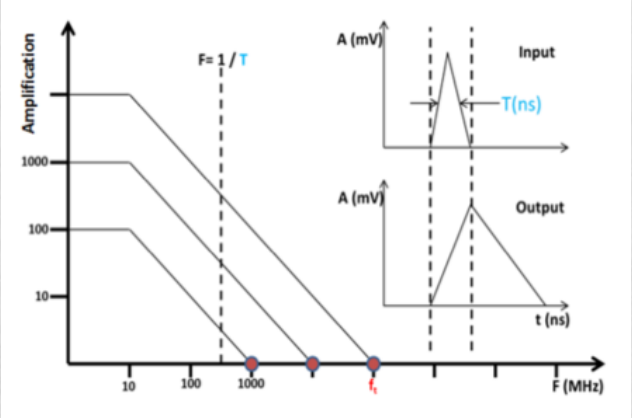
- Design of the first 128-channel VFAT3 started

FRONT END UPGRADES

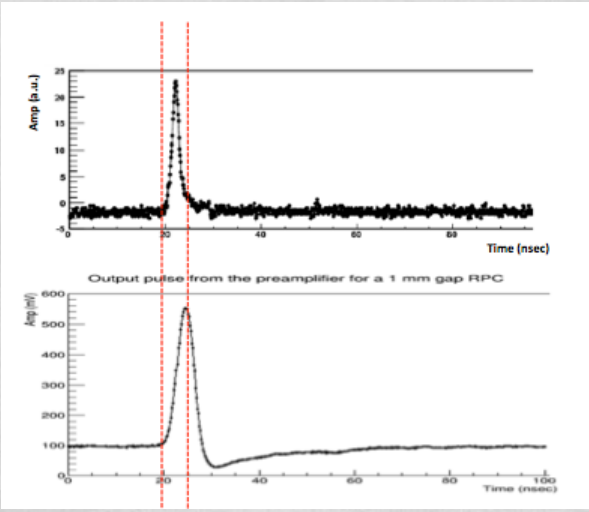
Ultra low-noise amplifiers R&D

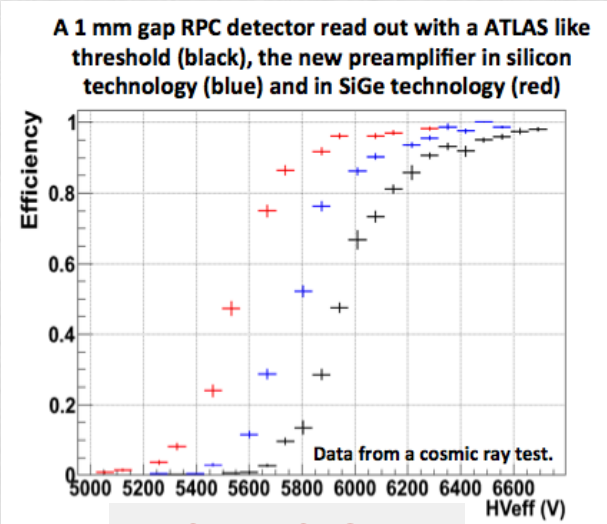
Working Strategy



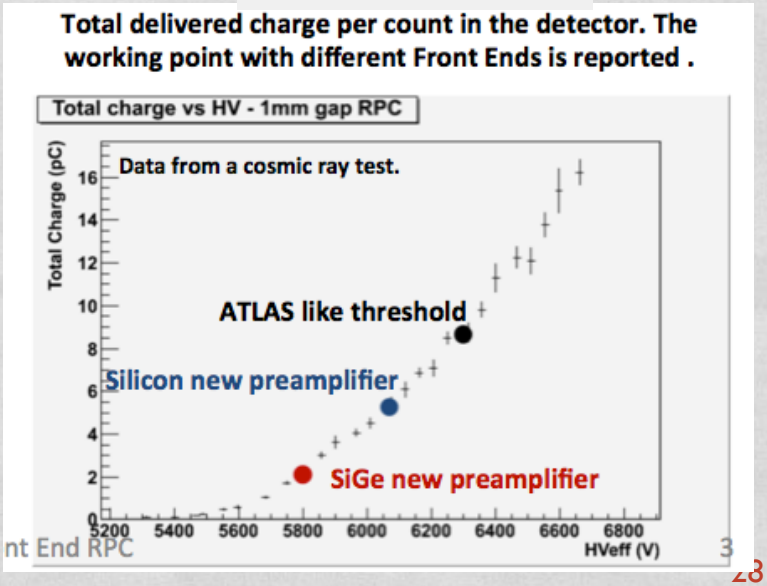
- small integration time 10ns (pileup)
- fast rise time: 100 ps (uncorrelated bkgnd)
- low noise (500e⁻ RMS)
- low power (1.5V power supply)
- amplification transferred from the detector to the front end electronics
- suitable for large detector capacitance (up to 1nF)
- can interconnect the preamplifier to the detector via a coaxial cable

Actual Result for an RPC detector





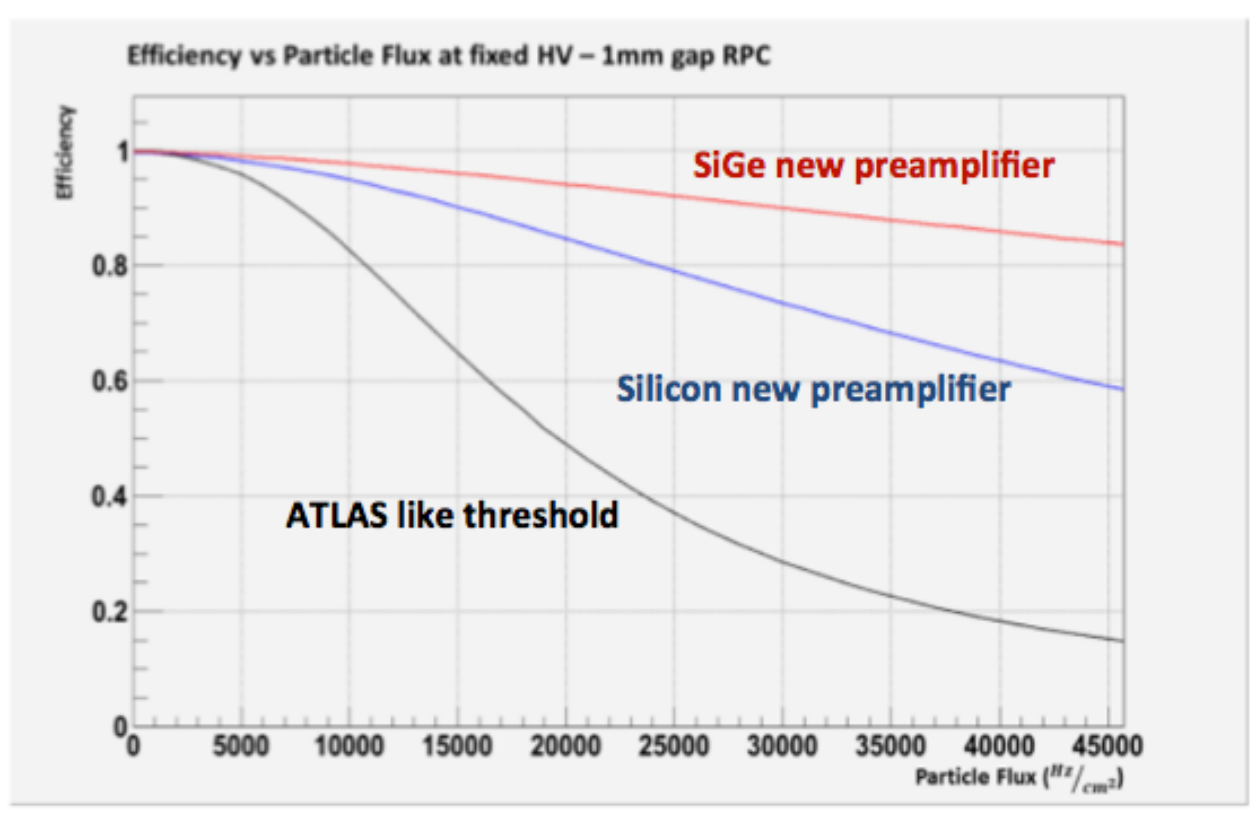
Si vs SiGe



FRONT END UPGRADES

RPC SiGe Front-end

Efficiency at different fluxes for 1mm gap RPC operated 200 V after efficiency knee (at cosmic ray rates)



- Using a more sensitive front end allows to operate the detector at a lower gain
- Operating the detector at a lower charge per count means improving rate and in most cases reducing the ageing of the detector
- The simulations are in agreement with experimental data collected at the Gamma IrradiaBon Facility at CERN

FRONT END UPGRADES

RPC SiGe Front-end

- small integration time 10ns (pileup)
- fast rise time: 100 ps (uncorrelated bkgnd)
- low noise (500e$^-$ RMS)
- low power (1.5V power supply)
- amplification transferred from the detector to the front end electronics
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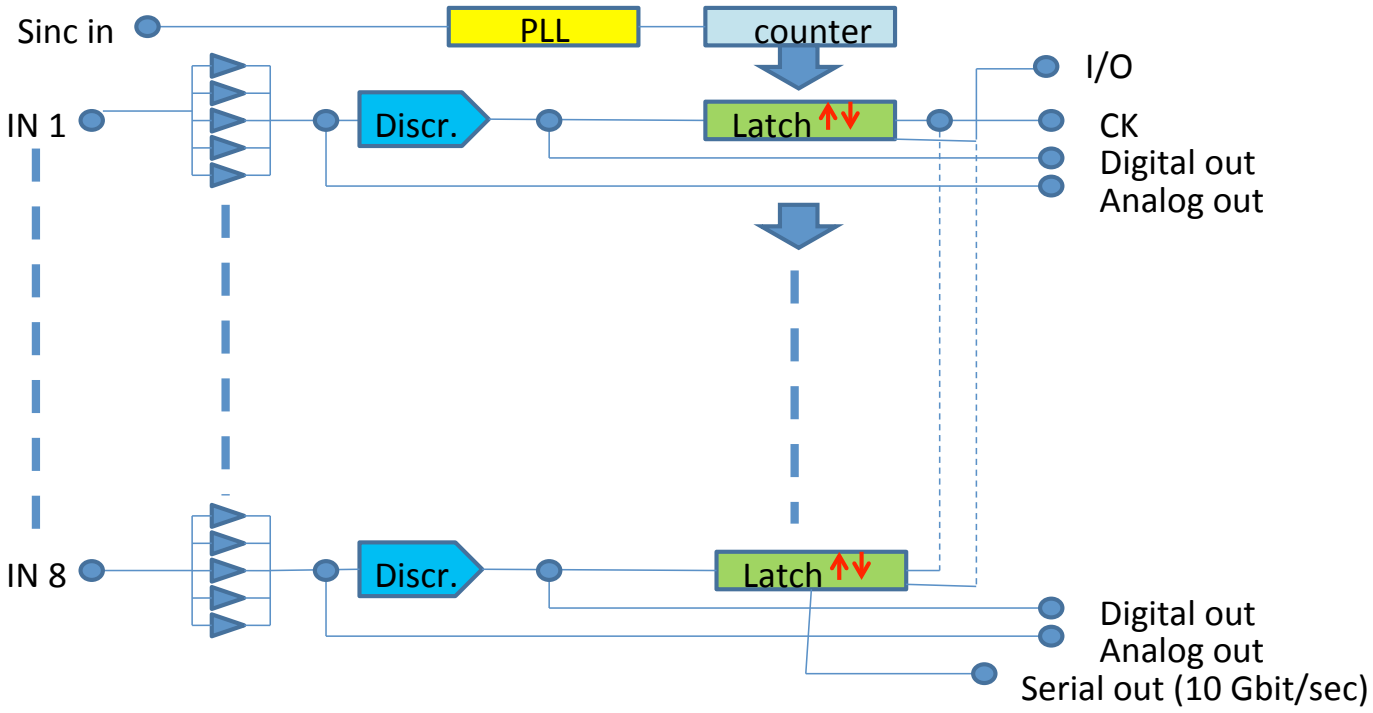
Block diagram and performance of a new full custom front-end chip in SiGe technology

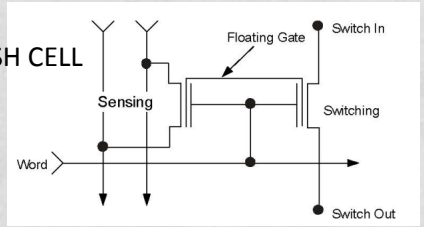


FPGA R&D

Use of Radiation tolerant FPGA in LHC Upgrade

Configuration in Flash cell (Actel Microsemi) Simpler FPGA

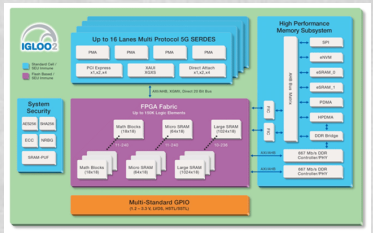
FLASH CELL



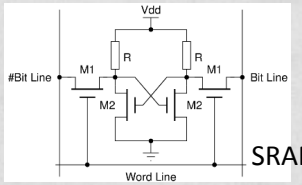
The Flash CELL is more robust to radiation than SRAM based . About 1 SEU every 10^{11} Protons/cm^2.

OLD family Actel Proasic in all LHC experiments.

New family IGLOO2 flash tecnology as Proasic more performance but no data from Radiation tolerance.



Configuration in SRAM (Xilinx,Altera) High end FPGA



SRAM CELL

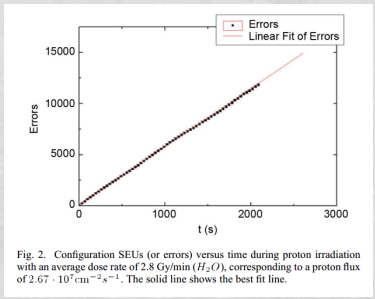
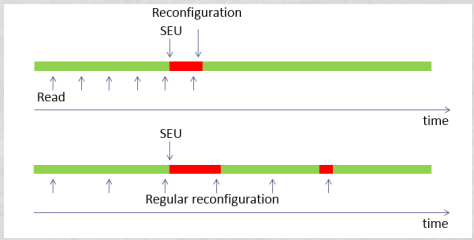


Fig. 2. Configuration SEUs (or errors) versus time during proton irradiation with an average dose rate of 2.8 Gy/min (H_2O), corresponding to a proton flux of $2.67 \cdot 10^7 cm^{-2} s^{-1}$. The solid line shows the best fit line.

Linearity
errors vs Radiation
About
1 SEU every every 10^8 /cm^2



Mitigation Strategy:
Periodic reconfiguration
or configuration on error.

Old Xilinx Virtex in Atlas (muon) and CMS (Tracker)
new family: some study inside INFN during SuperB.

V.Bocci 2014