IFD2014
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Future Detectors for HL-LHC
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Hybridization and Interconnection technologies

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Introduction

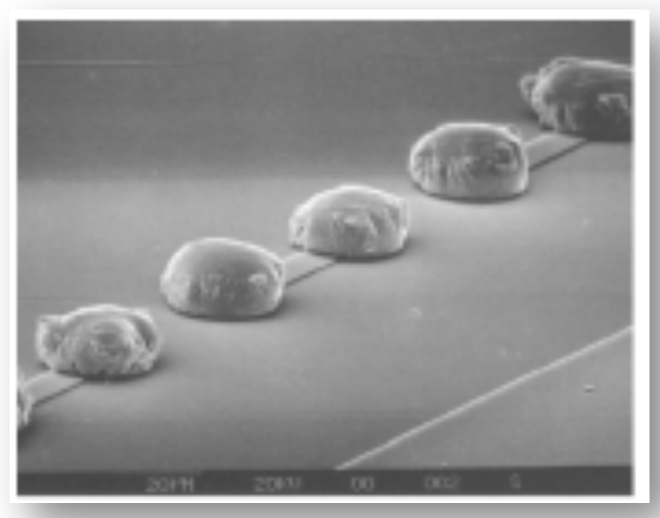
✓ We describe interconnections between sensor elements to read-out electronics or between on-detector electronics to the external services.

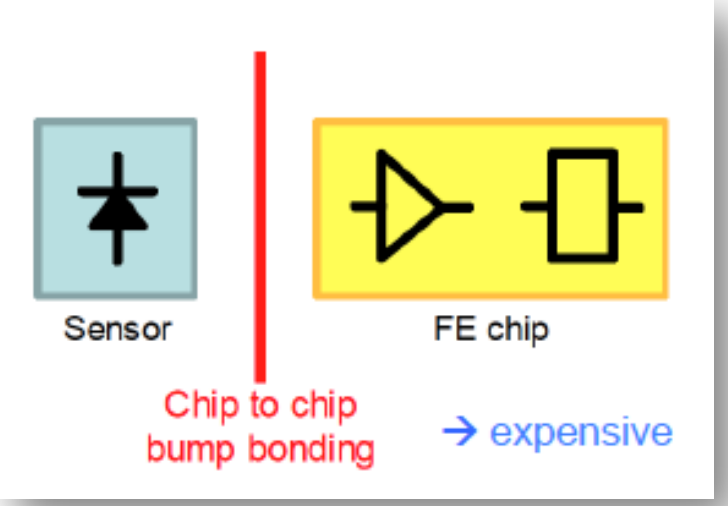
✓ Sensor → Read-out at the pixel level

✓ Read-out→ external services
- Flex-hybrid
- Wire-bonding
- Tab-bonding
- Laser soldering

✓ 3D integration

Bump-Bonding

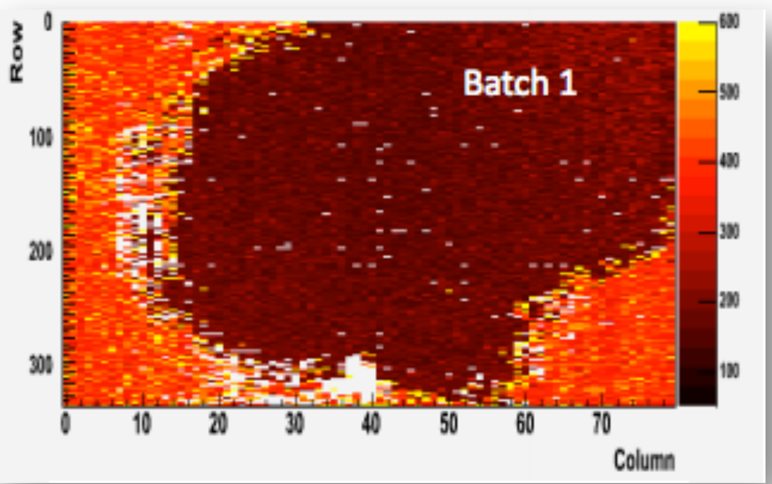




- ✓ For current detectors we have used bump-bonding techniques (ATLAS: *Selex/IZM*, CMS: *IZM/PSI/RTI*, ALICE: *VTT*).
- ✓ Challenges and cons for HL-LHC:
  - Smaller pixel size → Minimum pitch ~30 μm or alternate bump pads
  - Large surfaces → High cost (~100 CHF/cm^2) of chip-chip hybridization
  - Small material budget → Irreducible substrates thickness ~100 μm
- ✓ Still, Bump-Bonding is the most (only) qualified joining option of next trackers in Phase-2.

Bump-Bonding

Noise in a FEI4B module with several disconnected bumps



- ✓ In order to produce the sizeable surface needed for the simultaneous ATLAS and CMS upgrades, we must qualify several vendors.
  - The recent past experience in IBL is a lesson on how it might be a bottleneck otherwise.
- ✓ Besides the minimum pitch, the critical parameters for the bonding process are the larger size of the read out chip, together with the requirement of a much thinner chip.
- ✓ Possible origin of problems for the hybridization step are:
  - handling of such a thin and large chip
  - planarity with respect to the sensor during flip-chip
  - deformations coming from internal stress of the chip and/or working temperature during the bonding step
  - Otherwise a supporting wafer is needed (as in IBL at IZM).

Bump-Bonding@Selex

- The indium bump bonding technique is an appealing candidate for coping with these problems because it requires just one Under-Bump Metallization (UBM) step and a low (90°C) maximum working temperature.
- The process is intrinsically simple and offers a natural support for the chip during the high-temperature step of the bonding
- ✓ A step in this direction has been done with Selex to assemble ATLAS IBL FE-I4 chip:

	FEI3 (ATLAS)	FEI4 (ATLAS IBL)
Chip area (mm^2)	7x11	19x20
Chip thickness	180	100 (150 μm in IZM)
Bumps/chip	2880	26880
Pixel area (μm^2)	50x400	50x250

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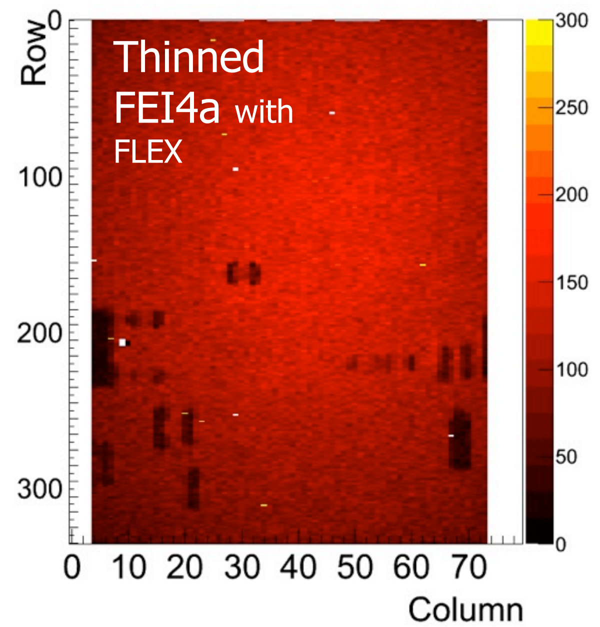
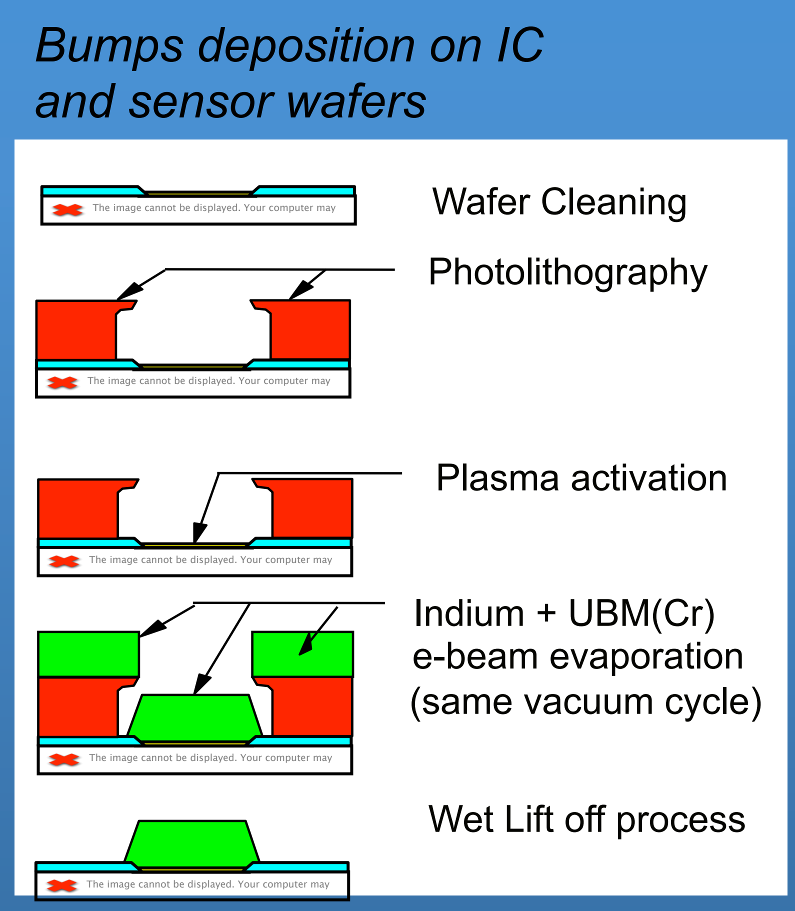
✓ A step in this direction has been done with Selex to assemble ATLAS IBL FE-I4 chip:

  - Selex indium bump bonding process can be used both with planar and 3D sensors and 100 μm thinned electronics, provided small changes in the procedures.

Development of Indium bump bonding for the ATLAS Insertable B-Layer (IBL)
G Alimonti *et al,* 2013 *JINST* **8** P01024



Bump-Bonding@Selex: next steps

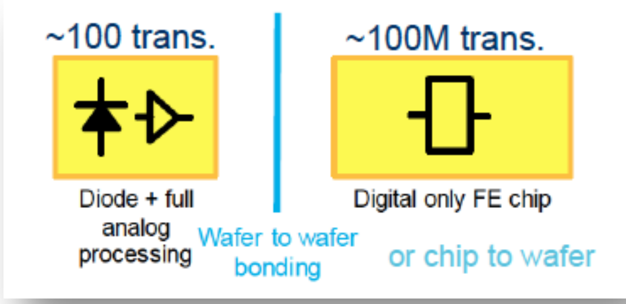


- ✓ Interest in R&D with Selex by ATLAS (Ge/Mi) and CMS (Fi/Pi).
- ✓ Next step in Selex is to verify the possibility to deposit taller indium bumps on one side only.
- ✓ It is an advantage in price and also allows to delay 6" upgrade (Selex can work on 4" as IBL sensor or 8" wafer as FEI4 electronics).
  - Moreover it could greatly simplify the technological process, avoiding the bump-deposition and protection during the working steps of the IC wafer.

Alternatives to Bump-Bonding

- ✓ Capacitive coupling between an "active" sensor and a read-out chip
  - Signal amplification allows capacitive contact. Contact pads must be aligned O(10um) and dieletric thickness O(5 um) controlled.
  - Aiming to "simple" process, ideally wafer to wafer bonding.

More in Usai's talk



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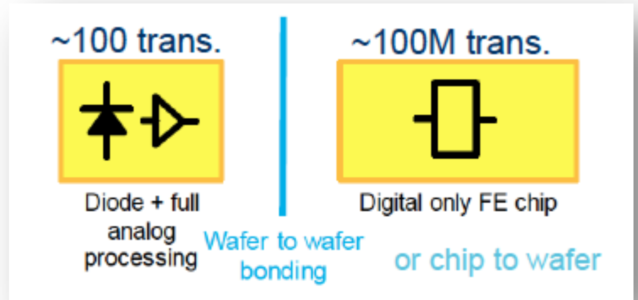


- ✓ Monolithic pixels
  - Possible to be used in Alice upgrade given the looser requirements on radiation hardness (700 krad) and readout speed (integration time ~30 μs).
  - Advantage for material budget (0.3% X_0 for the inner layers) and pixel dimension (O(20 μm x 20 μm)).

More in Usai's talk

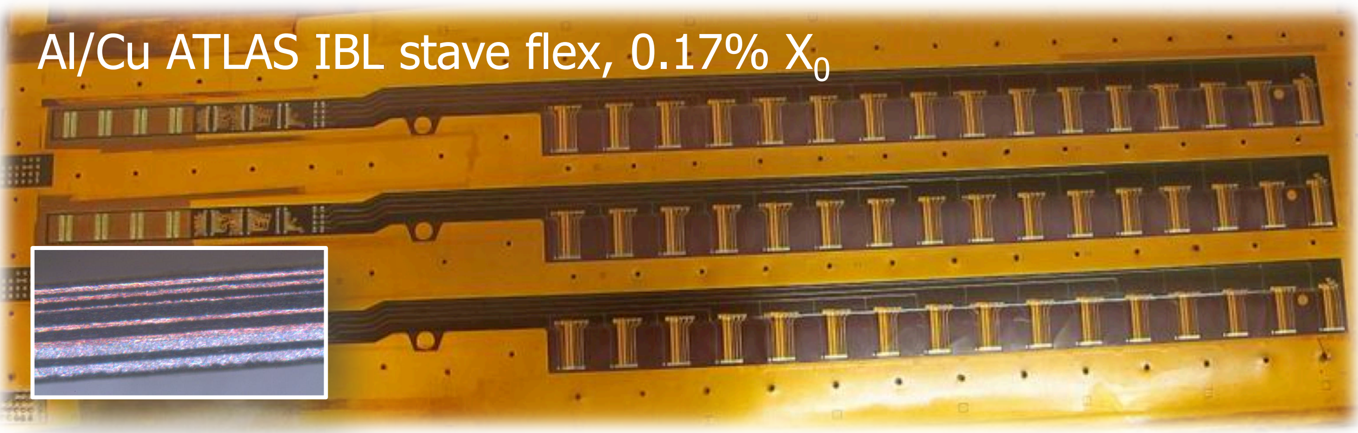
- 3D integration (see next)

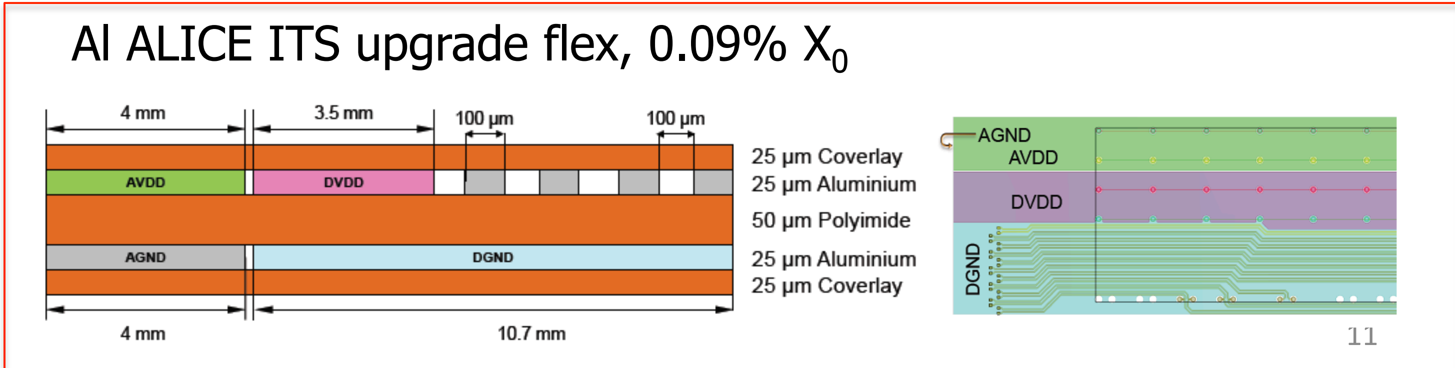
Front-End Readout to external world connection

- ✓ For current detectors we have used wire (CMS/ATLAS) and tab bondings (Alice) with flex hybrids.
- ✓ Challenges and cons for HL-LHC:
  - Reliability!
  - Reduce material budget.
- ✓ Italian Interests
  - Flex circuits
  - Interconnections

Flex circuits

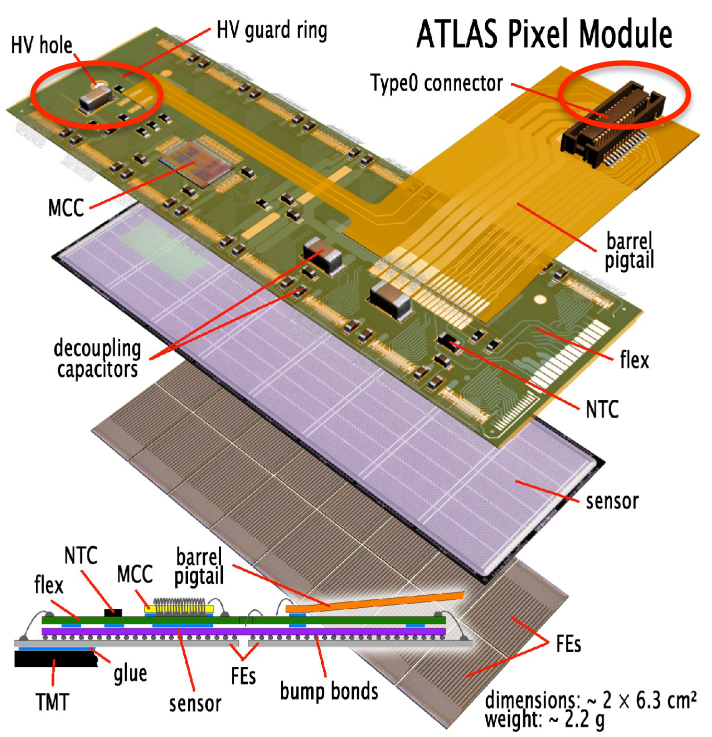
- ✓ Several Italian groups have experience and interest in low-material Flex circuits
  - ✓ Alice: *Torino, Bari*
  - ✓ ATLAS: *Genova, Milano (was SuperB)*





Wirebonding

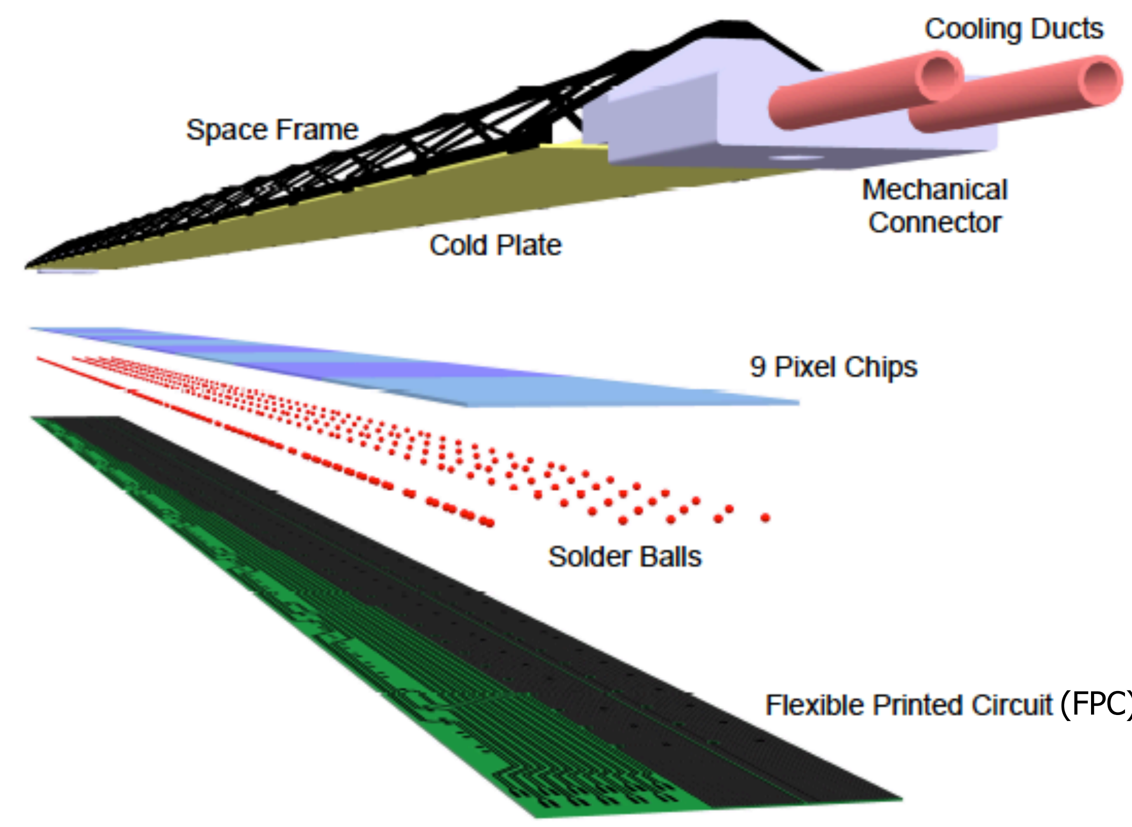
- Wire-bonding based on Al wedge bonding between read-out/sensor and services extensively used in current detectors.
  - Issues have been reliability (ATLAS HV) and recently corrosion (ATLAS IBL).
  - Use in B-fields is a design constraint. It Needs space for bonding pads.



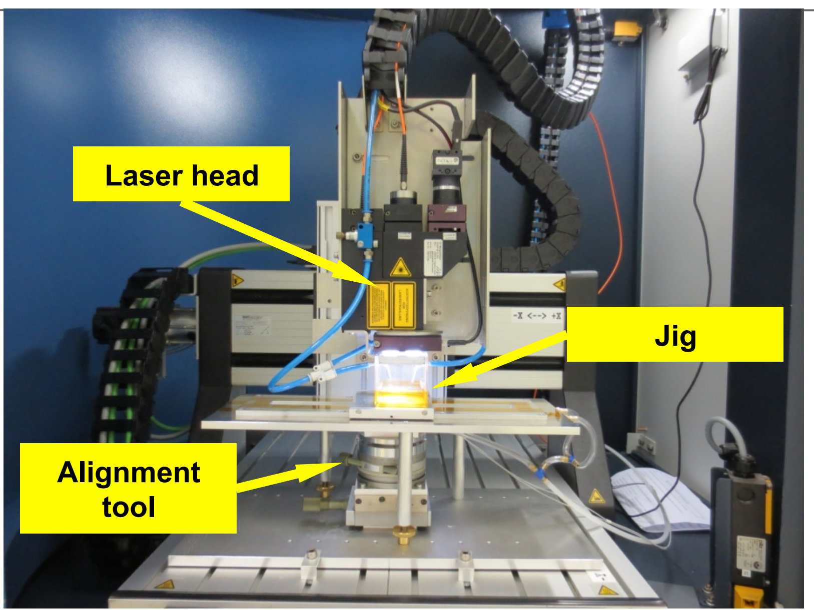
White residue (Al Hydroxide) on Al/Ni/Au interface. Devices went below dew point during thermal cycles.

Interconnections: Laser soldering

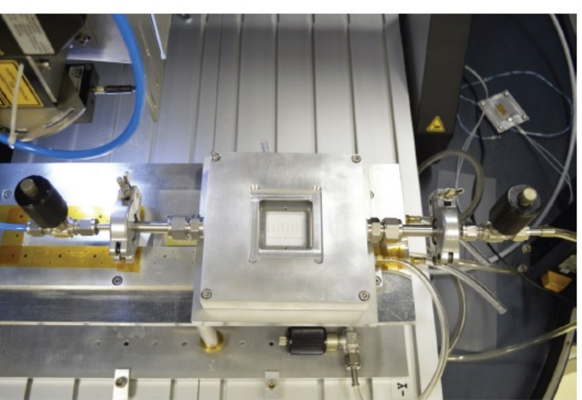
- In Alice ITS upgrade all connection pads are located on the chip top surface.
  - Baseline: SnAg balls are deposited for laser soldering connection with the flex. (Other solution: TAB bonding).



Interconnections: Laser soldering (Bari)

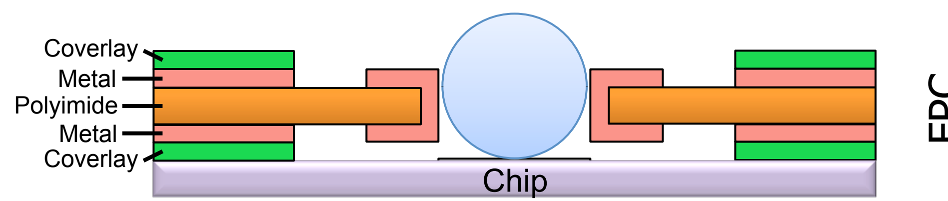


Vacuum system



Soldering Test done with :

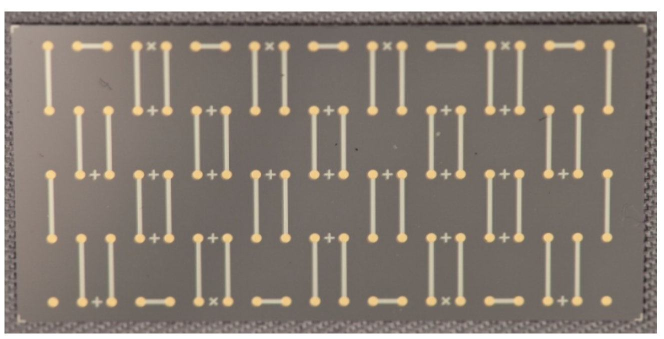
- Ni/Au metallized chip (next slide)
- Balls: 200 μm diameter (SnAg)
- Soldering under vacuum



Interconnections: Laser soldering *(Bari)*

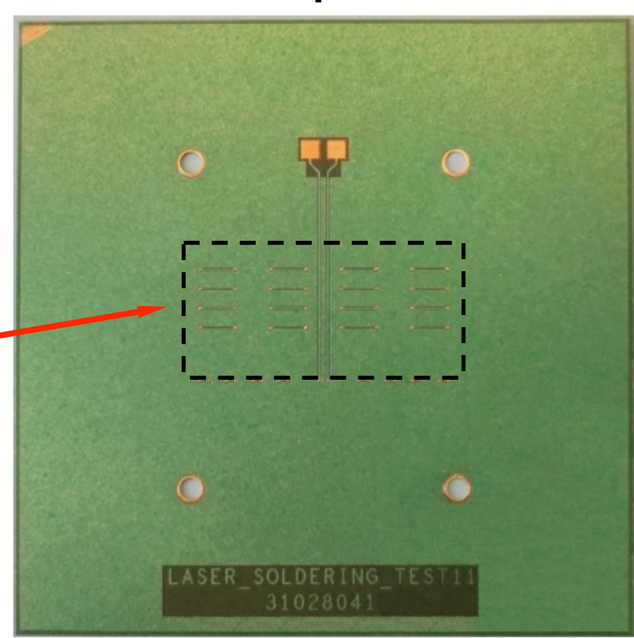
"PAD" CHIP

- 15 mm x 30 mm
- 50 µm thick
- Metal pads and traces on SiO_2/Si
- Ni/Au pads metallization
- Daisy chain connections



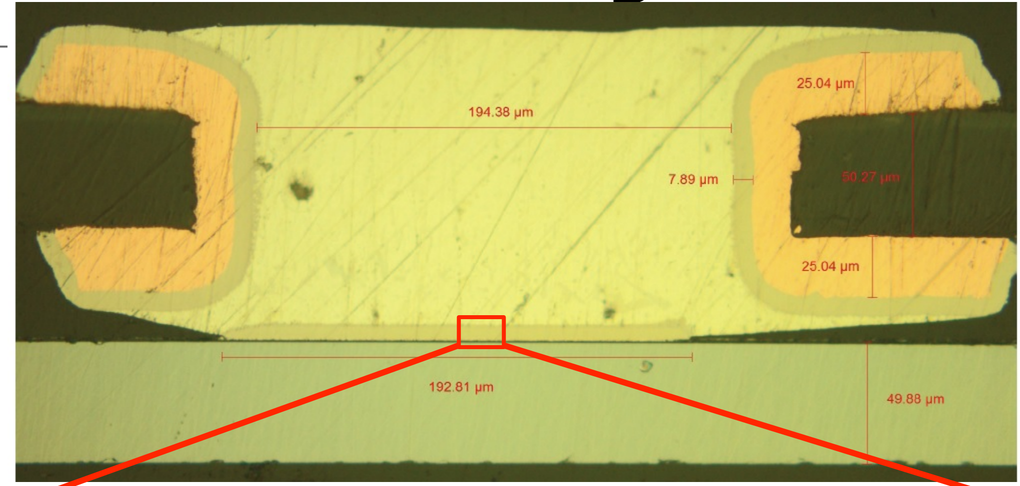
Chip on the back side

Single die connected to a sample FPC



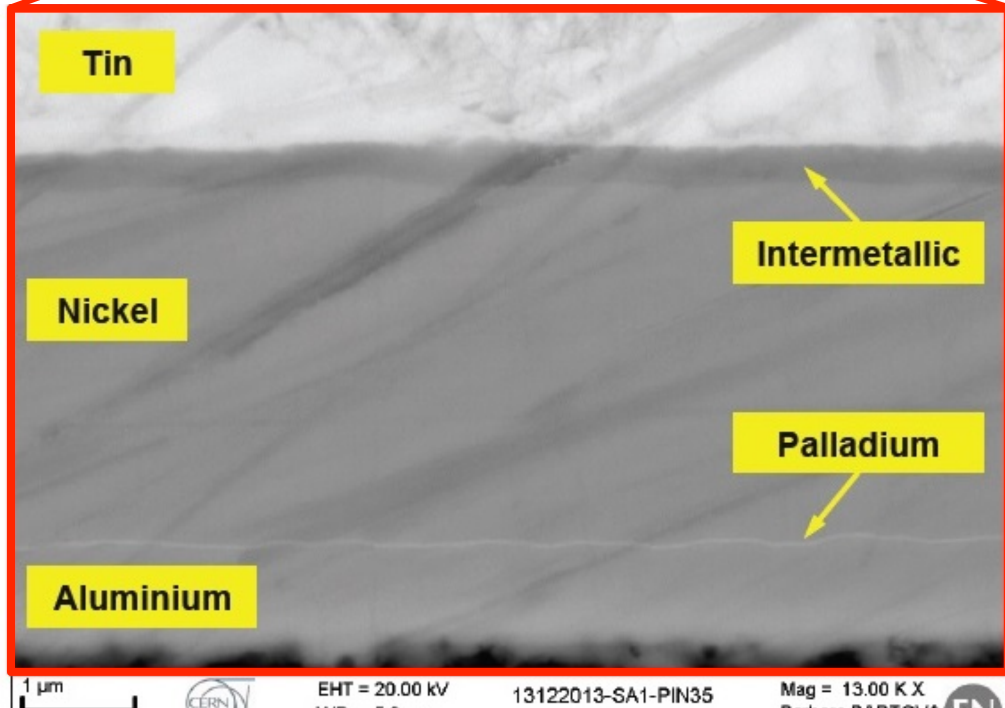
Soldering sphere view before and after laser soldering

Interconnections: Laser soldering *(Bari)*

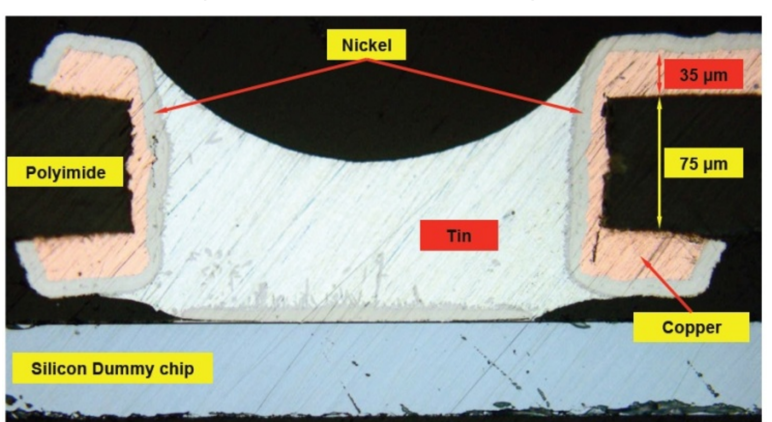


Extensive test to tune the laser profile and validate the procedure

- Electrical daisy-chain test of 50 contacts
- Microscope inspection
- Metallurgical cross-section analysis + SEM

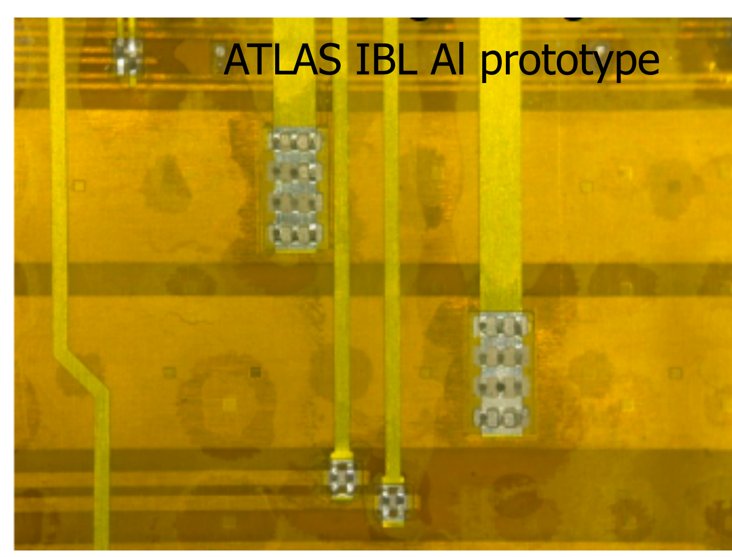


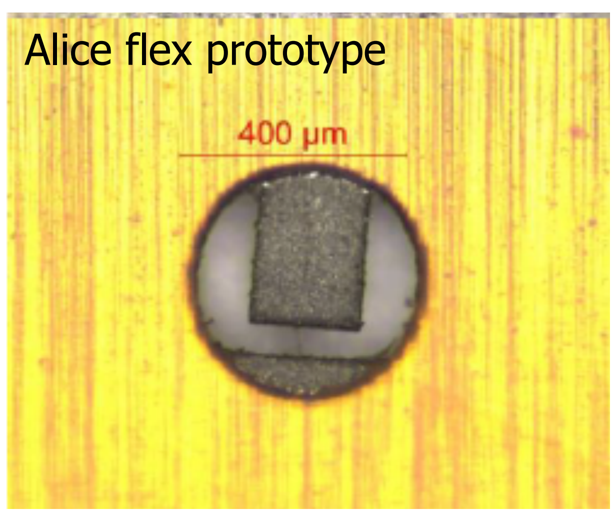
Optimization of the FPC hole geometry (diameter and depth)



Interconnection: TAB Bonding

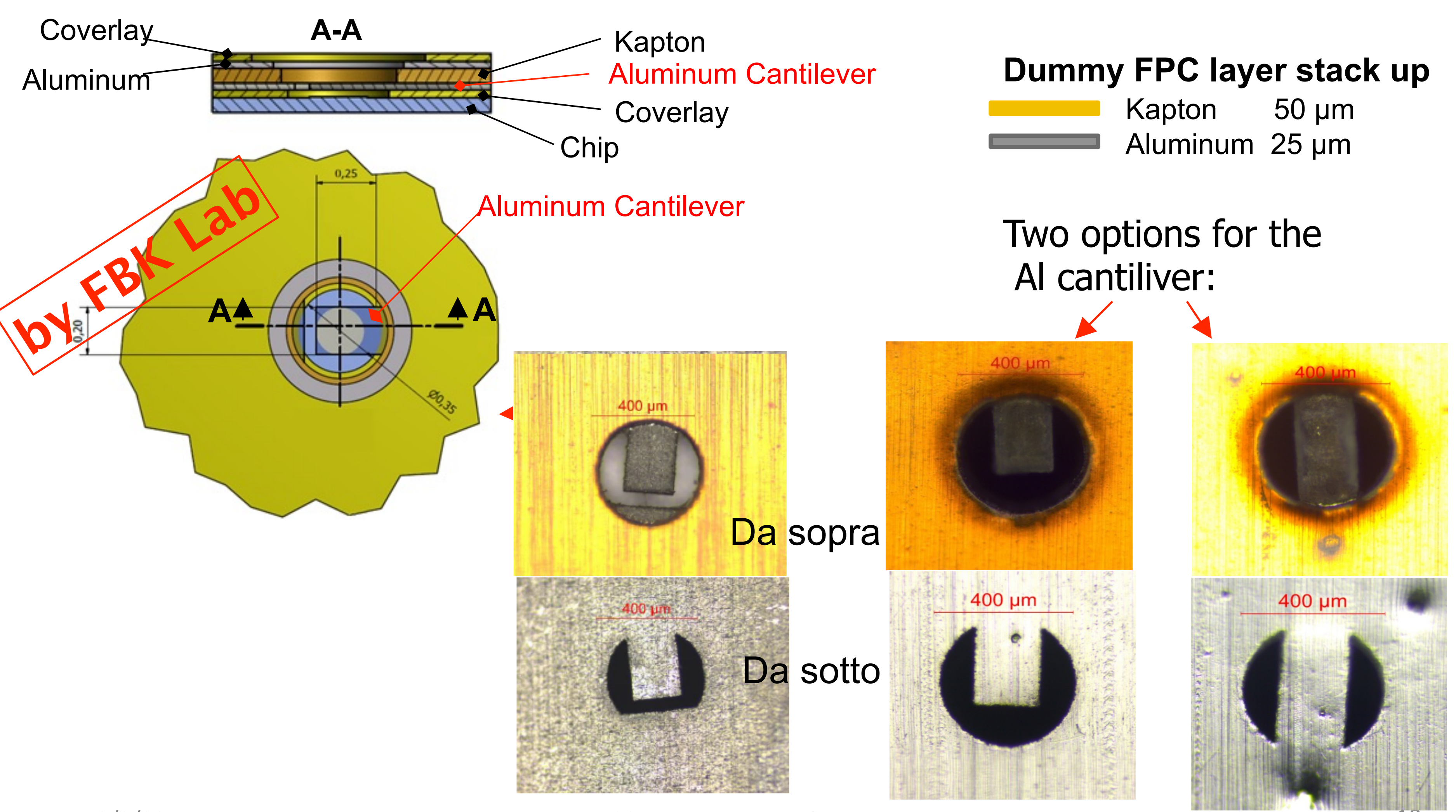
- ✓ Connection between the FPC and the Pixel Chips is the Single point Tape Automated Bonding (SpTAB) technique, which exploits an Aluminium ribbon leads ultrasonic assembly process.
- ✓ Used in Alice Si strip and Si Drift detector developped by Ukrainian team for Al-only flex hybrids. Difficult to upgrade to large scale.
  - Discarded for ATLAS IBL.
  - Possible solution for Alice tracker, in collaboration with FBK.





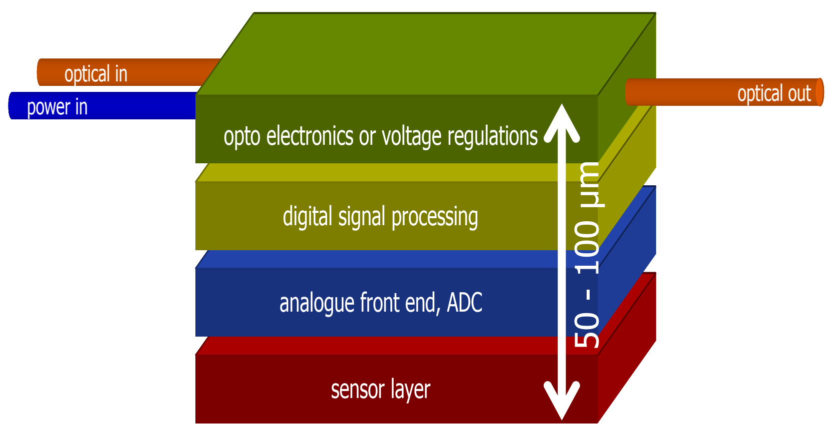
Interconnection: TAB Bonding (Bari)

✓ Collaboration with FBK/Micro Technologies Lab, Italy and Kirana

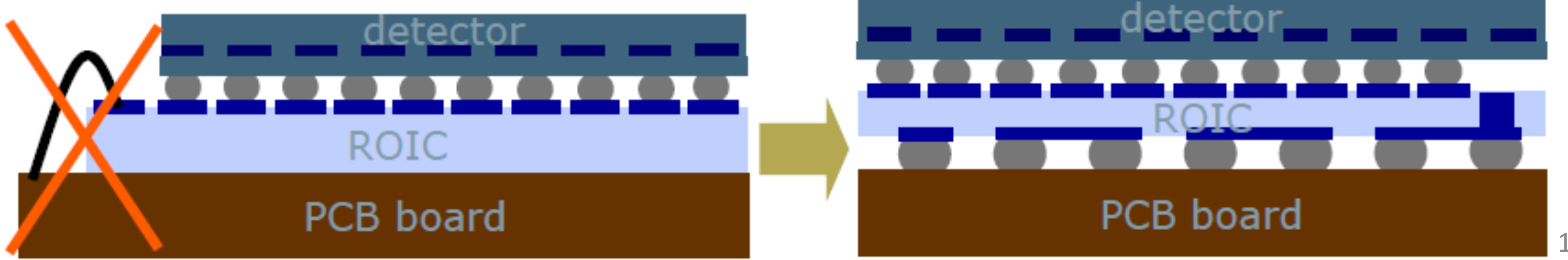


A step forward: 3D integration

- ✓ A 3D integrated circuit is a stack of thinned IC layers that are bonded together and have numerous electrical connections between them by means of small vias or pads.

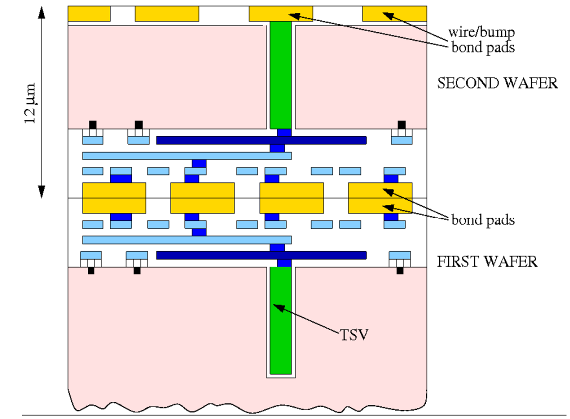


- ✓ 3D integration promises
  - Reduction of pixel size, presently limited by the need of complex electronic functions in the pixel cell and by limits in the bump bonding pitch,
  - Larger memory capacity in pixel readout cells or pixel regions,
  - Advanced pixel-level or region-level hit processing,
  - 4-side buttable tiles for a large area detector with minimum or no dead area.

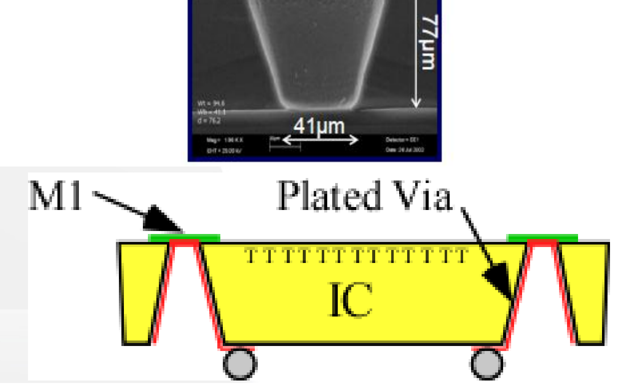


3D approaches: "via first" vs "via last"

- ✓ Different approaches to 3D integration differ in terms of the minimum allowed pitch of bonding pads between different layers and of vertical Through-Silicon Vias (TSVs) across the silicon substrate.

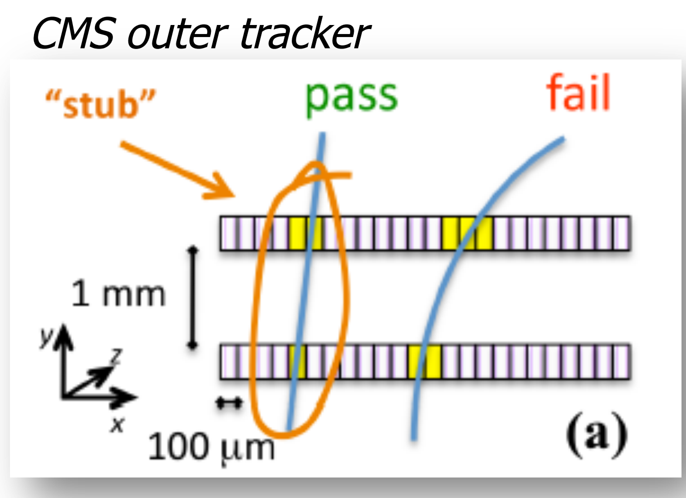


- ✓ Via first, Via middle: Vias are part of wafer processing at the CMOS foundry
  - High density TSVs (few µm pitch) through thinned wafers, allow multiple connections at the cell (pixel) level between transistor layers.
- ✓ Via last: Vias are fabricated on fully processed CMOS wafers, at a facility outside the CMOS foundry
  - Low density TSVs (tens of µm pitch) through unthinned wafers or partially thinned wafers, allow connectivity at the pad level in the chip periphery.



3D integration use in pixel-strip detector (CMS)

CMS outer tracker



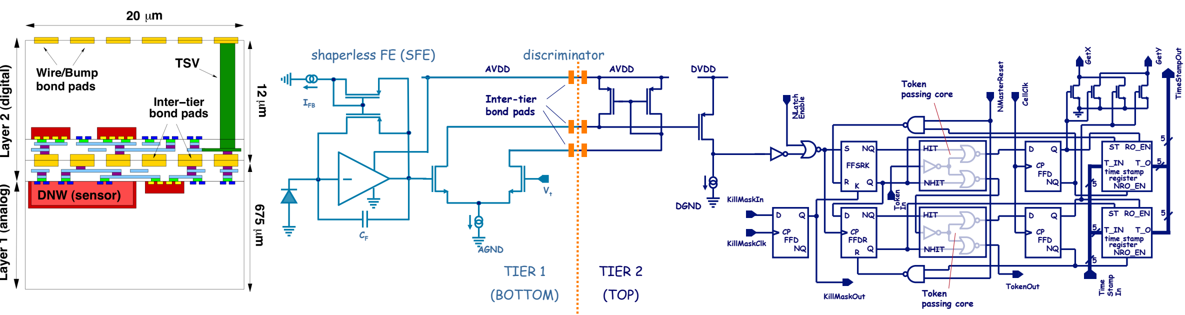
3D integration may provide information for Level-1 trigger processing, with local rejection of low-momentum particles, correlating signals in two closely-spaced sensors.

Through-Silicon Vias (TSVs) at the periphery of the pixel ASICs "bridging" two rows of chips in the middle, avoiding regions of stub finding inefficiency.

D. Abbaneo, A. Marchioro, **A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC,** JINST 7 C09001

INFN effort on 3D integration: the VIPIX project (Vertically Integrated PIXels) in CSN5

- ✓ 6 labs participating in this program (2009-2013): BG/PV, BO, PI, PG, RM3
- ✓ Development of pixel systems for thin charged particle trackers based on 3D vertical integration technologies
- ✓ To pursue its goals, VIPIX was proactive in establishing international collaborations that are investigating diverse approaches to 3D integration:
  - 3D-IC Consortium: "via middle", homogeneous 3D
    - INFN: fully functional prototypes of 2-tier 130 nm CMOS sensors (sensing and analog layer + digital layer)

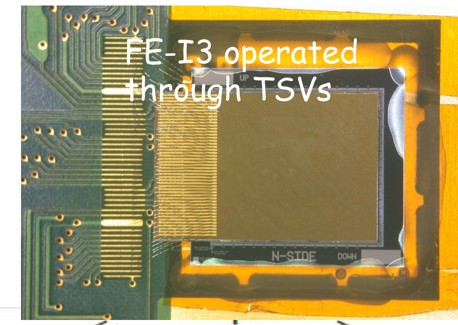


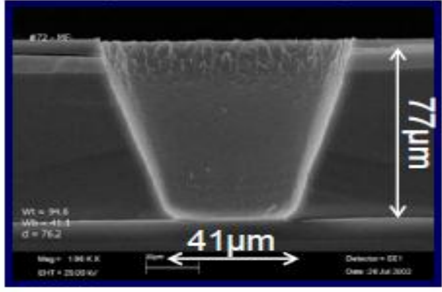
  - AIDA Workpackage 3: a network for the qualification of 3D interconnection technologies "via last", heterogeneous 3D
    - INFN: high-density interconnection (≈ 20 μm pitch) of a sensing layer (CMOS sensor) with a readout chip, in collaboration with IPHC-Strasbourg
  - … to be continued in H2020 in a new project "AIDA-2"

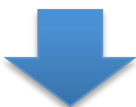
3D integration in AIDA WP3

- ✓ AIDA WP3 successfully tested "low-density" 3D flavors, based on the "via-last" vertical integration of heterogeneous layers: 50–100 μm density of interconnections and TSVs in the chip periphery to reduce dead areas.
  - FE-I3 (ATLAS pixel chip) and MEDIPIX3 (X-ray imaging) chips with 3D features are available.
  - FE-I4 chips with TSVs are expected by the end of 2014.
- ✓ Based on this success, there is now a strong interest for qualifying more aggressive 3D processes with finer pitch interconnections and TSVs (<50μm)

M. Barbero,T.Fritzsch, L. Gonella, F. Hügging et al., JINST 7 (2012) P08008







AIDA-2

- ✓ Qualify high-density interconnections to pixel sensors with < 50 μm pitch and TSVs in 65 nm CMOS chips so that these technologies can be used on a large scale with high yield and reasonable cost.

Italian interests and possible synergies

- ✓ Bump- Bonding:
  - Important experience for all the experiments in the past. Interest in R&D with Selex for CMS (Fi/Pi) and ATLAS (Mi/Ge).
- ✓ 3D integration:
  - Bergamo, Pavia, Pisa, Perugia
- ✓ Others (capacitance coupling)

  Genova for HV-CMOS
- ✓ Flex
  - Experience for ATLAS IBL (Ge), SuperB (Mi), Alice (Ba/To) on light flex
- ✓ Laser Soldering/Tab bonding:
  - Alice (Bari) is interested on laser soldering and TAB bonding.

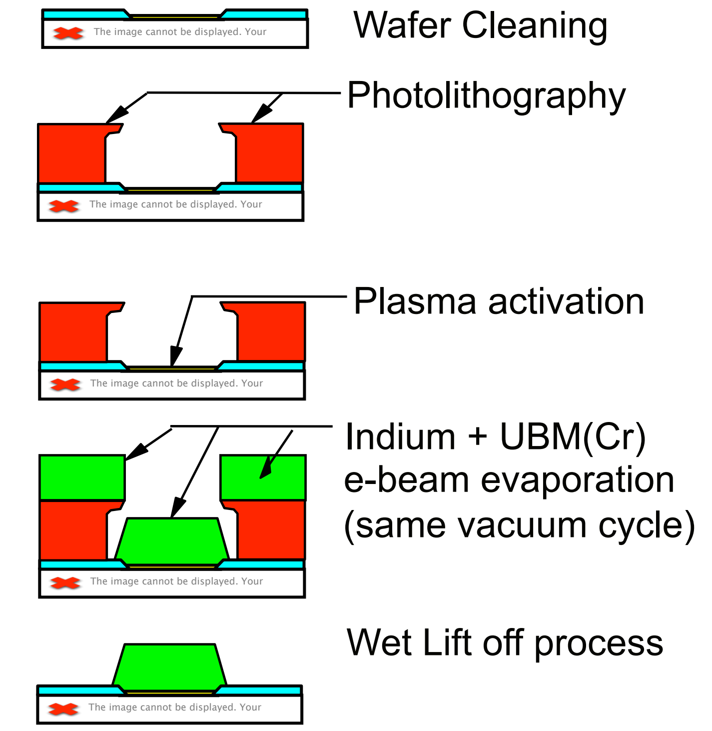
Technical

The indium bump-bonding technique is a two-step process: the bumps deposition on both the silicon sensor and the IC wafers and the flip-chip assembly.

In the first process the indium bumps evaporated through a polyimide mask are about 9 μm tall with a defect rate, measured by optical inspection, on the order of 10^{-5}.
The UBM process is very simple: after plasma activation, about 10 nm of chromium are deposited just before indium is evaporated in the same vacuum cycle, with the temperature never exceeding 50°C.

Process parameters:

- **Resist Thickness: 15 μm**
- **100 Å Cr UBM**
- **Deposition rate: 0.5 μm/min**
- **Dep. Pressure: 9 x 10 $^{-7}$ Torr**
- **T during Dep.: < 50 °C**
- **Final Bump Thickness: 9 ± 0.2μm**

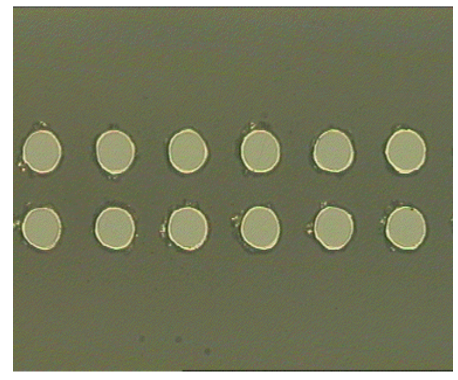


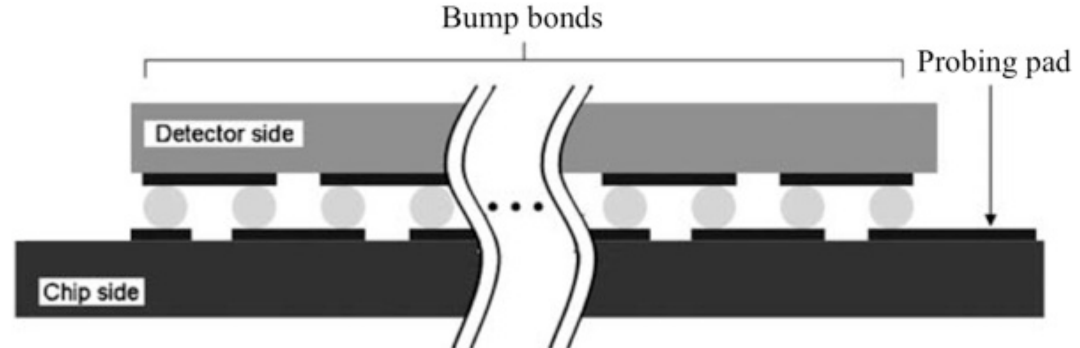
A cycle with controlled temperature and pressure allows the bumps to establish the electrical and mechanical connections. The resulting bump has an height of about 12 μm and a diameter of about 20 μm.

A custom pick-up tool for the bonding machine has been designed to match the larger size of the new modules.

The tuning of the process parameters has been performed using both glass substrates, having the same size of the dies, in order to better investigate the effects on bumps by simple inspection under optical microscope, and dummy chips. Glass substrates are also used to periodically check the flip-chip planarity and the alignment of the mating parts, monitoring the uniformity of the front-end corner bumps, which are the most sensitive to the machine settings.

For reference Only





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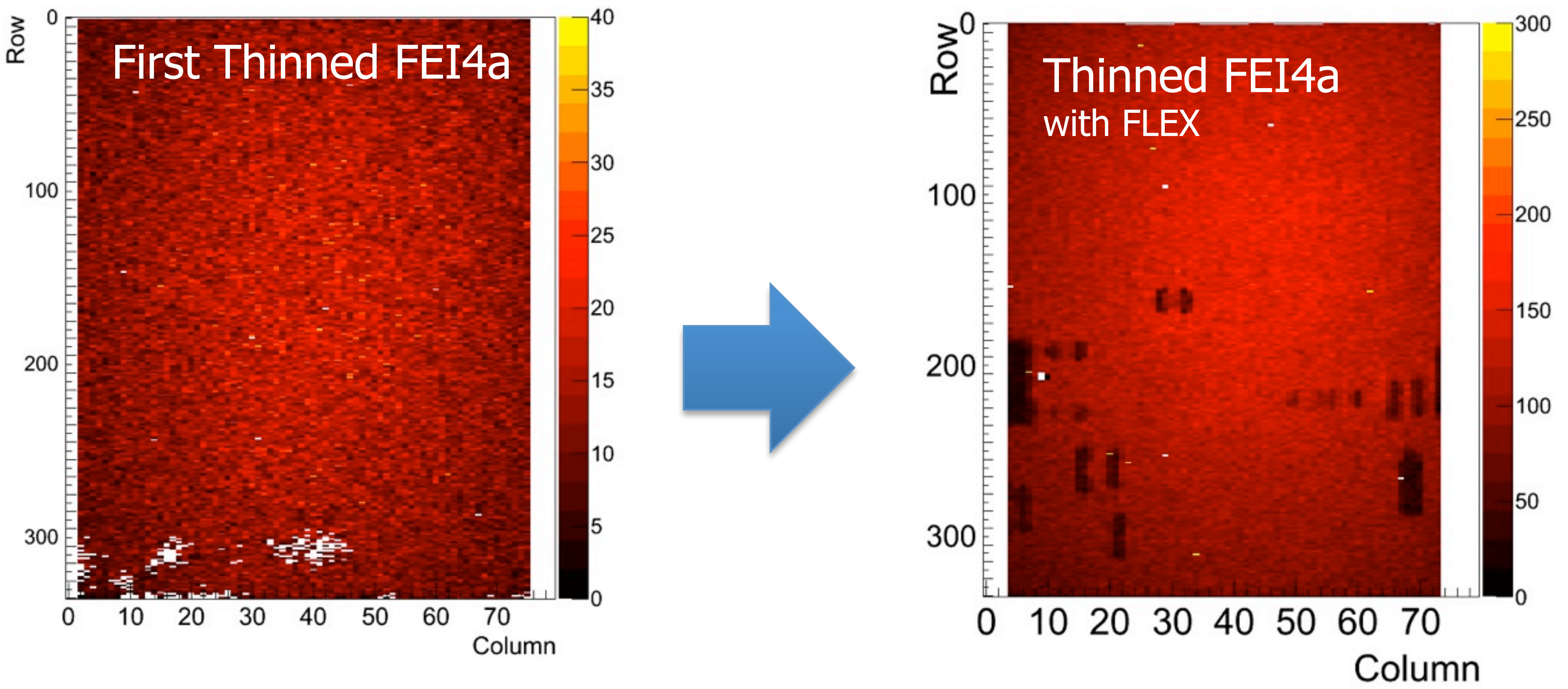


- ✓ Selex indium bump bonding process can be used both with planar and 3D sensors and 100 μm thinned electronics, provided
  - A stress relief process is applied after thinning to reduce the deformation of the 100 μm chips observed before bonding.
  - the flip-chip step is slightly modified allowing the working temperature to go below 50°C before releasing the pressure.

Alternatives to BB → Semi-monolithic

✓ Coupling between an "active" sensor and a read-out chip

- Signal amplification allows capacitive contact
- Aiming to "simple" process, ideally wafer to wafer bonding

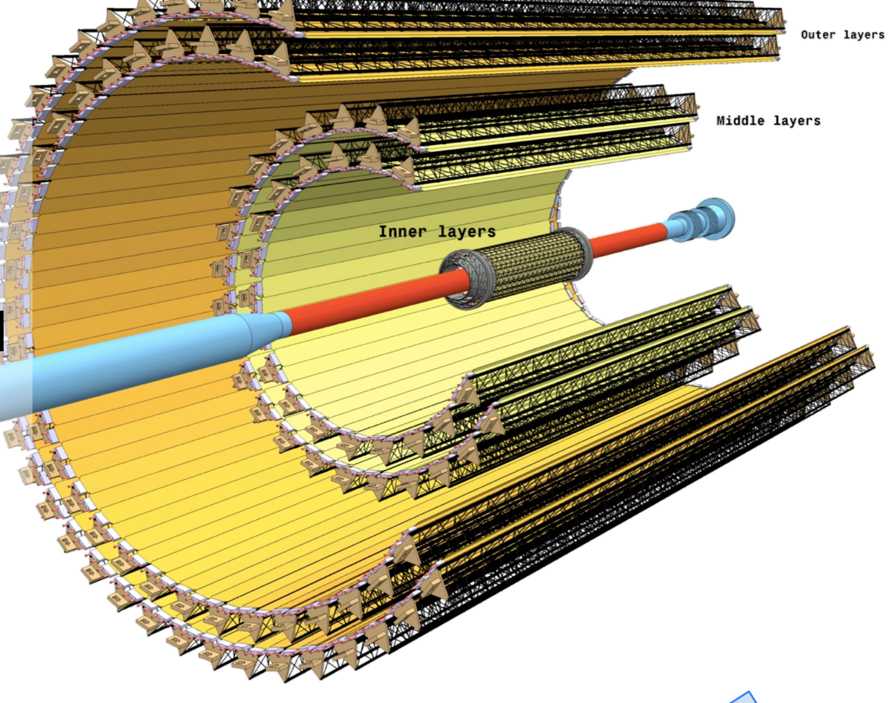
More in Usai's talk

- HYBRID pixels using "smart" sensors
  - 8" **HV** or **HR** sensor w/ few transistors
  - (voltage) signal cap. coupled to R/O-chip
  - eg. CCPD to FE-I4
- DEPFET pixels (one in-pixel transistor)

- depleted CMOS ACTIVE Sensors + digital R/O chip
  - **HR** or **HV** CMOS sensor with CSA+disc
  - dedicated digital R/O chip
  - CCPD -> DMAPS -> goal wafer to wafer

Alternatives to BB → Monolithic (Alice)

- ✓ Improve impact parameter resolution by a factor ~3 (r-ϕ):
  - Get closer to IP (39 mm) → 21 mm
  - Reduce material budget (1.14% X_0) → 0.3% X_0 (inner layers)
  - Reduce Pixel size (50 μm x 425 μm) → O(20 μm x 20 μm)
- ✓ High standalone tracking efficiency and p_T resolution
  - Increase granularity and radial extension → 7 pixel layers
- ✓ Faster readout
  - Readout of Pb-Pb interactions at >50 kHz and pp interactions at several 10^5 Hz (now limited to 1 kHz with full ITS, and ~ 3kHz without silicon drift).



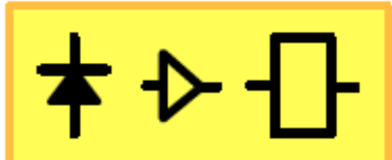
More in Usai's talk

Alternatives to BB → Monolithic (Alice)

More in Usai's talk

- Very thin sensors
- Very high granularity
- Large area to cover
- Modest radiation levels

Monolithic silicon pixel detectors



Diode + Amp + Digital

Parameter	Inner barrel	Outer barrel
Max. silicon thickness	50 µm	
Intrinsic spatial resolution	5 µm	30 µm
Chip size	15 mm × 30 mm ($r\phi \times z$)	
Max. dead area on chip	2 mm ($r\phi$), 25 µm (z)	
Max. power density	300 mW/cm^2	100 mW/cm^2
Max. integration time	30 µs	
Max. dead time	10 % at 50 kHz Pb–Pb	
Min. detection efficiency	99 %	
Max. fake hit rate	10^{-5}	
TID radiation hardness[a]	700 krad	10 krad
NIEL radiation hardness[a]	10^{13} 1 MeV n_{eq}/cm^2	3×10^{10} 1 MeV n_{eq}/cm^2

[a] This includes a safety factor of ten

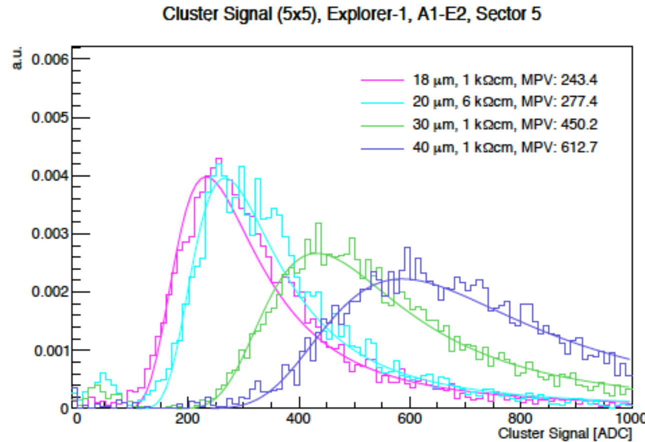
Electrode

Pwell Nwell Pwell Nwell

Deep Pwell

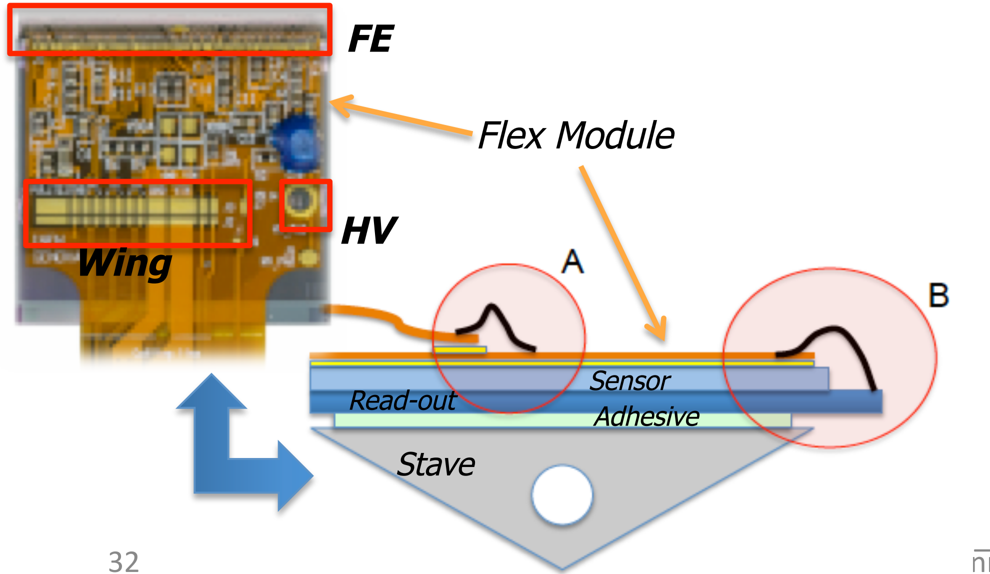
P-epitaxial layer

P-substrate



Corrosion observed!

- ✓ In September we were close to the **production completion**:
  - 12 staves built out of 14 needed and 90% of modules delivered by IZM.
- ✓ Triggered by **an accident at CERN** in early September (staves #7&8 got frozen), we have observed clear signs of **corrosions** on wire bondings in the wing area (A) and on FE bondings (B) on almost all assembled staves.
  - Only Stave #11, which had not been exposed to thermal cycling in Geneva or in SR1 looked more or less the same as when it was assembled.

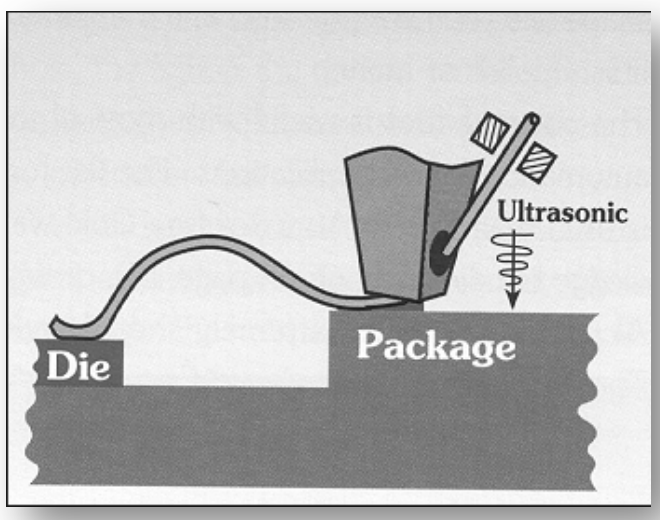


Typical corrosion region on FE-bonds at Module Flex end of bond wires.

White residue is Aluminum Hydroxide

Corrosion investigation in IBL

- Essentially all wire-bonding in any Silicon tracker is based on Al wedge bonding.
- No metallurgy issues for bonding Al wire to the Al pads on modern ASICs. However, there are issues for the Al/Au bonding on the Flex side, as Au (rather electro-positive) and Al (very electro-negative) in an electrolyte form a galvanic couple.

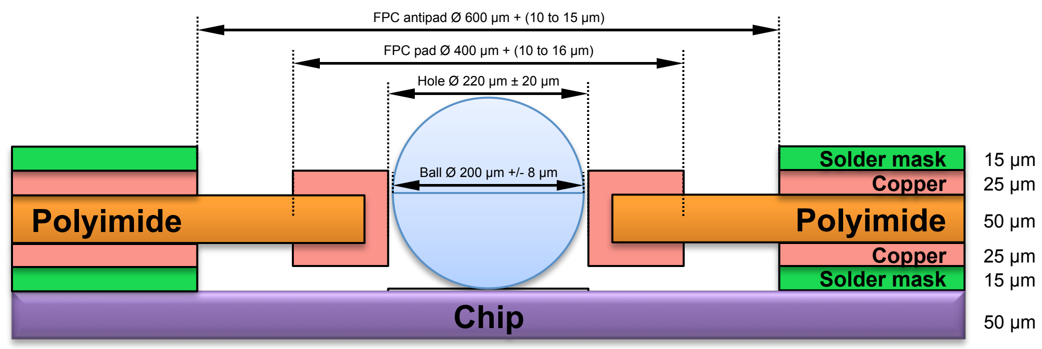


- Al is normally protected by an oxide layer. However, this layer can be damaged in water, or due to mechanical or chemical attack (for Al, halogens are the worst combinations).

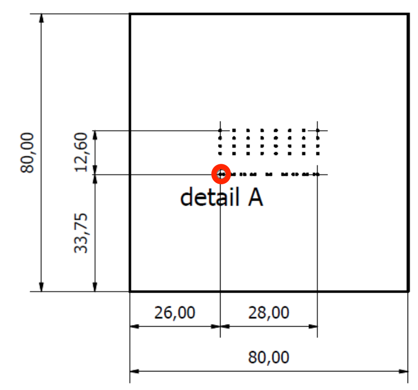
- In IBL, corrosion observed in Al/Au but also on the ASICs side.
- Months of investigations and huge amount of tests has driven some conclusions for IBL case.

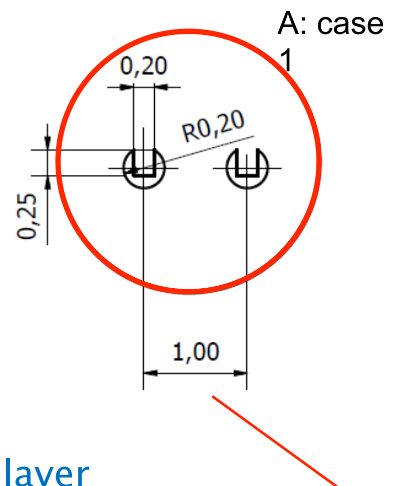
IBL Status – CSN1

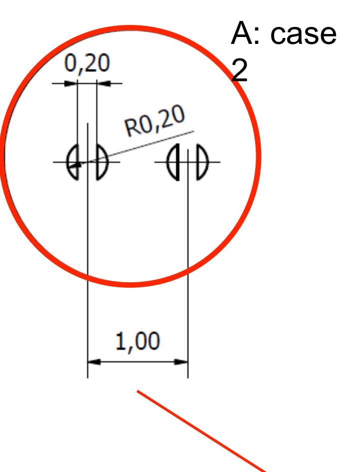
Alice



Interconnection: TAB Bonding





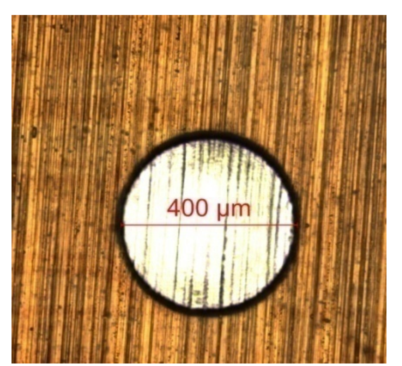


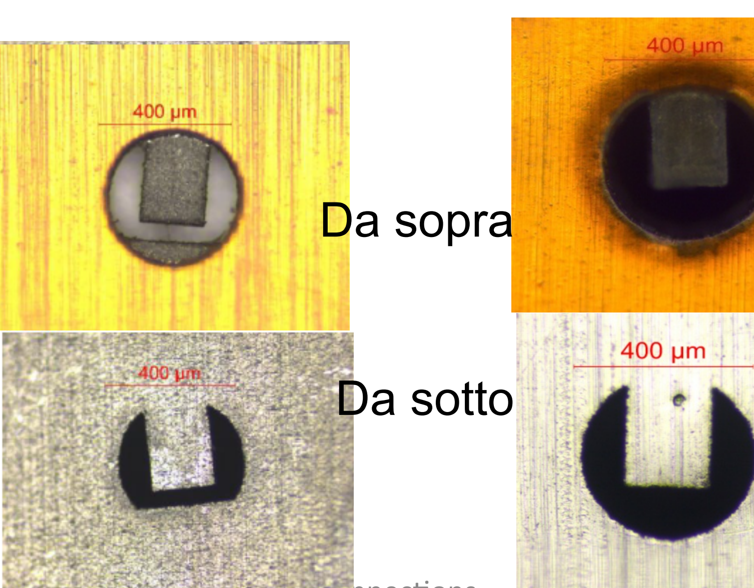
Laser tuned to remove Kapton up to the Al layer

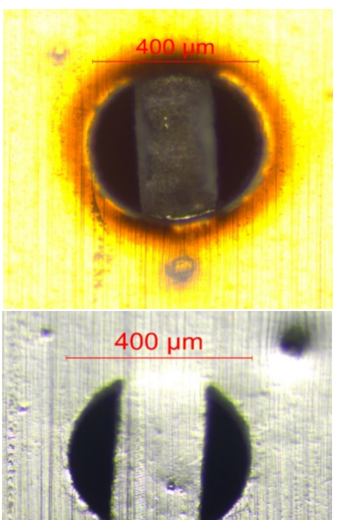
Dummy FPC layer stack up

Kapton 50 µm

Aluminum 25 µm

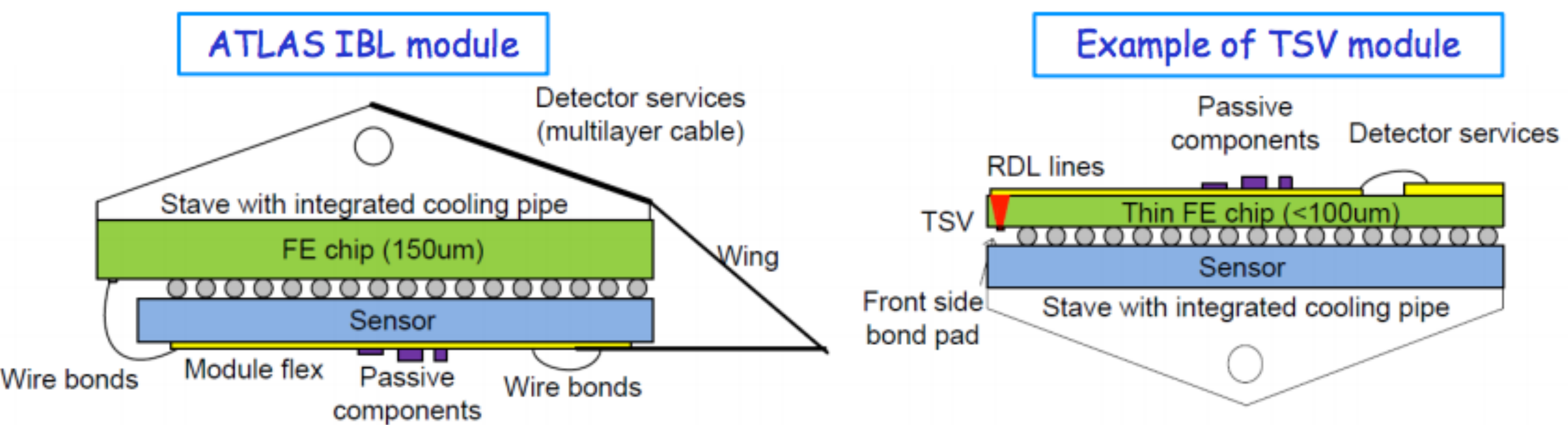




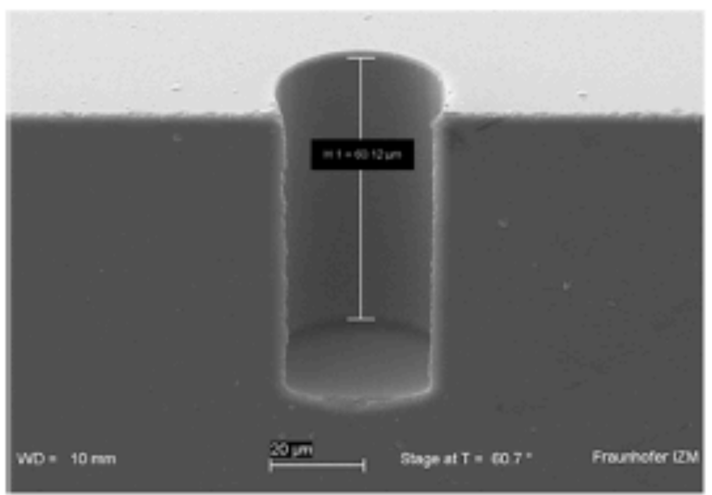


TSV

- ✓ Through-Silicon Vias (TSVs) across the silicon substrate is a valuable alternative for connections between layers.



- ✓ Via last: Vias are fabricated on fully processed CMOS wafers, at a facility outside the CMOS foundry.
  - Low density TSVs (tens of mm pitch) through unthinned wafers or partially thinned wafers, allow connectivity at the pad level in the chip periphery



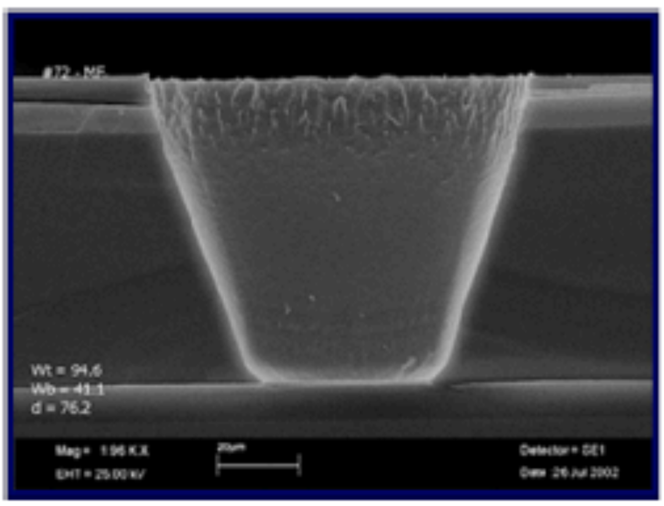
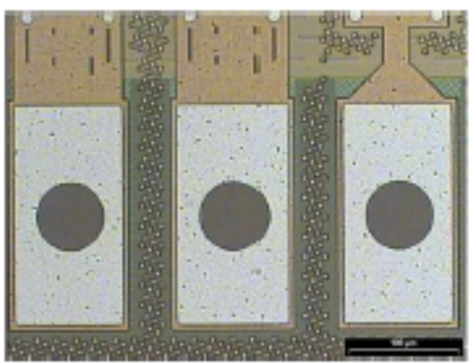
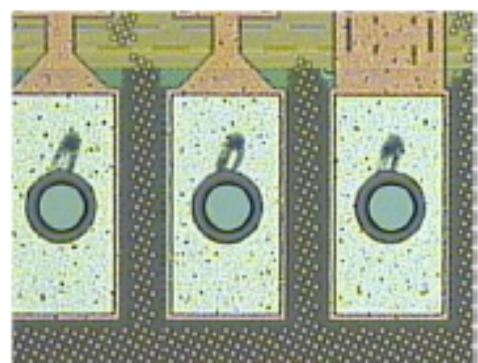


Figure 2. Example of straight (left) and tapered (right) side wall TSVs on a monitor wafer. The straight profile TSV has a depth of approximately 60 μm and an opening of 30 μm. For the tapered TSV, bottom and top via diameters are respectively of 41 and 95 μm, the side wall angle is 70°, and the wafer thickness is 77 μm.





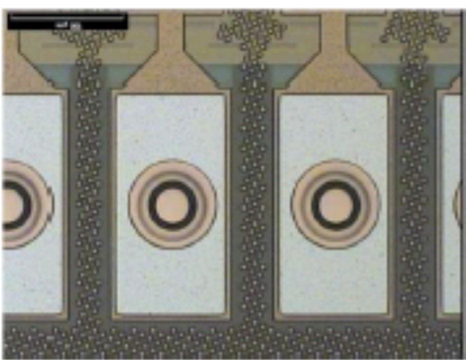


Figure 3. Front side processing on the ATLAS FE-I3 wafers. From left to right: Al pad opening, BEOL SiO_2 etch, plug formation.