Planar Pixel Silicon Detectors

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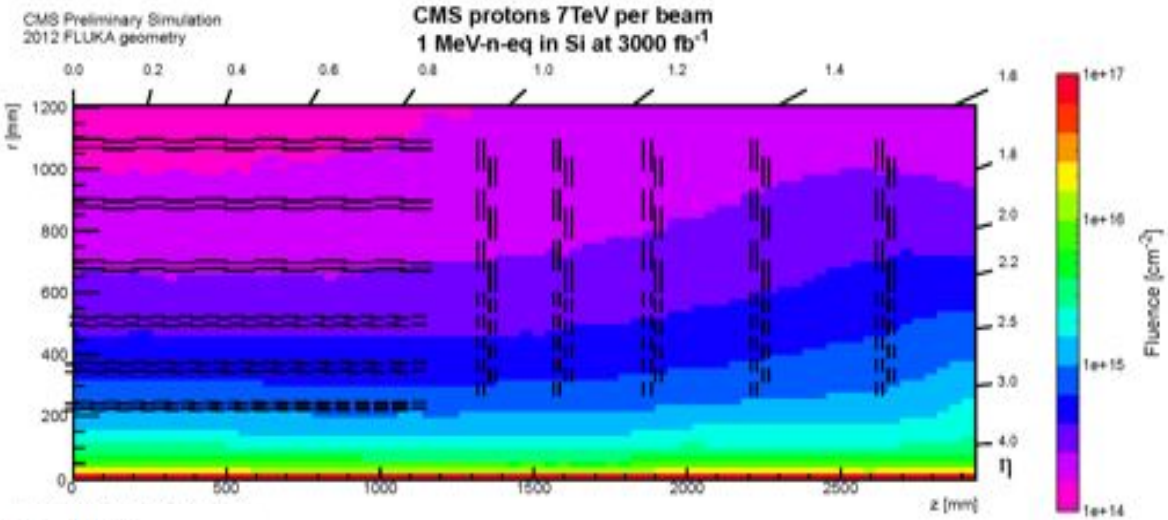
Outline

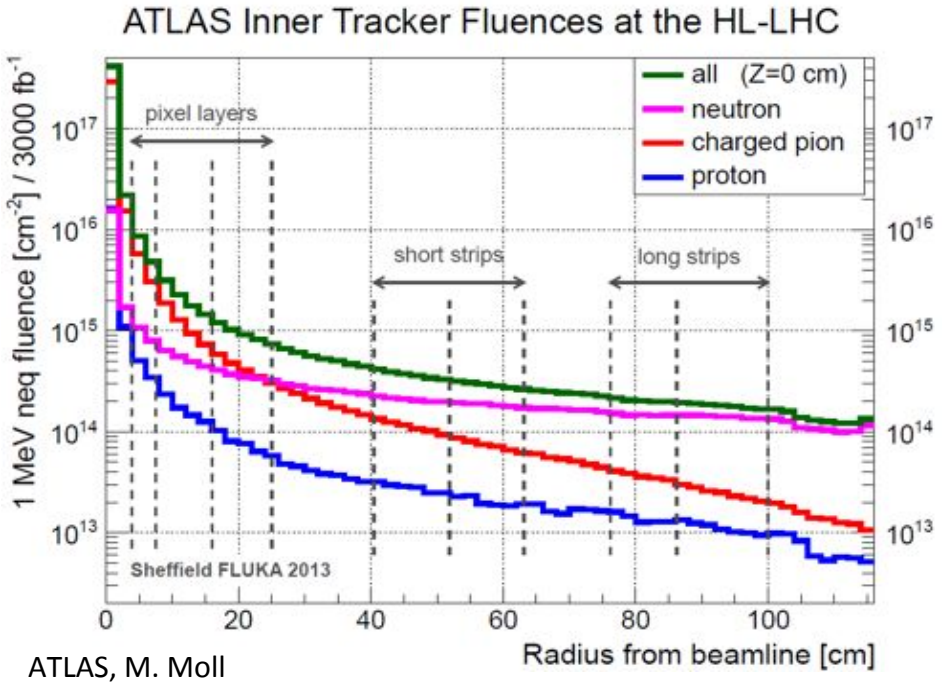
- Introduction:
  - Radiation environment and trackers evolution towards Phase-2 in ATLAS & CMS
- R&D indications from experiments
- Results Overview and present status
- Critical points to be studied
- INFN R&D program
- Conclusions

HL-LHC Fluence for Tracker Detectors

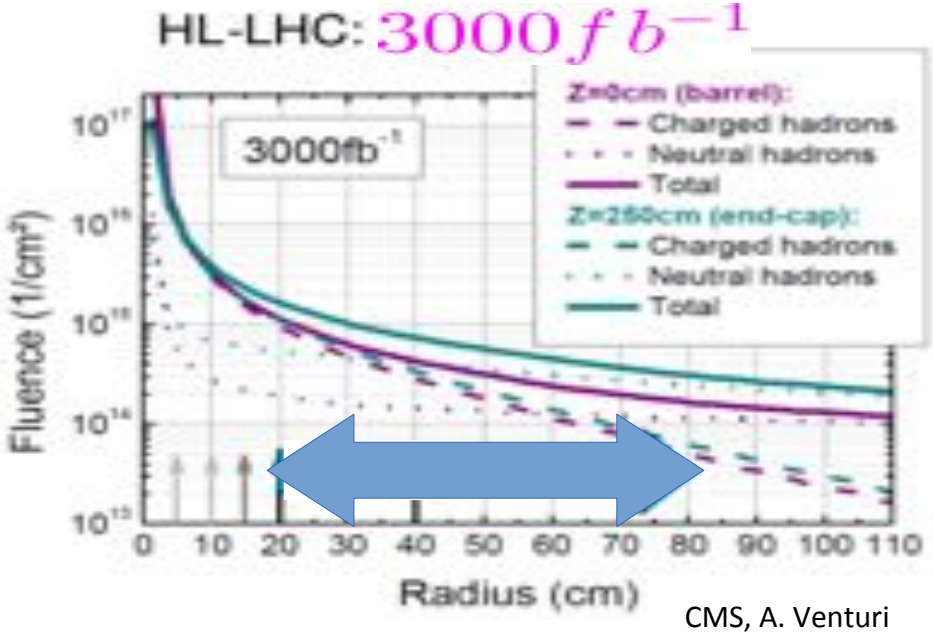
Phase-2 Trackers for both ATLAS and CMS will have to reach Integrated Luminosities of 3000 fb^{-1} with fluences of about $2x10^{16}$ 1 MeV neq/cm^2 in the inner layers

Same problems, join R&D efforts





ATLAS, M. Moll



CMS, A. Venturi

Pixel Detector Challenge

Pile-Up 140-200 events/bunch crossing

Extremely radiation resistant

Enhance Pt resolution

Pt Trigger capabilities

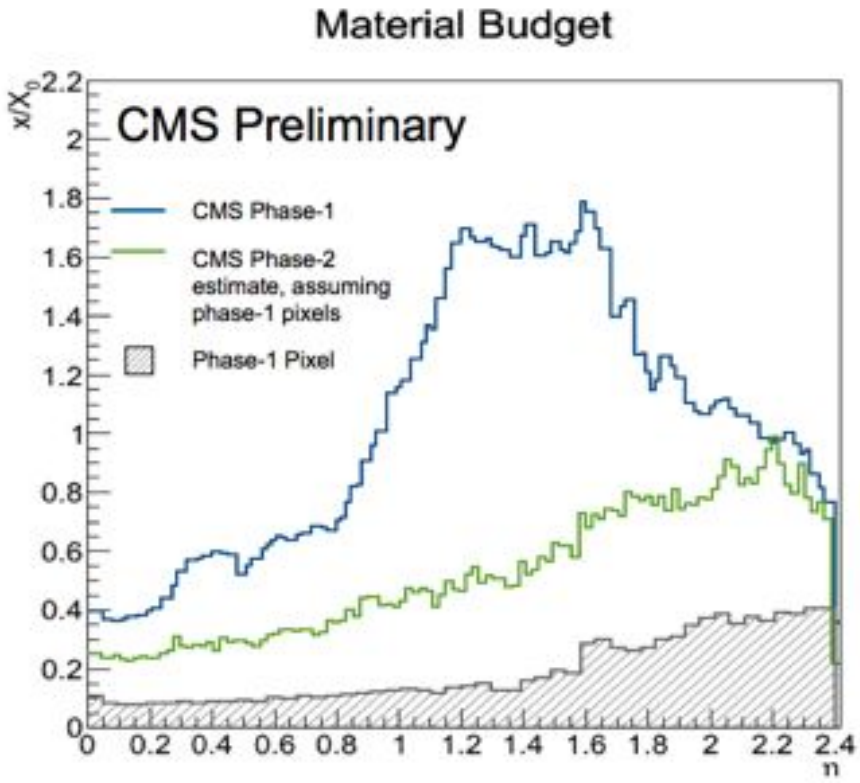
Low material budget

Occupancy below 1%

Higher Granularity, Vertex Identification, Pile-up mitigation

High efficiency, minimize inactive area

New pixel readout chip (see previous talk, RD53)

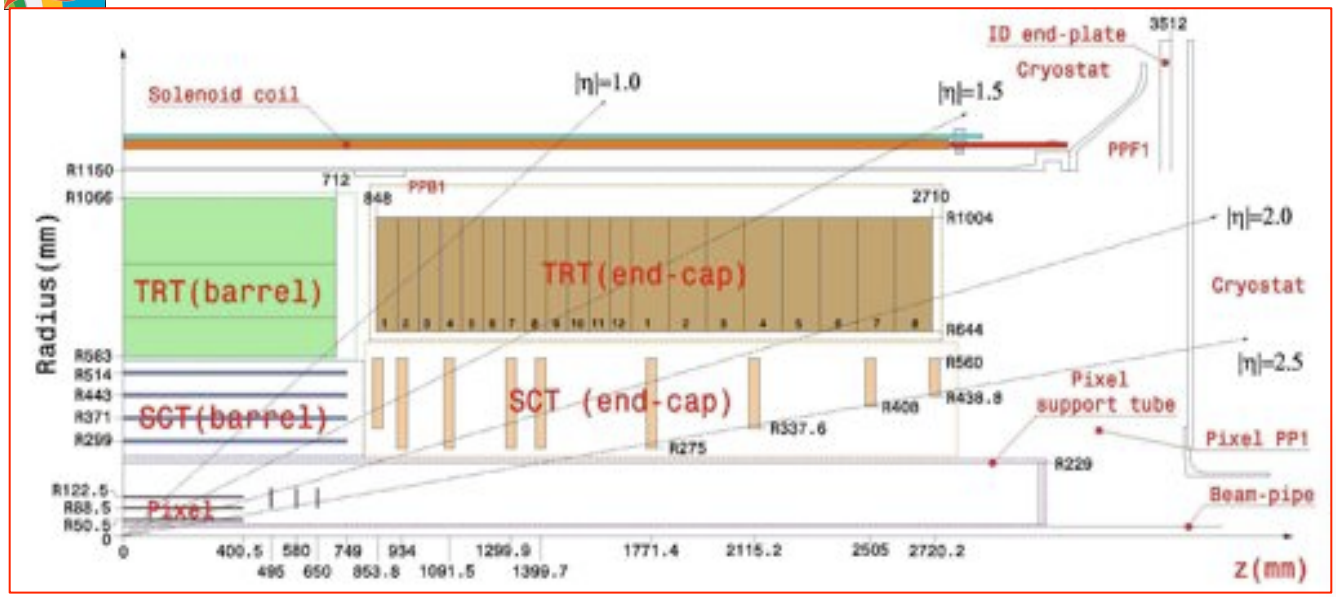


… and last but not least: cost/channel must go down!

Once more planar pixel are very likely to be the majority of pixel detectors even in the future HL-LHC trackers

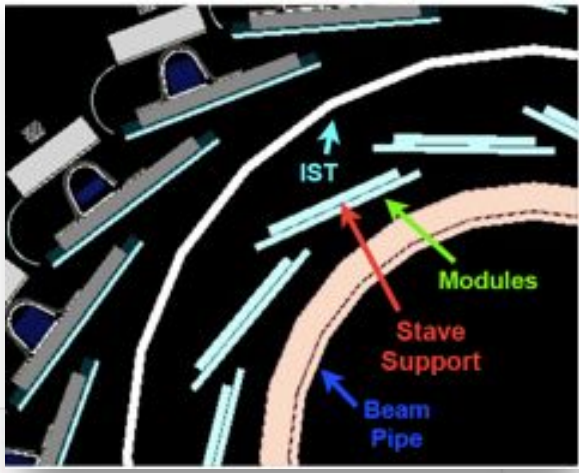
Cost is a driving issue: to be solved

From Current to IBL Tracker: ATLAS

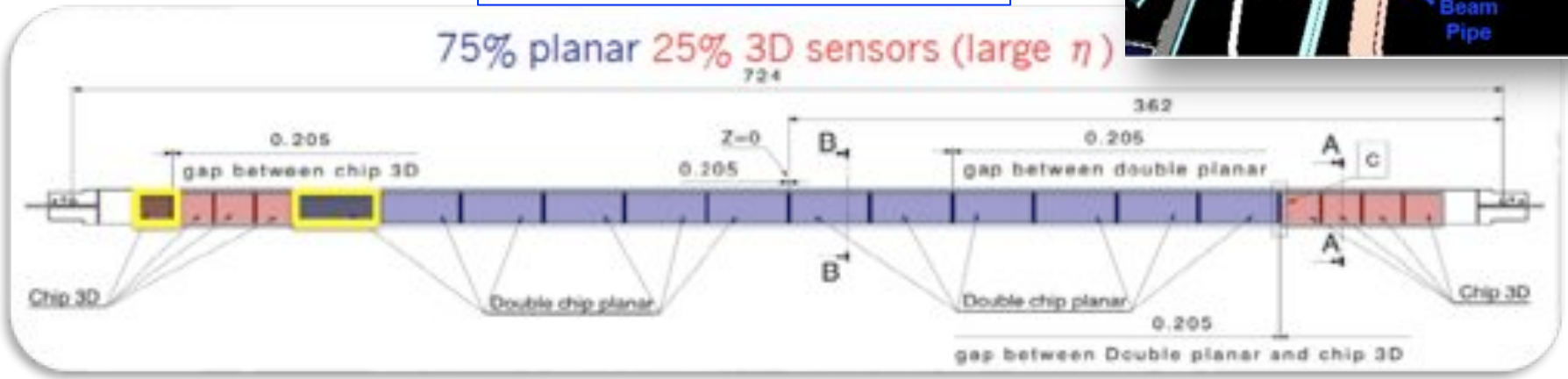


ATLAS Current Tracker

A New 4th pixel silicon barrel layer with r = 3.3 cm, 12 Million Pixel

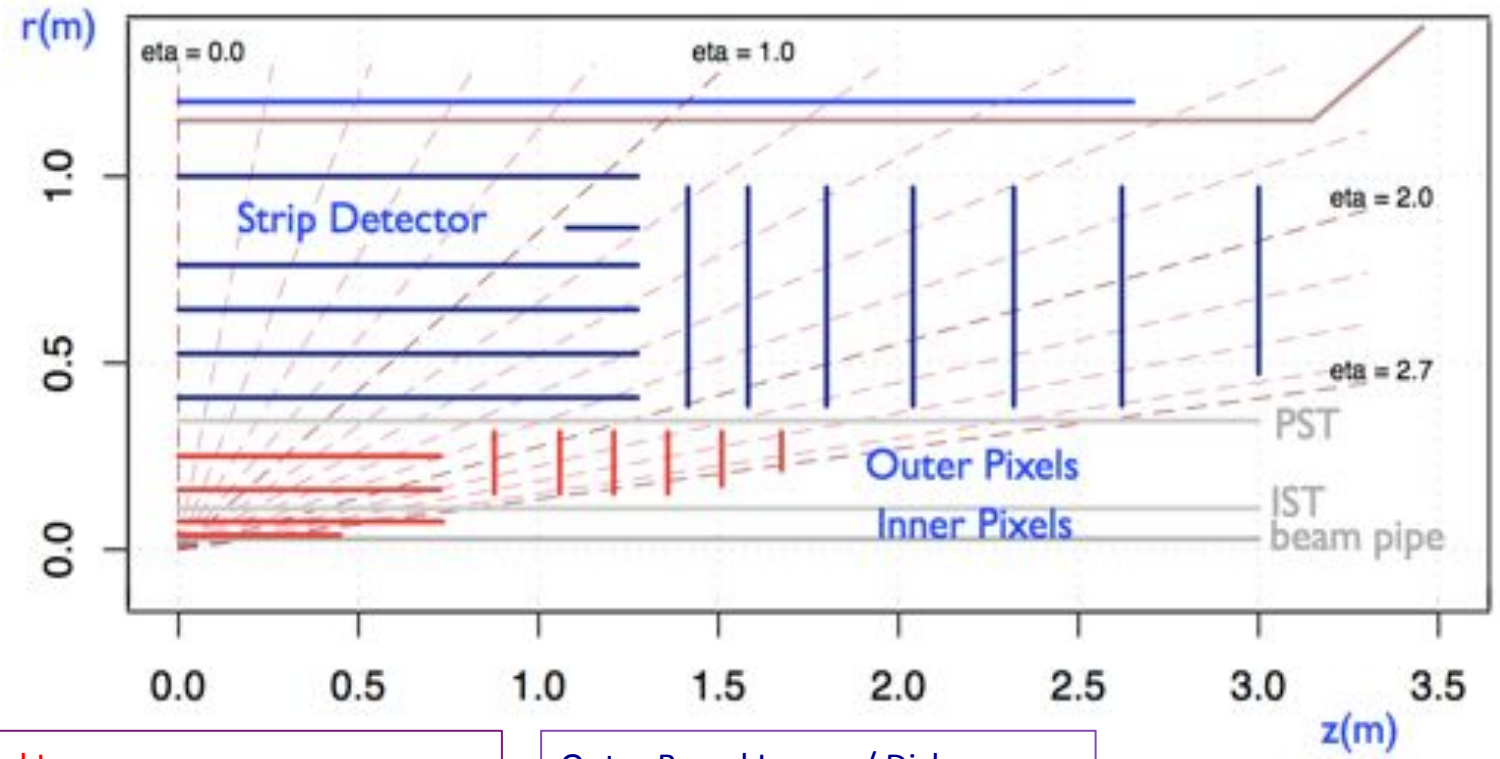


IBL: the Insertable B Layer



From Next one to Phase-2 Tracker: ATLAS

ATLAS Tracker as it could be in 2025

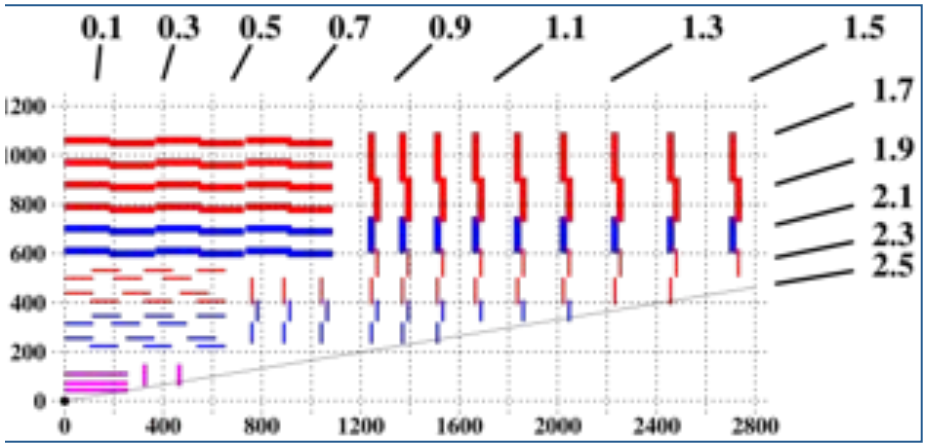


Inner Barrel Layers
Sensors: different materials and technologies possible
Radiation hardness up to 2×10^{16} n_{eq}/cm^2
Thickness: 150 μm or lower
Pixel pitch in r-ϕ 25 μm → FE-chip in 65nm CMOS technology

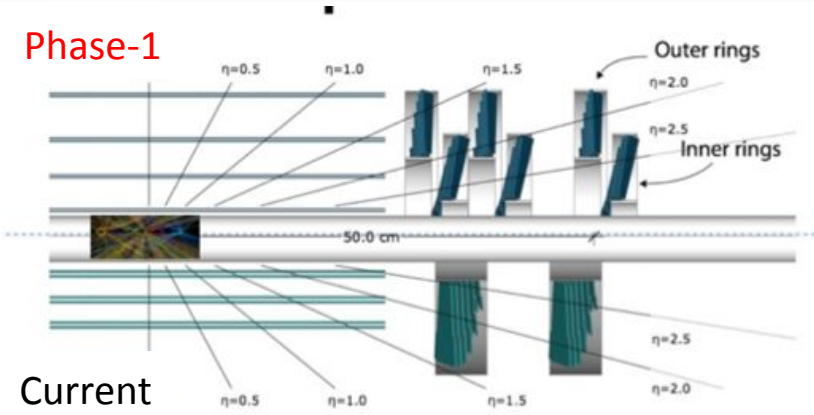
Outer Barrel Layers / Disks
Probably planar n-in-p
Sensor thickness 150 μm
Pixel size 50x250 μm^2
2x2 (Quad) chip modules

The layout proposed in the LoI provides 14 points/track to $|\eta| < 2.7$
Pixel: 4 layers + 6 disks

From Current to Phase-2 Trackers: CMS



CMS Si Tracker today



CMS **New Pixel Phase-1** as it will be in 2017; all planar pixel

Current & Phase-1: Planar pixels

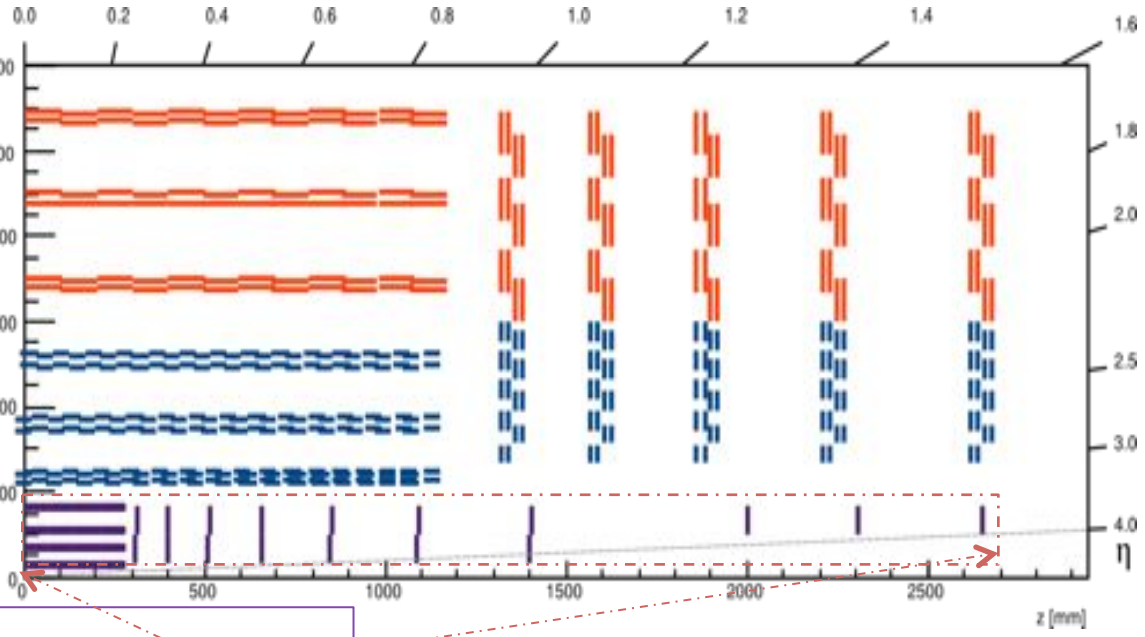
Strip/Strip modules SS

Outer Tracker, new Pt modules
3 more Pixelated layers
5 more Pixelated disks
1.5x01.mm2 PLANAR pixel size

Strip/Pixel modules PS

Inner Tracker, new
Disks to η=4

Pixel modules



Pixel Area 1.6m^2 Barrel + 2.0m^2 Disk
Possible pixel size ~25x100μm^2 ? Planar plus 1 or 2 layers 3D?

CMS Si Tracker as it could be in 2025

HL-LHC Planar Pixel R&D

- Many R&D activities in international context; INFN can have a significant role
- To get an optimal planar pixel detector for HL-LHC one has to act on many different fronts, here I list a few ones:
  - choice of bulk material
  - spark protection techniques for n in p sensors
  - low thickness
  - sensor edge: try to get small inactive sensor edges, edge-less sensors or, even better, active edges
  - pixel design, electrode configuration and isolation, bias scheme
- On the industrial side:
  - availability of suppliers for the relevant quantities
  - expected cost: reduction?
  - extreme wafer thinning and its consequences
  - bump bonding with high density and high number of bumps/module
- In Italy ATLAS & CMS have just started a new R&D on 3D and Planar n in p Pixel development for HL-LHC (still to be reviewed by INFN referees)

Excerpt from CMS Phase-2 Pixel Review on Nov. 2013

- The CMS Review highlighted the points reported in the previous page
- Qualify planar silicon sensors as the obvious likely baseline choice, at least for a large fraction of the active surface
- Assess the feasibility of sensor thinning

- Assessing the radiation tolerance of readout electronics and of planar silicon sensors is the highest priority for the phase-2 pixel project,
- Radiation tolerance is a key factor to assess the possible advantage of using 3D sensors in the inner layers. The collaboration should focus the effort and shift resources towards this activity

- Collaboration with ATLAS should be pursued wherever appropriate, e.g. through common submissions and sharing of experimental results

All this is exactly in the spirit of what we are doing in our R&D
We will try to follow these guidelines

CMS Planar Pixel from HPK Production

T. Rohe, PSI Zurich

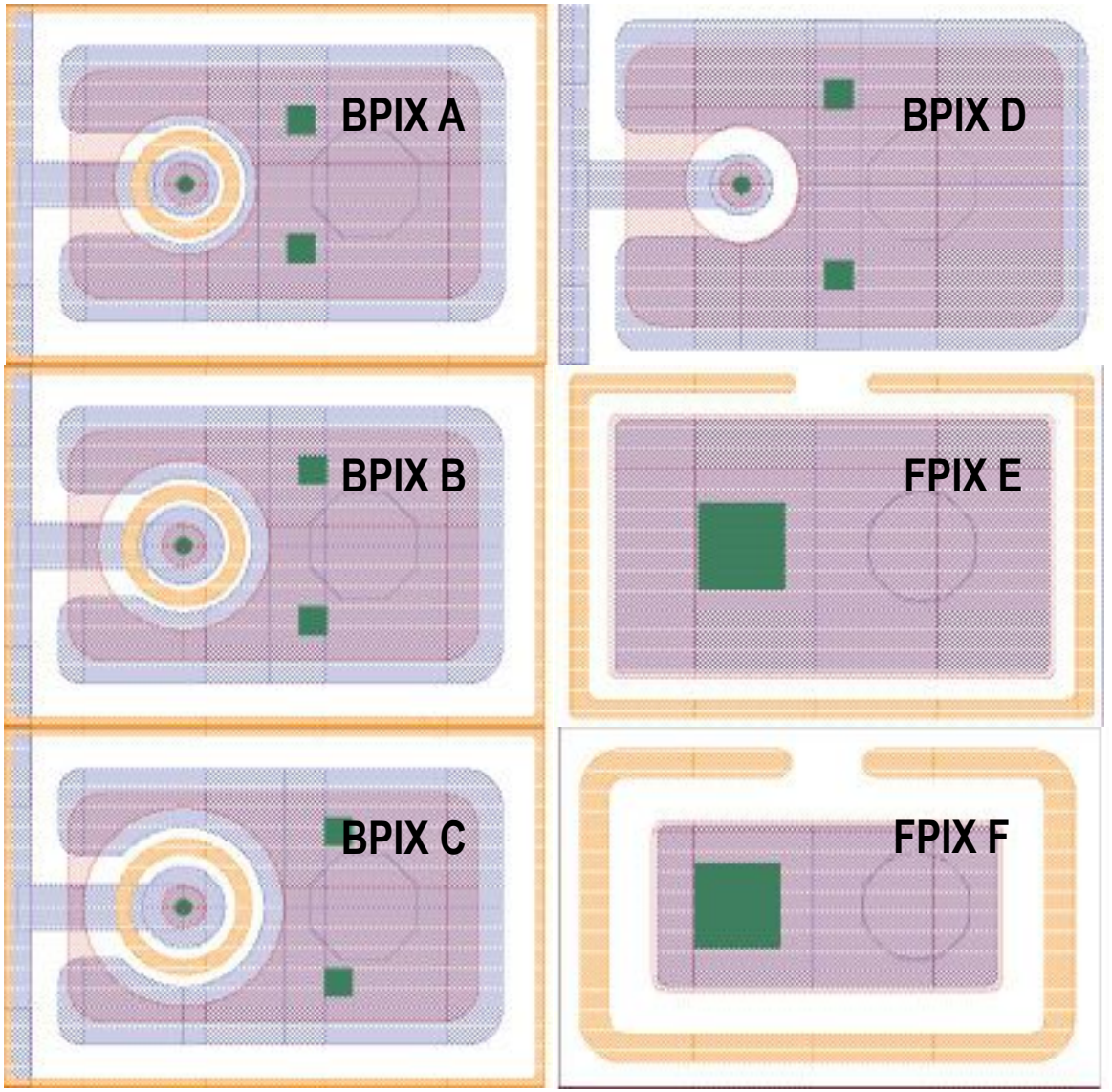
Summary of devices for CMS R&D studies at PSI and US labs

HPK wafer contains 6 different layouts

- **BPIX A-C**: Gap in the bias structure between 14 µm (~8% affected area) and 22 µm (16% of the area affected), gap between pixels: 36 µm contain p-stop mask and (in principle) work with p-stop isolation also.
- **BPIX D**: No p-stops, small bias structure (10 µm gap, ~5% affected area), gap between pixels: 22 µm (all measures are close – but not identical – to the present BPIX sensor)
- **FPIX E+F**
  - Open p–stop
  - Different gap size (~30 and 50 µm)

Available substrates (all n- and p-type)

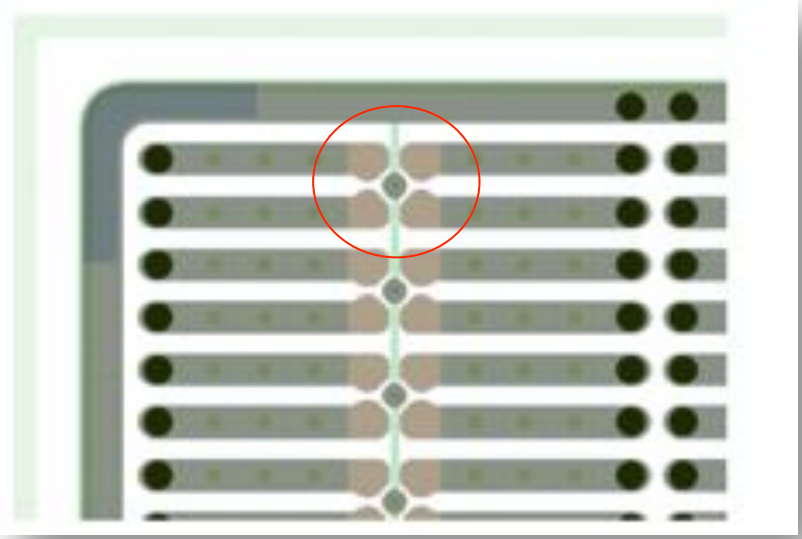
- FZ 320, 200, (120) µm
- mCz 200 µm
- Epi 100 (70), 50 µm
- FZ 200 µm, 2 metal layers



Open questions and Issues

- Pixel Isolation: compare performance of the two options p-stop or p-spray
- Is the region between the p-stops a source of charge loss?
- How severe is the impact of the bias dot (for different dot sizes)?
- Does the biasing structures work?
- How to reduce inefficiencies due to punch through structures?

We plan to address most of these issues in the CMS-IT R&D work packages

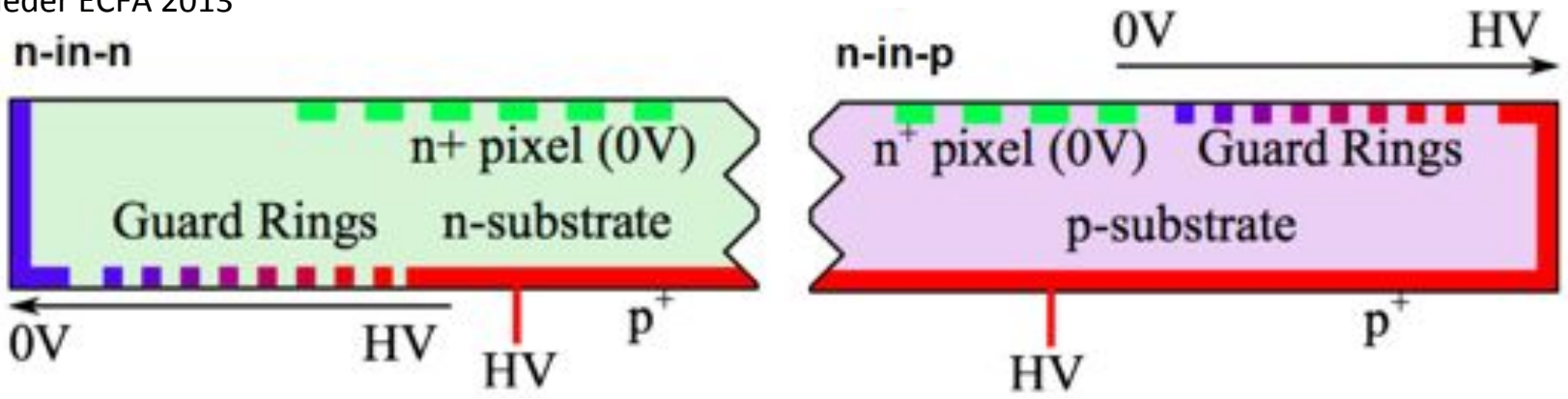


An example: a possible solution to increase efficiency is to connect four pixels with a single punch through structure. Requires new layout design

ATLAS pixel, A. Macchiolo, MPI, 9th Trento WS

Bulk Material

Julia Rieder ECFA 2013

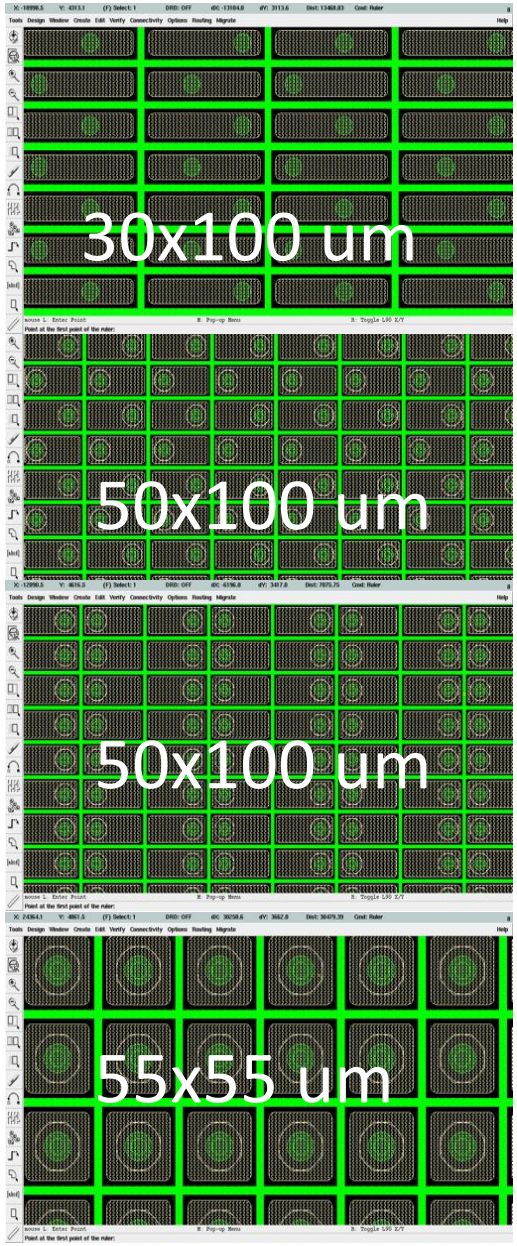


- Read out chip side at ground potential
- Double-sided processing
- Type inversion
- Partly depleted operable
- Well proven design

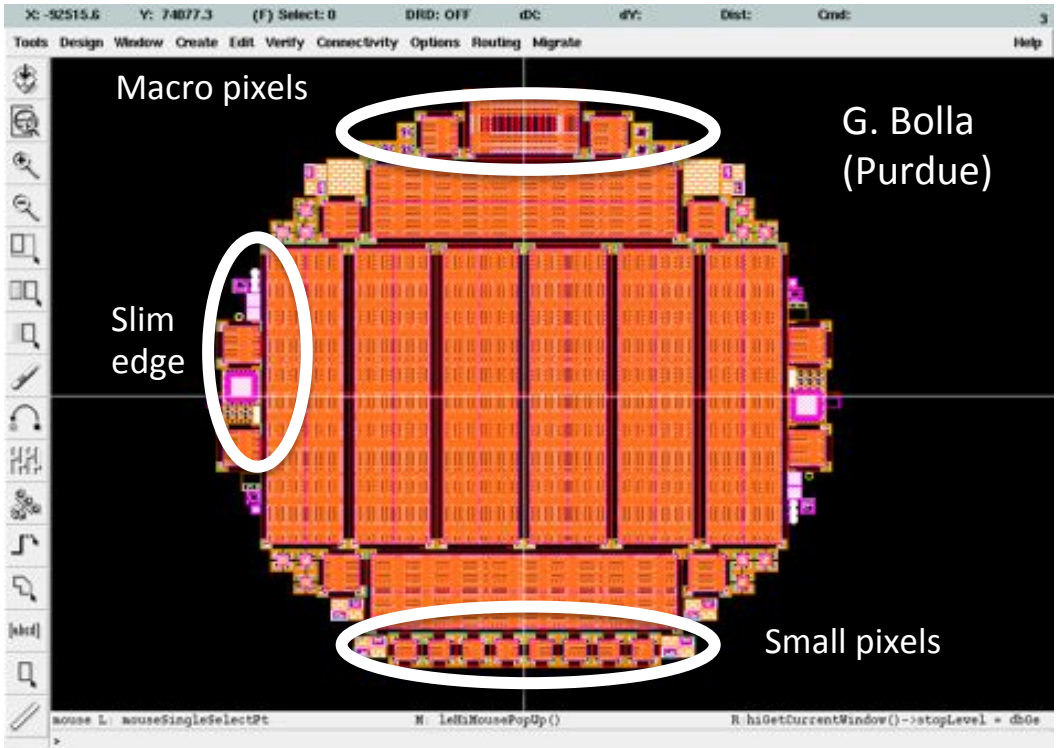
- Voltage drop on read out chip side
- Single-side processing
- Presumably lower production costs
- No type inversion

- CMS has already chosen p-type material for strip sensors
- Both n-readout options open for Pixels (n^+ in n or n in p): to be defined with R&D

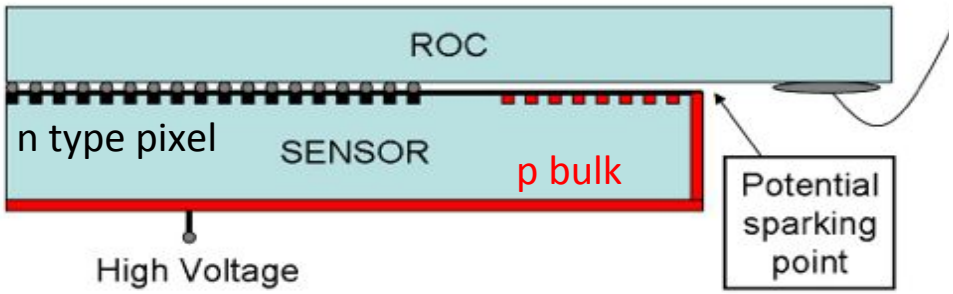
CMS R&D in USA



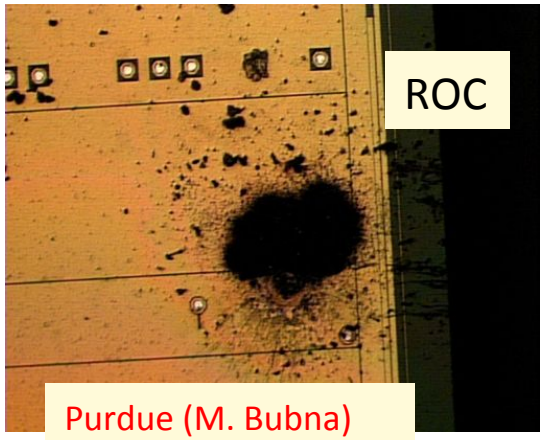
- New planar devices designed in US in the shadow of Pixel Phase-1 Production
- Macro-pixels, Slim-edge, Small size pixels
- **INFN R&D:**
  - **start re-using part of these structures in next INFN batches at FBK**
  - **proceed with irradiations, test beams, design of new pixels of small size (RD53 readout)**



R&D against Sparks



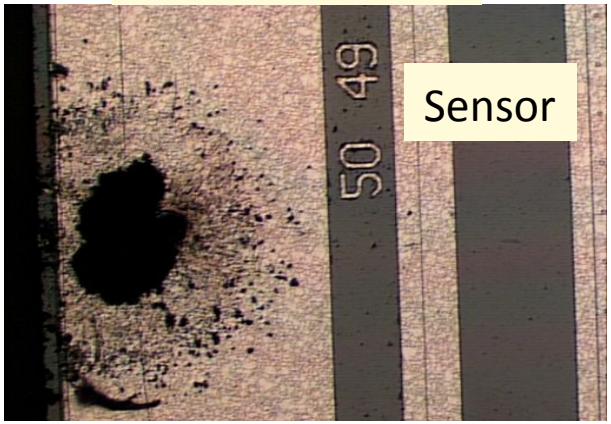
ROC at Ground

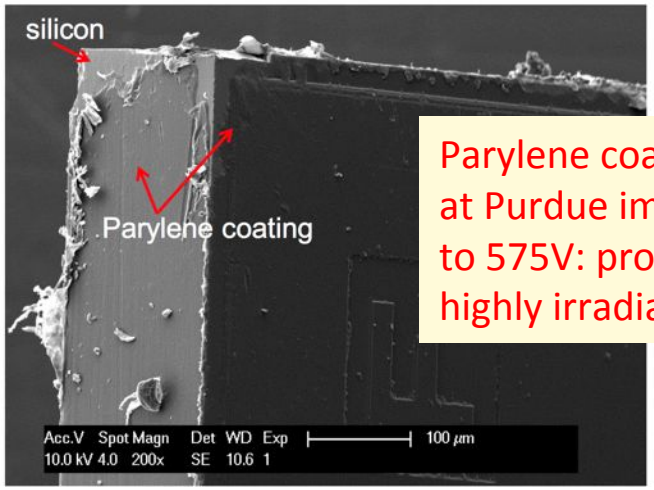


Purdue (M. Bubna)

Air gap between sensor and ROC can be as low as 10μm with Indium Bump Bonding: high spark probability

We need to investigate how to avoid this kind of problems
Crucial for pixel detectors to be operated at High Voltage Bias
Two chemical compounds have been tested p to know:
Parylene
Benzocyclobutene





Parylene coating 2 μm thick tested at Purdue improves Breakdown up to 575V: probably not enough for highly irradiated pixel

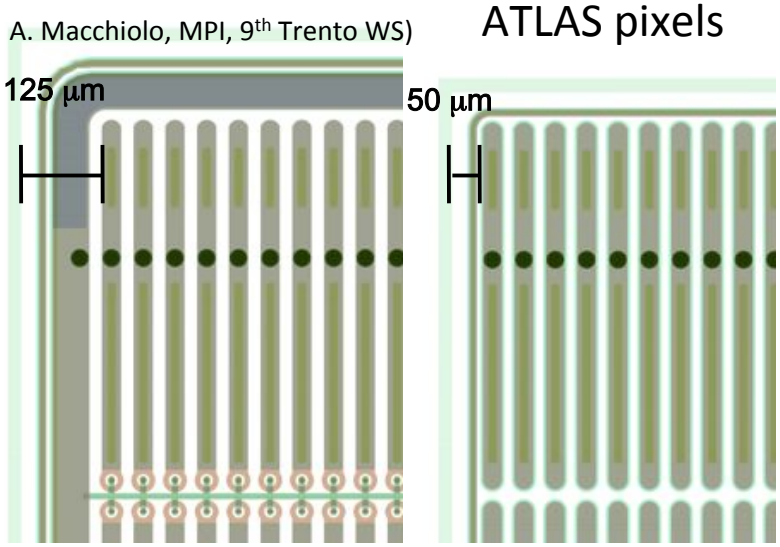
Dielectric strength:
- Parylene 280 V/μm
- BCB 5300 V/μm

Require Industrial partners, more steps, add lithography, masking, insulator deposition. More effort, new ideas are needed. Coating can largely affect mass production and cost

Slim and Edge-less Pixel

- Reduce the inactive region at sensor periphery
- Reduce the number of Guard Rings or even eliminate Bias Ring
- Already tested in ATLAS, can be implemented in CMS starting from current layout

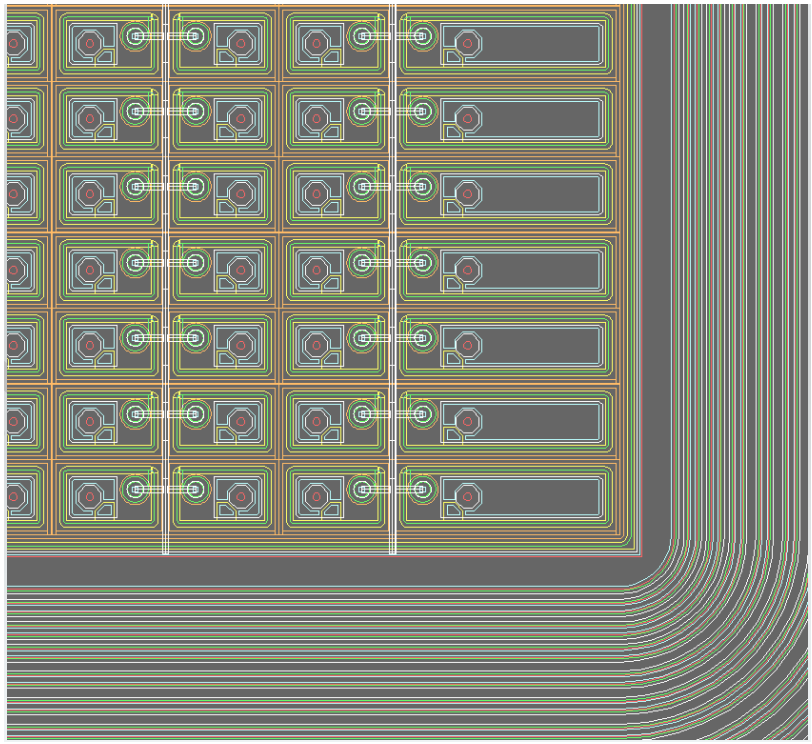
ATLAS pixels



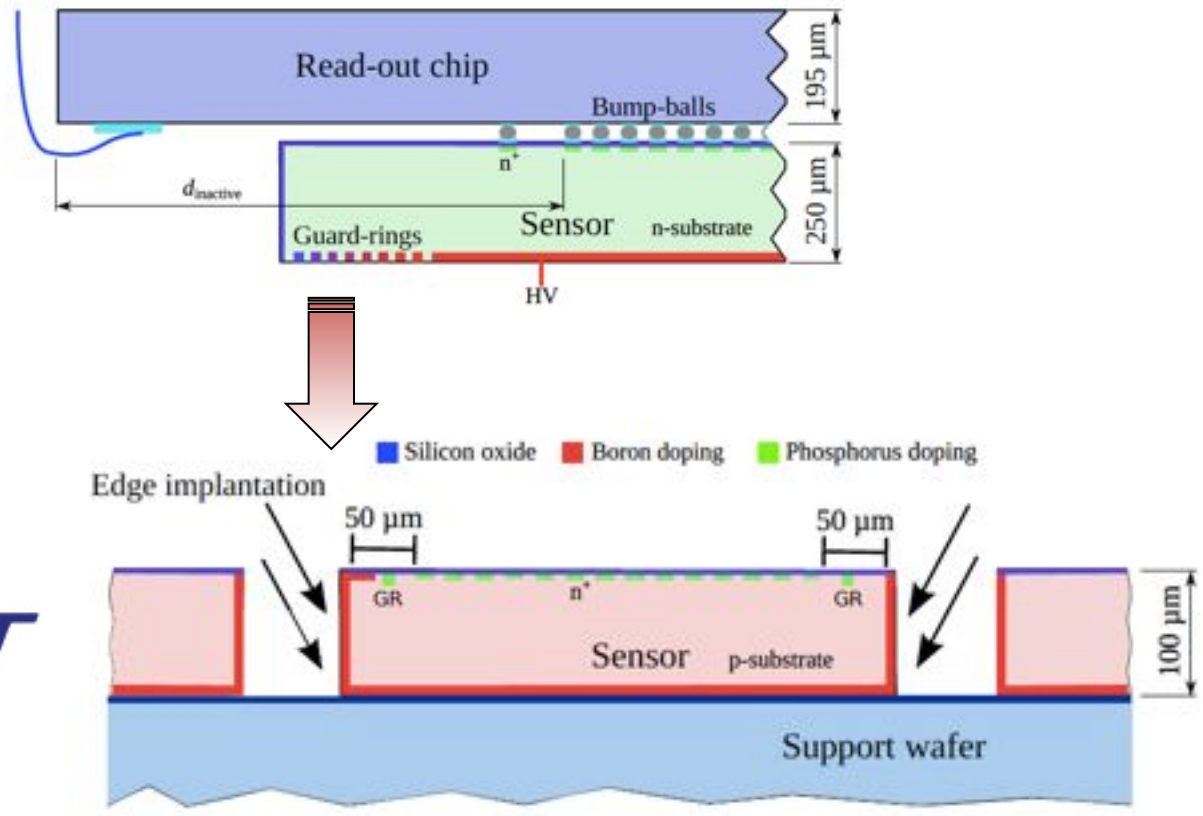
125 μm edge implemented In FE-I3 and FE-I4 sensors: Bias Ring + floating Guard Ring

50 μm implemented only in FE-I3 sensors: Floating Guard Ring

CMS pixels, current design



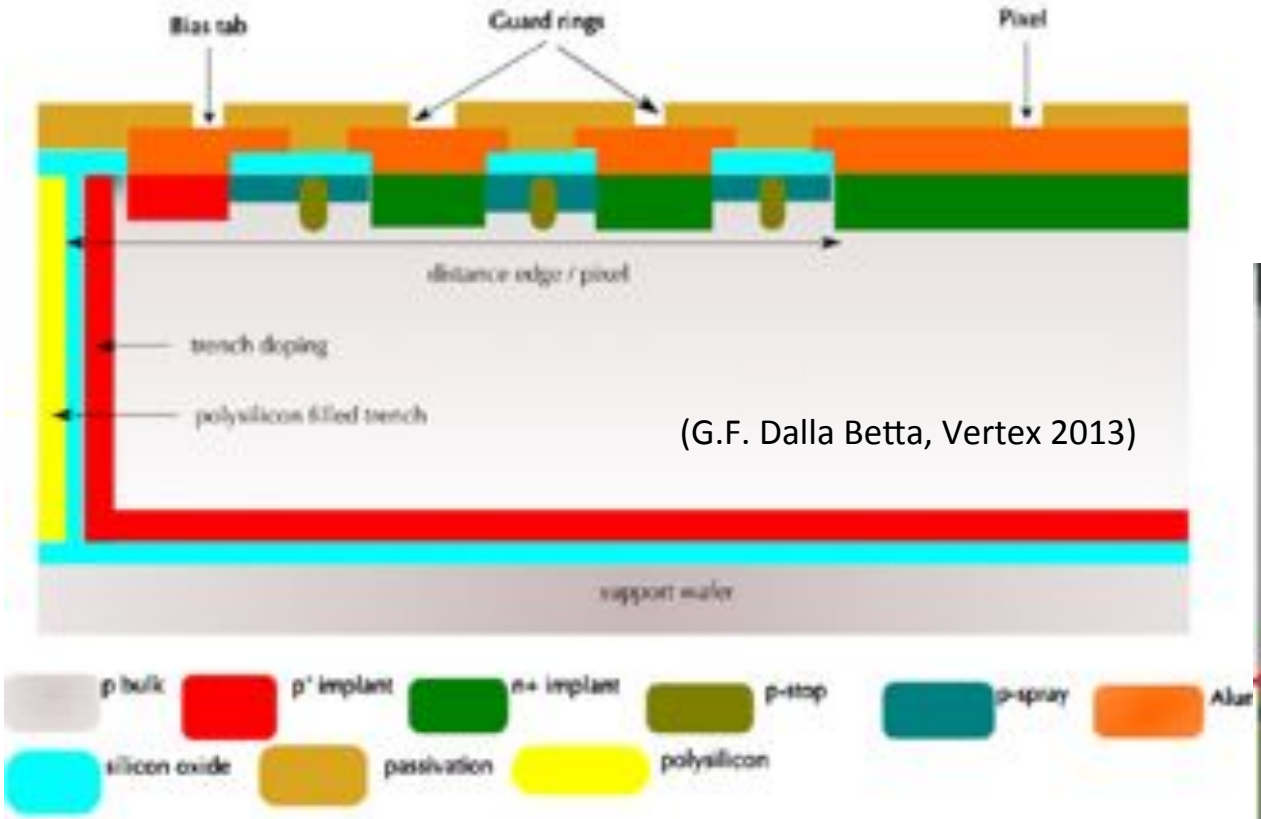
Active Edge Planar Pixel



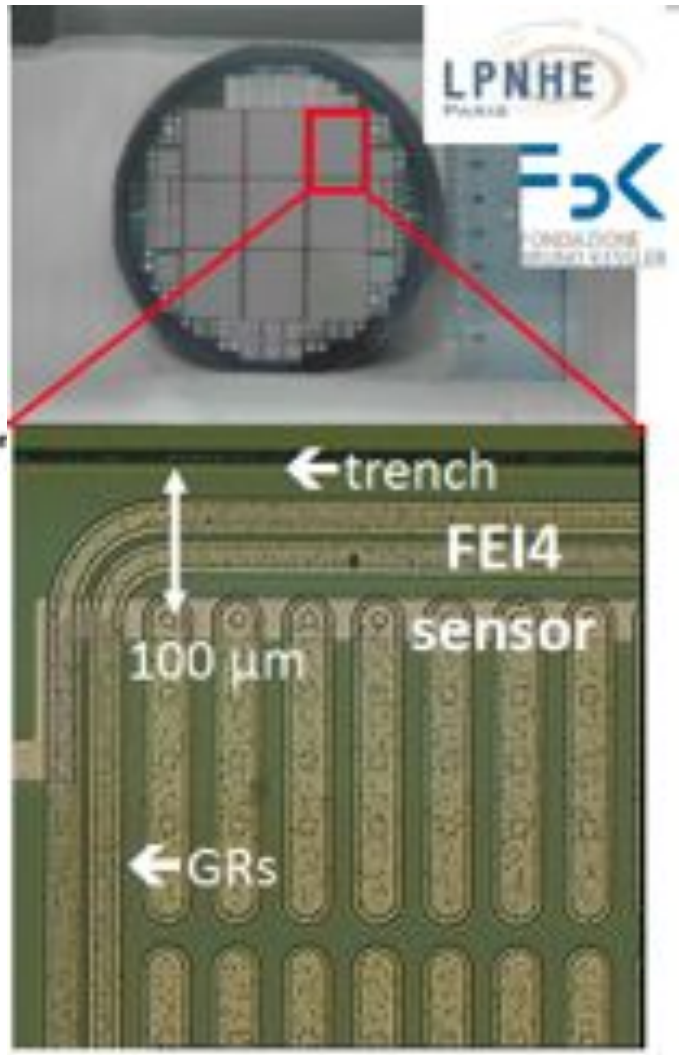
ATLAS achievements:
n in p pixels on FZ and MCZ material
100 µm and 200 µm thickness
p-spray isolation method transferred from HLL to VTT
Flip-chipping performed at VTT after removal of support wafer (from A. Macchiolo, MPI, 9th Trento WS)

Active edge technology now available at processing facilities (e.g., VTT, SINTEF, FBK).

Planar Active Edge at FBK



Edgeless pixels (n-on-p) for ATLAS upgrade within PPS collaboration (collaboration with LPNHE Paris)



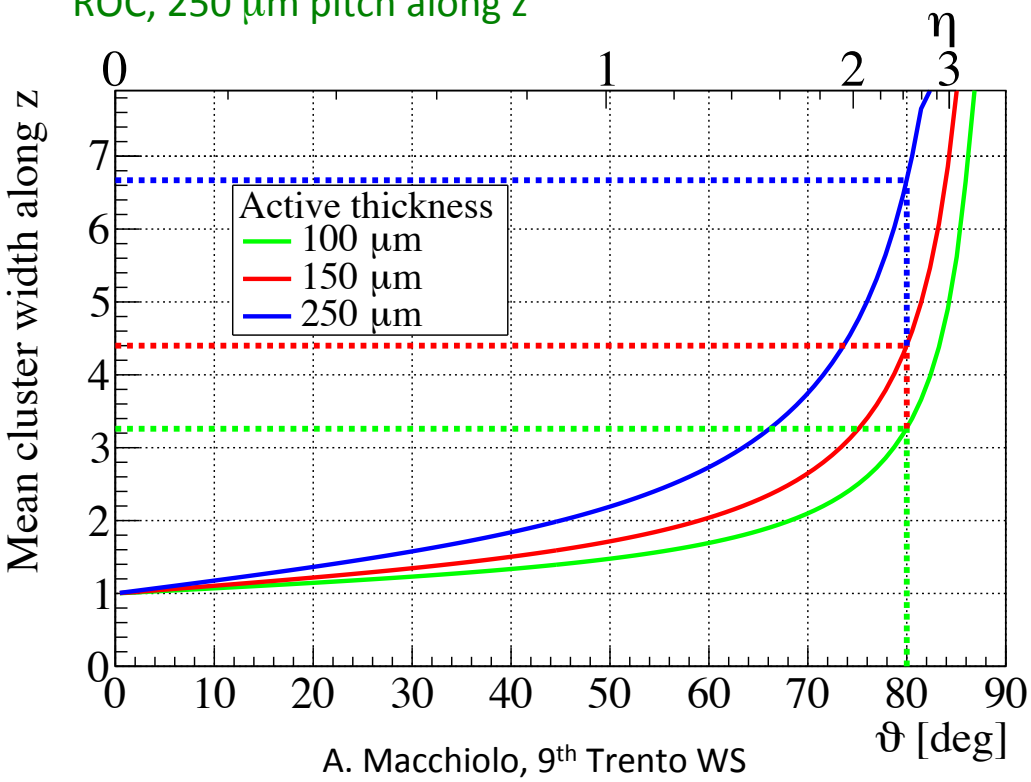
- FEI4 and FEI3 pixels (ATLAS)
- 4.5 x 200 µm trench, doped by diffusion
- Different edge/GR designs, typically 100 – 200 µm

Similar design sensors will be included in next INFN R&D, 6" batches in 2014 (standard planar and active edge)
Presently active edge are expensive: reduce cost

Go Thinner!

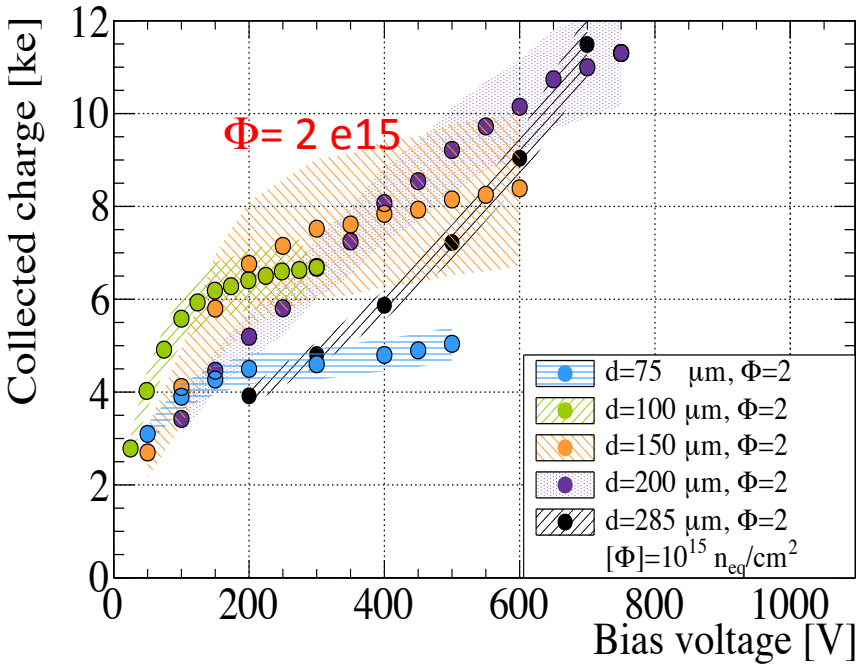
- Thin devices imply
  - lower depletion voltage
  - less bias current after irradiation (and easier cooling)
  - smaller cluster width at high η
  - lower material budget
- but also
  - lower collected charge
  - lower yield

Expected mean cluster width along the beam direction as a function of the pseudo-rapidity for FE-I4 ATLAS ROC, 250 μm pitch along z



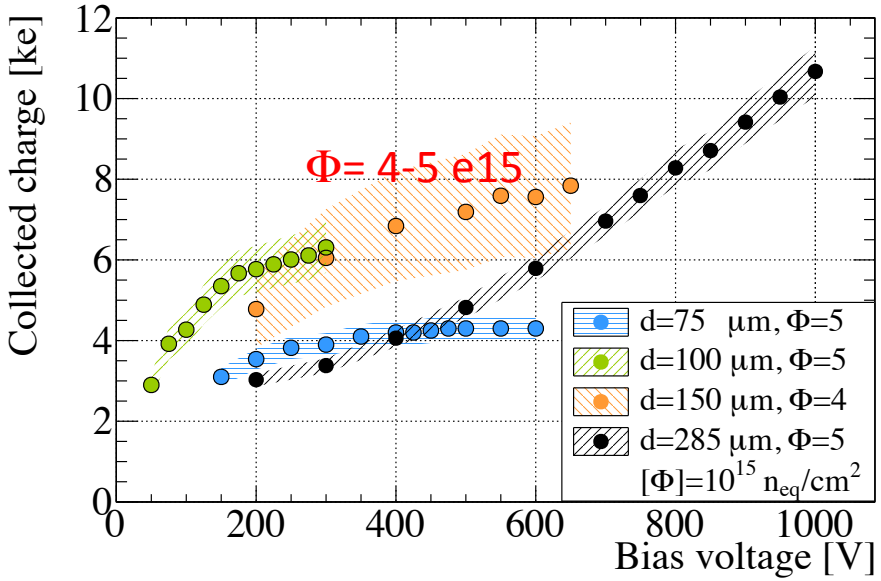
A. Macchiolo, 9th Trento WS

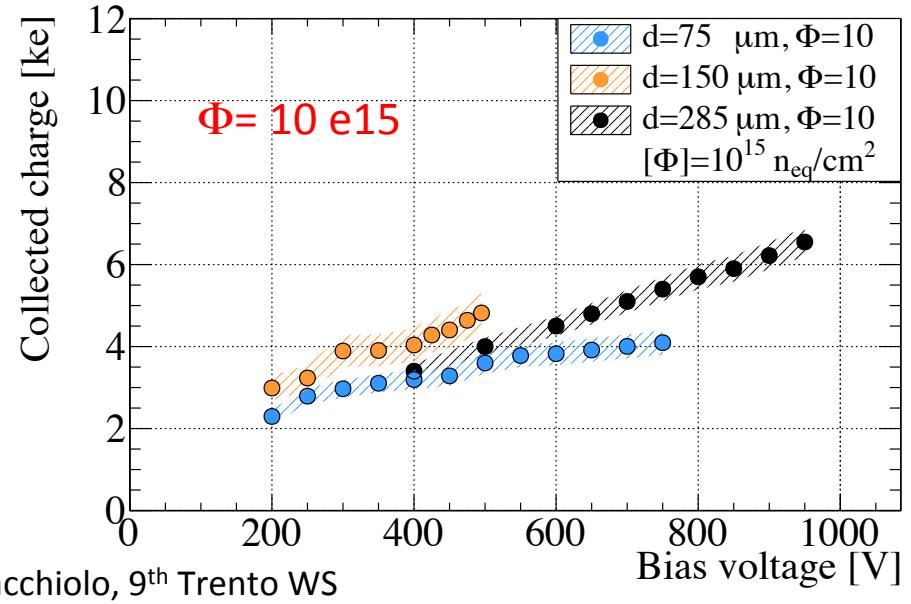
Charge Collection for Pixels of Different Thickness



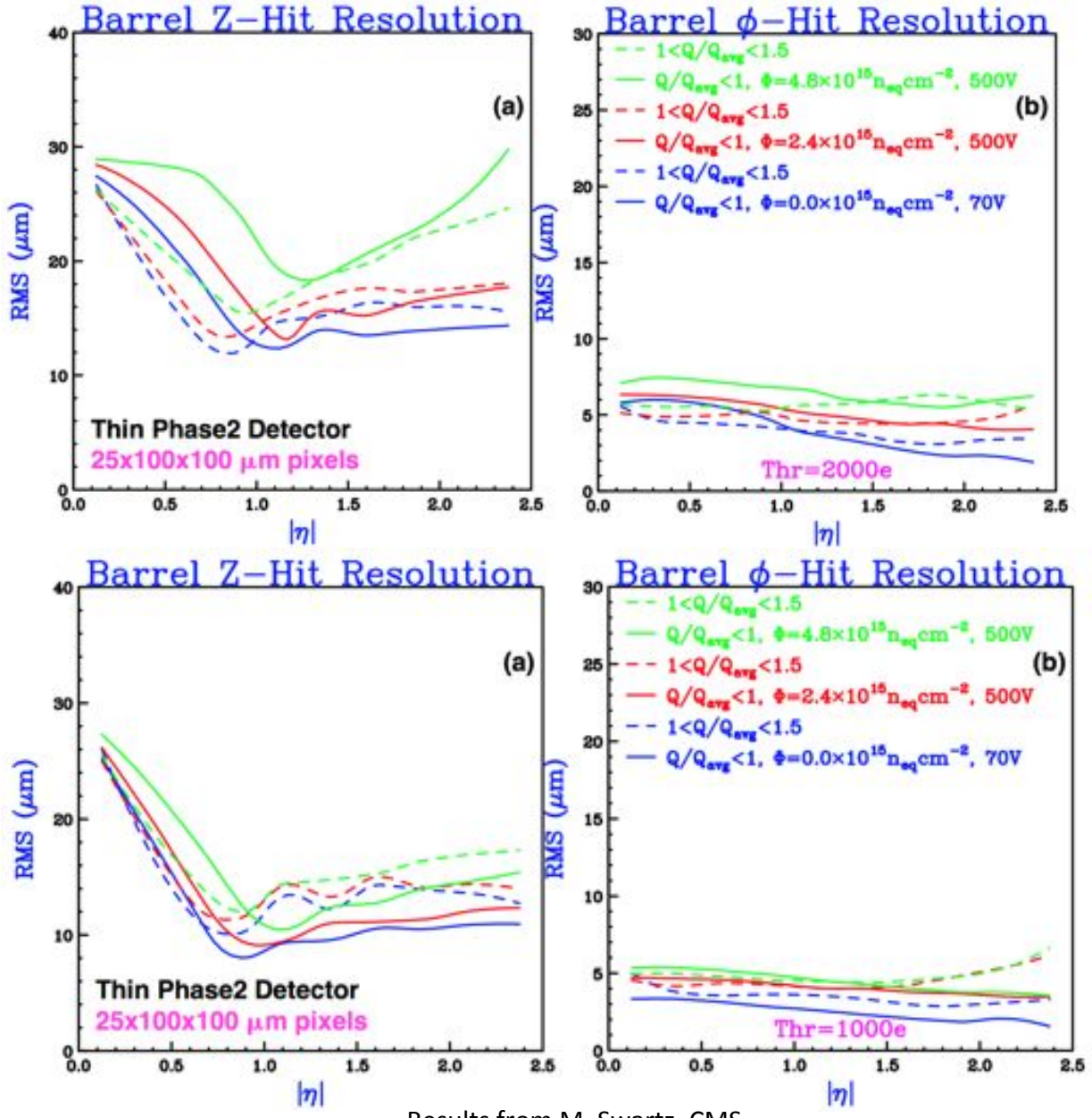
- The 100-150 μm thick sensors show higher charge collection up to a fluence of 4-5x10^{15} n_{eq} / cm^2
- At higher fluences the effect of charge trapping tends to equalize the charge collection efficiency for all thicknesses

- What about 2x10^{16} n_{eq} / cm^2 ?
- Can thin pixels be operated at 1KV Bias?
- At what temperature?
- Can we live with 4000 collected electrons?





CMS Planar Device Simulation: Spatial Resolution vs η



Thickness 100μm
Pixel size 25x100μm²
P-Spray isolation

GREEN = 4.8×10^{15} n_{eq} / cm^2

RED = 2.4×10^{15} n_{eq} / cm^2

BLUE = not irradiated

RMS resolutions include non-Gaussian tails
~30% of hits in high charge bands (dashed curves)
~70% of hits in low charge bands (solid curves)

Extremely good results at 1k e^- threshold, and still very satisfactory ones at 2ke threshold
Let's do it for real!

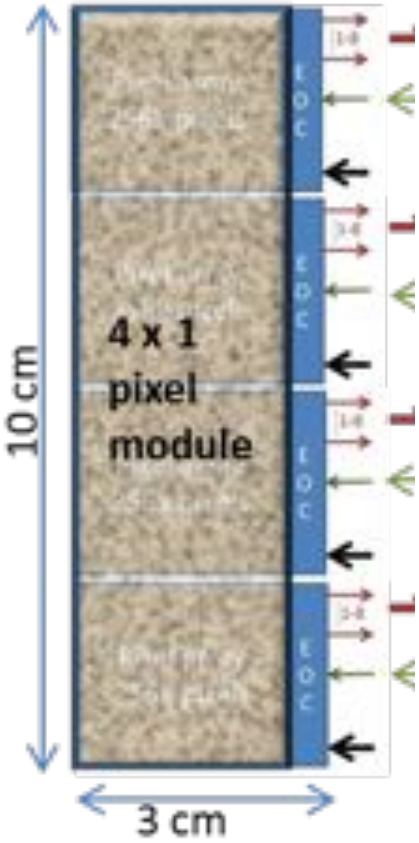
Results from M. Swartz, CMS

Technological Challenges for the Future

- Thinning to very low thickness both sensor and ROC wafers causes problems of bowing, leading to poor yield after bump bonding
- Bowing is depending on industrial process and single or double side implants
  - n in p pixel cheaper but lower yield?
- In the hypothesis of
  - single pixel size 25x100 μm^2
  - full ROC size 30x25mm^2

→ each ROC has > 250k channels to be bump bonded: a nice challenge. A "4-chip module" can have 1 Million bumps!

- Pixel size and readout chip cell size must be developed in close collaboration, driven by Physics requests and 65nm process needs (RD53)



Sketch of a possible Phase-2 pixel module

Planned INFN-FBK R&D ATLAS & CMS: a Three Year Plan (1)

- In collaboration with FBK under MEMS3 agreement (partially funded) starting in 2014:
  - n in p pixel program on 6" using Silicon-Silicon Direct Wafer Bonding (DWB) of different thicknesses
  - Standard Planar Pixel batch with sensors from ATLAS and CMS design plus test structures
  - Design of innovative pixel devices according to most recent results
- By late Autumn 2014:
  - 3D Pixel batch with sensors from ATLAS and CMS design, plus test structures (see next talk)
  - One Planar Active-Edge/Slim-Edge Pixel batch
  - New pixel size design

Planned INFN-FBK R&D ATLAS & CMS: a Three Year Plan (2)

- For every batch
  - Laboratory characterization of sensors
  - Sensor Bump Bonding (Flip Chip)
  - Irradiation campaign of test structures and sensors
  - Test beam measurements before and after irradiation
- In 2015/16 proceed with a second round of sensor production
  - based on obtained results
  - final pixel size?
  - Again characterization, irradiation, test beam

- The R&D program will be discussed with INFN referees in March/April 2014

Conclusions

- What to do in INFN?
- We want to keep pace with evolving technologies
- Italian Industry cannot be left aside off the Planar Pixel business
- If we want to play an active role in HL-LHC Tracker detectors we must act now
- This is a good playground for young physicists interested in HW
- Let's not miss this opportunity!

Acknowledgements

- I wish to thank all ATLAS and CMS people which contributed to this talk, most of them totally unaware they were contributing ☺