3D Silicon Detectors

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Future Detectors for HL-LHC
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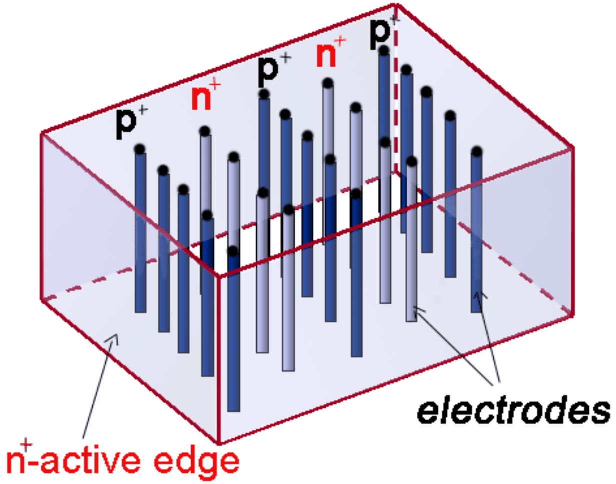
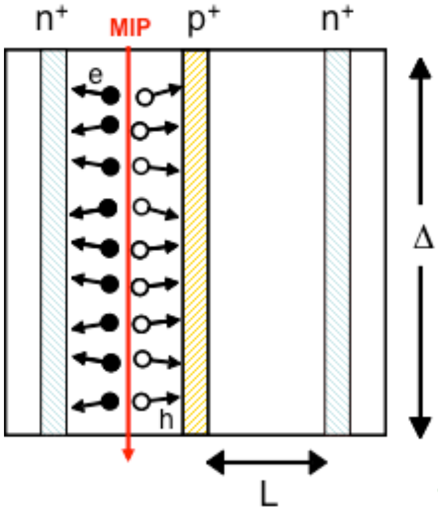
Outline

- Introduction
- State of the art
- 3D pixels for HL-LHC
  - requirements
  - ideas
  - strategy
- Conclusions

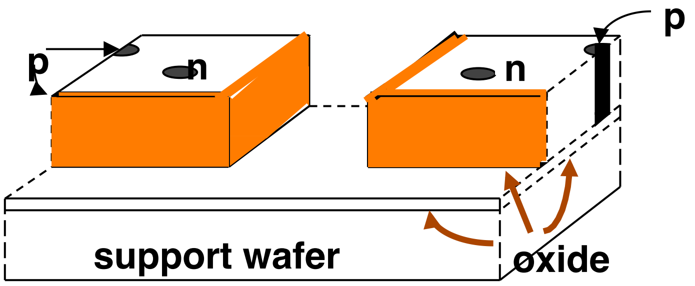
3D detectors

S. Parker et. al. NIMA 395 (1997) 328





Electrode distance (L) and active substrate thickness (Δ) are decoupled → $L<<\Delta$ by layout



C. Kenney et. al. IEEE TNS 48(6) (2001) 2405

ADVANTAGES:

- Low depletion voltage (low power diss.)
- Short charge collection distance:
  - Fast response rise
  - Less trapping probability after irr.
- Lateral drift → cell “shielding” effect:
  - Lower charge sharing
  - Low sensitivity to magnetic field
- **Active Edges**

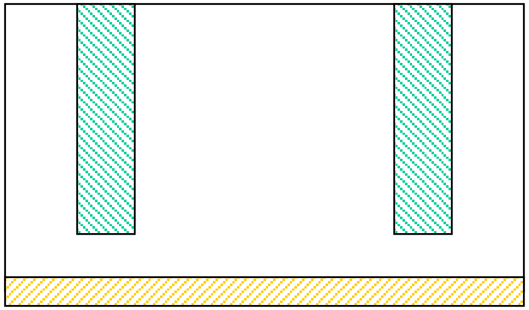
➡ **HIGH RADIATION HARDNESS**

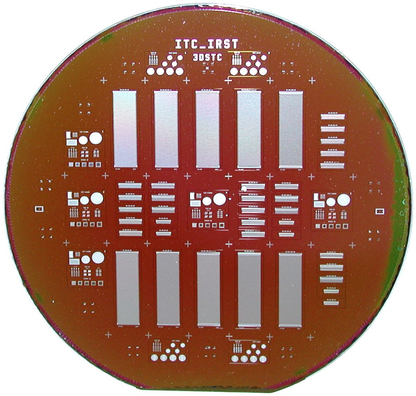
DISADVANTAGES:

- Non uniform spatial response (electrodes and low field regions)
- Higher capacitance with respect to planar (~3-5x for ~ 200 μm thickness)
- Complicated technology (cost, yield)

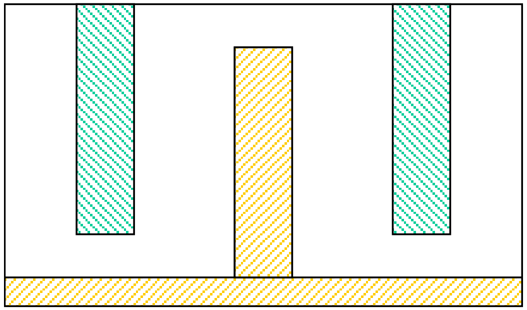
FBK-INFN 3D detector developments

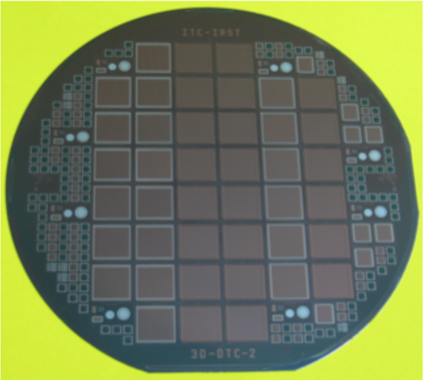
STC (2004-2006)



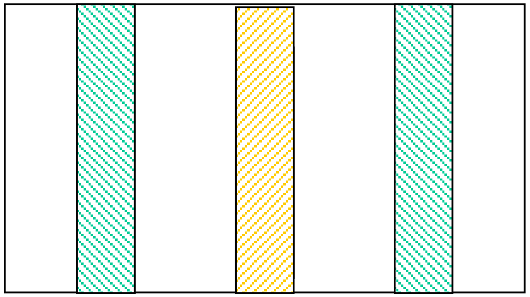


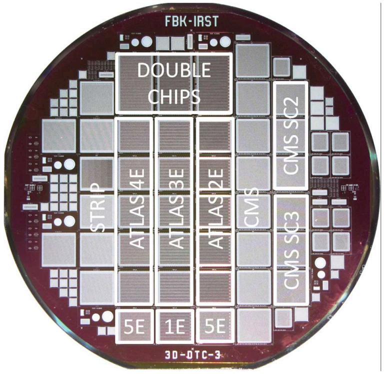
DDTC (2007-2009)

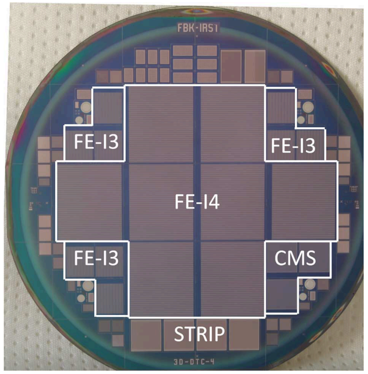




DDTC+ (2009-2012)







- FBK/INFN/PAT “MEMSx” agreements (since 2004)
- INFN CSN5 TREDI (2005-2008) → STC, DDTC + PAE
- INFN CSN5 TRIDEAS (2009-2012) → DDTC+
- INFN CSN1 ATLAS (since 2010) → IBL production (SoA)

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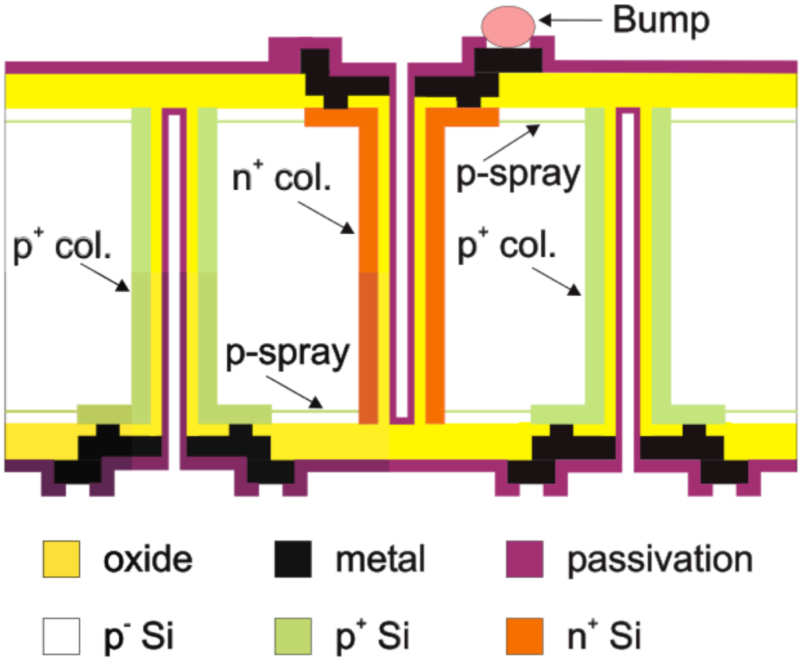
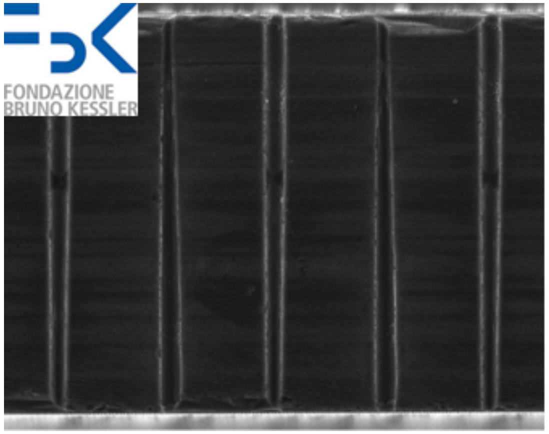
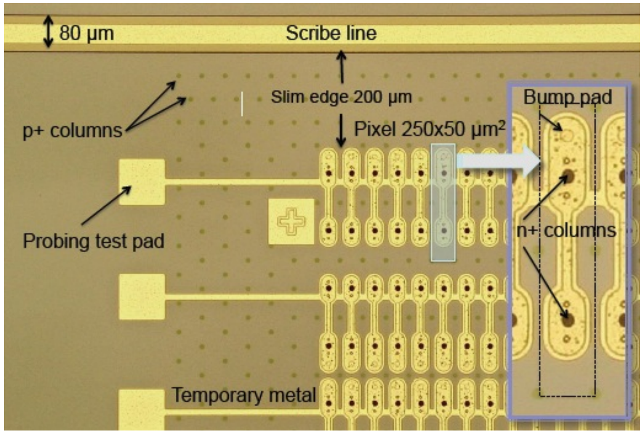
FBK 3D detectors: process and design

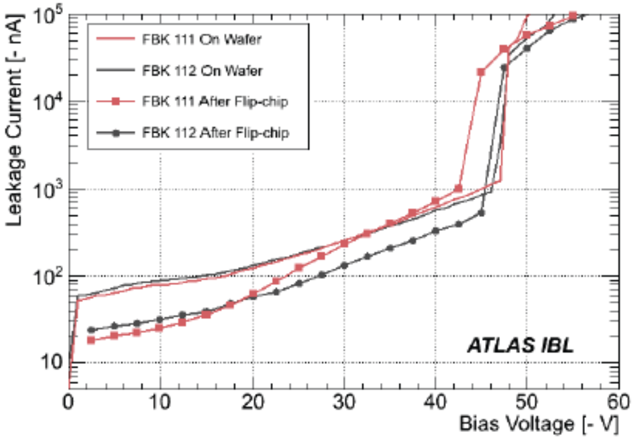


- Fully double-sided process
- No support wafer (bias from back side)
- Empty columns, with 11 um diameter and 230 um thickness (proved up to 260 um)
- Slim edge (200 um for IBL, proved down to 75 um for AFP)
- Temporary metal for I-V tests

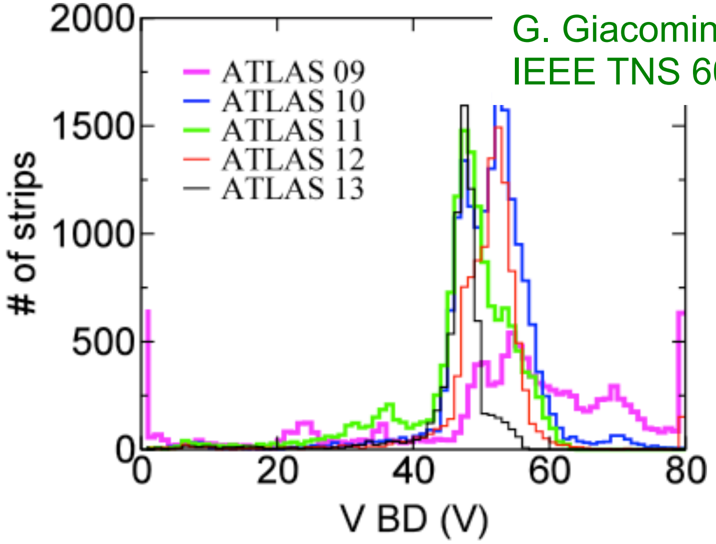
C. Da Via, et al., NIMA 694 (2012) 321
G.F. Dalla Betta, et al., JINST 7 (2012) C10006
ATLAS IBL Coll., JINST 7 (2012) P11010



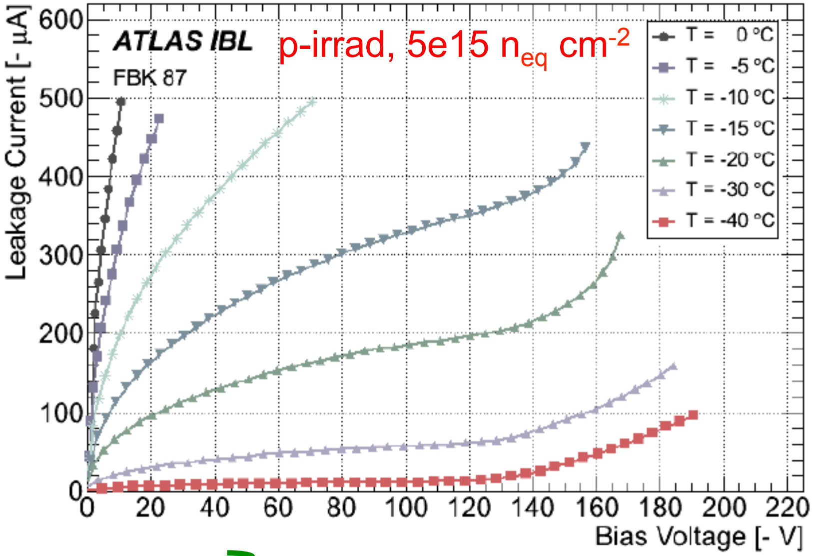




Critical issues in the IBL technology



G. Giacomini, et al., IEEE TNS 60(3) (2013) 2357



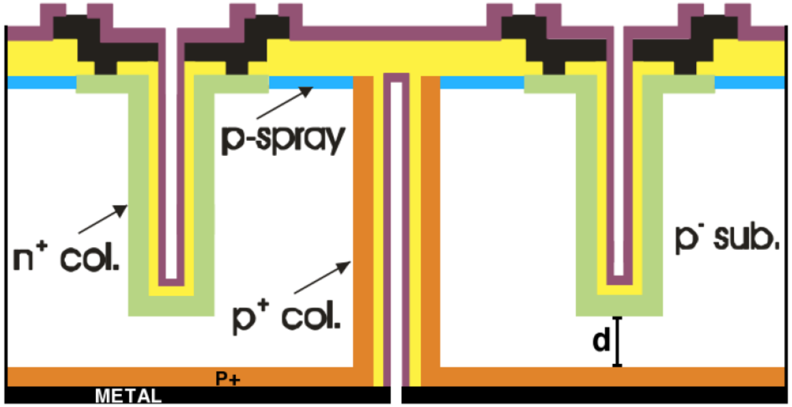
- Relatively low intrinsic breakdown voltage (due to p-spray)
- V_{BD} increase after irradiation not as high as expected
- High sensitivity to process defects → High yield variability

Understood and improved, see next slide

Batch	Tested Wafers	Selected Wafers	Total Sensors	Number of Good Sensors	Yield on Selected Wafers (%)
3D ATLAS 10	20	12	96	58	60%
3D ATLAS 11	11	4	32	14	44%
3D ATLAS 12	16	13	104	63	61%
3D ATLAS 13	11	4	32	15	47%

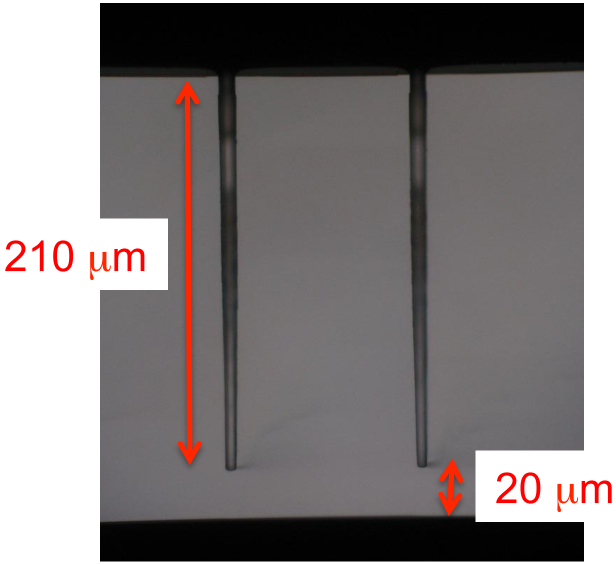
A modified technology at FBK

M. Povoli et al., IEEE NSS 2012

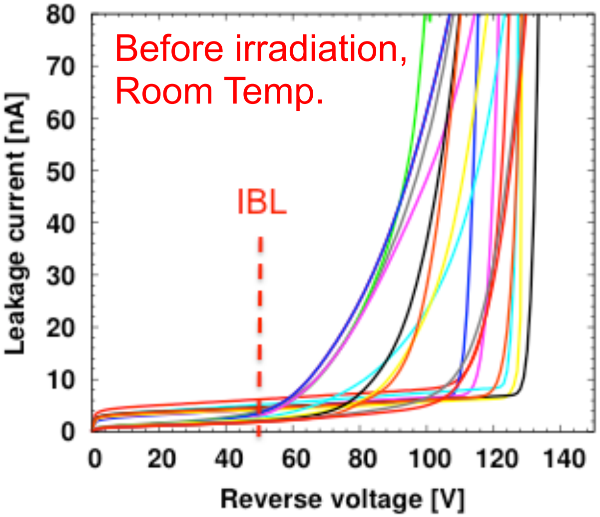


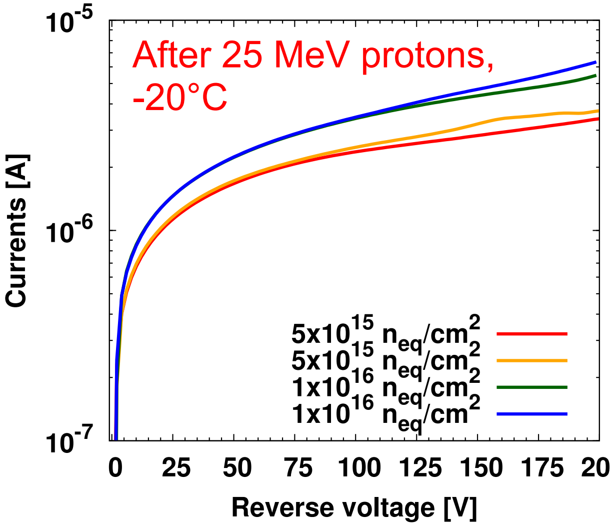
- Last 3D batch on 4” wafers (2012)
- Partially etched junction columns
- Passing-through ohmic columns for effective slim edges (50 μm achieved !)
- Reduction of back-side mask number & overall process simplification (~1/3)
- Large increase of V_{BD} before and after irradiation

Optimization of the DRIE step to accurately control columns depth



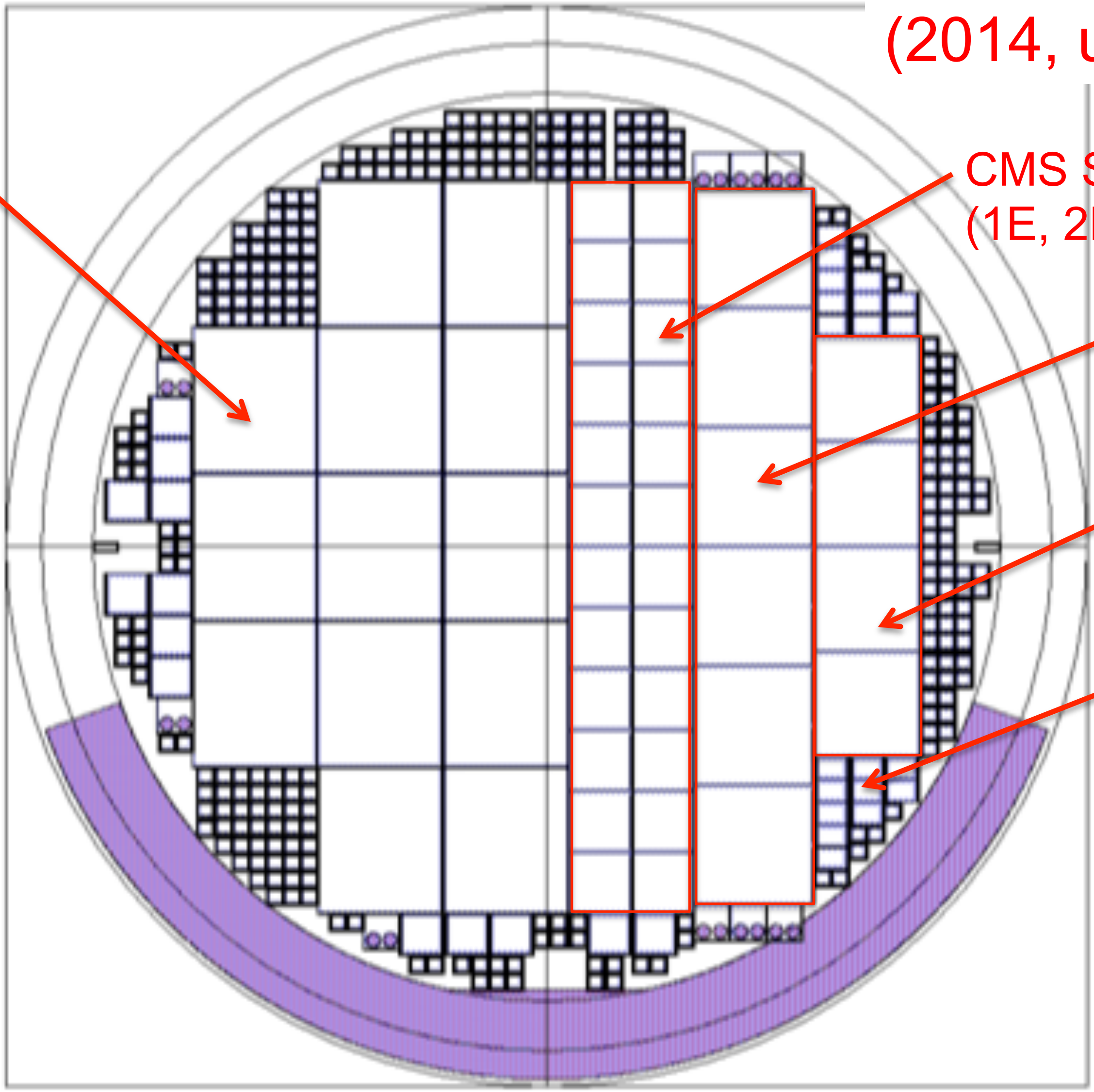
G.F. Dalla Betta et al., IEEE NSS 2013





First 3D batch on 6” wafers at FBK

(2014, under way)



ATLAS FE-I4 (13x)

CMS Single chip (24x) (1E, 2E, 3E, 4E)

CMS Quads (6x) (2E, 3E)

MEDIPIX2 (4x)

NA62 test chip (20x)

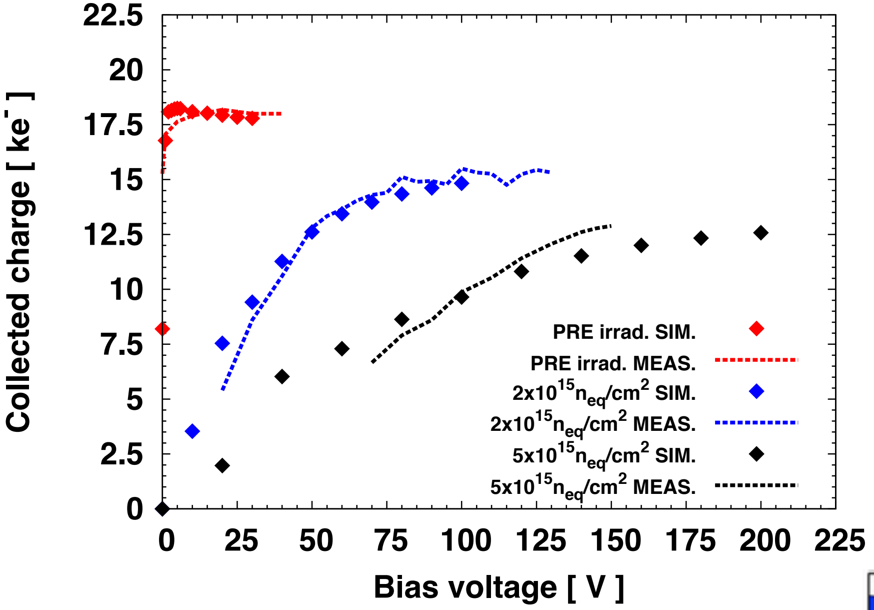
4” wafers (IBL):
8 FE-I4 sensors
6” wafers (future):
~ 30 FE-I4 sensors

→ Cost reduction

Functional tests (1): ATLAS IBL

3D pixels with FE-I4 ROCs

G.F. Dalla Betta et al, Vertex 2012

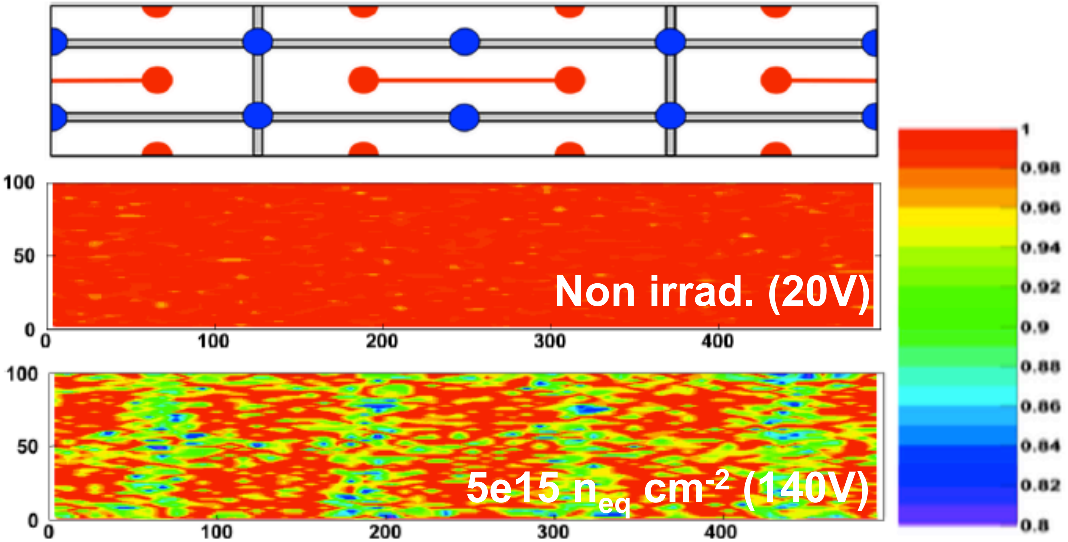


- CCE results from ^{90}Sr β-source tests in good agreement with TCAD simulations
- Qualified for ATLAS IBL: >98% hit efficiency for 15° tracks at 160 V, -15°C (<20 mW/cm^2), after 5x10^{15} n$_{eq}$/cm^2

Beam test results with 120 GeV pions at CERN (15° tilt, before and after 25 MeV proton irradiation)

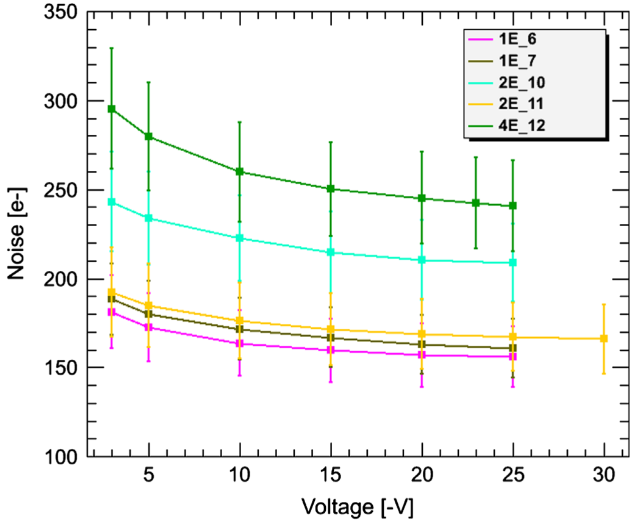
Sensor ID	Bias (V)	Fluence (n$_{eq}$/cm^2)	Threshold (e-)	Hit Eff. (%)
FBK13	20	-	1500	99.4
FBK90	60	2x10^{15}	3100	99.2
FBK87	**140**	**5x10^{15}**	**2400**	**95.3**
FBK87	**160**	**5x10^{15}**	**1500**	**98.2**

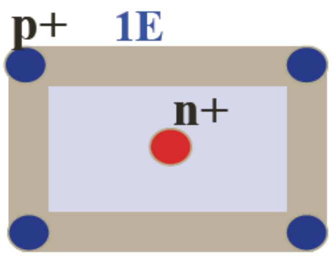
4GeV positrons at DESY



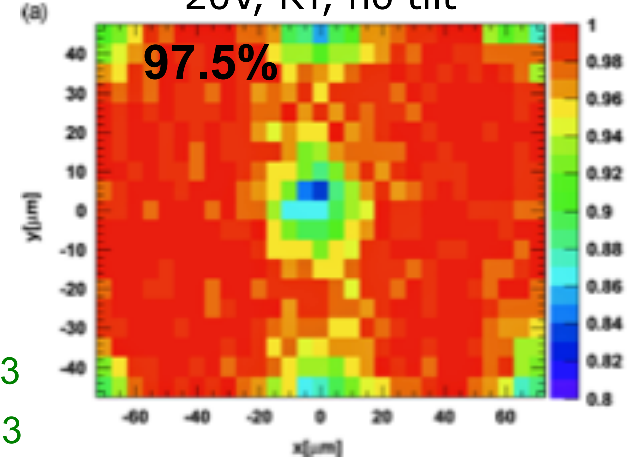
Functional tests (2): CMS

- Tests performed by with PSI46v2 ROC (laboratory and beam tests)
- Mostly on sensors from an earlier FBK batch (lower quality)
- Feature higher noise and higher threshold wrt FE-I4





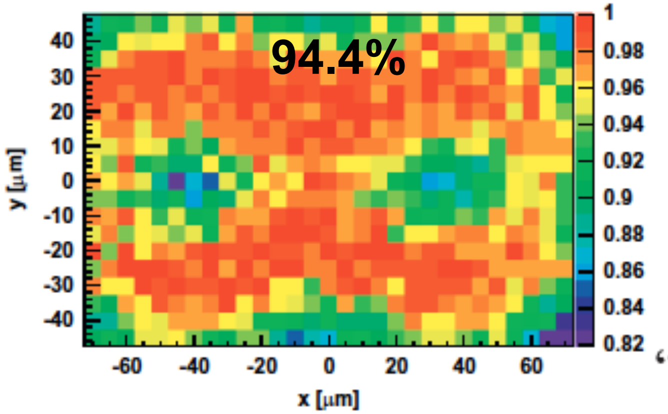
Before irrad.,
20V, RT, no tilt



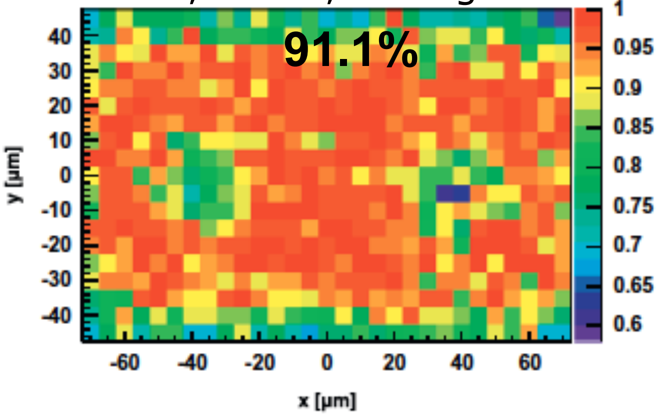
M. Obertino, et al., NIMA 730 (2013) 33

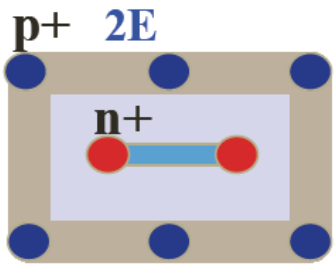
E. Alagoz et al. JINST 7 (2012) P08023

Before irrad.,
5V, RT, 0° angle



After irrad., 7E14 n_{eq}/cm^2
30V, -20°C, 0° angle





M. Bubna, et al.,
NIMA 732 (2013) 52

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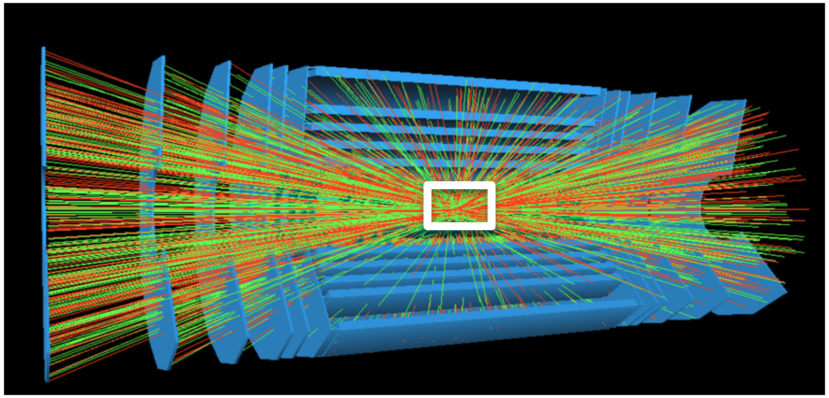
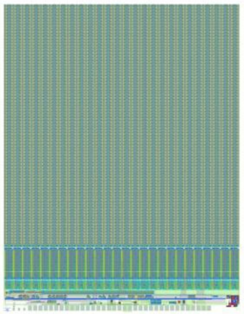
Pixel Roadmap LHC → HL-LHC

N. Wermes, TN workshop 2014 in Genova



Increased luminosity requires

- higher hit-rate capability
- increased granularity
- higher radiation tolerance
- reduced material budget

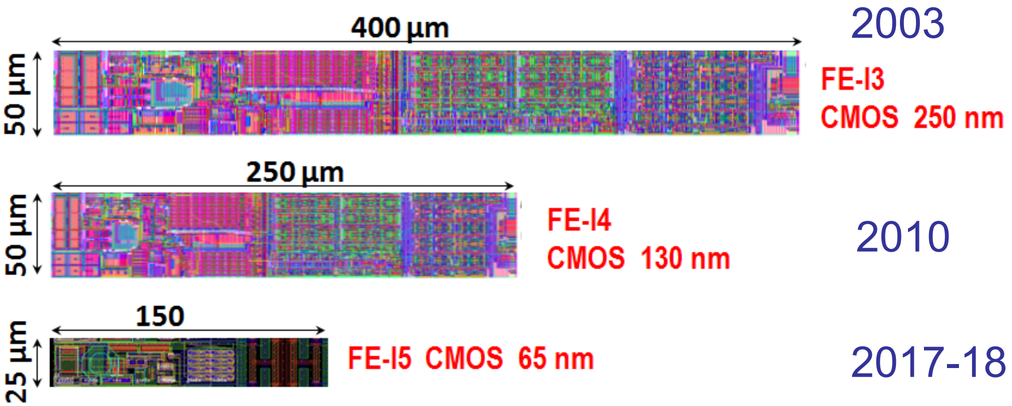


CMS Pixels for LHC & LHC Phase I:

- PSI46dig
- Tech: 250 nm
- Size: 100 x 150 μm^2

G. Darbo, CSN5-ACTIVE, 2013

ATLAS roadmap → Pixel Size



Technology roadmap →

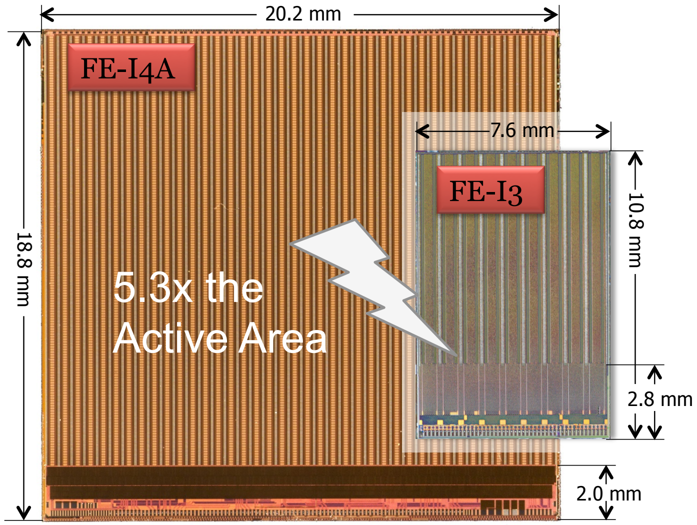
5x Chip Size

½ threshold

20x TID dose

20x NIEL

6x event pile-up



3D pixels are an option for inner layers

Implications for new 3D pixels

- Smaller pixel size (e.g., 150 x 25 μm^2) requires thinner sensors (or at least the collecting charge thickness) to take advantage of the high-pixel spatial resolution avoiding too large cluster sizes.
- Radiation hardness after $2x10^{16}$ n_{eq}/cm^2 requires smaller inter-electrode spacings, and reduced material budget calls for very slim or active edges

→ Need for higher column density and bump density

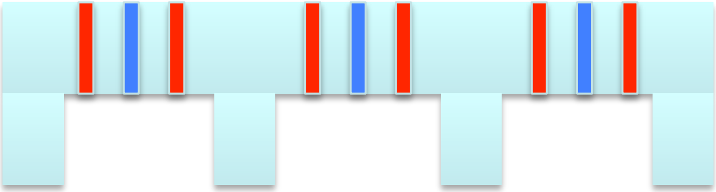
→ Narrower electrodes are necessary for higher geometrical efficiency and lower capacitance (and can be achieved with thinner substrates, given a ~constant aspect ratio with DRIE)

→ Narrower electrodes help with electrode (at least partial) filling with poly-Si to obtain some efficiency and to ease fabrication.

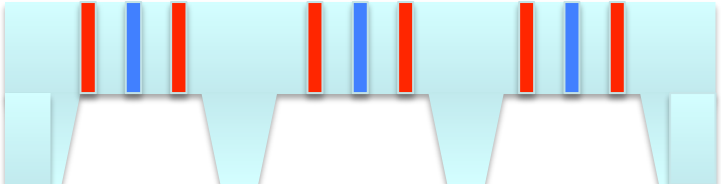
Are thin double-sided 3D feasible ?

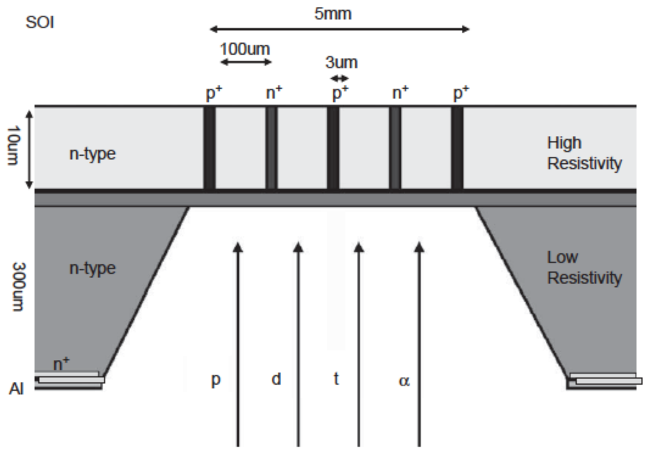
- Processing with ~150 μm thick 6” wafers not possible
- Processing thicker wafers with local thinning of sensor active areas by DRIE (1) or TMAH (2) could be an option

(1)



(2)



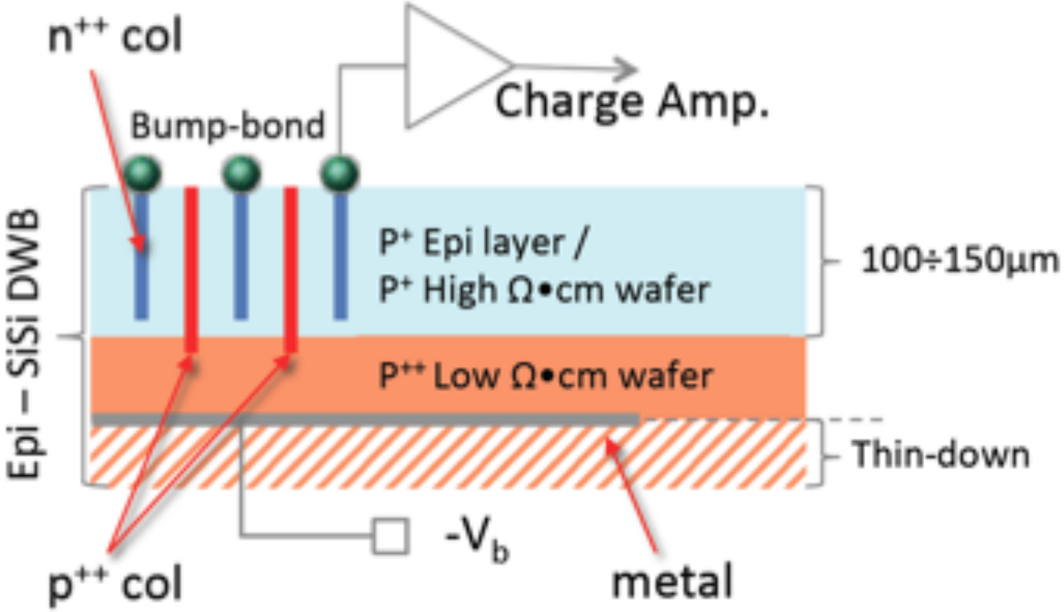


- Advantages: exploit the experience with double-sided processing, no support wafer (bonding and removal), easy sensor bias from the back-side
- Disadvantages: mechanical fragility (yield), processing on deep-etched regions, active edge not feasible

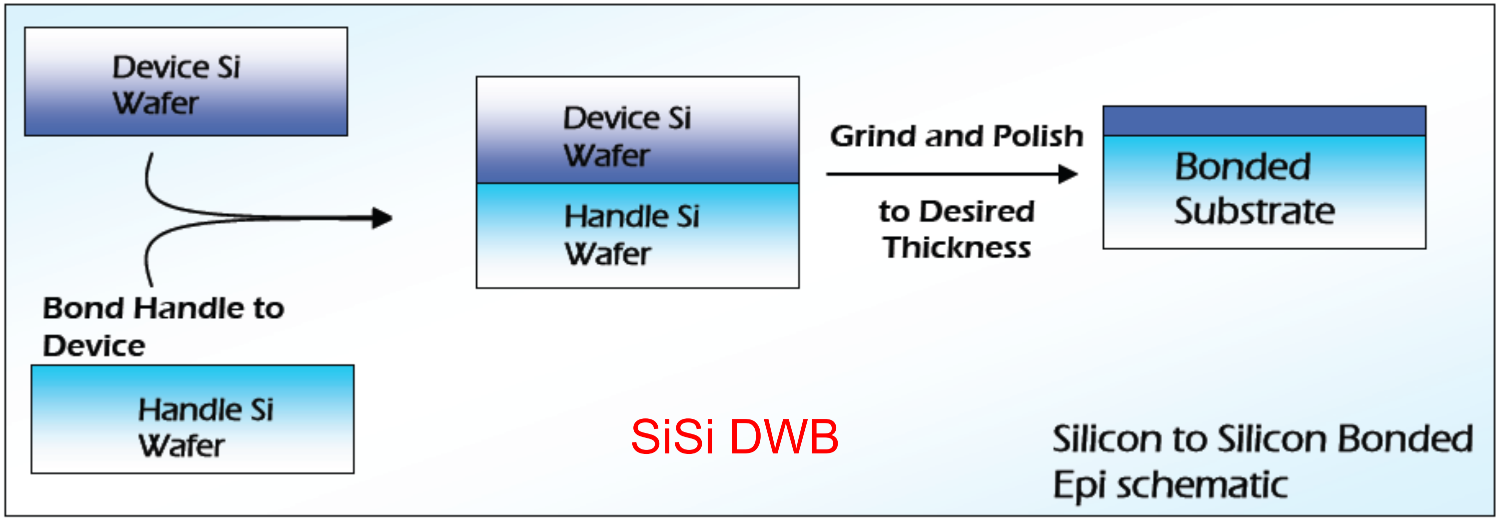
- Ultra Thin 3D’s (for plasma diagnostics at Tokamaks) processed with a similar approach at CNM (SOI+ SS process + TMAH) had 1cm^2 area

G. Pellegrini et al., NIMA 604 (2009) 115

Proposed fabrication approach



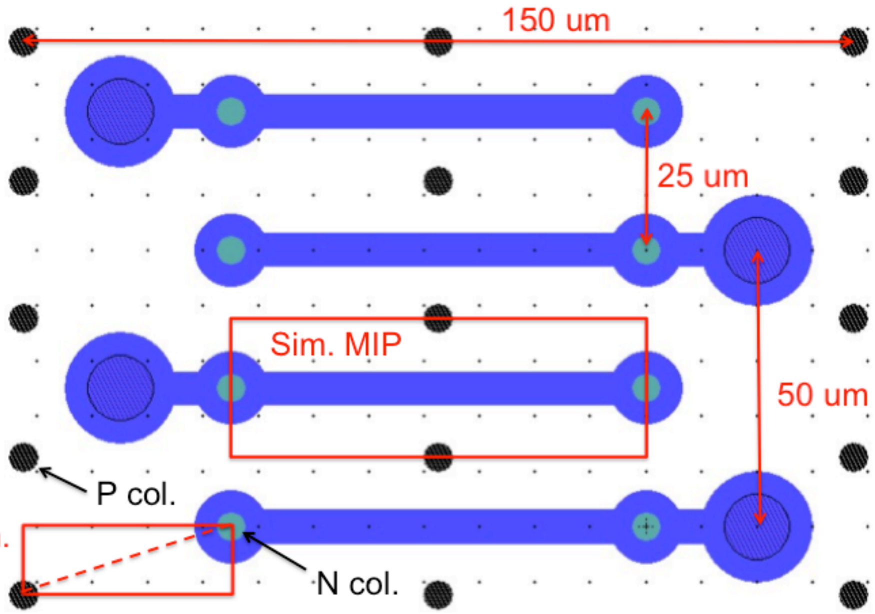
- Single-sided process with support wafer
  a) Epi or SiSi DWB
  b) SOI
- Support wafer thinning (removal) and back-side metal deposition proved but need to be engineered

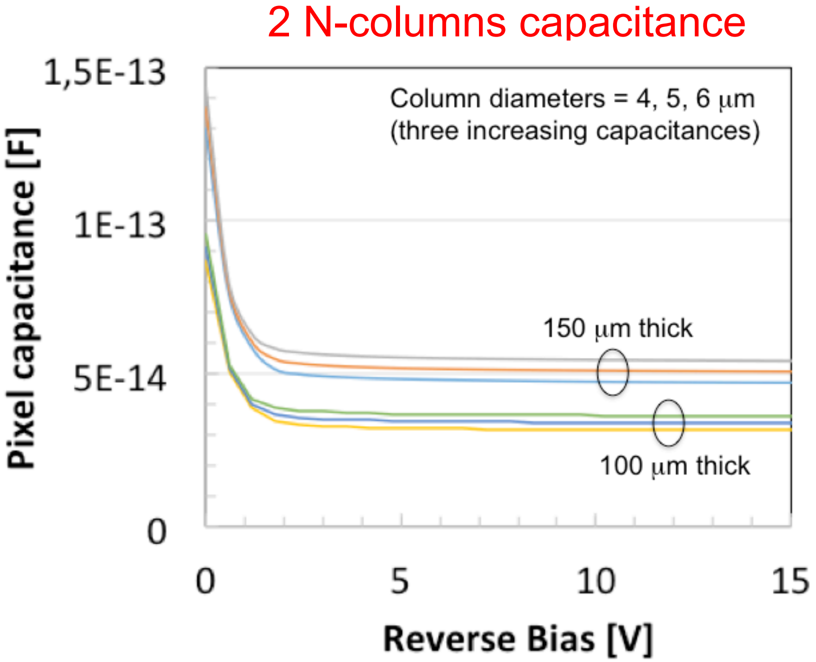


SiSi DWB

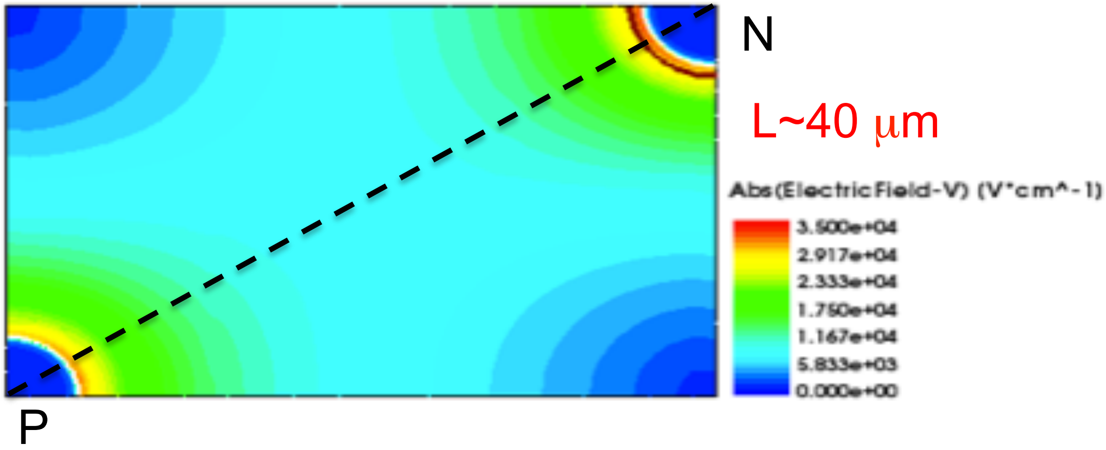
Silicon to Silicon Bonded Epi schematic

Layout and TCAD simulations (1)





Electric field distribution at 50V



\+ Additional surface contributions:

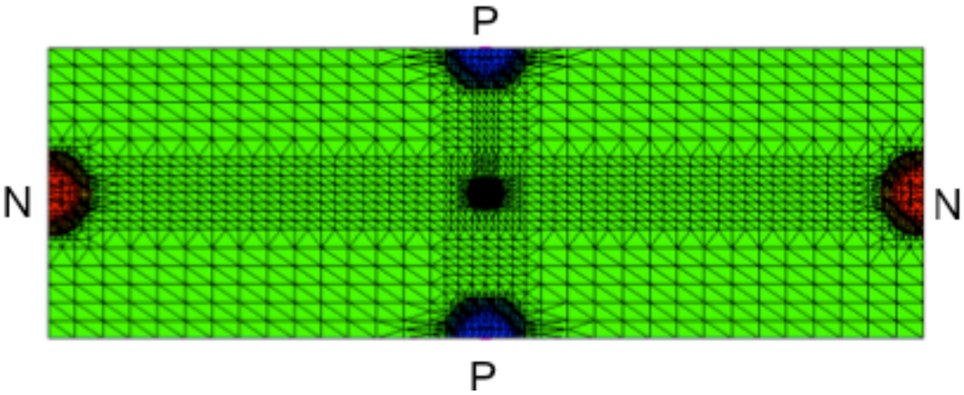
1) N-columns to p-spray (5 fF)
2) Metals (connection, field-plates, bump pad) (32 fF)

Total capacitances for d=5 µm:

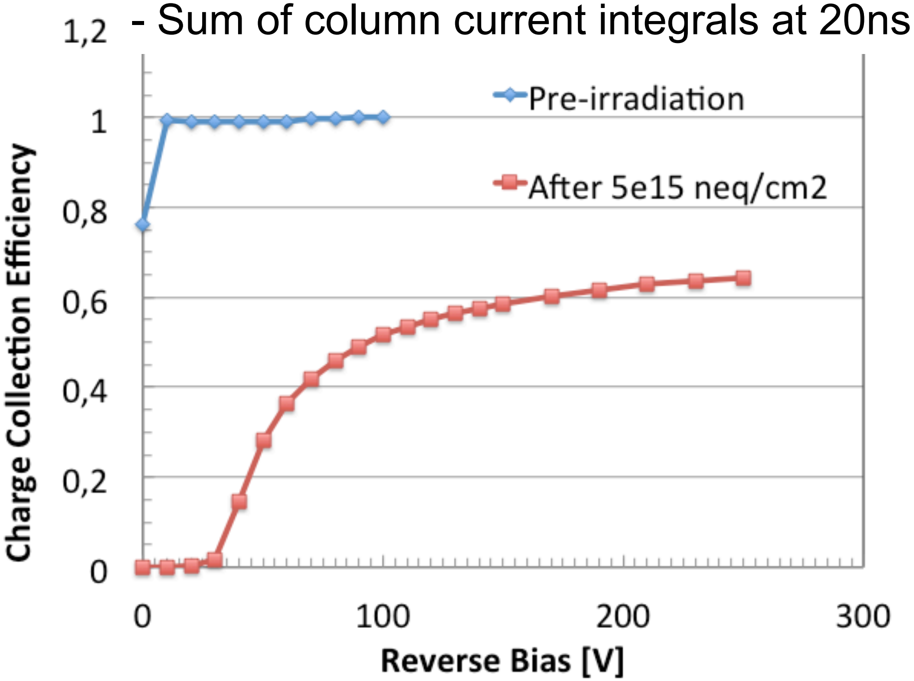
- 100 µm thick → 71 fF/pixel
- 150 µm thick → 88 fF/pixel

(it was ~200fF for IBL 3D pixels)

TCAD simulations (2)



- MIP impinging in null-field point
- Sum of column current integrals at 20ns



- From tests on existing 3D strips (L~56 μm), the signal efficiency at 2×10^{16} n_{eq}/cm^2 was found to range from 30% to 40%, in agreement with geometrical considerations

- The expected MPV of signal for L~40 μm at 2×10^{16} n_{eq}/cm^2 is:
- 100 μm thick → 2500 – 3200 e^-
- 150 μm thick → 4000 – 5000 e^-

- Sensor thickness will have to be optimized depending on the signal/ threshold ratio

Proposed 3-year R&D plan (1)

GOAL

- Fabrication of new thin 3D pixel sensors on 6” wafers at FBK
  - Technology and design to be optimized and qualified for extreme radiation hardness (2x10^{16} n_{eq}/cm^2)
  - Pixel designs compatible with present (for testing) and future (65nm) FE chips of ATLAS and CMS

STRATEGY

- Preliminary “technological tests”
  - check the feasibility of the most critical process steps (e.g., narrow column DRIE)
  - one batch of planar sensors to check the raw wafer quality
- Two 3D sensor batches fabricated and fully tested

Proposed 3-year R&D plan (2)

Year	Deliverables
2014	DRIE technological tests Planar test batch fabricated and tested 3D simulation and design (1st submission)
2015	First 3D batch fabricated and tested Back-end steps (thinning and BS metal) on some wafers 3D simulation and design (2nd submission)
2016	Second 3D batch fabricated and tested Back-end steps (thinning and BS metal) optimized

Most critical issues

- Process sensitivity to defects (→yield) in case of high column densities
- Back-end steps (support wafer thinning/removal and BS metal) still to be engineered and properly combined with interconnect processes.

Proposed 3-year R&D plan (3)

INVOLVED INFN GROUPS

- ATLAS: TN, GE, MI, CS, UD
- CMS: TO, MIB, PG, FI, PI, BA

INTERNATIONAL COLLABORATIONS

- Former ATLAS 3D Collaboration being re-organized and extended to CMS groups

ADDITIONAL FUNDING

- 3D Pixel activities proposed to AIDA2
- ERC (individual) proposals being submitted
- Others ?

Conclusions

- Very impressive progress has been achieved in 3D detectors in the past few years, boosted by the ATLAS IBL, including demonstration of medium volume productions

- 3-years R&D proposed to push 3D pixel technology towards HL-LHC requirements

- An ATLAS-CMS synergy can give a unique opportunity for technical leadership in the most demanding inner-most layers of HL-LHC detectors

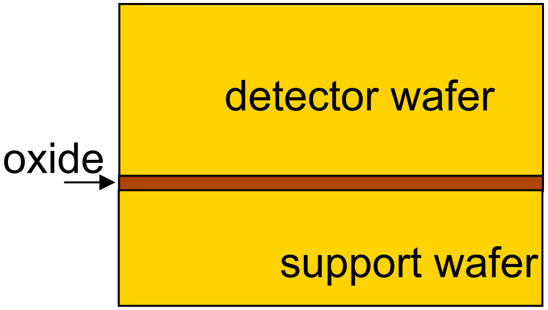
- Tight partnership with FBK is an added value

Back-up slides

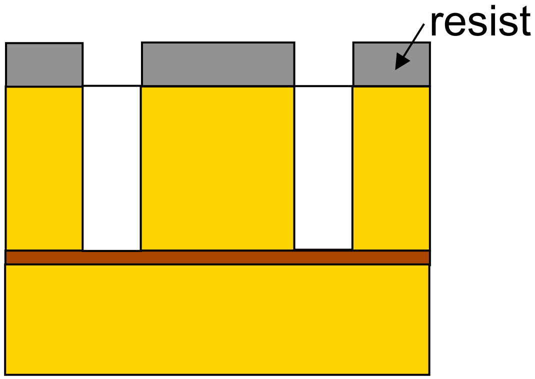
Full 3D with active edge

3D CONSORTIUM
The Stanford Nanofabrication Facility
SINTEF

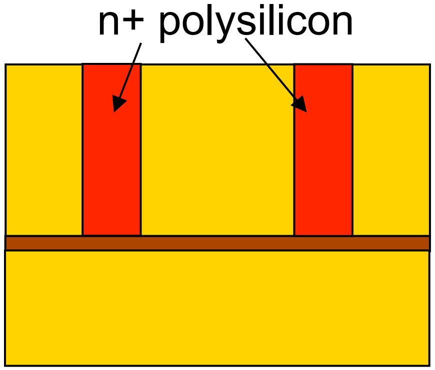
C. Kenney et al., IEEE TNS, vol. 46, n. 4 (1999) 1224
T.E. Hansen et al., JINST 4 (2009) P03010



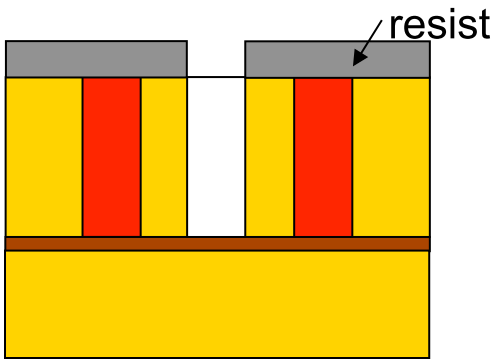
1) wafer bonding



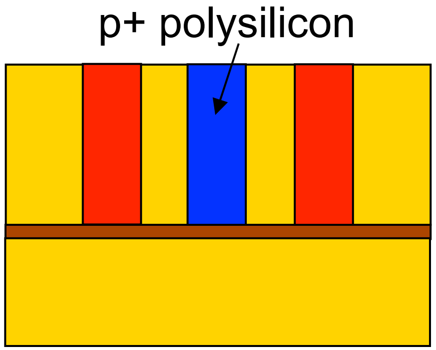
2) n+ hole definition and etching



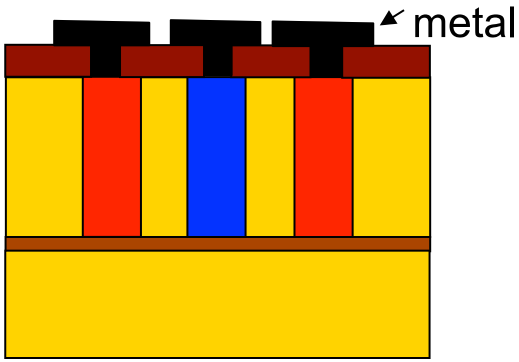
3) hole doping and filling



4) p+ hole definition and etching



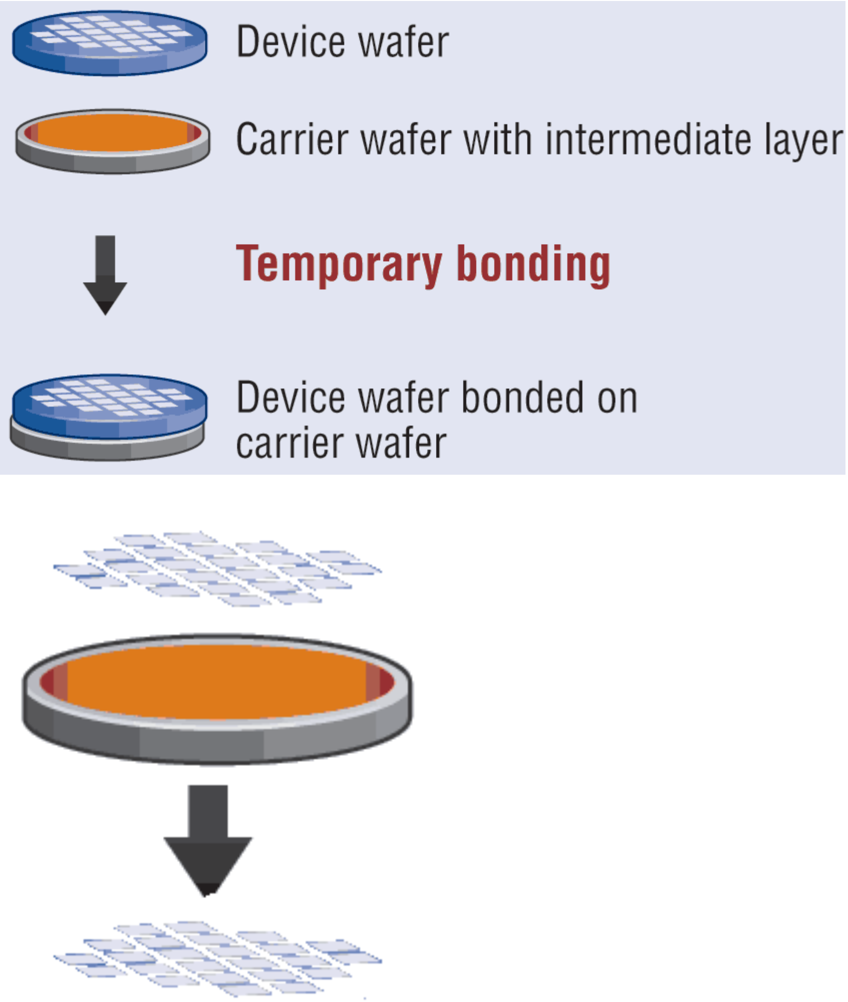
5) hole doping and filling



6) Metal deposition and definition

Reversible Wafer Bonding from Brewer Science performed at SINTEF

Slide from A. Kok (SINTEF) and C. Da Via (Manchester)



Device wafer

Carrier wafer with intermediate layer

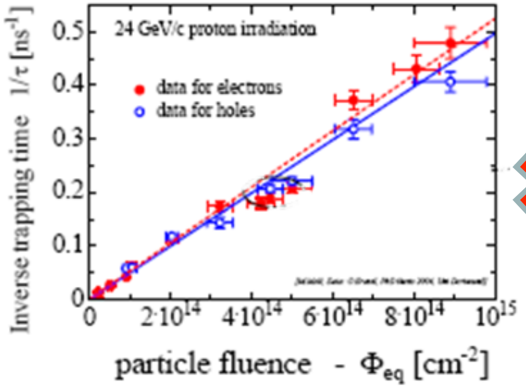
Temporary bonding

Device wafer bonded on carrier wafer

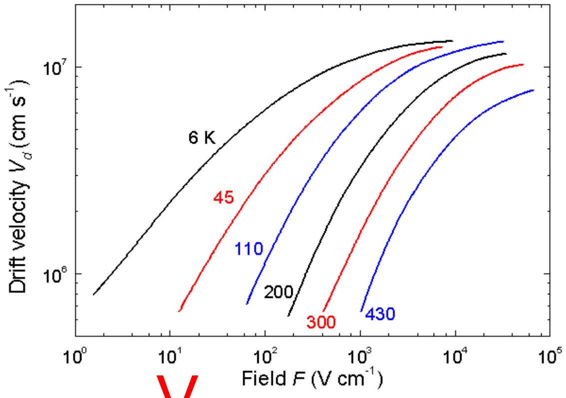
- Detach devices from carrier wafer using Wafer Bond Clean (several hours to a day of immersion), follow by a isopropanol clean
- Individually picked up by tweezers
- 500 devices one wafer takes one hour of manual work
- This method tested on dummy wafers and wafers containing full 3D active edge sensors
- Tests so far promising

Work supported by ATLASUK Manchester, and Purdue University, US

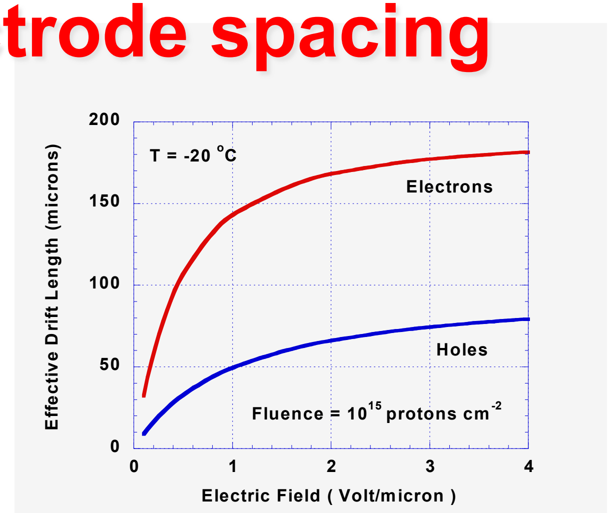
Charge trapping and inter-electrode spacing



τ_{tr} Trapping Times



V_n Drift Velocity



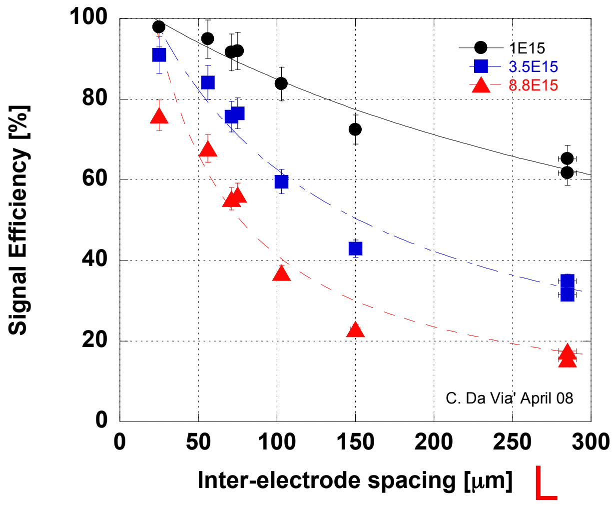
λ Effective drift length

$$\frac{dS}{dt} = q\frac{dV_W}{dx}\frac{dx}{dt}\exp\left(-\frac{x}{\lambda}\right)$$

$$S = \frac{\lambda}{L}\left[1-\exp\left(-\frac{L}{\lambda}\right)\right]$$

Expected signal efficiency after irradiation (without multiplication) depends on λ/L

$$SE = \frac{1}{1+0.6L\frac{K_\tau}{v_D}\Phi}$$

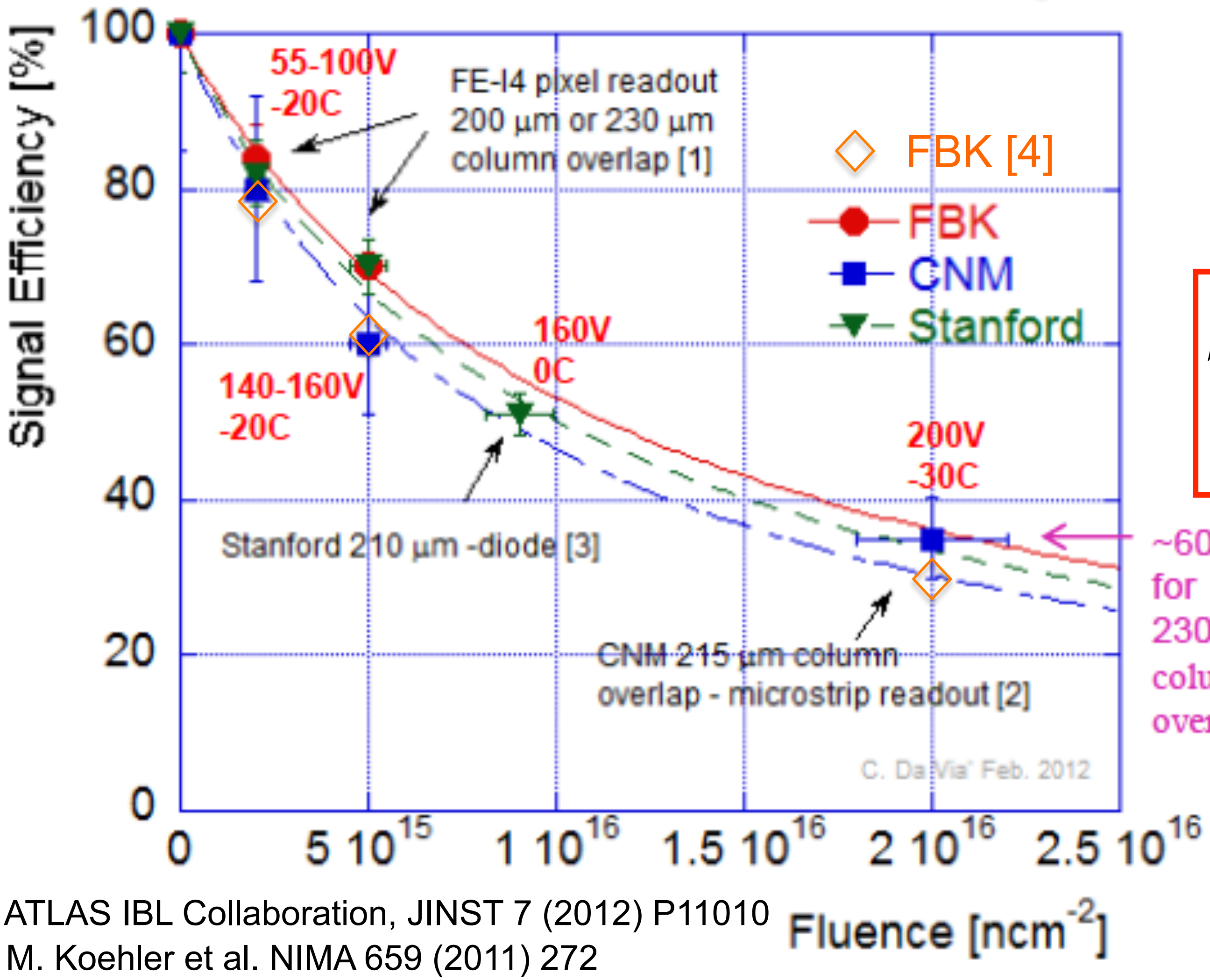


L

Trapping times from G. Kramberger et al, NIMA 481 (2002) 100, NIMA 501 (2003) 138

Calculations from C. Da Via, NIMA 603 (2009) 319

Performance comparison



~6000e- for 230µm column overlap

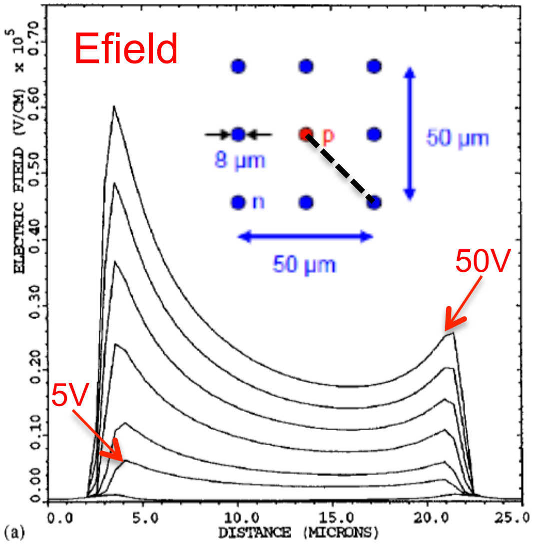
Signal Efficiency =
Ratio of max. signal
after irradiation
and before irradiation

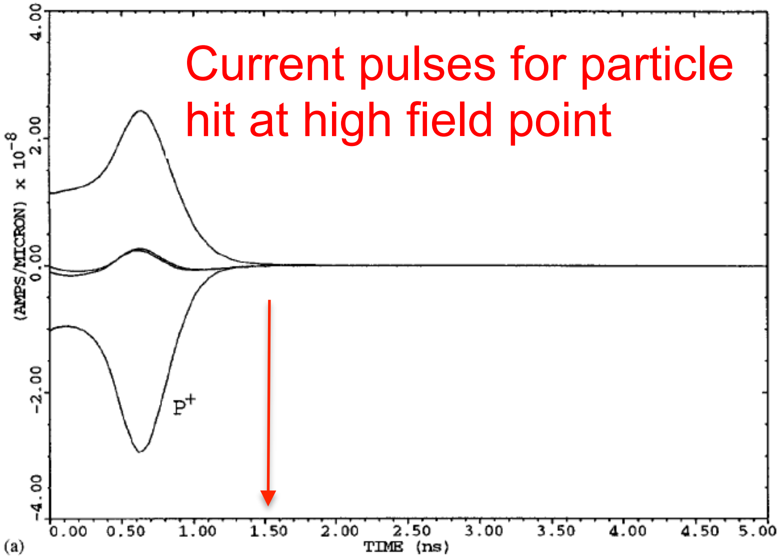
$$SE = \frac{1}{1 + 0.6 L \frac{K_\tau}{v_D} \Phi}$$

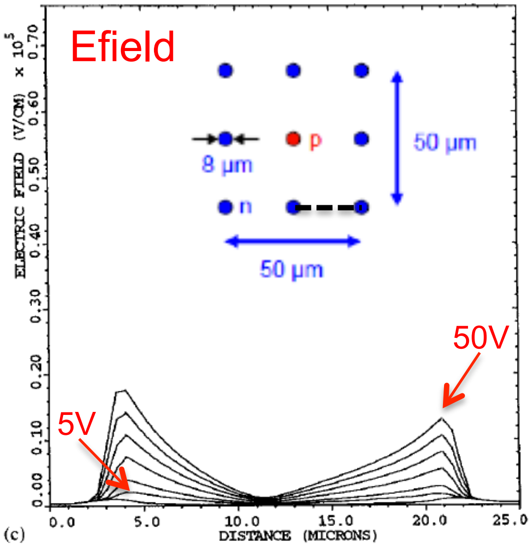
[1] ATLAS IBL Collaboration, JINST 7 (2012) P11010
[2] M. Koehler et al. NIMA 659 (2011) 272
[3] C. Da Via, et al., NIMA 604 (2009) 505
[4] G.-F. Dalla Betta, et al., HSTD9 (2013)

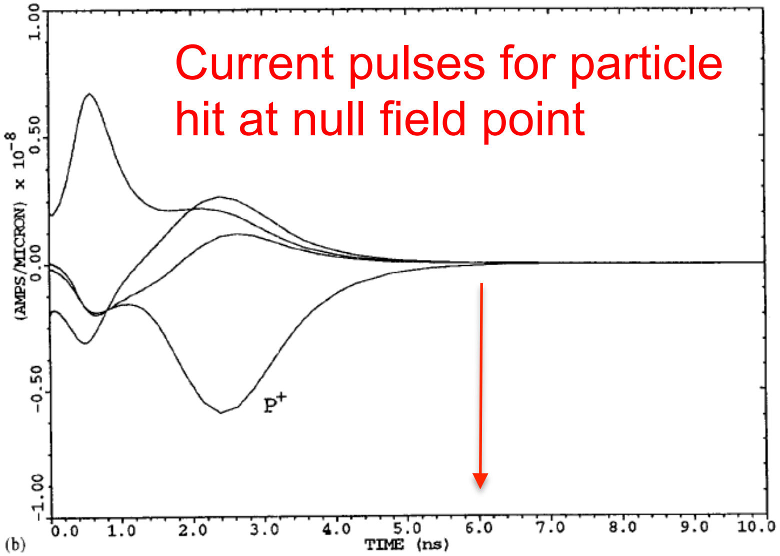
Original Compilation by C. Da Via

Null field points and delayed signals





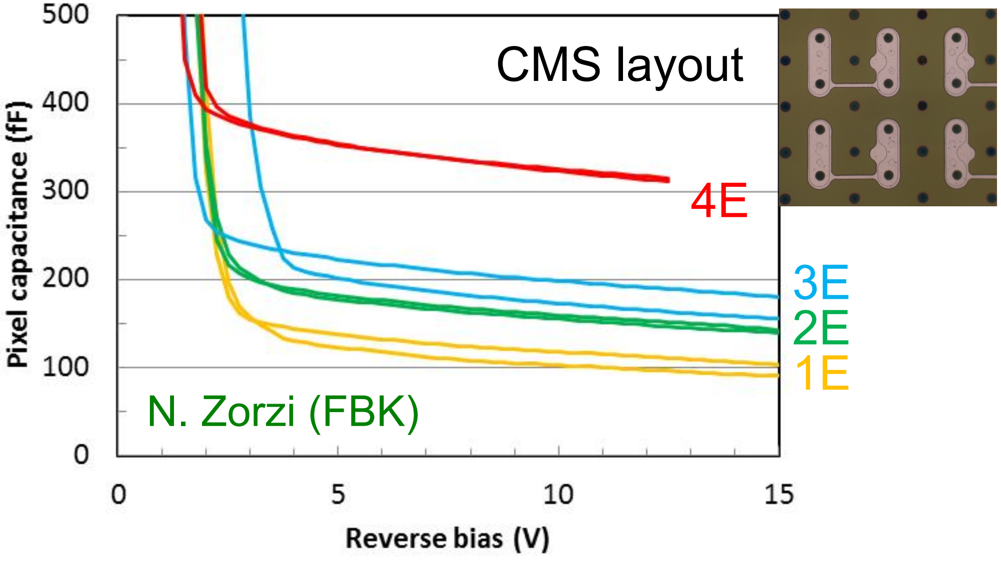




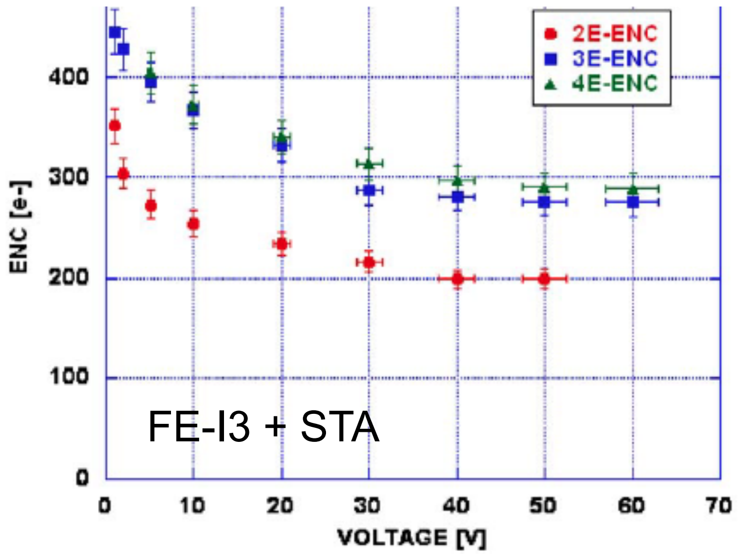
S. Parker et al. NIMA395 (1997) 328

- 3D structure implies null field points in between columnar electrodes of the same doping type
- Carriers generated at null field points first have to diffuse before drifting, thus delaying signals
- This can be improved with trenched electrodes, but at the expense of higher capacitance and reduced geometrical efficiency

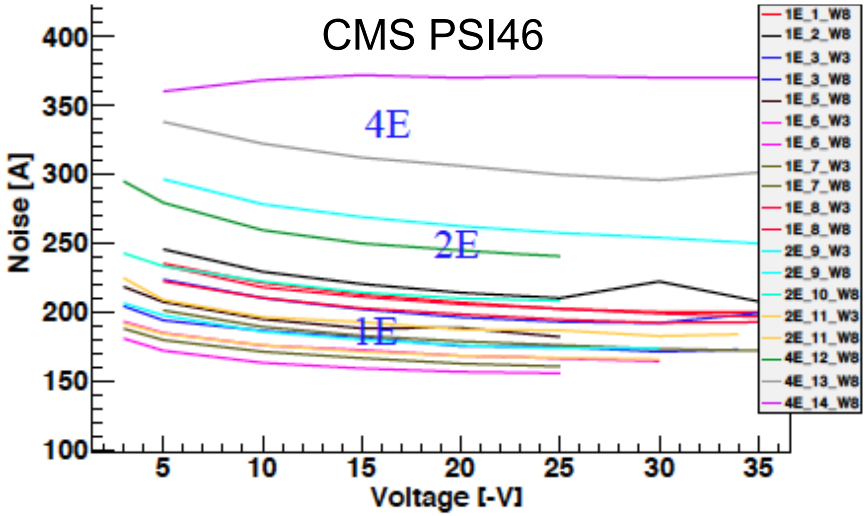
Capacitance and noise

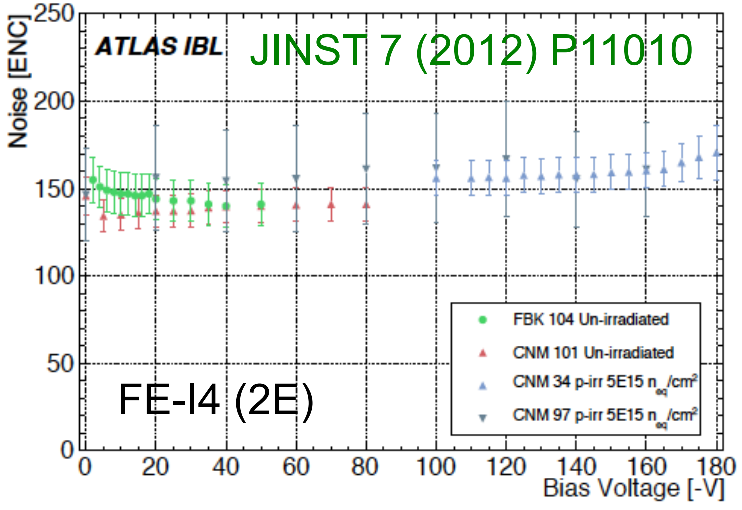


C. Da Via et al. NIMA 604 (2009) 505



E. Alagoz et al. JINST 7 (2012) P08023

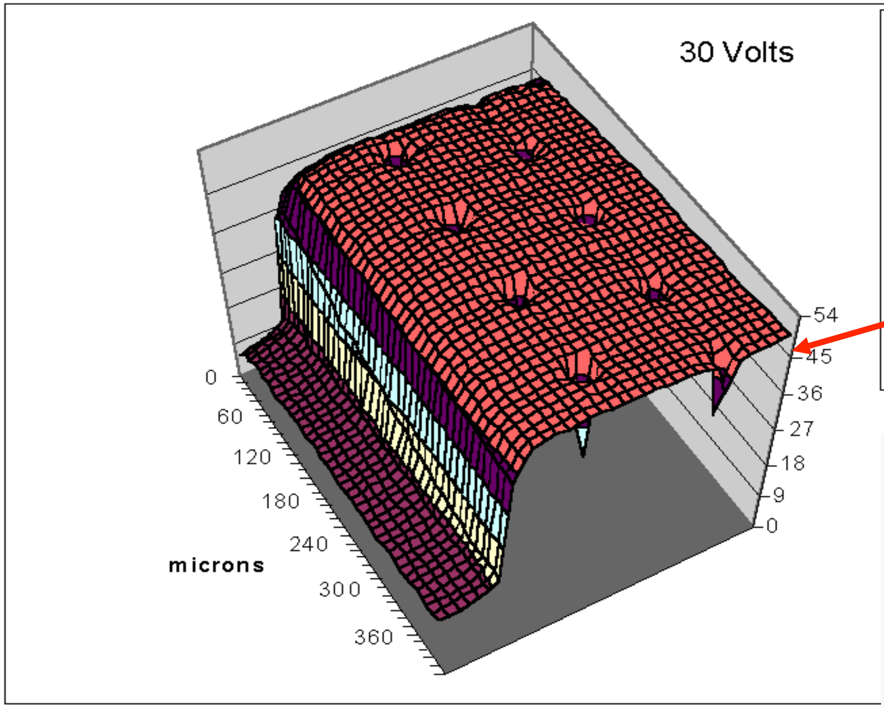


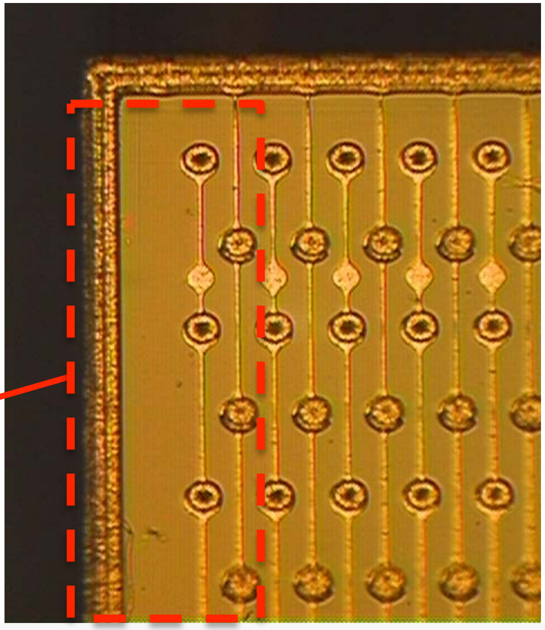


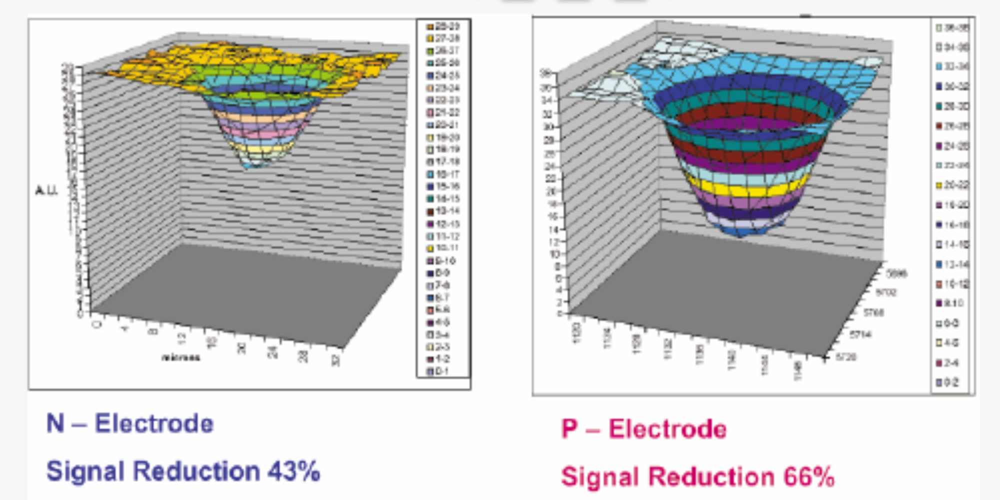
Poly-Si electrode inefficiency

J. Hasi, PhD thesis, Brunel, 2004

Electrode response using 12 keV X-ray beam (ALS at LBNL), beam size ~ 2µm







N – Electrode

Signal Reduction 43%

P – Electrode

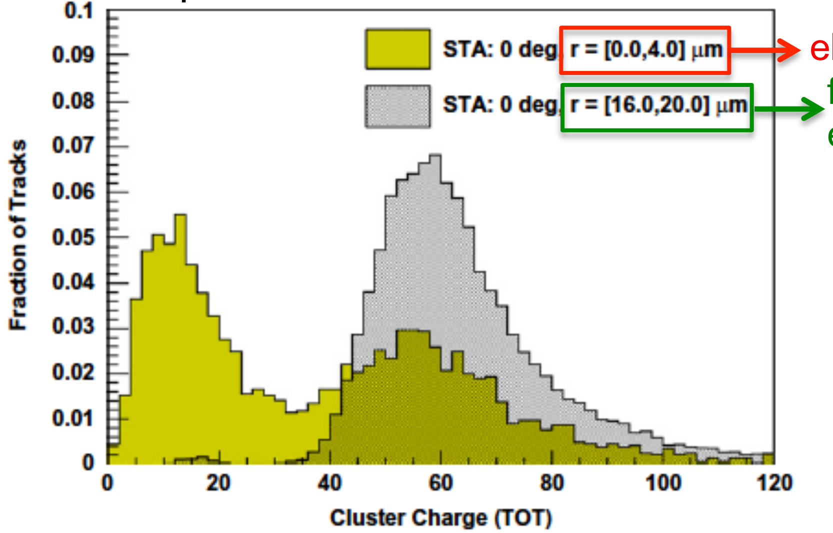
Signal Reduction 66%

- Diffusion, lifetimes (poly-Si grain sizes)
- Oxide barrier effect at the interfaces …
  - → Replace $POCl_3$ with PH_3
  - → Replace BBr_3/O_2 with B_2H_6

Performance in a pion beam test

120 GeV/C pions from CERN SPS

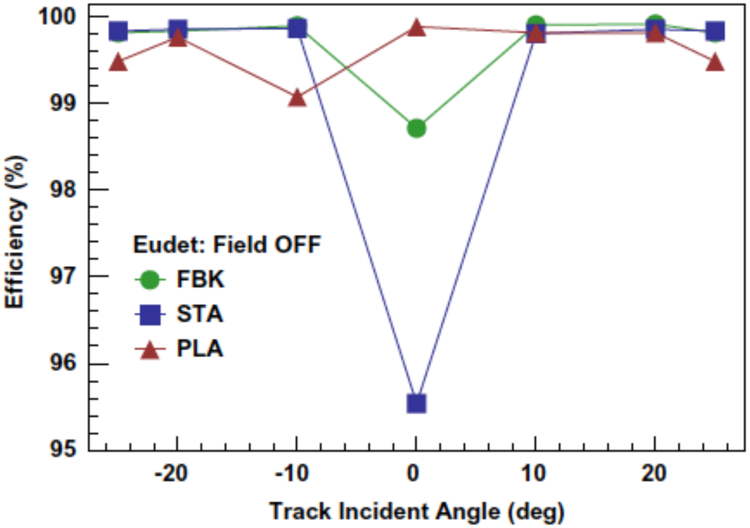
3D pixel FE-I3 assemblies



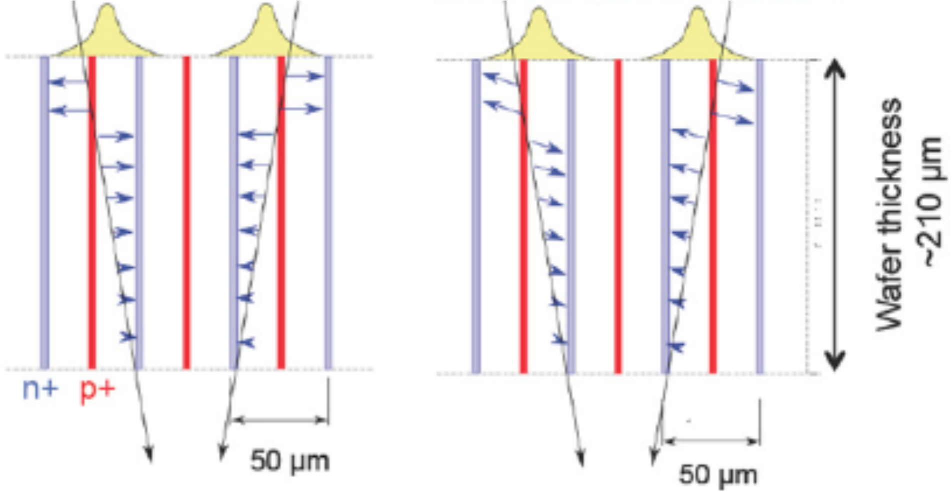
electrode

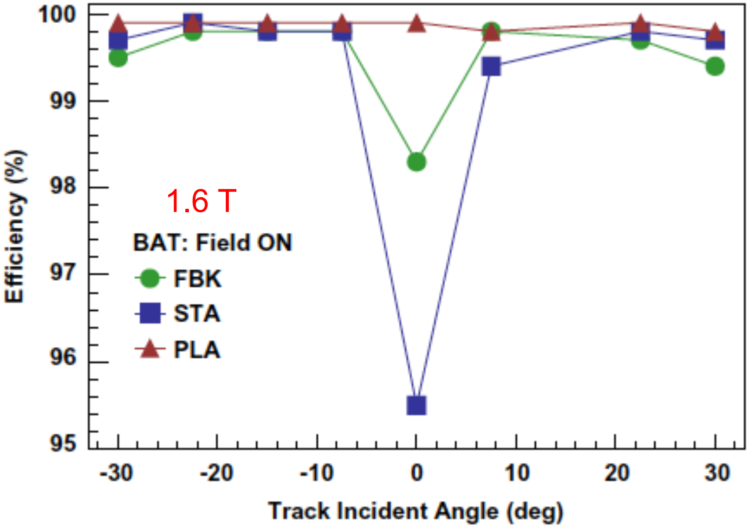
far from electrode

P. Grenier et. al. NIMA 638 (2011) 33



Magnetic field OFF Magnetic field ON



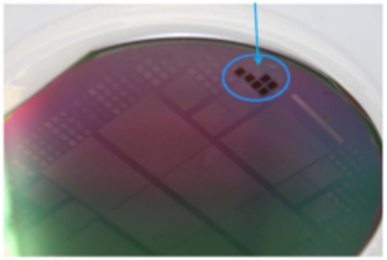


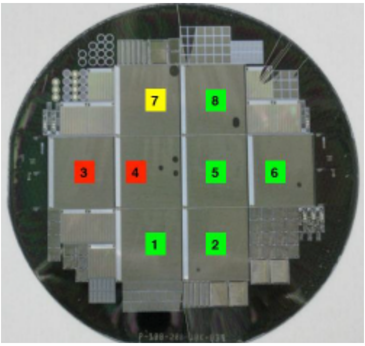
The ATLAS 3D Sensor Collaboration

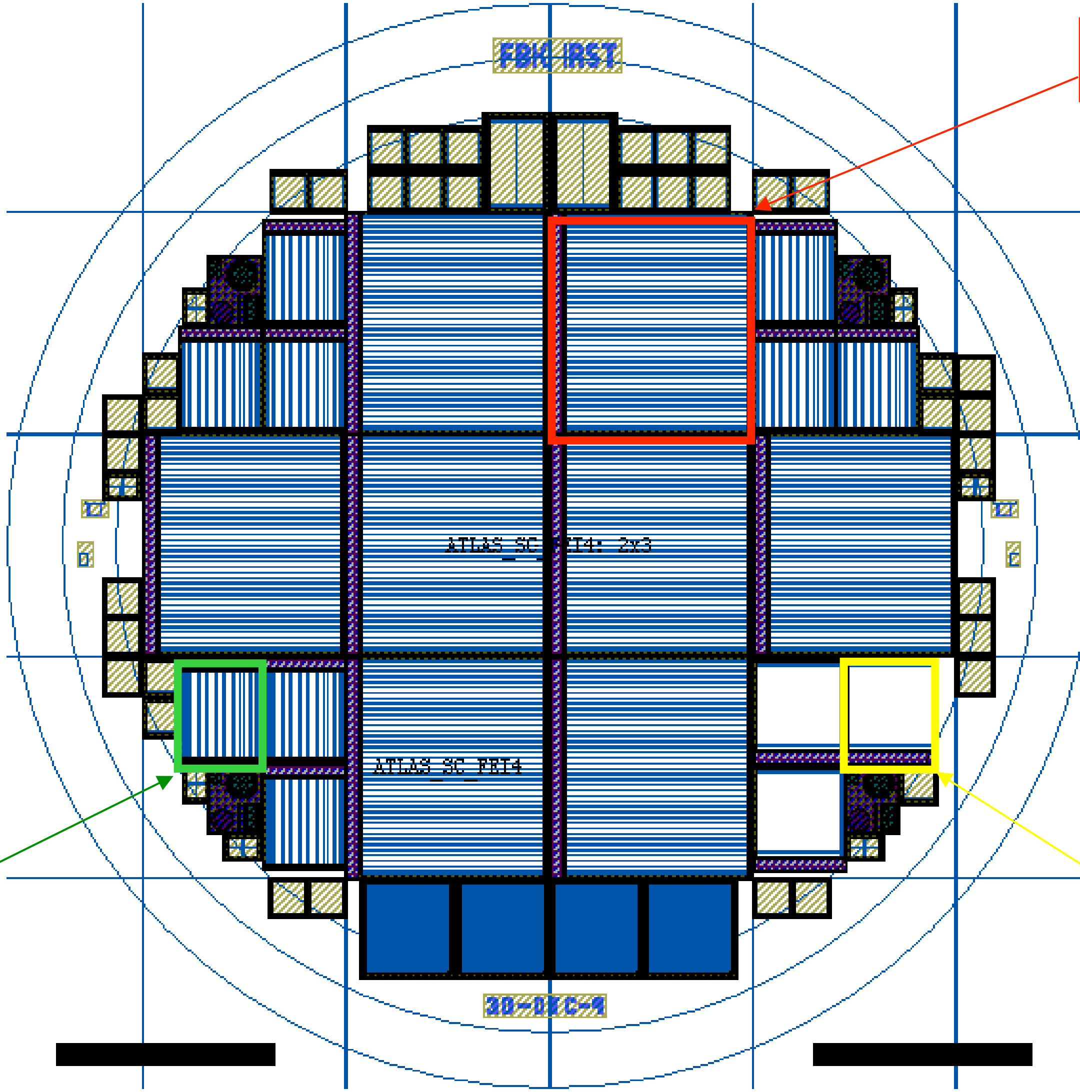
- Approved in 2007 with the goal of "Development, Testing and Industrialization of Full-3D Active-Edge and Modified-3D Silicon Radiation Pixel Sensors with Extreme Radiation Hardness".
- The Collaboration includes 18 Institutions and 4(+1) processing facilities: SNF, SINTEF, CNM, and FBK (VTT joined later).
- Systematic studies on existing 3D samples from different foundries proved comparable performance
- Focus on the ATLAS IBL since 2009

ATLAS 3D common floor-plan

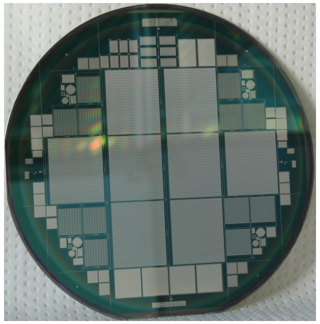
Test structures at the periphery

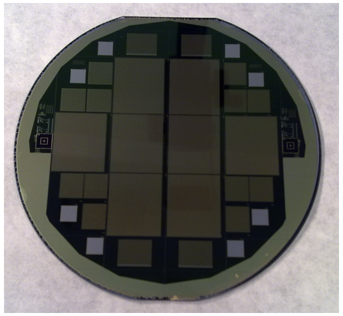






FE-I4 (8x)



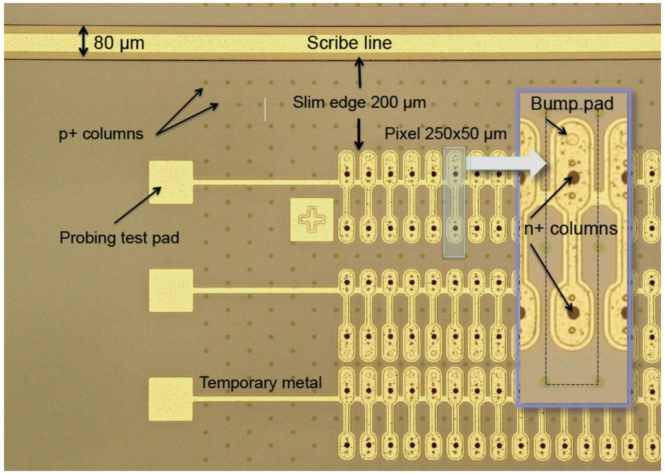


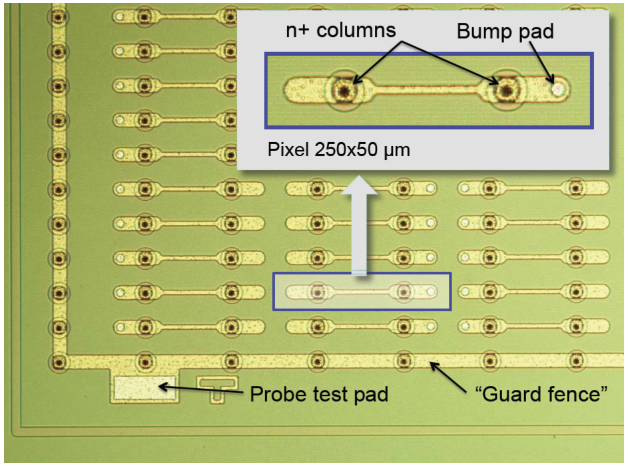
CMS (3x)

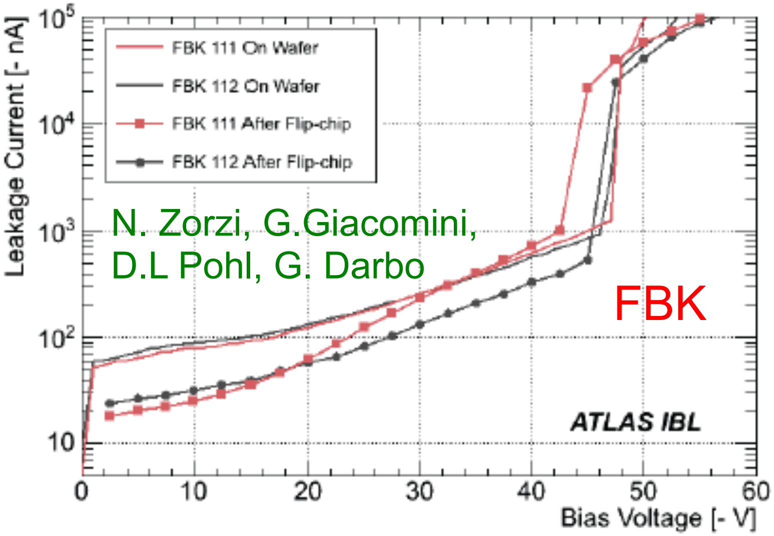
FE-I3 (9x)

Wafer-level electrical tests

The ATLAS IBL Collaboration, "Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip", JINST 7 (2012) P11010.

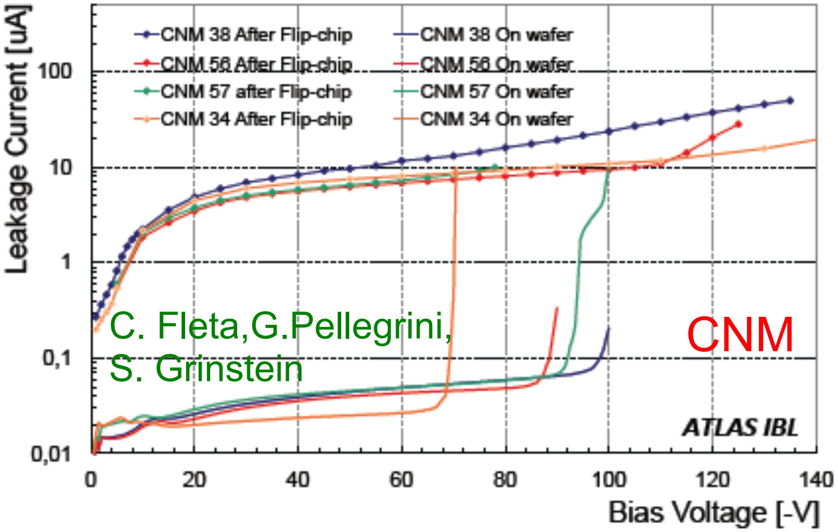






N. Zorzi, G.Giacomini, D.L Pohl, G. Darbo

FBK

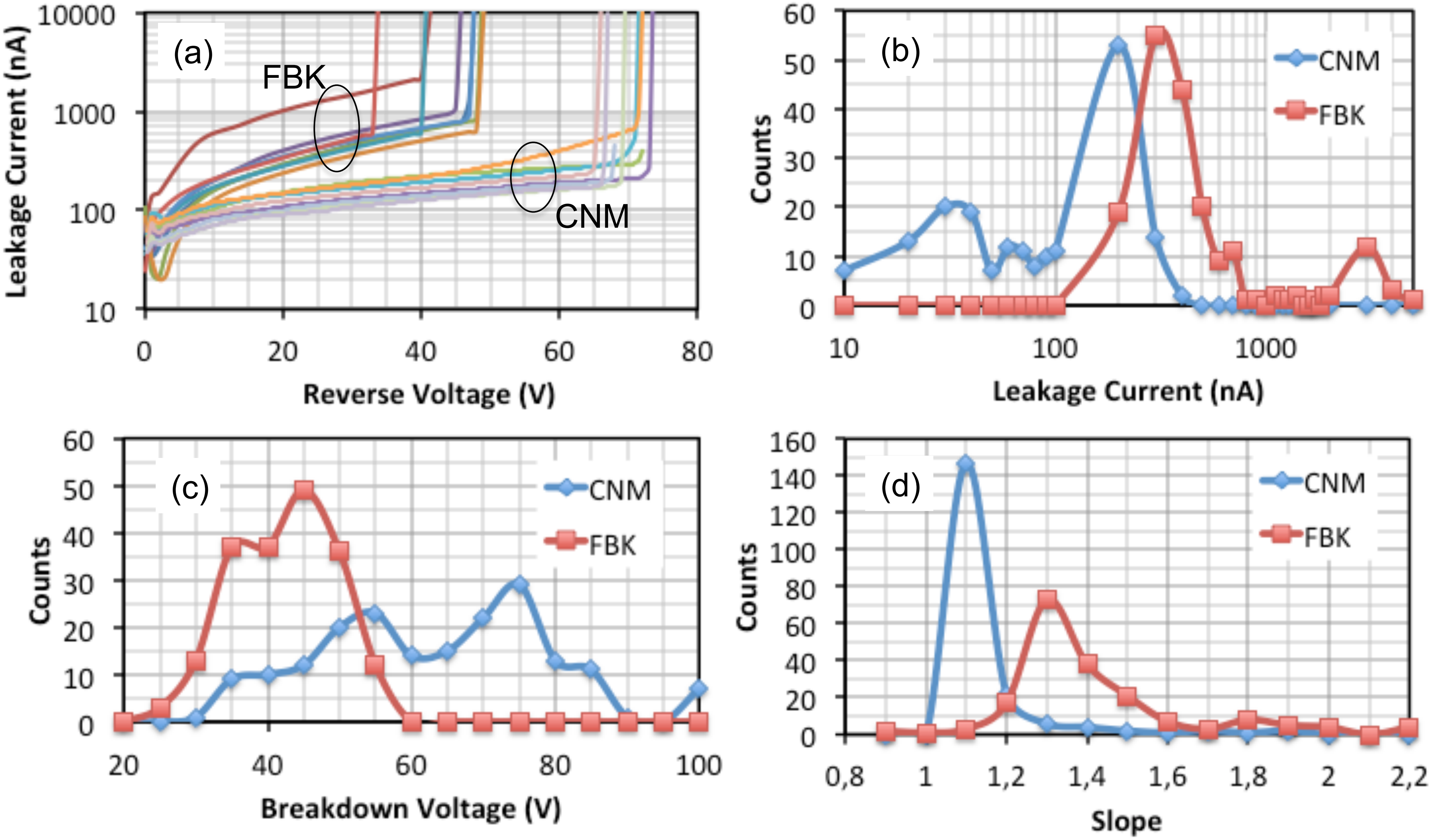


C. Fleta,G.Pellegrini, S. Grinstein

CNM

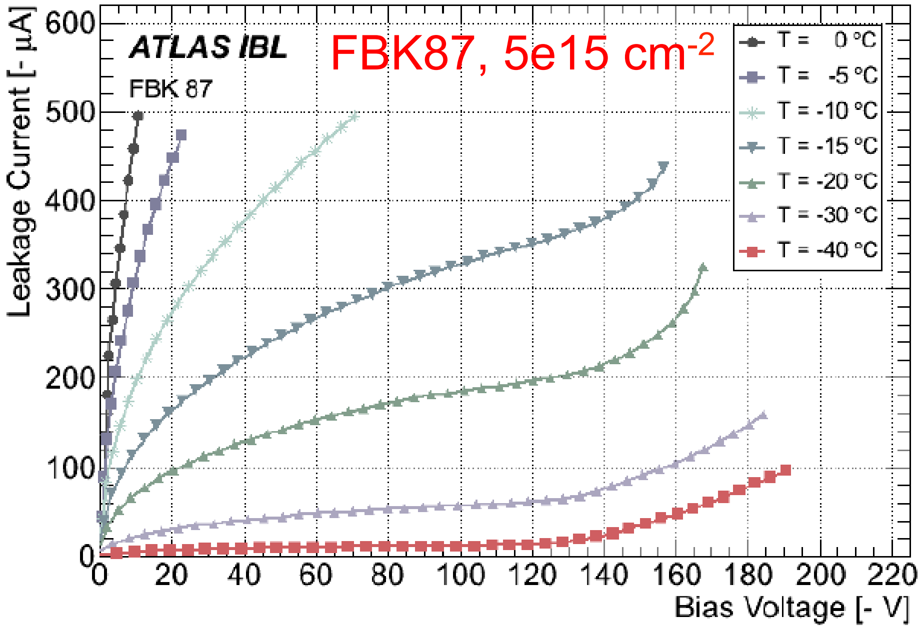
IBL Production Overview

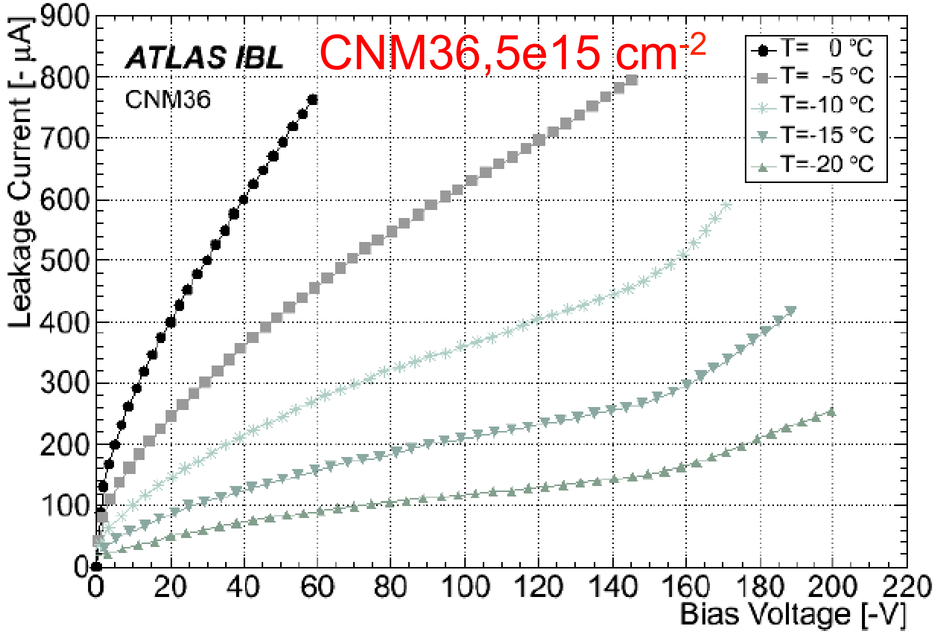
Completed in May 2012, yield on selected wafers ~ 60% (*)



Sensor irradiations

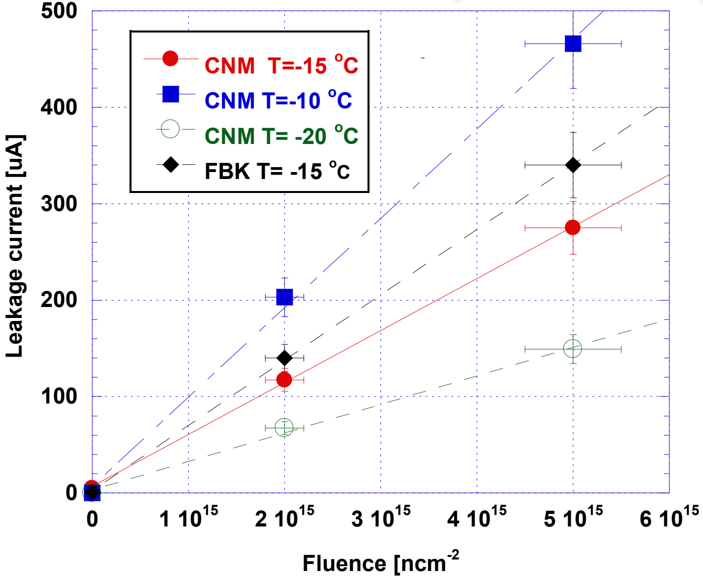
- Several 3D sensors irradiated up to IBL fluence (6E15 n_{eq} cm^{-2})
- Proton irradiation at KIT (beam energy 25 MeV)
  - Estimated TID dose ~ 750Mrad (IBL requirement: 250Mrad)
- Reactor neutron irradiation at Ljubljana
- Annealing: 120min at 60°C for beam tests

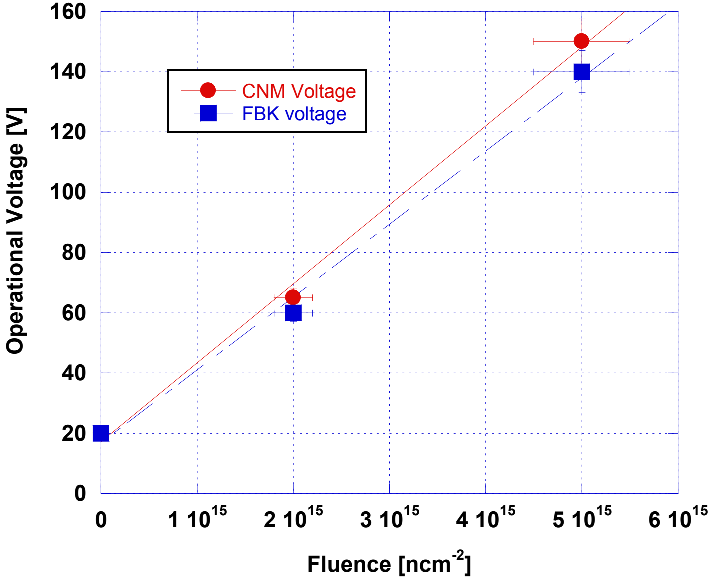


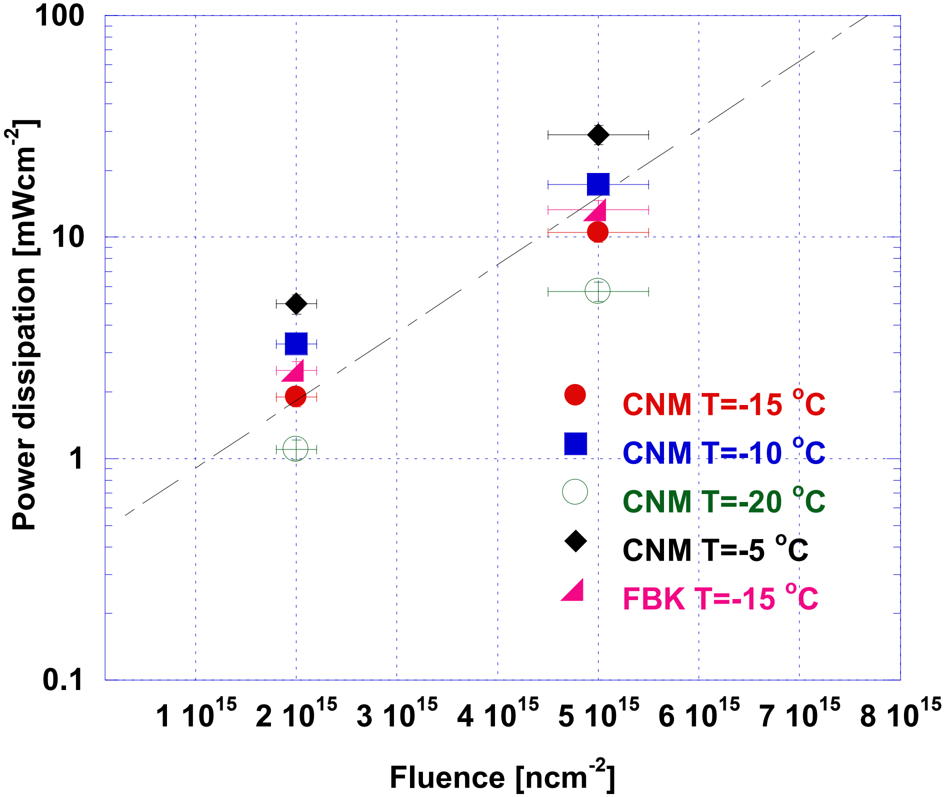


The ATLAS IBL Collaboration, “Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip”, JINST 7 (2012) P11010.

Current, voltage, and power dissipation



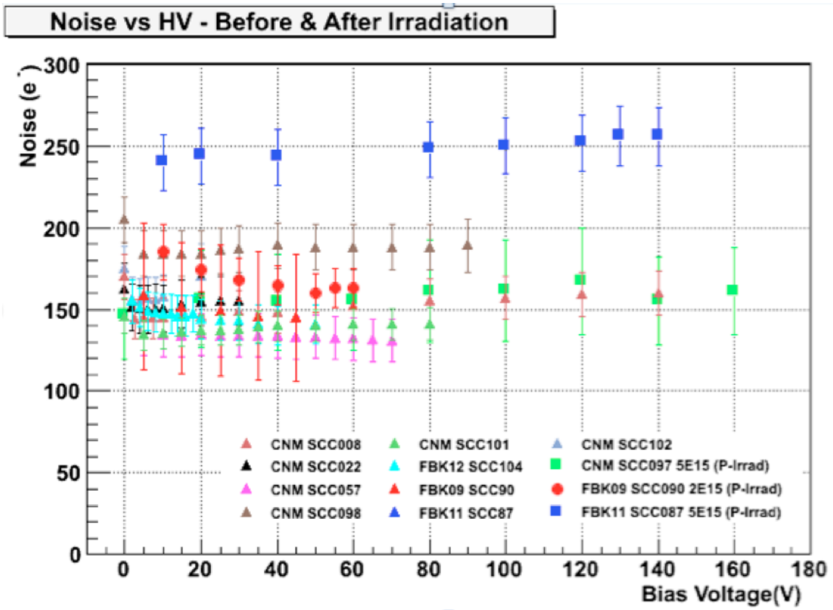




- IBL requirement on sensor power dissipation < 200 mW/cm^2 at 5 x 10^{15} n_{eq}/cm^2 and -15 °C (after annealing)
- ~10X safety margin …

C. Da Via, C. Gemme, A. Micelli, S. Grinstein

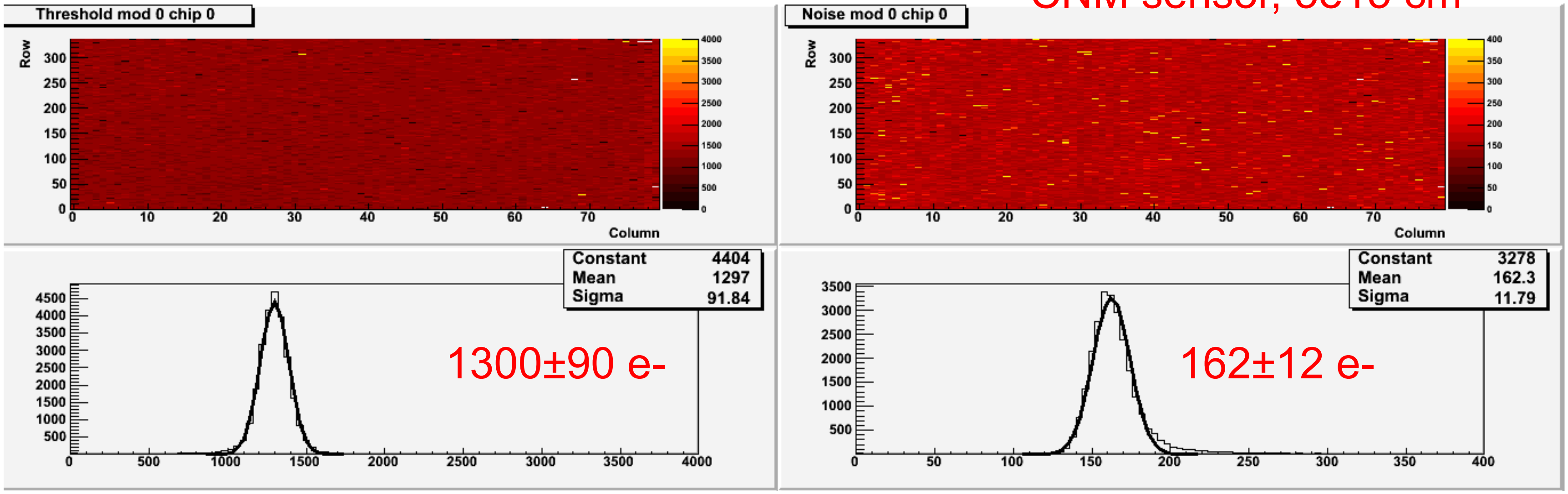
Noise and threshold tuning



C. Gemme, A. Micelli, S. Grinstein, C. Da Via

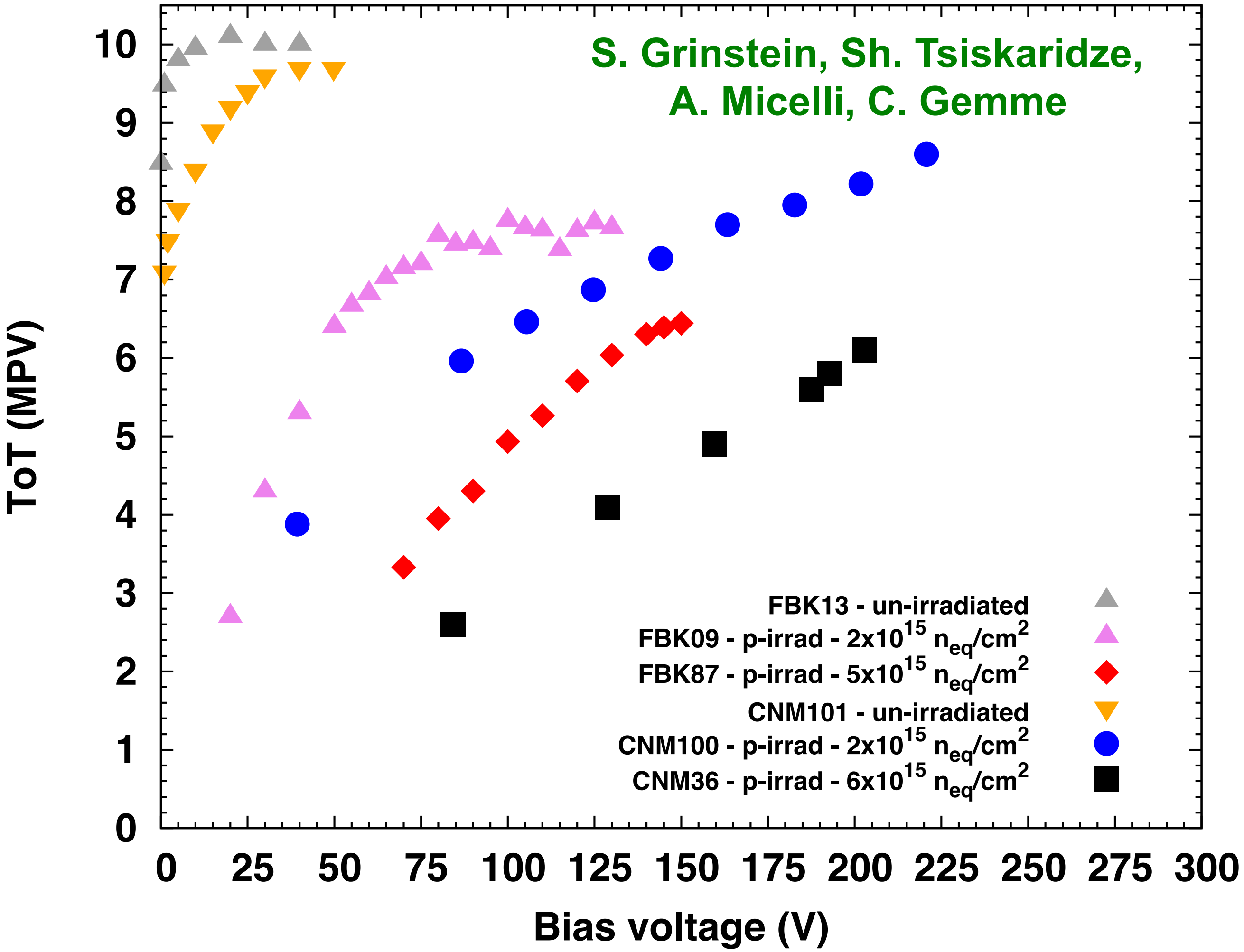
- Noise at acceptable levels in spite of the relatively high 3D sensor capacitance
- Minor changes of noise after irradiation
- Very important for hit efficiency: operation at low threshold with small noise increase is feasible.

CNM sensor, 5e15 cm^{-2}



Charge collection with ^{90}Sr beta source

Data from: ATLAS IBL Collaboration, JINST 7 (2012) P11010
+ S. Grinstein, unpublished results (FBK09)



Summary of CERN beam tests results

The ATLAS IBL Collaboration, "Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip", JINST 7 (2012) P11010.

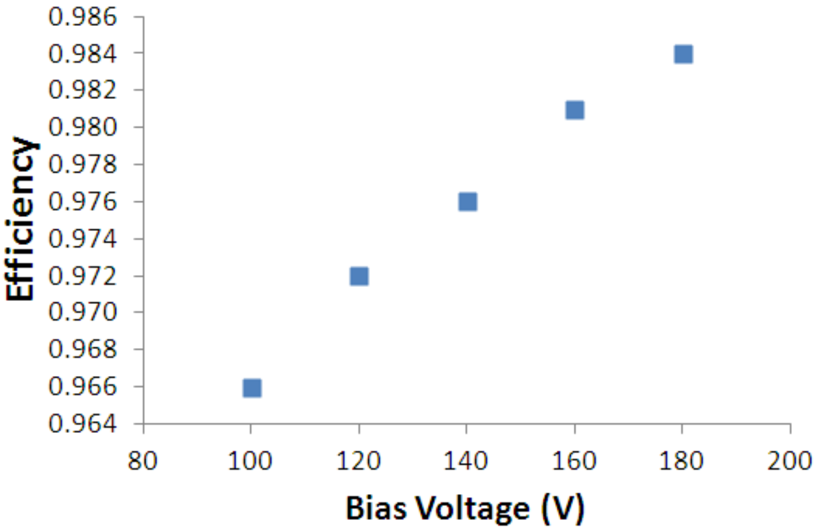
Sensor ID	Bias (V)	Tilt Angle °	Irrad.	Fluence (n_{eq}/cm^2)	Threshold (e-)	Hit Eff. (%)
CNM55	20	0	no	-	1600	99.6
FBK13	20	0	no	-	1500	98.8
CNM34	160	0	25 MeV protons	5×10^{15}	1500	98.1
CNM97	**140**	**15**	**25 MeV protons**	$\mathbf{5\times10^{15}}$	**1800**	**96.6**
CNM34	**160**	**15**	**25 MeV protons**	$\mathbf{5\times10^{15}}$	**1500**	**99.0**
CNM81	160	0	Reactor Neutrons	5×10^{15}	1500	97.5
FBK90	60	15	25 MeV protons	2×10^{15}	3200	99.2
FBK11	**140**	**15**	**25 MeV protons**	$\mathbf{5\times10^{15}}$	**2000**	**95.6**
FBK87	**160**	**15**	**25 MeV protons**	$\mathbf{5\times10^{15}}$	**1500**	**98.2**

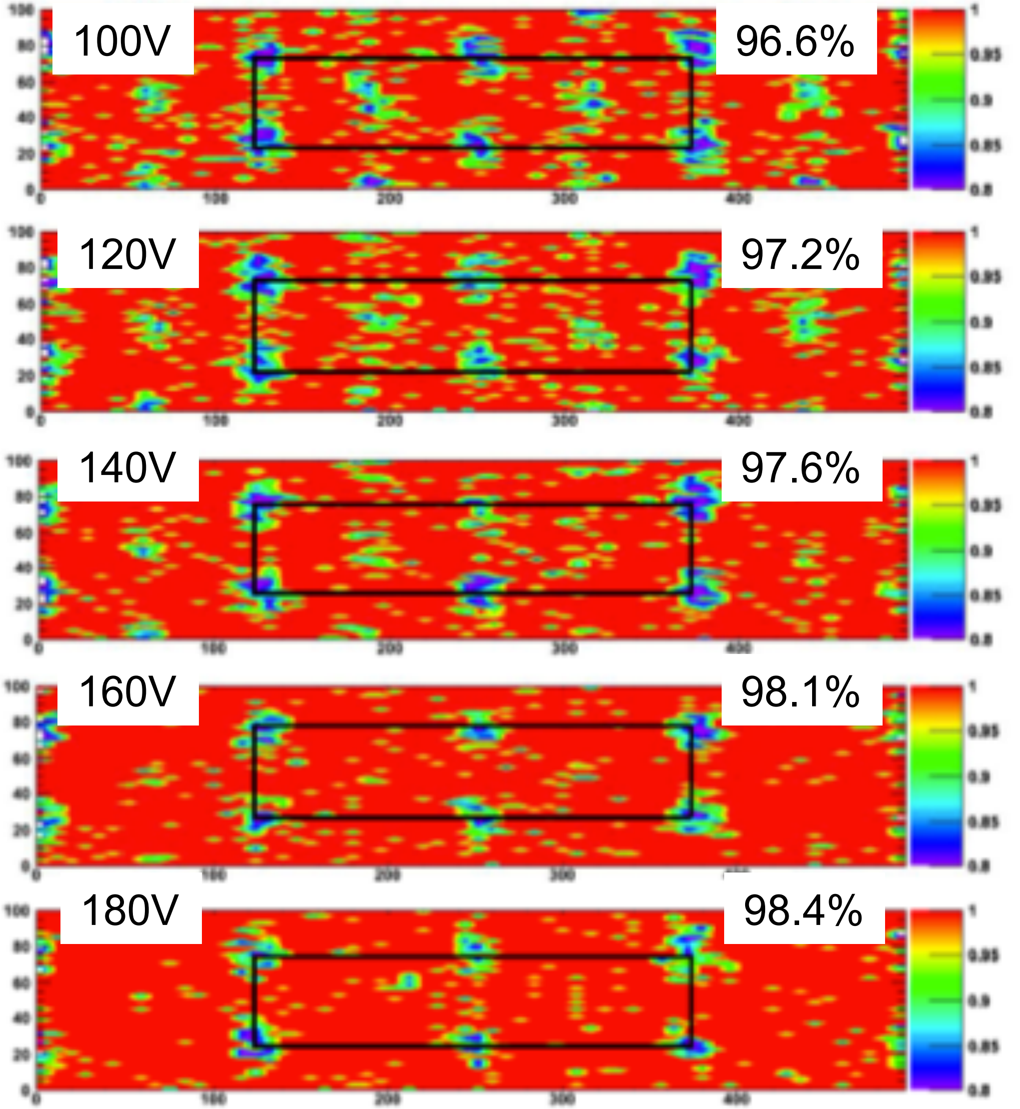
DESY, 04/2012

Hit efficiency vs bias voltage

S. Grinstein, Sh. Tsiskaridze

- CNM34, p-irrad 5e15 n_{eq} cm^{-2}
- Threshold at 1500 e-
- Efficiency and charge collection increase with voltage
- At 160V inefficiency regions due to n^+ columns disappear
- Noise occupancy becomes a problem beyond 170V

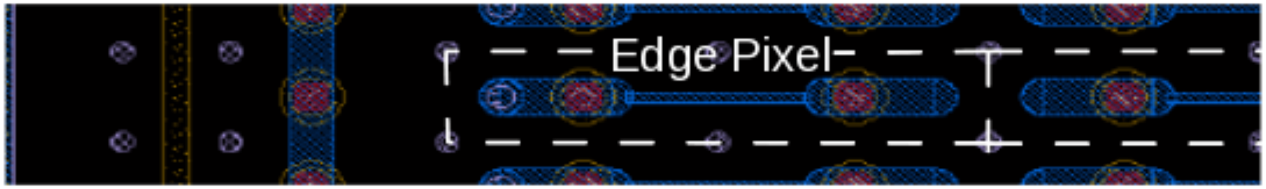


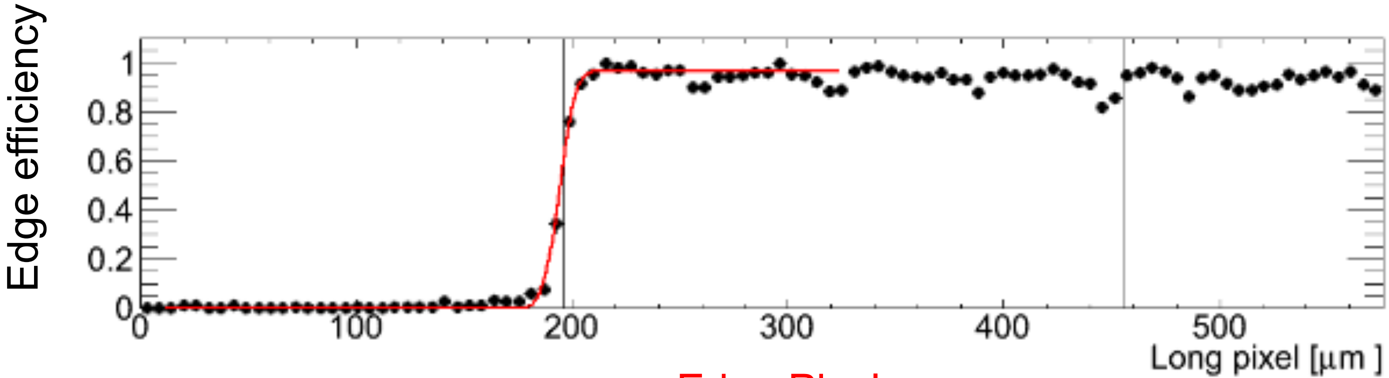


Edge efficiency

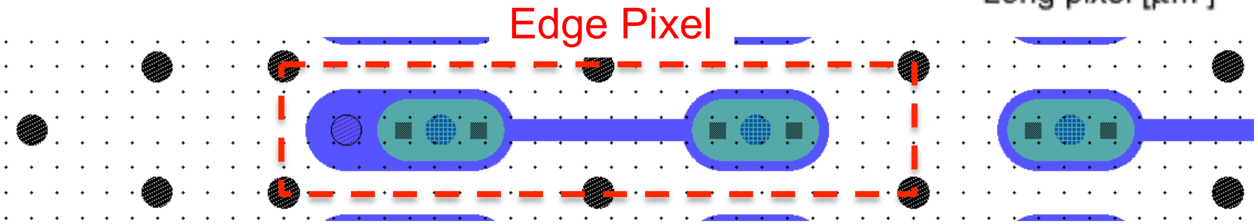
P. Grenier, S. Grinstein, Sh. Tsiskaridze

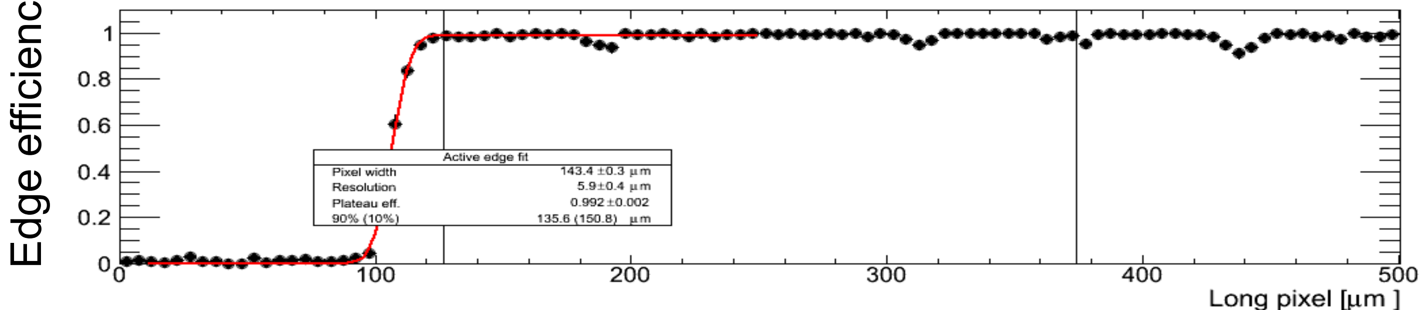
CNM34
p-irrad 5e15 n_{eq} cm^{-2}
Tilt 15°, 140V





FBK90,
p-irrad 2e15 n_{eq} cm^{-2}
Tilt 15°, 60V

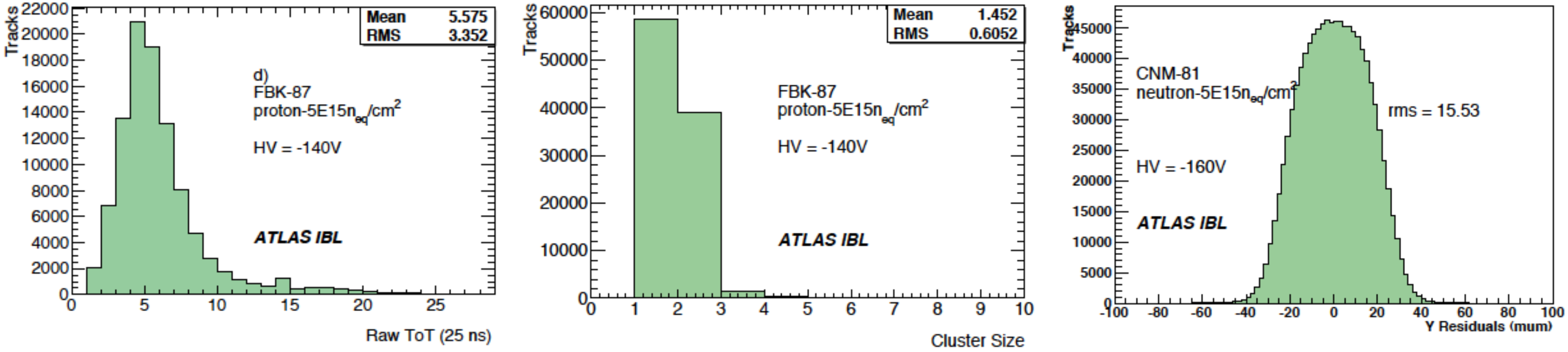




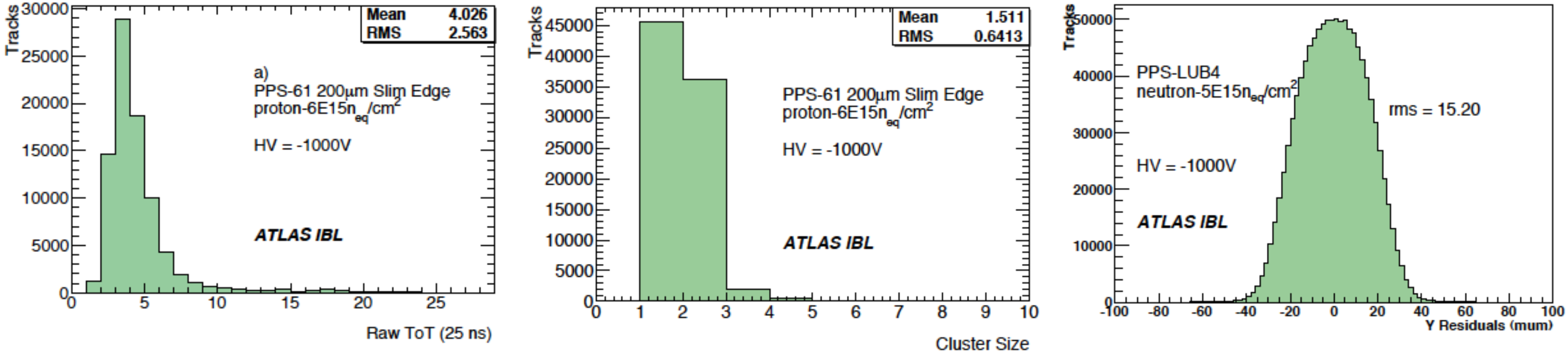
Beam test results

The ATLAS IBL Collaboration, “Prototype ATLAS IBL Modules using the FE-I4A Front-End Readout Chip”, JINST 7 (2012) P11010.

Irradiated 3D

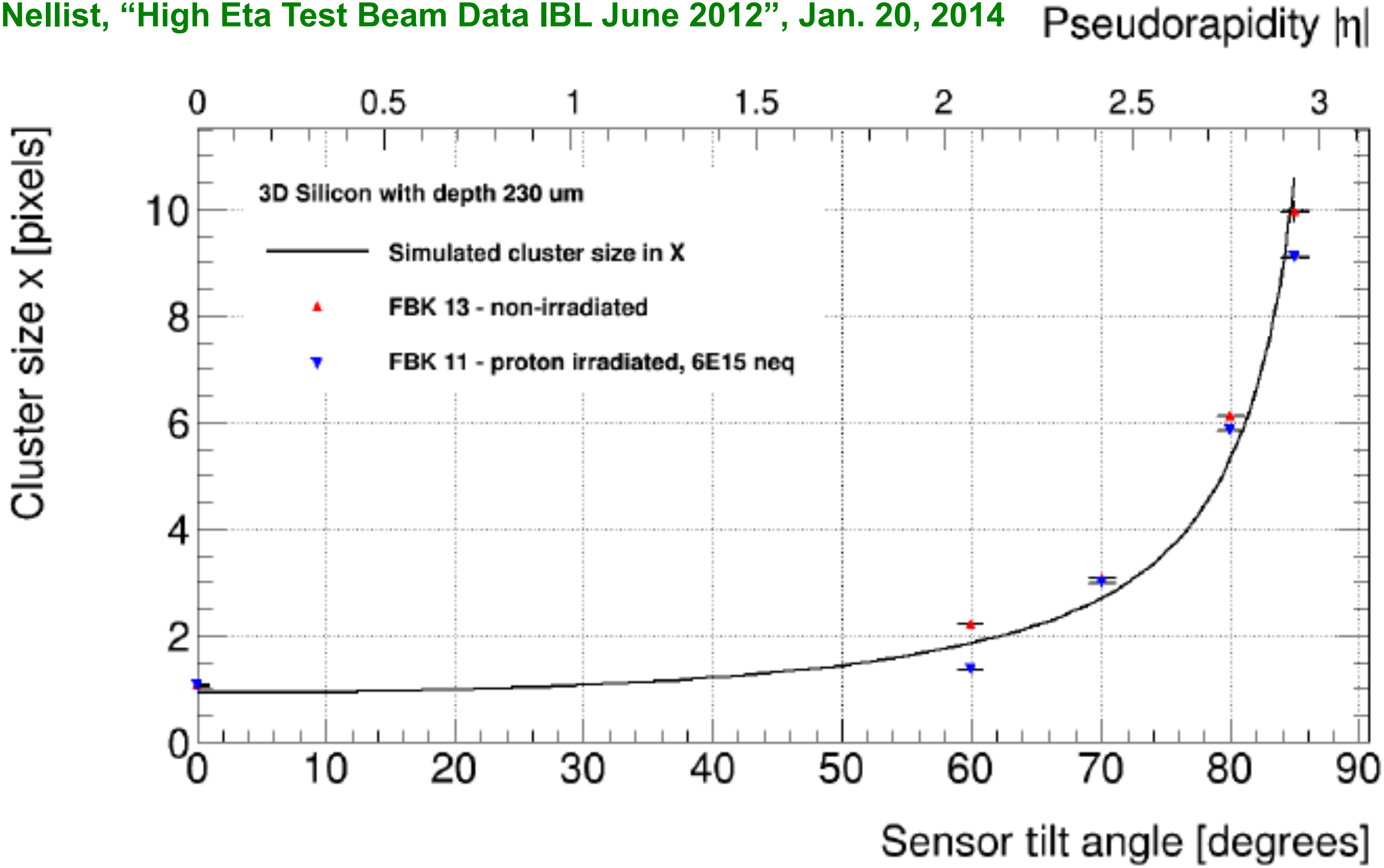


Irradiated planar



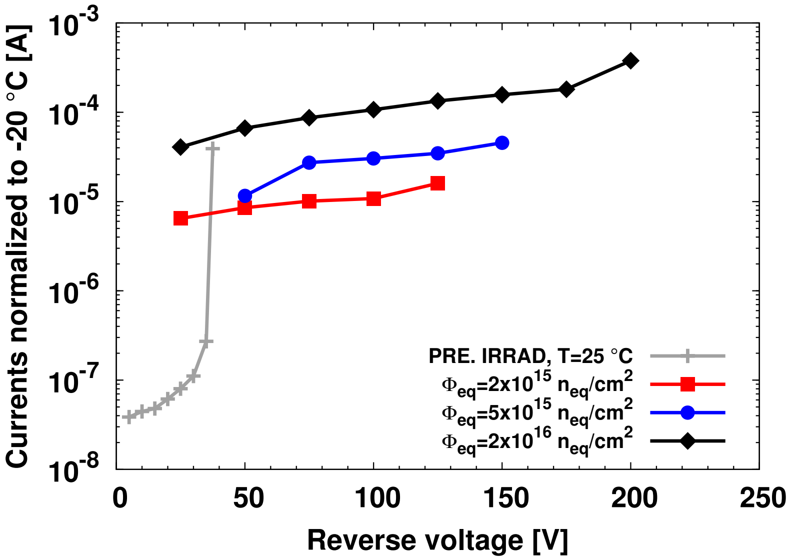
Cluster size at large eta

C. Nellist, "High Eta Test Beam Data IBL June 2012", Jan. 20, 2014

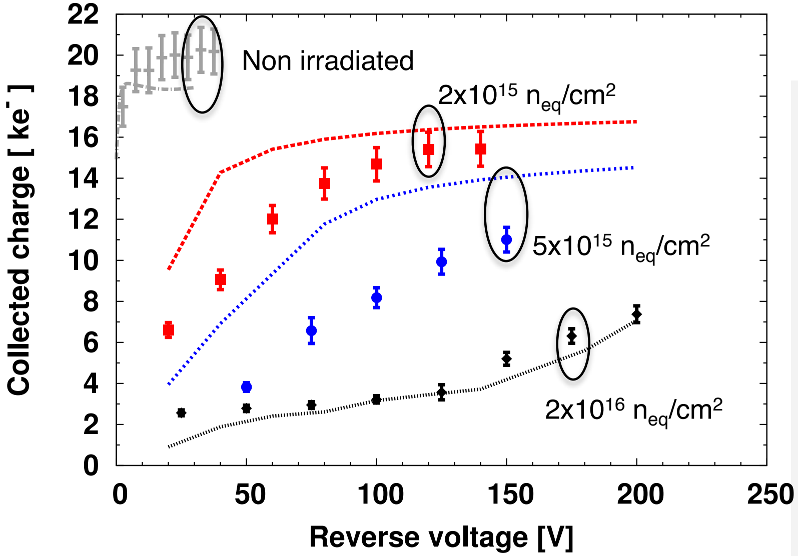


Looking at larger fluences with 3D strips

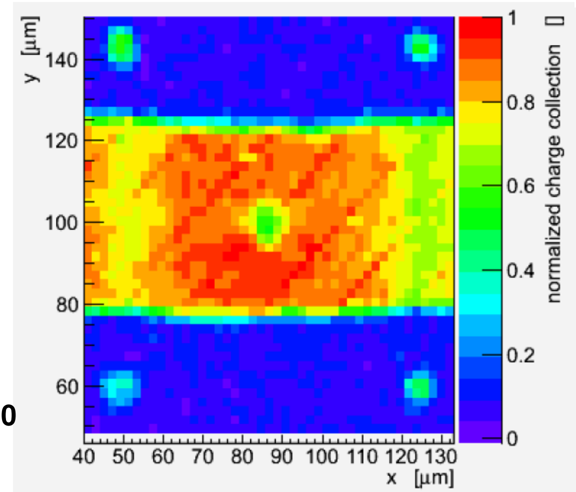
G.F. Dalla Betta et al, HSTD9 2013



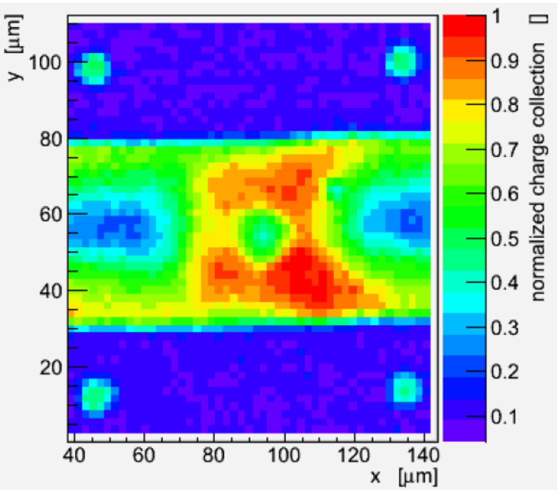
- Strip sensors from IBL prod. with ALIBAVA read-out
- Proton irradiation at KIT up to $2x10^{16}$ n_{eq}/cm^2
- Beta and laser tests performed in Freiburg
- Very good CCE, but clear saturation of the signal only for $2x10^{15}$ n_{eq}/cm^2
- For $2x10^{16}$ n_{eq}/cm^2 the bias voltage is not high enough to ensure uniform response …
- Need to improve breakdown voltage



$2x10^{15}$ n_{eq}/cm^2, 120V



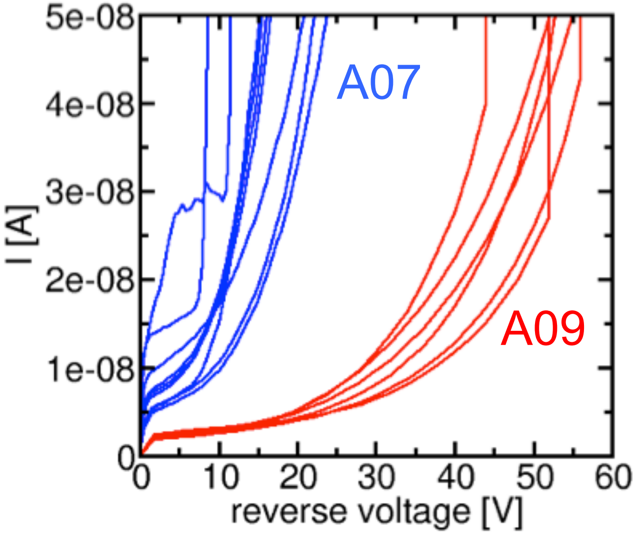
$2x10^{16}$ n_{eq}/cm^2, 150V



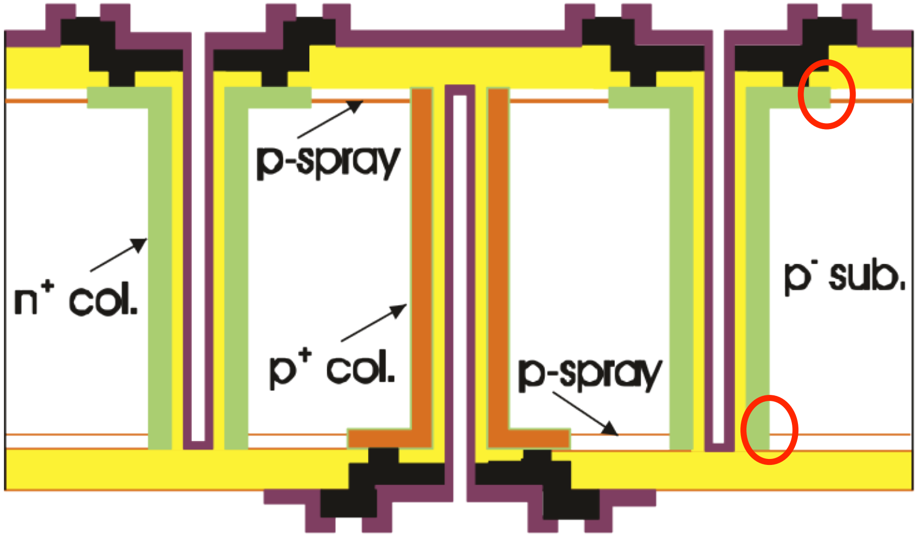
Breakdown voltage in FBK sensors

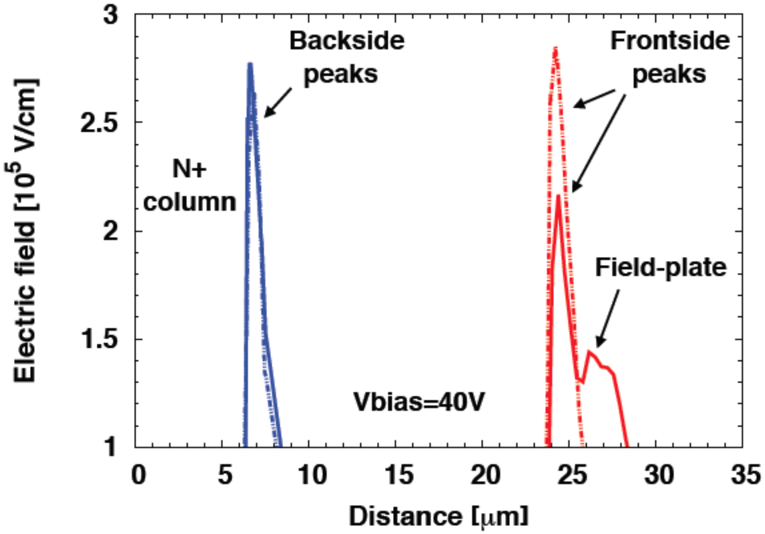
G. Giacomini et. al., IEEE TNS 60(3) (2013) 2357

- In FBK 3D sensors the intrinsic breakdown occurs at the n^+/p-spray junctions
- P-spray doping reduction improved V_{bd} from ~20 V (A07, R&D) to ~45 V (IBL production, from A09 on)
- For further improvements, it is important to learn more about breakdown behavior



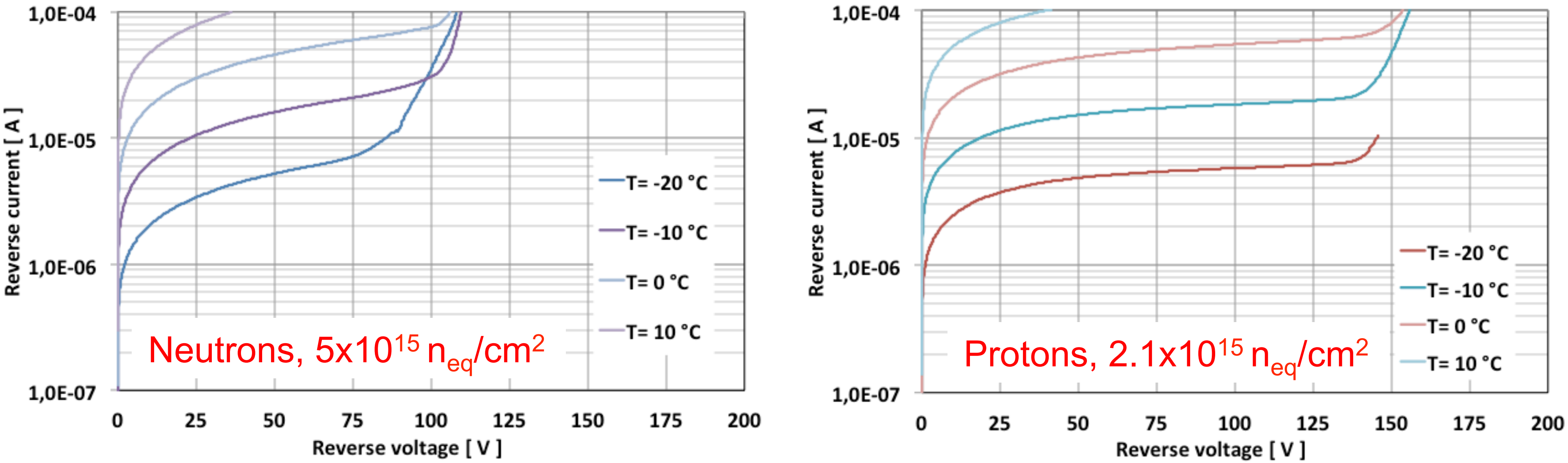
M. Povoli et. al., NIMA 699 (2013) 22





I-V curves after irradiation

- Neutron irradiation at TRIGA reactor (JSI, Ljubljana, Slovenia)
- 800 MeV proton irradiation (Los Alamos, USA)
- No high-temperature annealing (only RT handling)

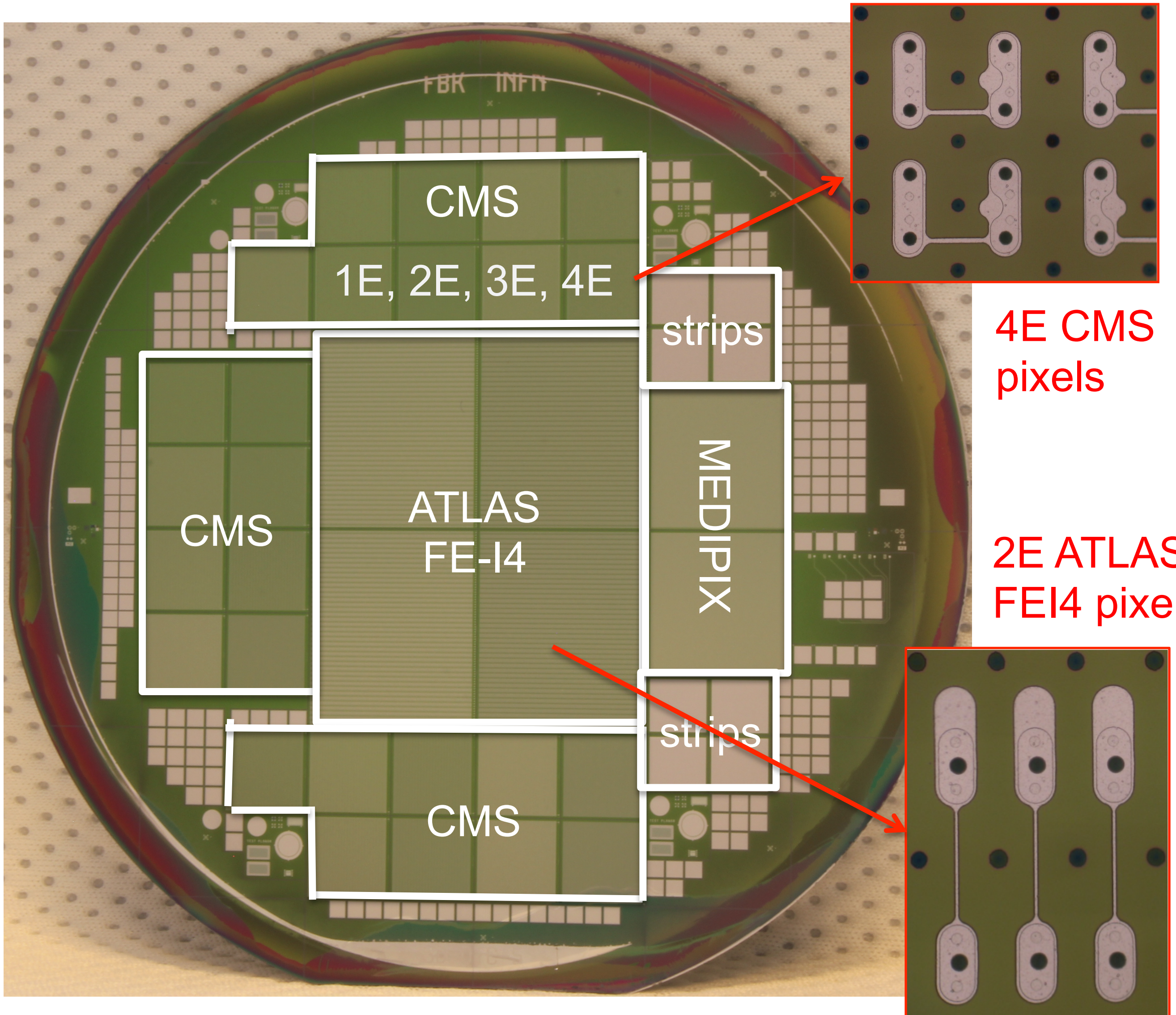


- Reactor neutrons mainly cause bulk damage
- Limited V_{bd} improvement (<50 V), mainly from γ–ray background

- Protons cause both bulk and surface damage
- Larger V_{bd} improvement (up to ~150 V) from larger ionization dose

New R&D batch: 3D-DTC-5

M. Povoli et al., IEEE NSS 2012



4E CMS pixels

2E ATLAS FEI4 pixels

- 4 ATLAS FE-I4 pixels
- 26 CMS pixels
- 2 Medipix2 pixels
- 8 strips, 80μm pitch
- Test structures

- High wafer bow Induced during processing
- Defects due to the stress had dramatic impact on functionality of large area devices
- Useful information could be extracted from 3D diodes (~ 2.2 mm^2)

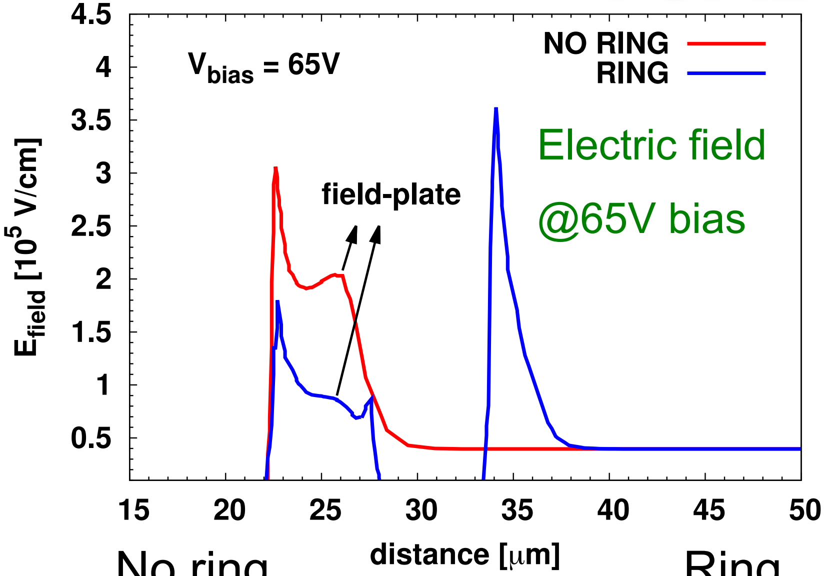
TCAD simulations

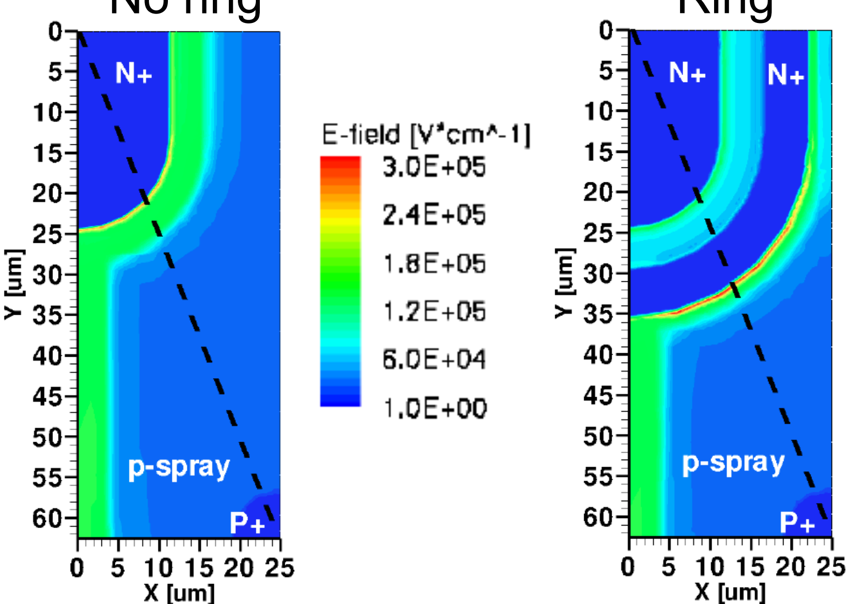
M. Povoli et al., IEEE NSS 2012

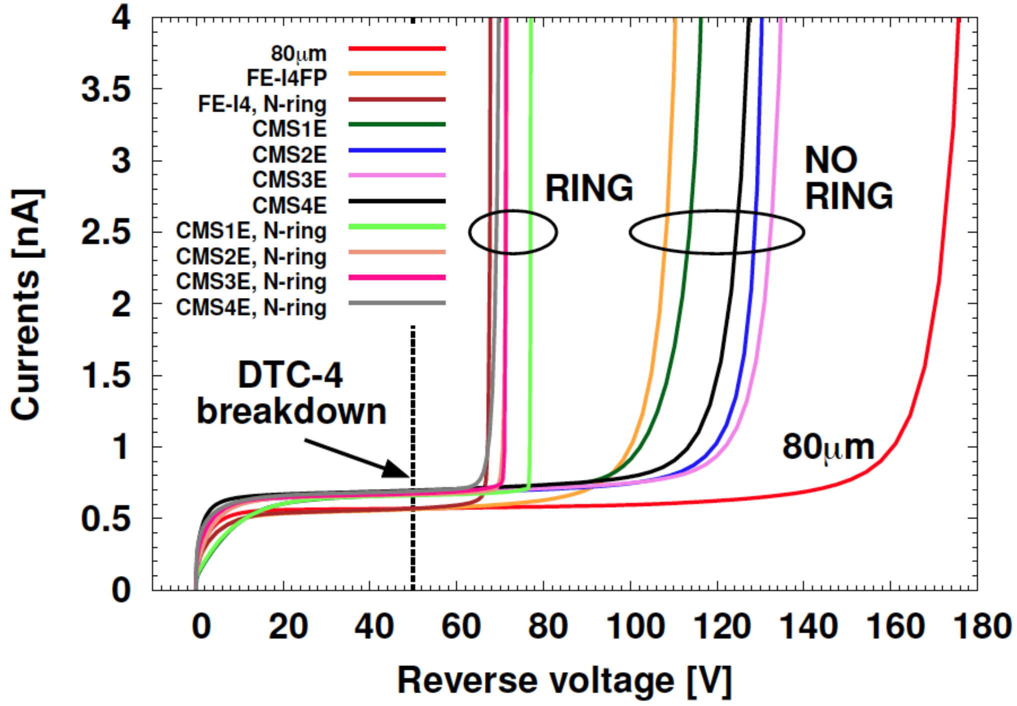
- Field plate on all structures
- Planar n-ring around column

- reduces p-spray potential in the inner region
- but space constraints limits its effectiveness

- Large V_{bd} increase wrt previous technology expected

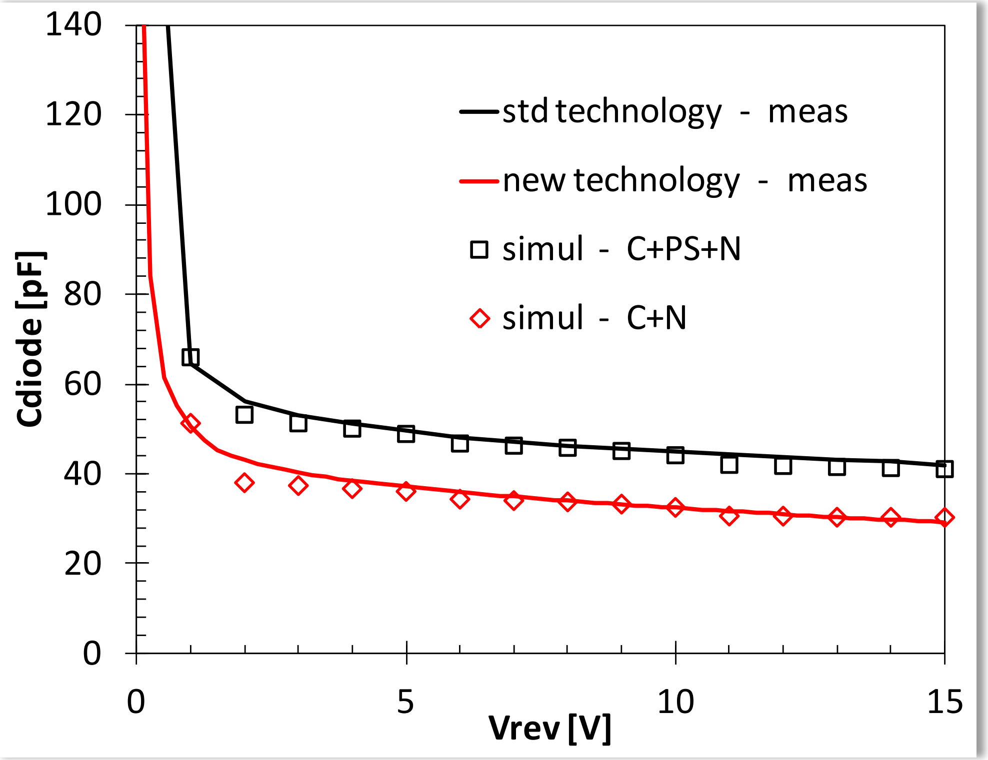






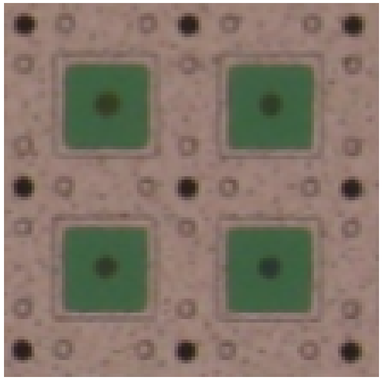
C-V curve comparison

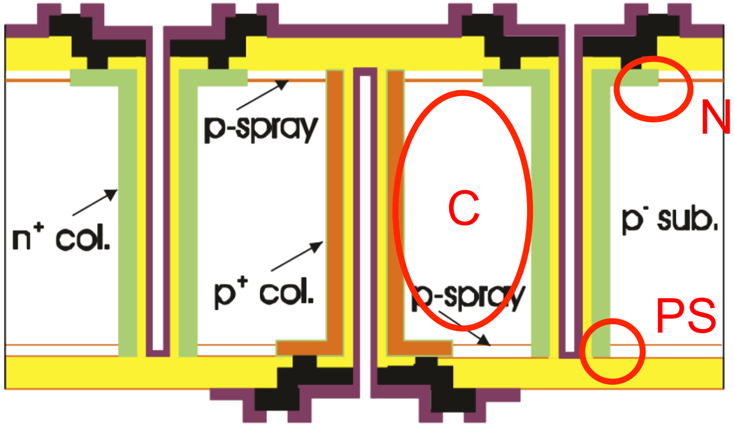
At 15 V, capacitance is decreased by ~10 pF (-30%)



3D diodes

80µm layout





Simulated capacitance contributions

- C: columns
- N: n-diffusion to p-spray at the top of the junction column
- PS: column to p-spray at the bottom of the junction column

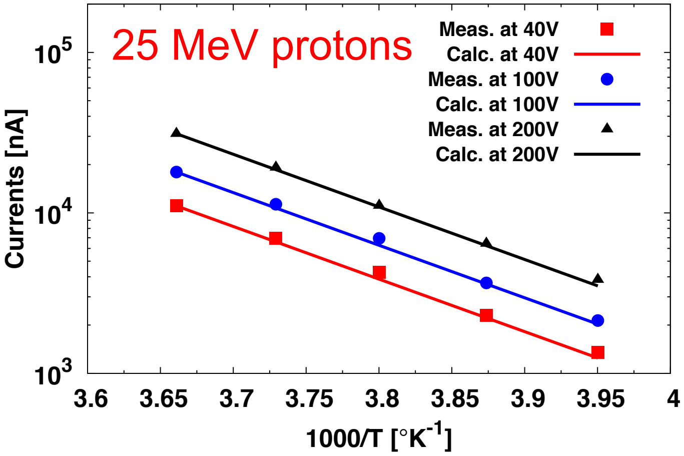
G.-F. Dalla Betta et al., IEEE NSS 2013

I-V curves after irradiation

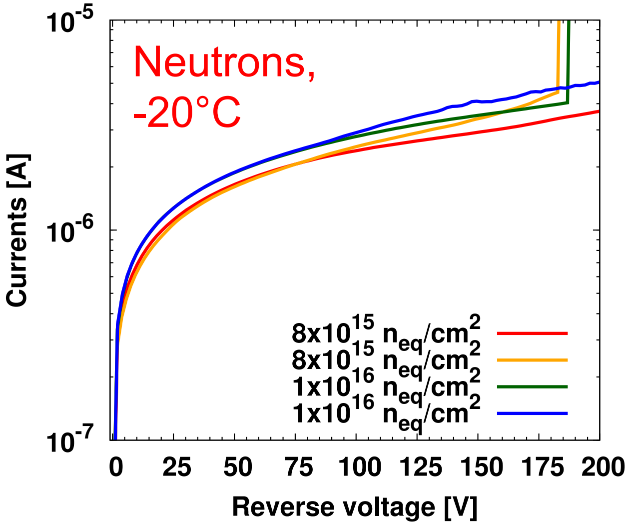
- Neutron irradiation at TRIGA reactor (JSI, Ljubljana, Slovenia)
- 25 MeV proton irradiation (KIT, Germany)
- 800 MeV proton irradiation (Los Alamos, USA)
- No high-temperature annealing (only RT handling)

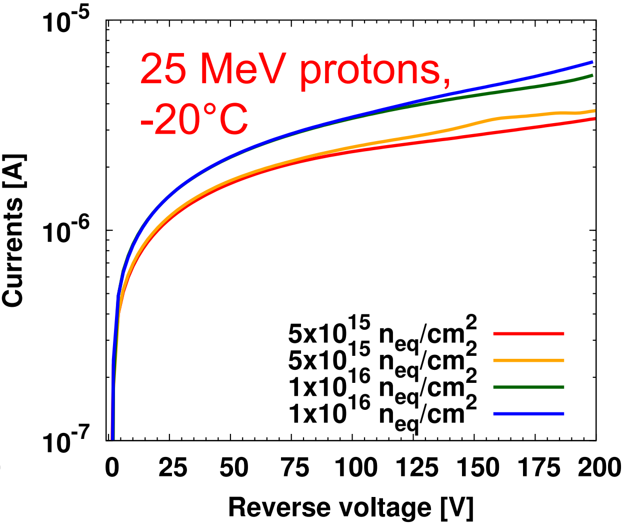
- Leakage current increase as expected
- Pure SRH behavior up to max voltage
- Large improvement in breakdown voltage

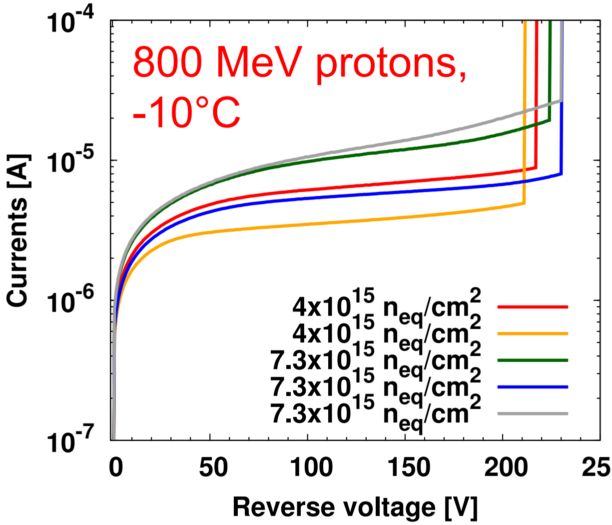
$$I(T) = I(T_R)\left(\frac{T}{T_R}\right)^2 \exp\left[\frac{E}{2k_B}\left(\frac{1}{T_R}-\frac{1}{T}\right)\right]$$



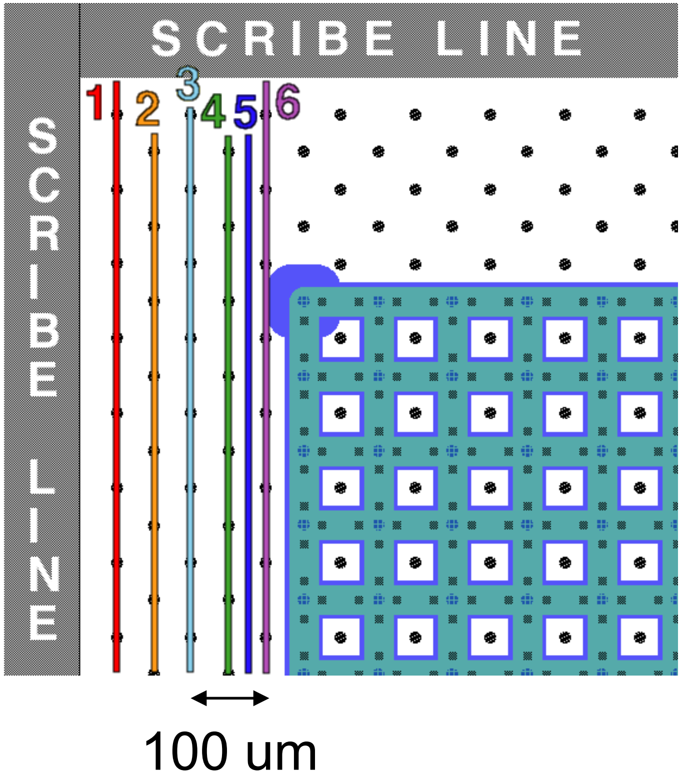
G.-F. Dalla Betta et al., IEEE NSS 2013

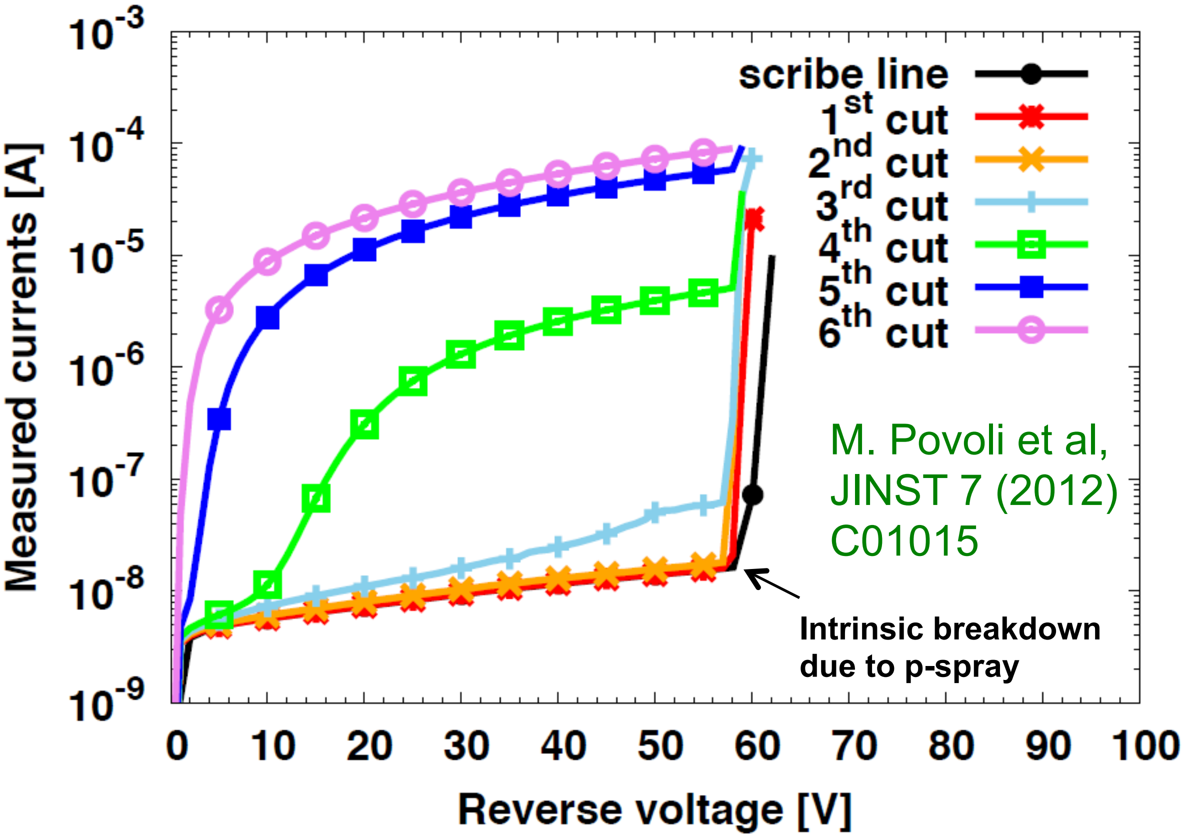






Slim edge in FBK 3D sensors



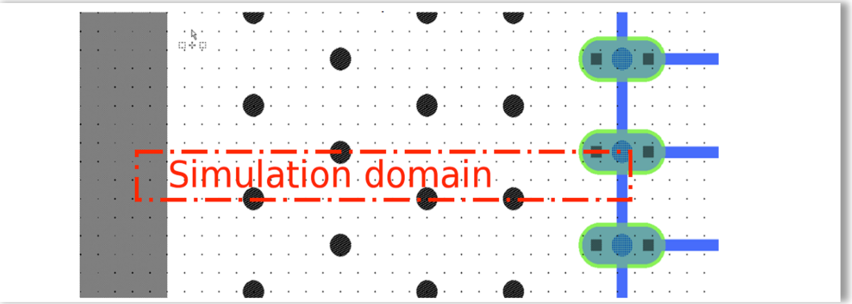


M. Povoli et al, JINST 7 (2012) C01015

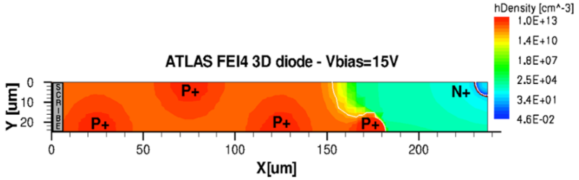
Intrinsic breakdown due to p-spray

- Repeated cuts starting from scribe-line, each one closer to the active area (the 6th cut dices the last row of ohmic columns of the active area)
- Devices can be safely operated up to the 3rd cut (i.e., with only one row of ohmic columns beyond the active area)
  → There's room for design optimization (dead region < 100 micron)

Slim edge optimization

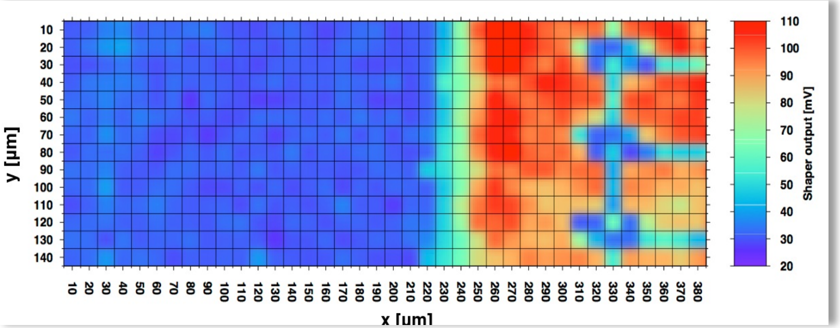


~200 µm slim edge used in IBL 3D pixels



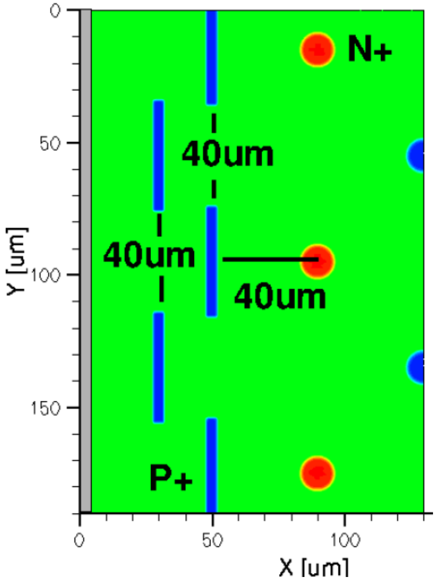
Simulated hole density

V_{bias}=15V



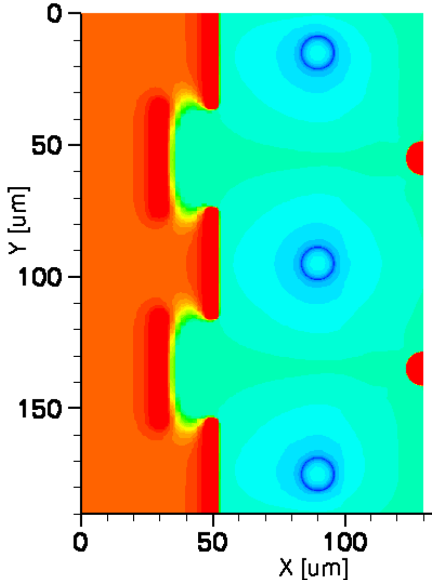
Output signal with IR laser scan

M. Povoli et al, JINST 7 (2012) C01015



Narrow trenches in place of columns

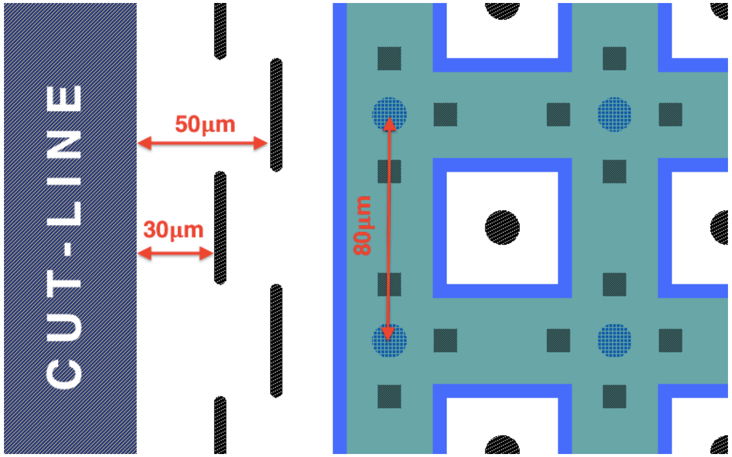
V_{bias}=50V

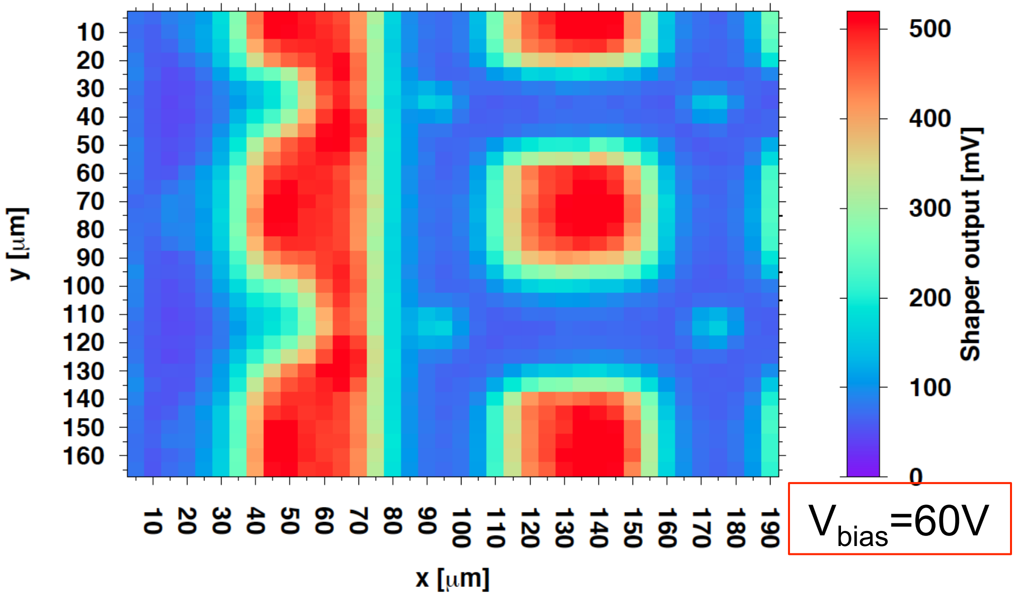


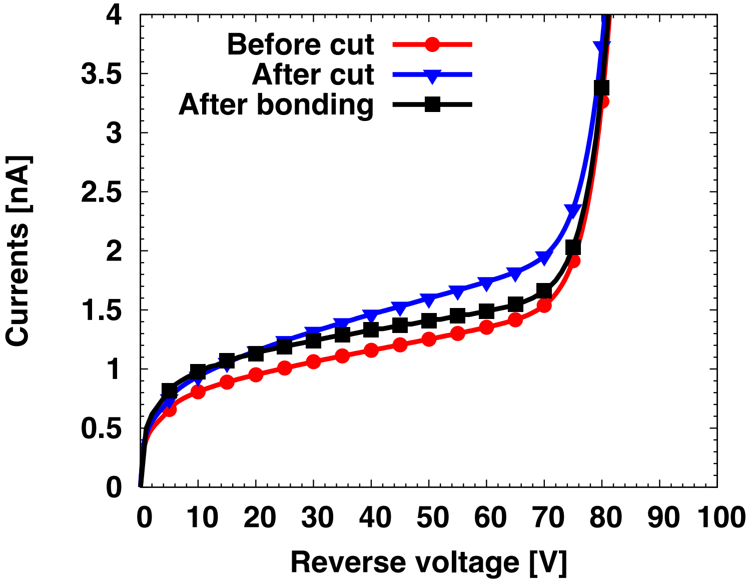
G.F. Dalla Betta et al., IEEE NSS 2011

New slim edge performance

M. Povoli et al., JINST 8 (2013) C11022



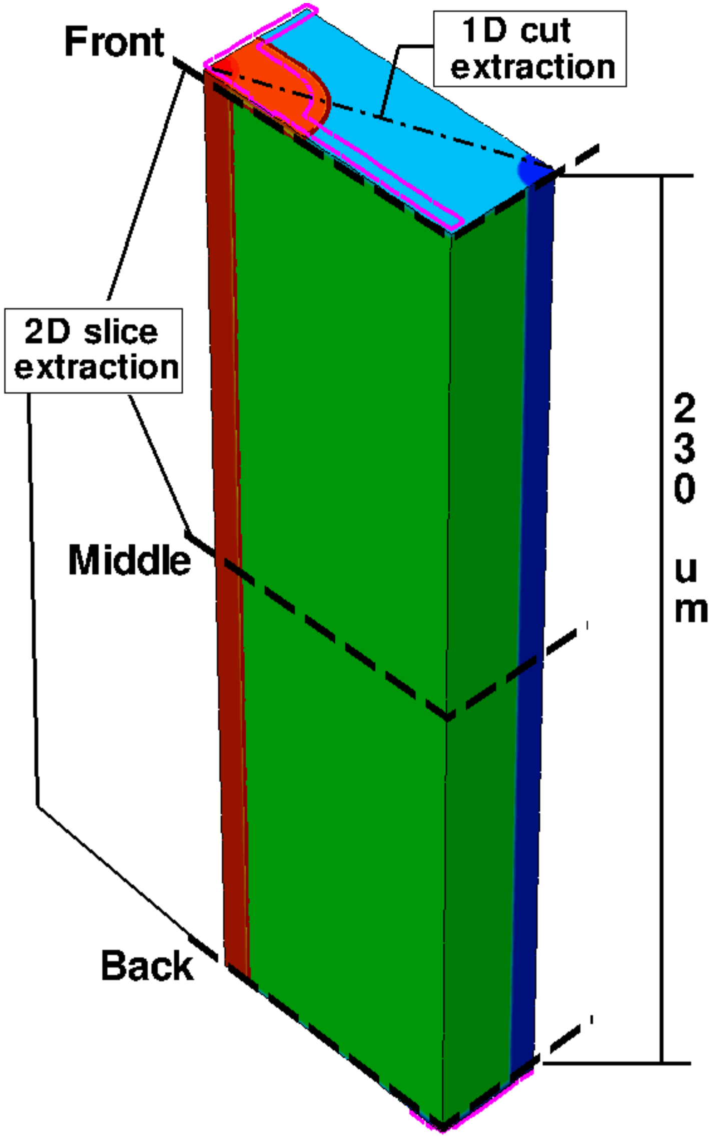




- Tested on 3D diodes with edge trenches of different shapes
- No appreciable change in the current after dicing
- IR laser scan confirms the depletion region is blocked by trenches
- ~ 50 µm slim edge achieved !

TCAD simulations

M. Povoli, PhD thesis, UniTN, 2013



Structure parameters

1/4 of elementary cell (exploiting symmetry)

Exact layouts implemented

FBK technology parameters

Measured (SIMS) doping profiles

Models and simulation

Mobility: Doping Dependent, High Field Saturation

Generation/Recombination: SRH, Avalanche

Data analysis

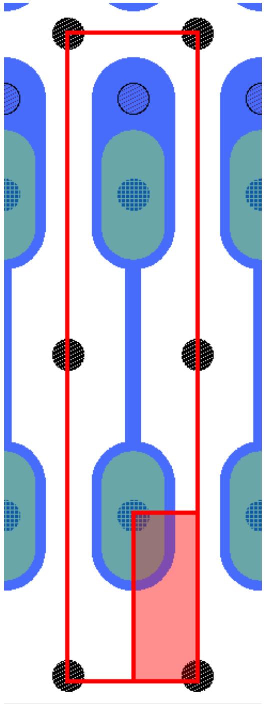
Monitor electrical quantities in different regions

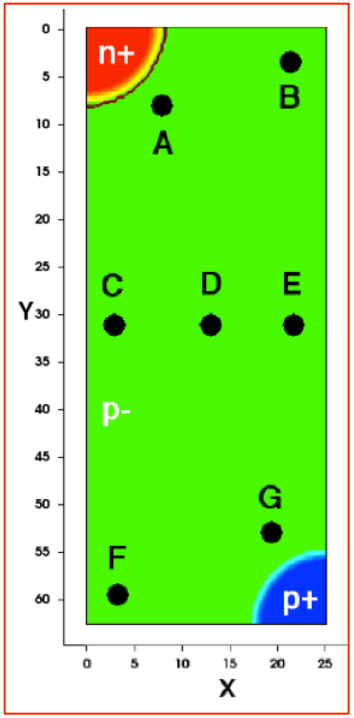
Understand where the breakdown occurs:

- 2D slices at different depths
- 1D cut extraction from 2D slices

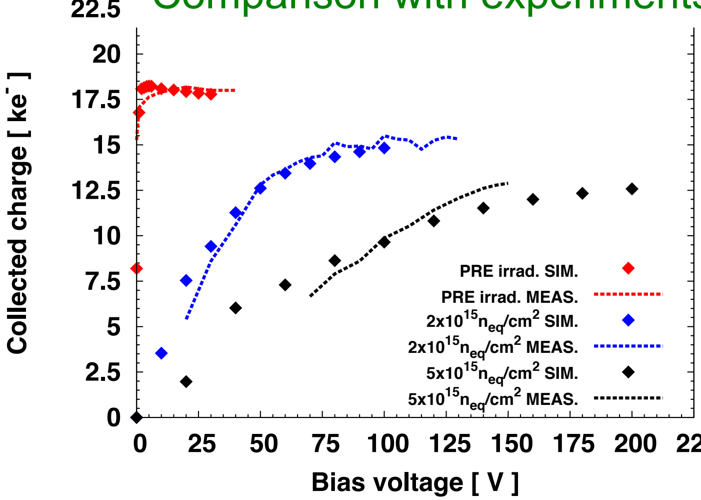
TCAD simulation of FE-I4 pixels

Simulations by Marco Povoli, UniTN

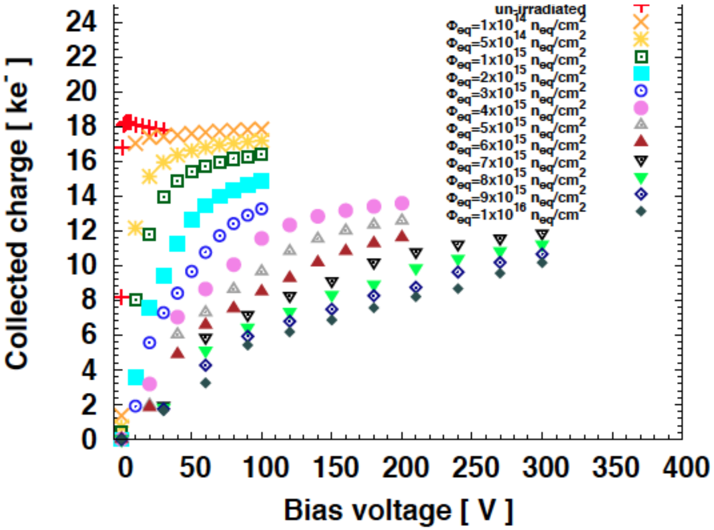




Comparison with experiments



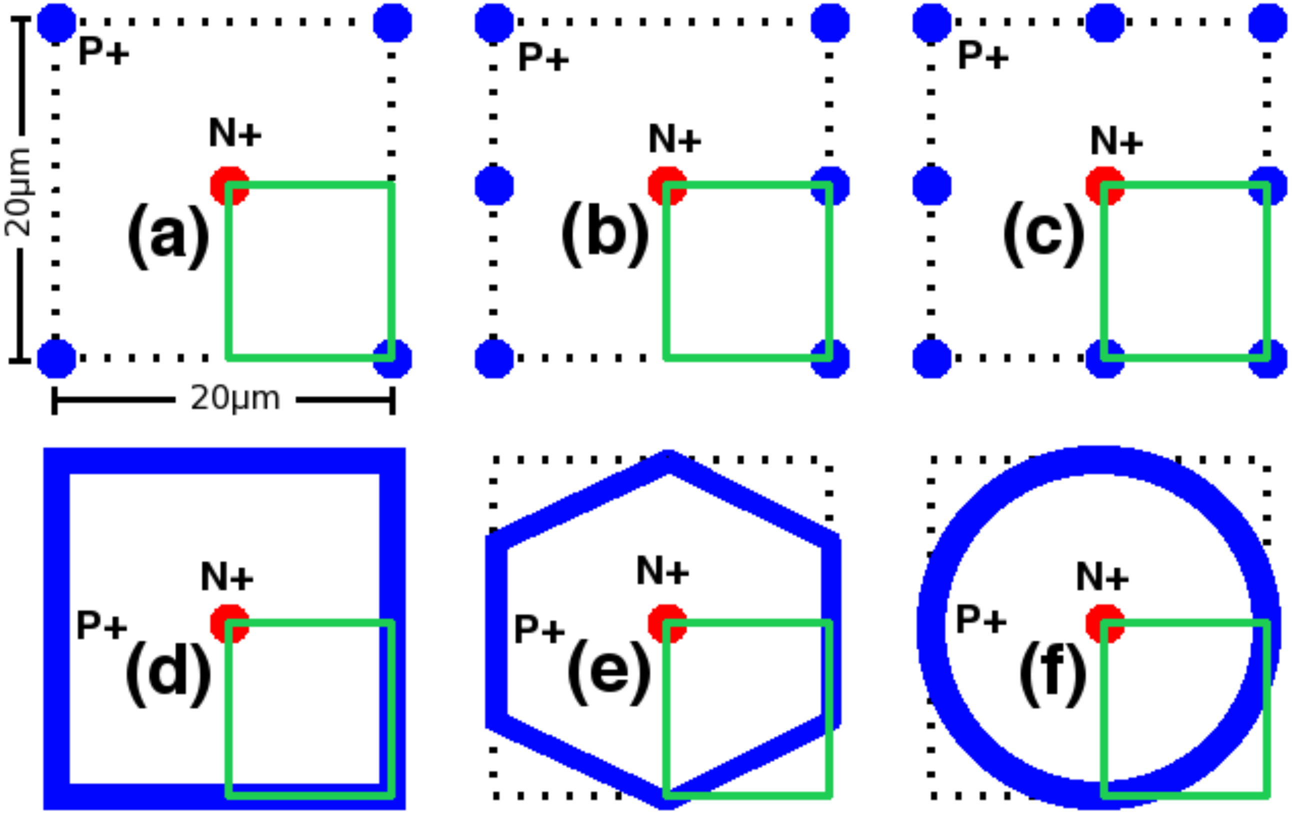
Simulations at different fluences



- 3-trap level "Perugia" model with parameters from D. Pennicard, et al., NIMA 592 (2008) 16
- 1 μm thick (~2d) slice
- MIP vertical hits at different points
- Integration of signals above threshold and average

Charge multiplication by design in thin 3D sensors

Exploiting high fields in thin 3D structures with small IES



🟩 Simulation domain

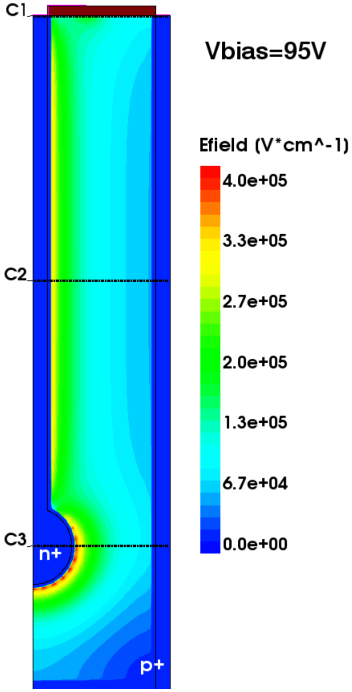
🟥 N+ electrodes

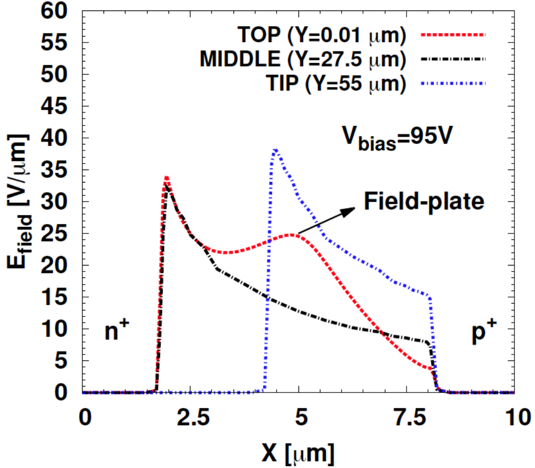
🟦 P+ electrodes

Single pixel size: 20x20 µm^2

Simulation domain size: 10x10 µm^2

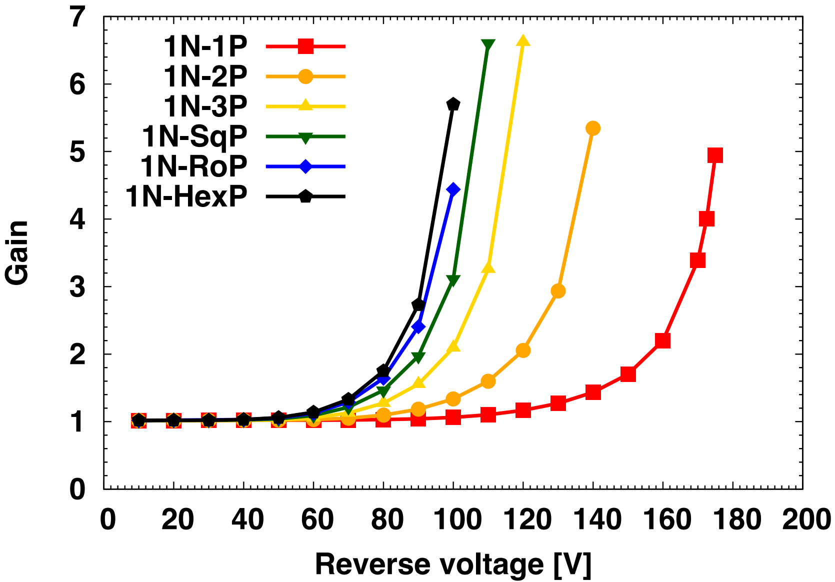
70 µm thickness

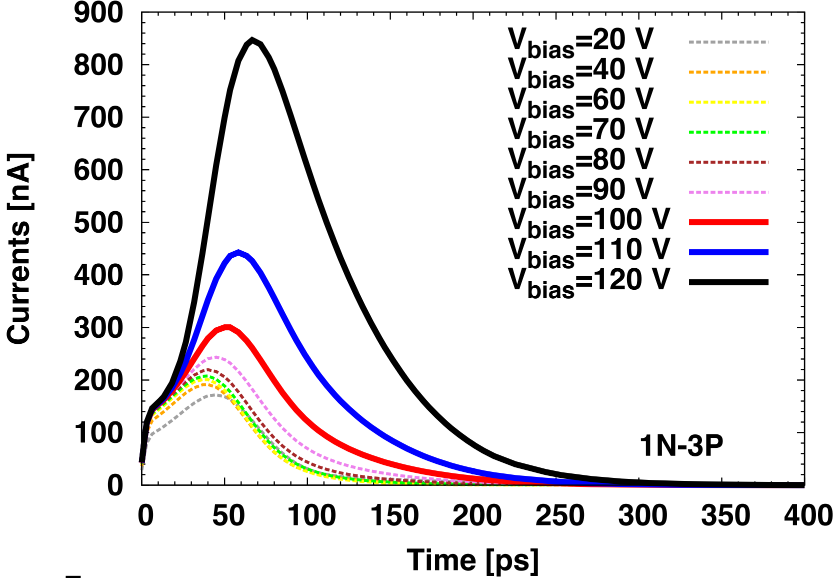


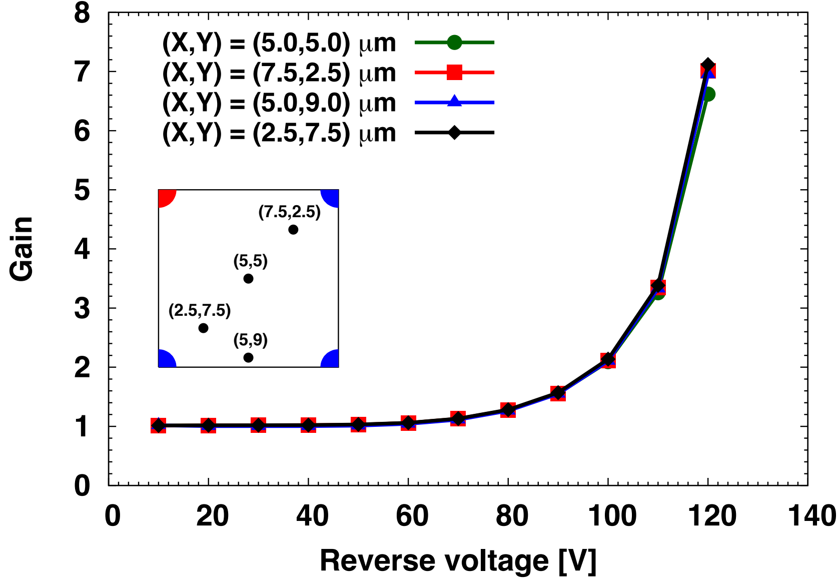


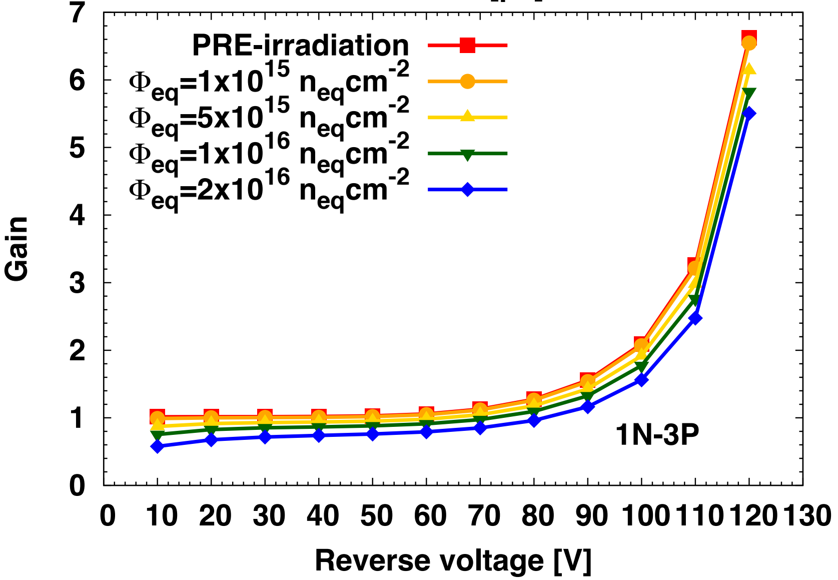
TCAD simulations

M. Povoli et al.,
To be published









3D cell layout