12 March 2014

RD53 and CHIPIX65: Pixel FE-chip for HL_LHC

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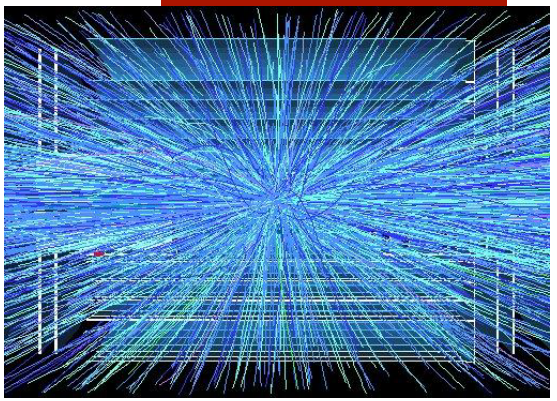
on behalf of CMS and ATLAS Collaborations, RD53 and CHIPIX65

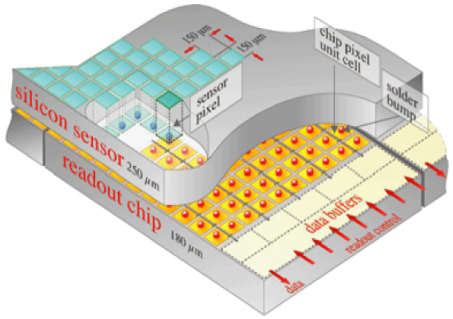
Talk layout

- HL_LHC challenges for pixel FE-chip
- RD53 Collaboration
  - Description, status and outlook
- INFN Contribution
  - CHIPIX65 project
- Conclusions

Phase 2 pixel challenges

- **HL_LHC LUMINOSITY:**
  - **Instant → Very high particle rates: 500MHz/cm² :** pixel rates: 1-2 GHz/cm²
  - **Integrated→ Unprecedented hostile radiation: 10MGy(1Grad), 10^{16} n(eq)/cm²**
- **Maintain detector performance**
  - **Smaller pixels: (25–50 x100 um²)**: good resolution; improved two track resolution
  - **Low threshold :** 2500 e- → 1000e- (less signal from sensor)
  - **Low mass -> Low power:** less average power per pixel
- **L1 challenges:**
  - **Increased rate: 100kHz -> 1MHz**
  - **Increased trigger latency → 3 to 20 usec**
  - **Contribution to first/second level trigger ?**





PARAMETER or FEATURE	1st generation LHC phase 0	2nd generation LHC Phase 1	3rd generation LHC Phase 2
CMOS technology	250nm	250nm / 130nm	65nm
Max Particle Flux	~50 MHz/cm²	~200 MHz/cm²	~500 MHz/cm²
Max Pixel Flux	200 MHz/cm²	600 MHz/cm²	2 GHz/cm²
Rad. Hardness	1.5 MGy	3.5 MGy	10 MGy
Pixel Dimension	100x150 μm² 50x400 μm²	100x150 μm² 50x250 μm²	25x150 μm² 50x100 μm²
Signal Threshold	2500-3000 e⁻	1500-2000 e⁻	~1000 e⁻
L1 Trigger Latency	2-3 μs	4-6 μs	6-20 μs
L1 Trigger Rates	100 KHz	~100 KHz	200-1000 kHz
L1 Trigger contribution	no	no	clustering info @L0 self-triggering
ASIC side	~1 cm²	~4cm²	1-4cm²
Hit memory per chip	0.1 Mb	1 Mb	~16 Mb
Chip output bandwidth	~40 Mb/s	~320 Mb/s	~3 Gb/s
Power Budget	~0.3 W/cm²	~0.3 W/cm²	<0.4 W/cm²

Hybrid pixel detector:

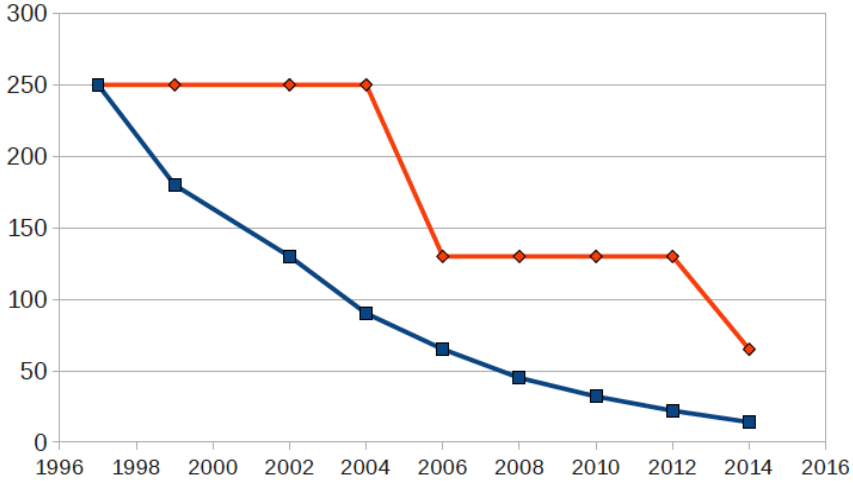
- fast, low power electronics
- Lot of data storage needed → local buffering

→ higher VLSI integration, beyond CMOS 130nm

Why CMOS 65nm for HEP ?

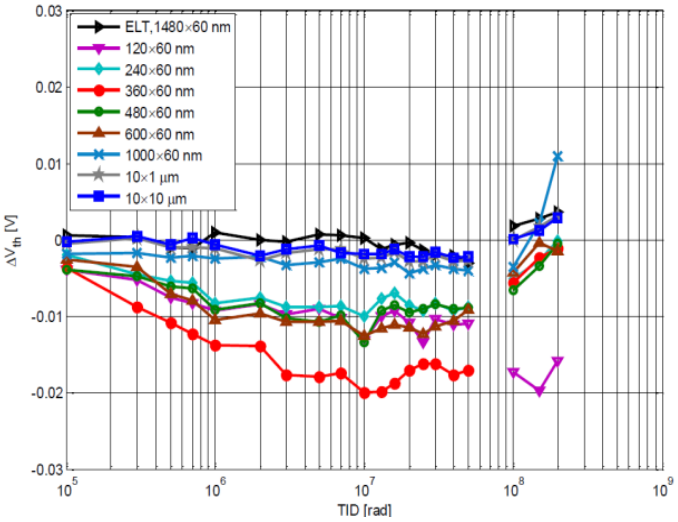
- Use of strong industrial technology ➔ looking to industrial standards in planar technology, accessible to HEP community
- CMOS 130nm is today the top technology in HEP, next technology nodes are 90nm, 65nm, 40nm, 28nm
  - 90nm is not a solid technology node (not much used);
  - 28 and 40nm are too expensive and rad-hardness is not obvious, since it uses dielectric other than SiO_2.
- CMOS 65nm is chosen
  - Clear and substantial gain (see next slide)
  - Stable technology node: long-lifetime
  - Still affordable
  - Uses SiO_2 as inter-dielectric that is known ok for radiation damage

Technology gap: HEP late compared to real-life applications

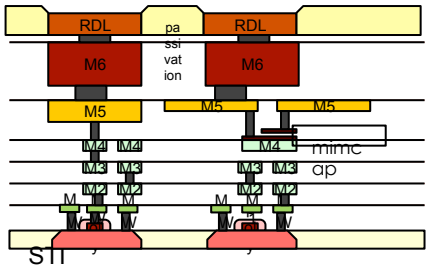


What we gain using CMOS 65nm

- Radiation Tolerance (dose,hadrons, SEU)
  - Uses thin gate oxide
  - Verified for up to 200Mrad, better than 130nm: to be confirmed for 1GRad
- Large amount of digital logic/ memory
  - Vital for small pixel
  - Logic density: 250nm:~1; 130nm:~4x; **65nm:~16x**
  - Speed: 250nm~1, 130nm:~2x; 65nm:~4x
- Low power (digital)
  - 250nm: 1, 130nm: (1/2-1/4) ; **65nm: (1/8-1/16)**
- Many metal(Cu) layers:
  - Power distribution, signal distribution, pixel readout busses, etc.
- Mature technology and stable



- Affordable (still…)
  - **MPW** from foundry and Europractice;
  - Masks costs a lot: ~1 M$ for an engineering RUN
  - Production similar as 130nm



6+1 metals (max to 9+1)

130nm up to 7+1

RD53: ATLAS-CMS pixel ROCs

- A group of Institutes from CERN Member and non-Member States, and CERN, have agreed to collaborate to form the RD53 Collaboration for the development of pixel readout integrated circuits for extreme rate and radiation.
- **Letter of Intent CERN-LHCC-2013-008** (LHCC-P-006) presented at LHC Committee on June 12th 2013 and received the recommendation to create a RD group.
- The **CERN Research Board approved** the RD53 Collaboration at its 205th meeting on August 28th 2013.
- RD53 is now a recognized "experiment"

- 17 institutes, ~100 people, 50% chip designers
  - 6 INFN- groups
- Spokes persons and Institute chair elected
- Pending requests for membership : **Milano**, Prague, OMEGA

	Country	Town	Institute	Representative	Experiment
1	Czech	(Prague)	(FNSPE-CTU / IP-ASCR)	Miroslav Havranek	ATLAS
2	France	Marseille	CPPM	Alexandre Rozanov	ATLAS
3	France	Paris	LPNHE	Giovanni Calderini	ATLAS
4	France	(Paris)	(Omega / LAL)	A.Lounis / C.De La Taille	ATLAS
5	Germany	Bonn	Bonn University	Hans Krüger	ATLAS
6	Italy	Bari	INFN and Politecnico	Flavio Loddo	CMS
7	Italy	(Milano)	INFN and University	Valentino Liberali	ATLAS
8	Italy	Padova	INFN and Politecnico	Dario Bisello	CMS
9	Italy	Pavia	INFN and University	Valerio Re	CMS
10	Italy	Perugia	INFN and University	Gian Mario Bilei	CMS
11	Italy	Pisa	INFN and University	Fabrizio Palla	CMS
12	Italy	Torino	INFN and University	Natale Demaria	CMS
13	Netherland	Amsterdam	NIKHEK	Nigel Hessey	ATLAS
14	Switzerland	Geneva	CERN	Jorgen Christiansen	ATLAS,CMS,CLICdp
15	Switzerland	Villigen	PSI	Roland Horisberger	CMS
16	UK	Didcot	RAL Centre for Instrumentation (CFI)	Mark Prydderch	CMS/ATLAS
17	USA	Chicago	Fermilab	David Christian	CMS
18	USA	Berkeley	LBNL	Maurice Garcia-Sciveres	ATLAS
19	USA	New Mexico	University of New Mexico	Sally Seidel	ATLAS
20	USA	Santa Cruz	U.C.Santa Cruz	Alex Grillo	ATLAS

Scope of RD53 Collaboration

- The development of pixel readout Integrated Circuits (IC) for the next generation of pixel readout chips to be used for the **ATLAS** and **CMS Phase 2 pixel detector upgrades** and **future CLIC pixel detectors**.
- This does not imply that ATLAS and CMS must use the same exact pixel readout chip, as most of the development, test and qualification effort needed is independent of the specific implementation of the final chips.
  - Multiple implementations are possible using the same technology foundation. In order to be effective, this collaboration is specifically focused on the design of pixel readout chips, and not on more general chip design or on other aspects of pixel technology.
- The IC challenges include: smaller pixels to resolve tracks in boosted jets, very high hit rates, unprecedented particle fluence, much higher output bandwidth, and large IC format with low power consumption in order to instrument large areas while keeping the material budget low.
- Although data rates, radiation levels, and trigger requirements are different, there is **synergy** with the development of **pixel detectors for future e^+e^- linear collider detectors** and therefore collaboration is **foreseen**.

RD53 Organization Structure

Main Bodies of the Collaboration:

- Collaboration/Institute Board
- Management Board
- Working Groups

Status

- Regular CB and management meetings have started
- RD53 workshop: April 10 -11at CERN
- **MOU in the pipeline**
- Working groups have regular meetings

	Name	Role	Town / Group
1	Jorgen Christiansen	Spokesperson for CMS	CERN
2	Maurice Garcia-Sciveres	Spokesperson for ATLAS	LBNL
3	Natale Demaria	CB Chair	INFN-Torino
4	Marlon Barbero	WGC - Radiation qualification	Marseille
5	t.b.d.	WGC - Top Level Design	
6	Tomaz Hemperek	WGC - Simulation Test Benches	Bonn
7	t.b.d.	WGC - I/O	
8	Valerio Re	WGC - Analog Design	Bergamo/Pavia
9	t.b.d	WGC - IP Blocks	

WG	Domain
WG1	Radiation test/qualification
	Qualification of technology to 10 MGy TID, 10^{16} n.eq./cm^2. Transistor simulation models after irradiation. Evaluation of logic cell libraries after irradiation. Expertise on radiation effects in 65nm
WG2	Top level design
	Design methodology, verification and test of ~5 x 10^8 transistor IC. Analog integration in large digital chip. Power distribution Synthesis constraints. Clock distribution and optimization
WG3	Simulation and verification test bench
	System Verilog simulation and Verification framework. Optimization of global architecture/pixel regions/pixel External system and external physics data. Verification of test chips and evolving designs
WG4	I/O
	Definition of readout and control interfaces (e.g. LPGBT). Definition of standardized I/O protocols and performance Implementation of readout and control interface blocks. Standardized interfaces: Control, Readout, etc.
WG5	Analog design
	Evaluate and compare alternate amplifier designs. Evaluate and compare charge ADC techniques vs. number of bits (TOT, shared ADC, etc.)
WG6	IP blocks
	Define common requirements for IP block design. Evaluate, document, and keep library of IP blocks Generate overview and recommendations. Each block will have its own prototyping milestones

RD53 WG status/progress

- **RADIATION**:
  - Systematic radiation testing program has started for 1Grad TID
  - **PMOS** transistors have shown **significant degradation**, relevant for digital electronics (minimum size)
    - Some mysteries to be understood/resolved
    - New unexplored territory (e.g. space 10^{-4} less radiation)
  - **Annealing scenario critical** (e.g. running pixel cold)
- **ANALOG**:
  - Front-end specs under definition
  - A large set of front-end architectures will be evaluated, designed and tested.
- **IPs**:
  - ~30 IP blocks have been defined
  - Good progress on defining who makes what.
  - Needs to define how to make IPs
- **SiMULATION**:
  - Prototype **framework** implemented in system Verilog + UVM
  - Benchmarked tool chain with FEI4 behavioural and gate level model
  - Framework will be used for initial comparison of different latency buffer architectures (critical for CMS with long trigger latency)
  - Starting to work on making realistic hit patterns/rates and link to Geant 4 simulations
- **TOP**:
  - Discussions have started on appropriate design methodology to implement large complex mixed signal IC.
  - Global architecture proposals will be collected and a program to compare/simulate these will be defined.
- **IO**: Not yet started

RD53 Outlook

2014:

- Release of CERN 65nm design kit: Very soon !
- Detailed understanding of radiation effects in 65nm
  - Radiation test of few alternative technologies.
  - Spice models of transistors after radiation/annealing
- IP block responsibilities defined and appearance of first FE and IP designs/prototypes
- Simulation framework with realistic hit generation and auto-verification.
- Alternative architectures defined and efforts to simulate and compare these defined
- **Common MPW submission 1**: **First versions of IP blocks and analog FEs**

2015:

- **Common MPW submission 2**: Near final versions of IP blocks and FEs.
- **Final versions of IP blocks and FEs**: Tested prototypes, documentation, simulation, etc.
- IO interface of pixel chip defined in detail
- **Global architecture defined and extensively simulated**
- **Common MPW submission 3**: Final IPs and Fes, Small pixel array(s)

2016:

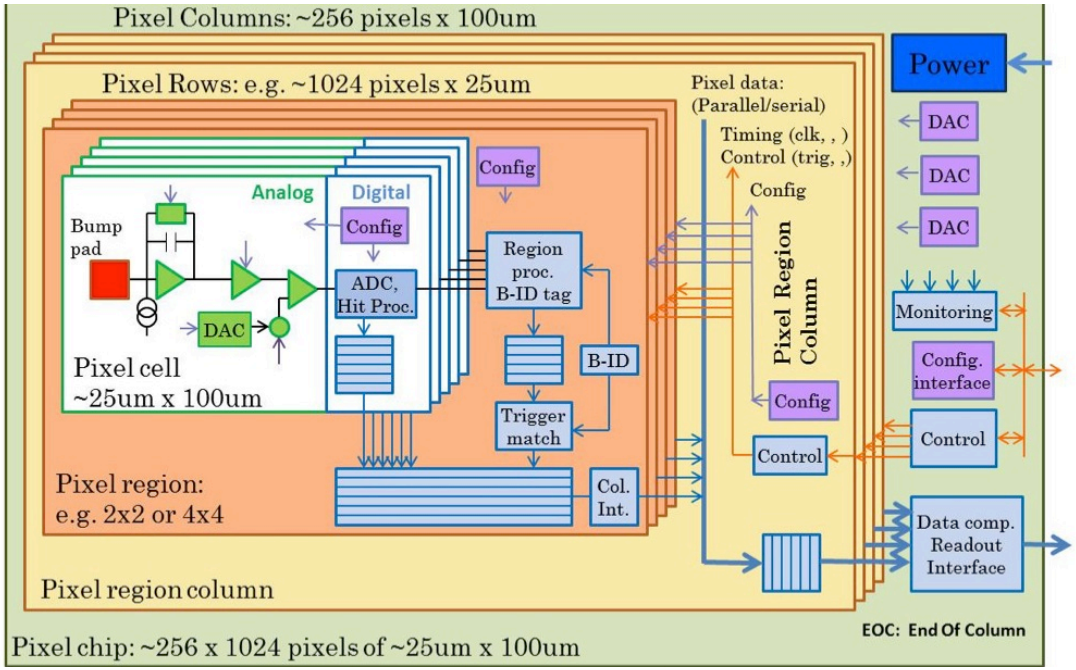
- Common **engineering run**: Full or reduced sized pixel arrays(s).
- Pixel chip tests, radiation tests, beam tests , ,

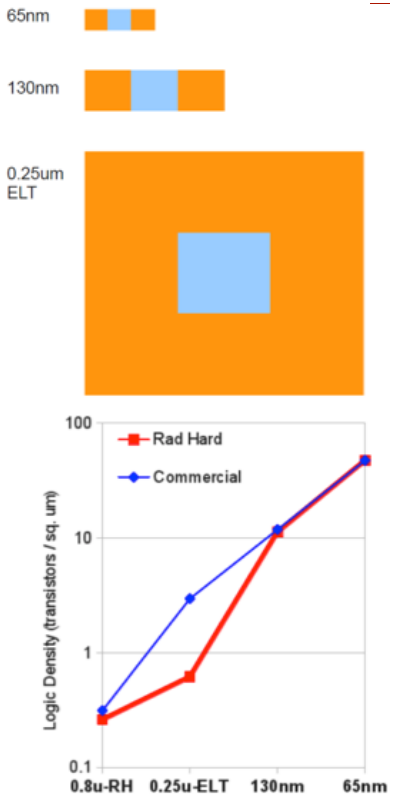
2017:

- **Separate or common ATLAS – CMS full – final pixel chip submissions**.

RD53 Chip architecture

CMOS 65nm: 16x smaller than 0.25 um

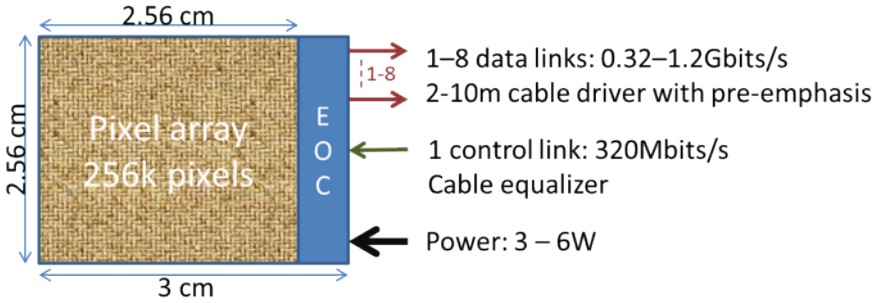




Pixels: ~256k, Chip size = ~2.6cm x ~3cm
~1G transistors, ~3Watt (~10uW per pixel; 0.4 W/cm^2)

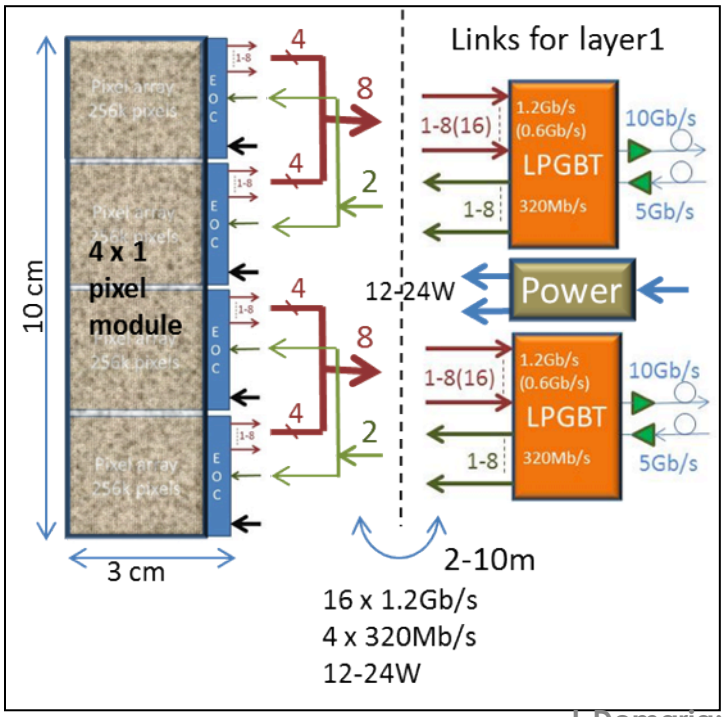
ReadOut and Configuration: assumption is to use the Low Power version of GBT, called LP-GBT and under-development in 65nm (up to 10 Gb/s output; 5 Gb/s input)

Constrains on FE-chip:
CMS case for L1@1 MHz

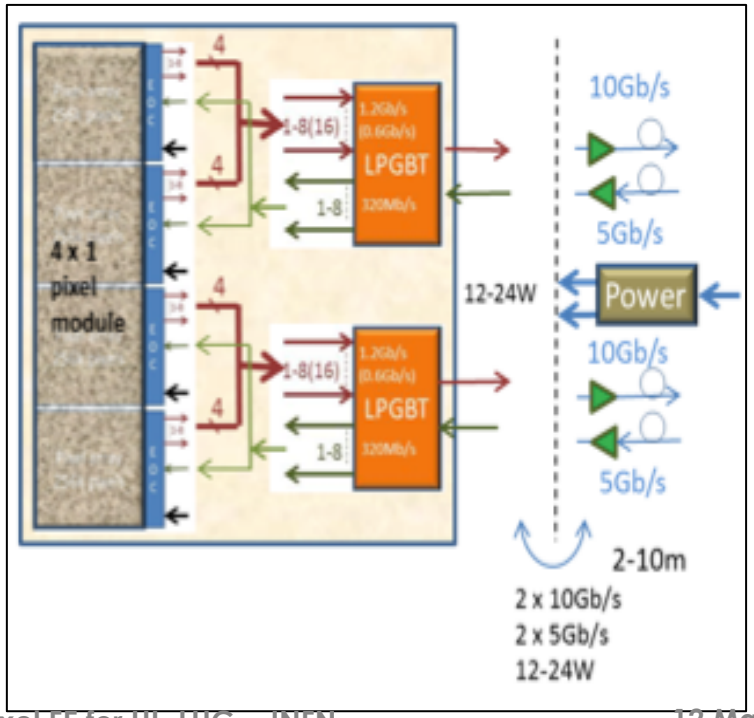


Overall Band Width defined by the L1 trigger rate and the Band Width of LP-GBT: 4x1 CHIP modules in L1, with TWO LP-GBT

LP-GBT well outside Pixel:
Lots of cable but less cooling



LP-GBIT on module: rad-hard? Power and cooling increased, cable. Place for LP-GBT



INFN interest in Pixel-FE

- Started on year 2010 with four CMS institutes (To, Pg, Pi, Pd) and on 2011 we had approved an initial funding. Collaboration with FNAL already started.
- On 2013 six INFN institutes took part to the foundation of **RD53 Collaboration**: Bari, Padova, Pavia, Perugia, Pisa, Torino
- On 2013 the Scientific Committee of INFN for Technological Research launched a call for large R&D projects and we submitted the proposal **CHIPIX65** that eventually was selected in October 2013. In the project both CMS and ATLAS groups/members were invited
  - Milano group joined, has large experience in 65nm with the FTK Atlas project

NB: if you see few names cited in slides are those of PhD students or young PostDoc working actively to the shown item (together with experienced staff)

CHIPIX65 CALL Project Proposal 2013 – CSN5

Principal Investigator: L.Demaria

Project Outline (from Project Abstract)

- The goal of this three years project is the development of an innovative **CHIP** for a **PIX**el detector, using a CMOS **65**nm technology for the first time in HEP community, for experiments with extreme particle rates and radiation at future High Energy Physics colliders. New circuits will be built and characterized, a digital architecture will be developed and eventually a final assembly of a first prototype will be made.
- CHIPIX65 **a unique opportunity for an efficient propagation across INFN of CMOS 65nm** technology and constitutes the **greatest collaboration on a microelectronics project ever made across INFN**.

Participant Research Units: Bari, Milano, Padova, Pavia, Perugia, Pisa, Torino

35 members of which 20 are micro-electronics designers. **9.85 FTE**. 6 units involved in CMS, 1 in ATLAS. New members from this year (2 new PhD students)

Work Packages:

- **Radiation Hardness** – P.Giubilato (Padova)
- **Digital Electronics** – R.Beccherle (Pisa)
- **Analog Electronics** - A.Rivetti (Torino)
- **Chip Integration** - V.Re (Pavia/Bergamo), V.Liberali (Milano)

International Collaborations / supports: RD53, ATLAS, CMS – All wrote support letters

Funding: ~700 kEuro for a three year project, subject to yearly peer review (milestones achieved).

- Mainly consumables and foundry submissions, no man power.

CHIPIX65 + RD53/INFN members

- **Bari**: Fabio Ciciriello, Francesco Corsi, Giuseppe De Robertis, Flavio Loddo, Camillo Tamma, F.Liciulli, Cristoforo Marzocca
- **Milano**: Valentino Liberali, Seyedruhollah Shojaii , Alberto Stabile
- **Padova**: Marta Bagatin, Dario Bisello, Lili Ding, Piero Giubilato, Alessandro Paccagnella, Nicola Bcchetta, Martino Dall'Osso, Stefano Gerardin, Andrea Neviani, Alessandro Paccagnella, Daniele Vogrid, Jefferey Wyss
- **Pavia/Bergamo**: Francesco De Canio, Lorenzo Fabris, Luigi Gaioni, Massimo Manghisoni, Valerio Re, Gianluca Traversi, Carla Vacchi, Alessia Mannazza, Lodovico Ratti, Stefano Zucca
- **Perugia**: Gian Mario Bilei, Elia Conti, Mauro Menichelli, Daniele Passeri, Pisana Placidi, Sara Marconi
- **Pisa**: Fabrizio Palla, Guido Magazzu, Fabio Morsani, Roberto Beccherle, Massimo Minuti, Maria Teresa Grippo, Luca Fanucci, Ronaldo Bellazzini, Andrea Rizzi, Sergio Saponara
- **Torino:** Natale Demaria, Pierluigo Civera, LucaPacher, Angelo Rivetti, Manuel Rocha Rolo, Ennio Monteil, Gianni Mazza

CHIPIX65:
Main Contributions to RD53

	RADIATION HARDNESS	SIMULATION TEST Benches	ANALOG FRONT END	IP-BLOCKS (see next slide)	I/O	Top Level
Bari				yes	To be discussed in RD53	To be discussed in RD53
Milano				yes		
Padova	X-ray machine SIRAD facility			yes		
Pavia			Design of VFE	yes		
Perugia	expertise in space rad-hard	Architectural studies				
Pisa		Clusterizer, L1		yes		
Torino			Design of VFE	yes		

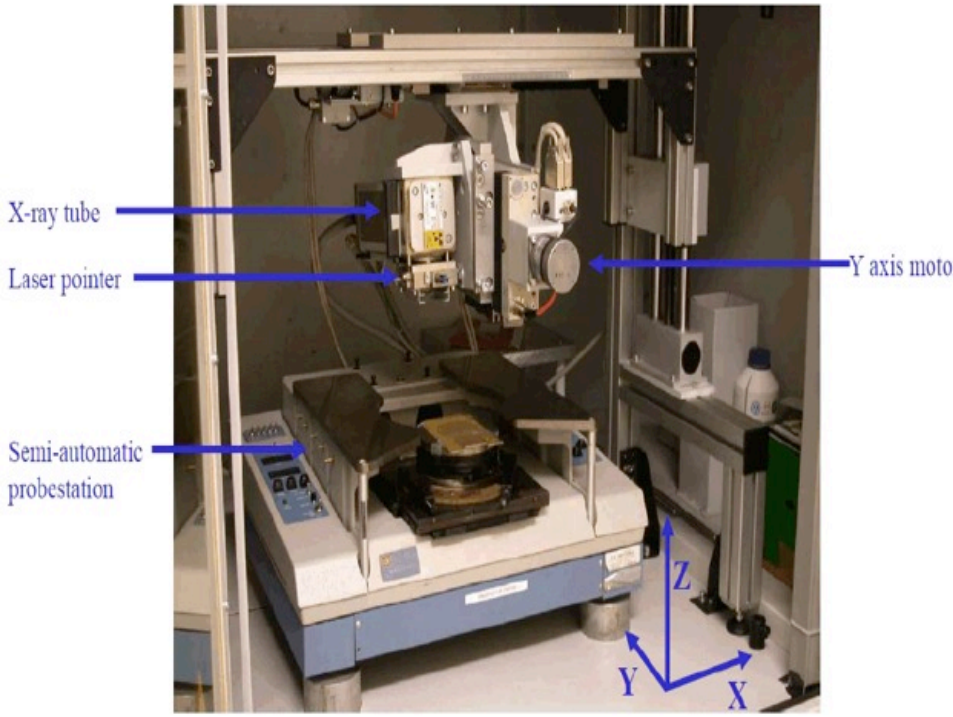
Additional contribution to I/O and Top Level are foreseen

CHIPIX65: Radiation Hardness

Characterization of the technology at the required radiation levels is of fundamental importance for the experiment. In particular:

- TID (Total Ionising Dose) Total effects on test structures and then on transistors at standard, reference,
  - X-ray machine
  - CN accelerator at LNL (low energy protons)
- DD (Displacement Damage) effects by exposing test structures to **proton** and **neutron** beams.
  - the SIRAD irradiation facility at the LNL Tandem+ALPI accelerator system
  - The CN accelerator at LNL
- Sensitivity to **SEE** (Single Event Effects) of logic cells with ion beams, in particular to
  - ion beams at the SIRAD+IEEM irradiation facility at the LNL Tandem+ALPI accelerator system

X-ray at Padova

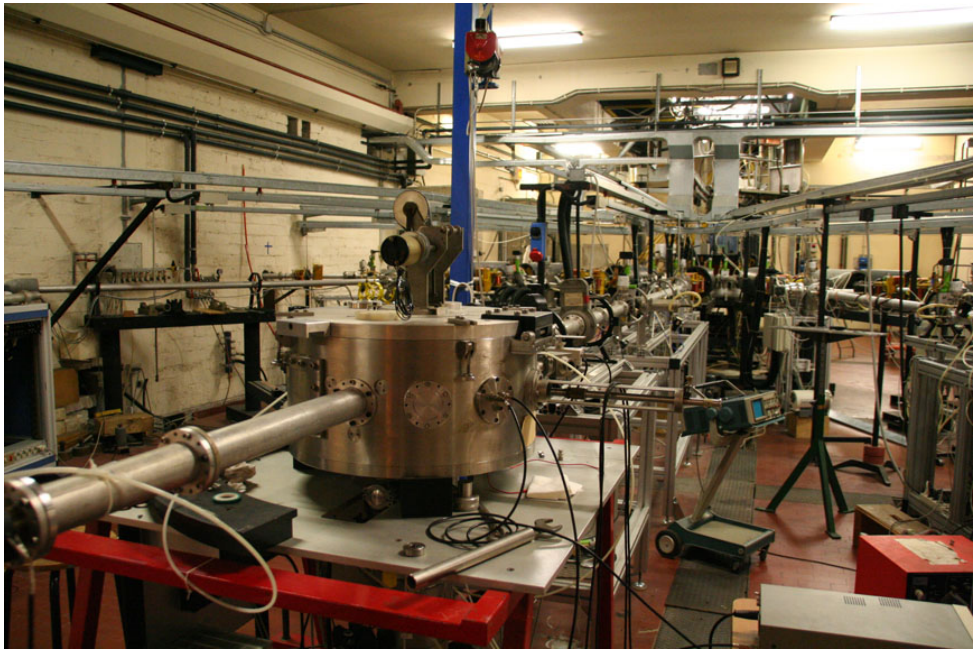


At **D=1 cm** from the sample with I=50 mA it is possible to reach **2000 rad(Si)/s** (7.2 Mrad(Si)/h or 4.2 Mrad/h (SiO_2) on a **square area 5 mm^2**.

1w to reach 1 GRad

Protons at CN Accelerator (Laboratori Nazionali di Legnaro)

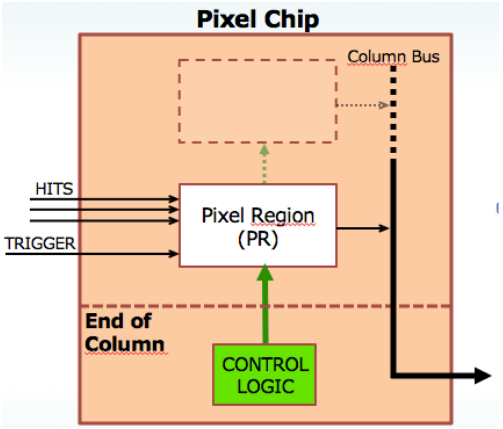
- Monoenergetic protons with energy between 2 MeV and 6 MeV
- Maximum proton current ~ 1 μA (1 Grad can be reached in few hours, if needed)
- Samples are placed in a vacuum chamber
- Used for total ionizing dose and displacement damage studies in electronic chips for space applications

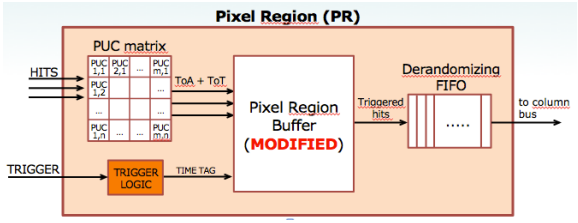


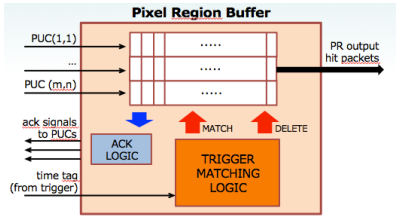
First irradiation of CMOS 65nm test structures with low energy protons for Total Dose study. Few TID points will be taken, up to 1 Grad and for few I Identical test structures

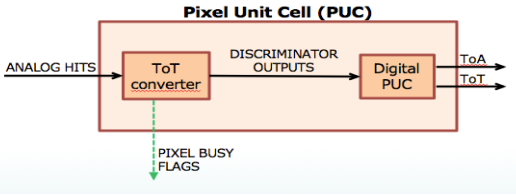
Planned for **31st March**

CHIPIX65: Digital architecture

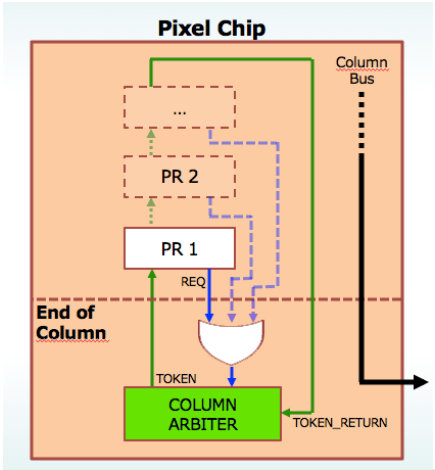






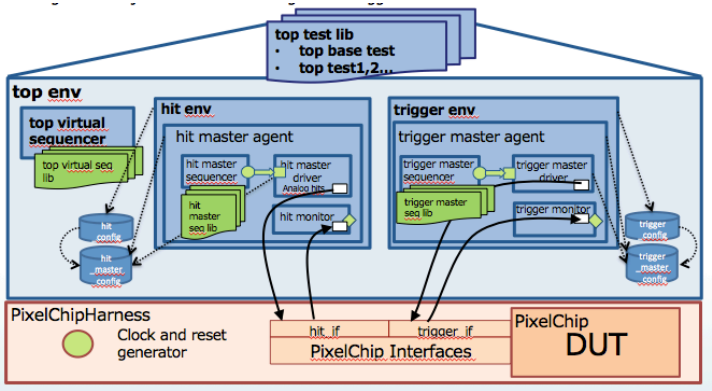


- Single pixel region with custom number of pixels
- PR buffer is an array of SystemVerilog queues



E.Conti, S.Marconi (Pg)

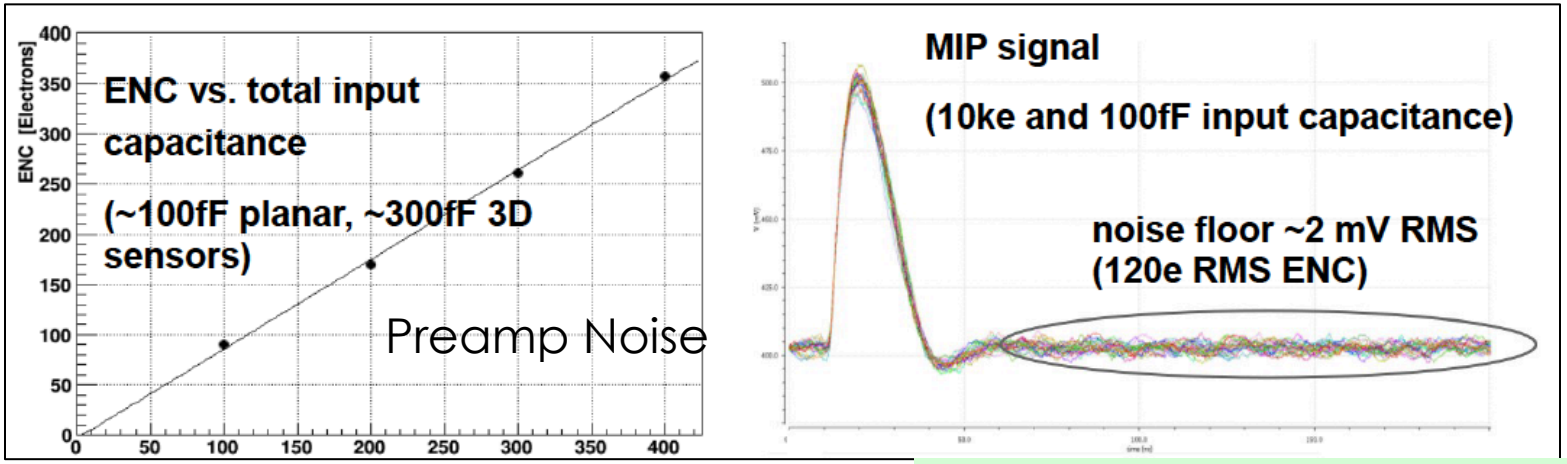
Verification Environment



Used Universal Verification Methodology (UVM)

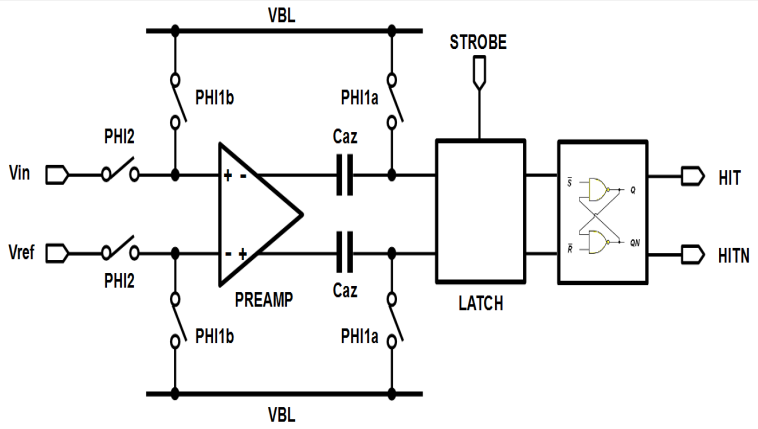
CHIPIX65: Very Front End

- Amplifier (CSA) with different feedback architectures (Krummenacher, Constant current, Discrete time)
- Asynchronous front-end (Bg/Pv)
- Synchronous front end (Torino)
  - Off-set compensation (Self-Calibration of threshold trimming)
- Different Signal Measurement
  - ToT-based, ADC, binary
- Signal injection and calibration

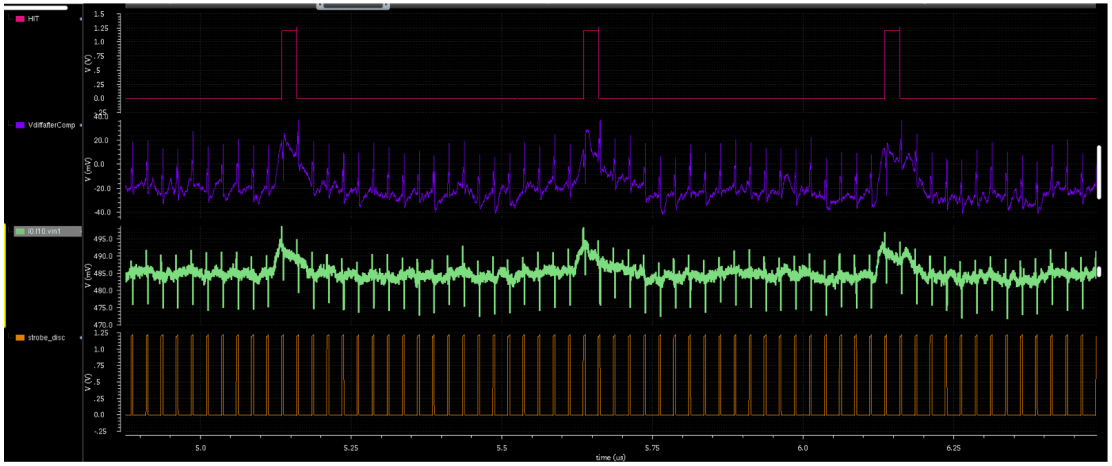


L.Pacher, E.Monteil (Torino)

Very Front End :synchronous comparator



- Always in-time answer
- No discriminator delay (threshold timewalk)
- Possibility of threshold variation self-calibration



- >50% efficient for 1000e- signal
- Tested for mismatch (process variations)

HIT generation

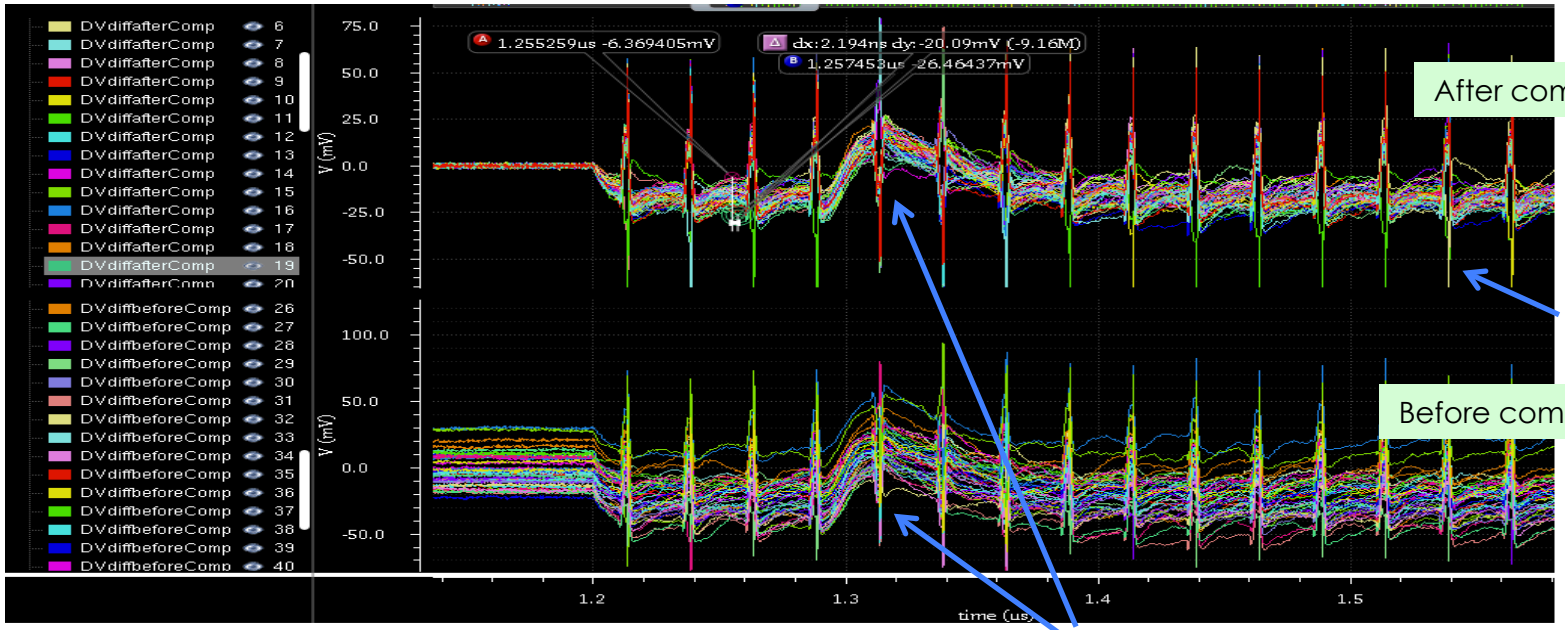
Input signal to Latch

CSA output (1000e-)

25ns strobe to comparator

Very Front End: self compensation of threshold variation

- No need for off-line calculation of threshold trimming
- Trimming calibration done by hardware (calibration cicle)
  - Process variation causing ~1500e- peak-to-peak threshold variation, normally corrected by off-line threshold trimming
  - Self-calibration compensate for those variation (<500e- peak-to-peak)



CHIPIX65: IP Block for RD53

Group		Bari	Pav/ Berg	(Milano)	Padova	Pisa	Torino
ANALOG: Coordination with analog WG							
Temperature sensor.							
Radiation sensor	to be evaluated						O*
Band gap reference	O		O				
MIXED							
8 – 12 bit biasing DAC	O	O					
10 - 12 bit slow ADC for monitoring	O	O					
PLL for clock multiplication	P				P	P	P
High speed serializer (~Gbit/s)	P					P	
(Voltage controlled Oscillator)	x				x	x	x
DIGITAL							
SRAM for pixel region	O			O			
SRAM/FIFO for EOC.	P			P			
DICE storage cell ?	O			O			
LP Clock driver/receiver	P		P				
(Dedicated rad hard digital library)	to be clarified					x	
(compact mini digital library for pixels)	to be clarified					x	
IO: Coordination with IO WG							
Low speed SLVS driver (<100MHz)	O		O			P	P
High speed SLVS driver (~1Gbits/s)	O		O			P	P
SLVS receiver	O		O			P	
POWER							
LDO(s)	P					P	P
SOFT IP: Coordination with IO WG							
Control and command interface	O	P				O*	
Readout interface (E-link ?)	O	P				O*	

Out of 34 IP-block identified in RD53, INFN has proposed to contribute at ~16 of them:

- as main organizer (11)
- as participant (5)

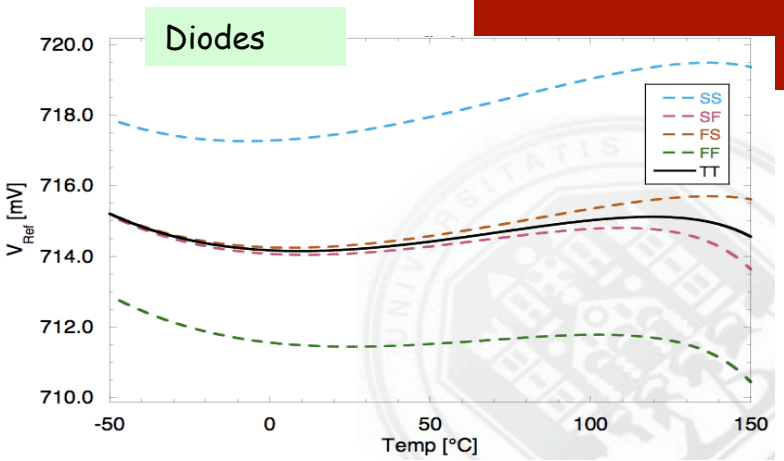
In the following few slides on first prototypes ready for submission in a short time (design in 65nm already present):

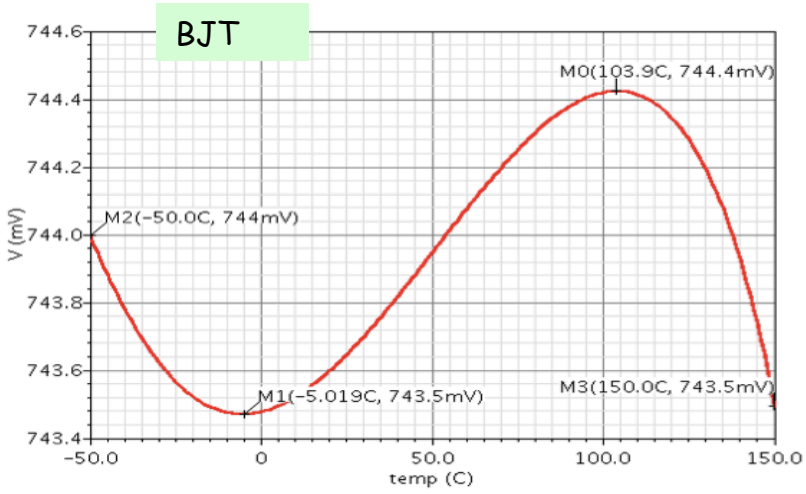
- Band-Gap
- SLVS driver
- SRAM

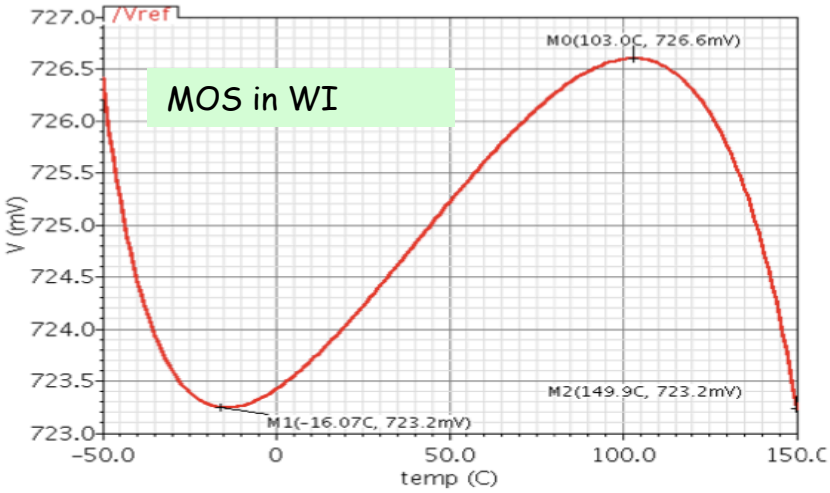
others IP-blocks could be ready for end of year

Band Gap reference (**Pv**)

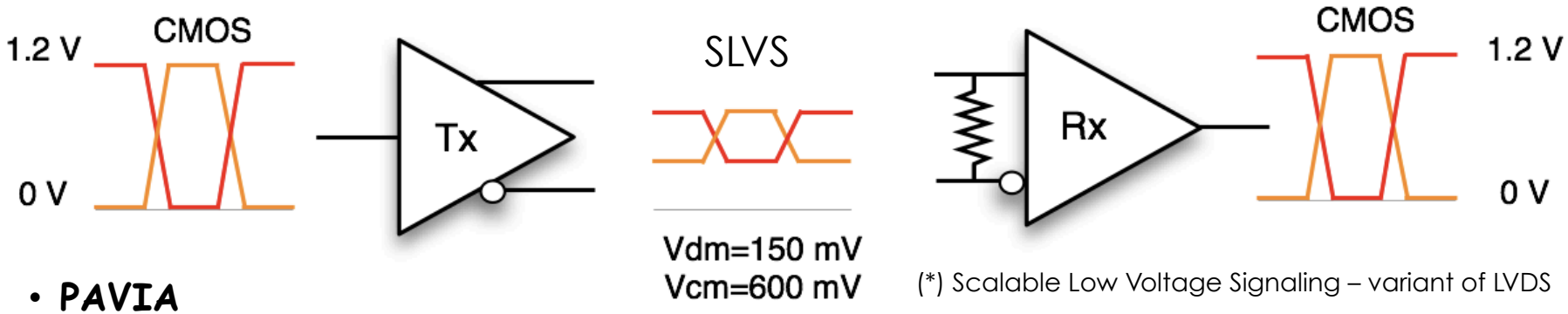
- State of the art at Pv:
  - Sub 1V operation bandgap voltage reference – 3 versions
    - (1) BJT version ; (2) Diode version ; (3) MOS WI version
  - **Layouts ready**
- Evaluate their performance and study their radiation hardness







Low-Medium / High speed SLVS* driver (Pv, To, Pi)



(*) Scalable Low Voltage Signaling – variant of LVDS

- **PAVIA**

✓ Design of low-voltage differential signaling driver + receiver with supply voltage of 1.2V (with only core transistors)

✓ Present activity:

  ✓ Design 1: 320MHz frequency operation with maximum power consumption=1.25 mW

  ✓ Design 2: 640MHz frequency operation with maximum power consumption=2.5 mW

✓ Schematics of the TX and RX were obtained by a merging of the UniBG and CERN version (in 130nm IBM) provided by Kostas

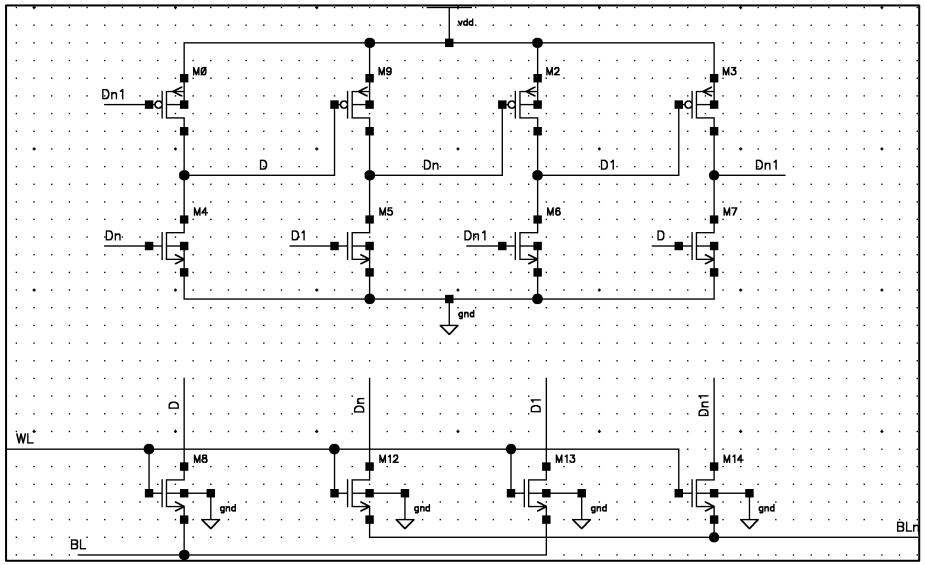
- **Torino**

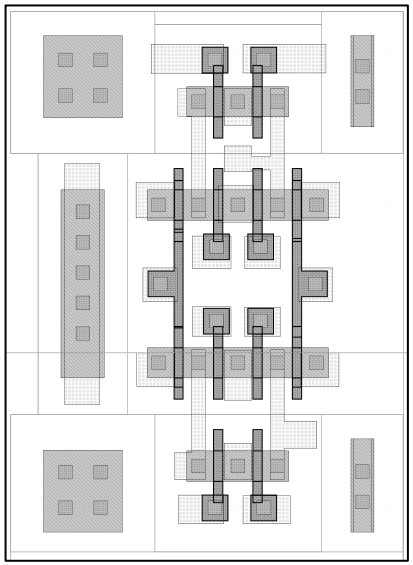
✓ There are design in 130nm for Panda (ToPix) that goes to 1 GHz and could be translated in 65nm

- **Pisa** is also interested

DICE RAM Cell (**Mi**)

- Interest of Milano (in CHIPIX65, applying for RD53) to develop radiation hard SRAM
- array of 256x256 DICE (Dual Interlocked storage Cell) RAM cells **almost ready for integration.** It comes from a work done in AIDA. Size of about 1.8x3.3 um^2
  - Layour made in three different version, one smaller (size about 1.8x3.3 um^2) the other more resistant to latch-up and/or Single Event Upset
- This could be used either in the **Pixel Unit Cell** or in the **End Of Colum**





Schematics

Layout V.1

A.Stabile, J.Shojali (Milano)

CHIPIX65 Milestones

Descrizione	Data completamento	
Results on Basic radiation test structures	30-10-2014	WP1
Test results on first Analog Blocks and Very Front End chain	30-11-2014	WP3
Test of digital basic IP blocks	30-09-2015	WP2
Digital architecture: pixel/region basic models in SystemVerilog	30-07-2015	WP2
Definition of Very Front End analog architecture	30-09-2015	WP3
Measurement with ion beam of SEU rate in digitasl cells	30-11-2015	WP1
Qualification of 65nm technology to 10 MGy TID, 10**16 n/cm2	30-11-2015	WP1
Ready for chip integration of prototype	15-12-2015	WP4
Definition of digital Architecture of chip Prototype	30-03-2016	WP2
Mixed signal blocks functional and radiation test results	30-03-2016	WP1 / 2 / 3
Submission of prototype to foundry	30-07-2016	WP4
Test results of chip prototype	30-10-2016	ALL
Final Report	10-12-2016	

2014 : measurement of basic structure for WP1; design and testing for WP2, WP3;
2015 : TID and SEU characterization (WP1); definition of architecture (WP2, WP3); ready for chip integration
2016 : results on small pixel array; design of small chip prototype, its submission and test.

CHIPIX65 SUBMISSIONs for 2014

- INFN / CHIPIX65 is foreseeing to submit designs on silicon to the foundry via MPW:
  - Small pixel matrix for studies of Very Front End analog designs
    - Synchronous front end
      - Binary, off-set compensated
      - Fast ToT
    - Asynchronous FE
  - IP-block prototypes

For the pixel matrix important to establish the PUC dimension (25x100, 50x50 ?). to make the pixel matrix bump-bondable to a silicon sensor: this should be better evaluated.

Earliest submission: July 2014, Area: ~(3x4)mm^2.

- Other submissions: possibly sharing with other collaborators (specially for IP-blocks). Open discussion in within CMS and RD53.

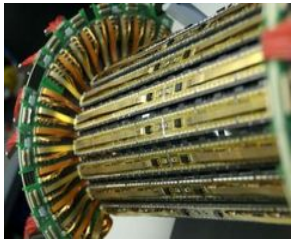
Conclusions

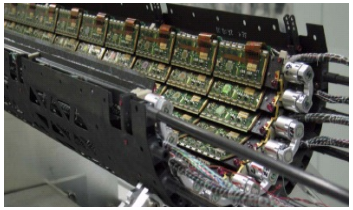
- INFN contribution to innovative pixel chip well structured and with presence of reputed experts in the field
  - CHIPIX65 project provide excellent synergy and coordination among institutes and finance oxygen for the R&D phase
- Good participation of INFN to the RD53 Collaborative effort and in all the area needed for the chip design
- Considerable experience already in hand on CMOS 65nm via Europractice. Now the CERN contract with TSMC / IMEC design kit for 65nm in order to speed up the work of designing in CMOS 65nm
- Right timing of RD53, CHIPIX65 for the R&D phase needed to eventually go to CMS and ATLAS pixel FE-chips ready for module prototypes in ~2018
- A wide experience in the CMOS 65nm to FE-electronics is important also for research areas other than pixel at HL_LHC

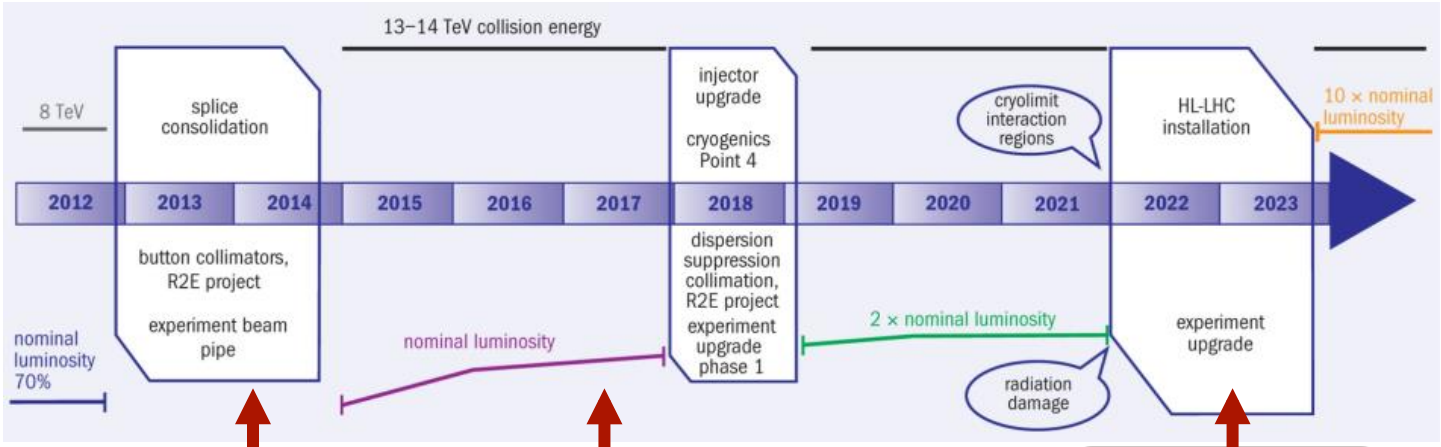
BACKUP SLIDES

Pixel Upgrades

- **Phase2 upgrades**:
  - Installation: ~ 2022-23 ➔ **First Modules prototypes should be ready for ~2018**
    - **Pixel chip R&D: needed NOW**
    - **Pixel Sensors R&D: needed NOW**
  - 3 years of dedicated R&D + 2 years to develop first prototype modules







ATLAS Pixel IBL

CMS Pixel phase1

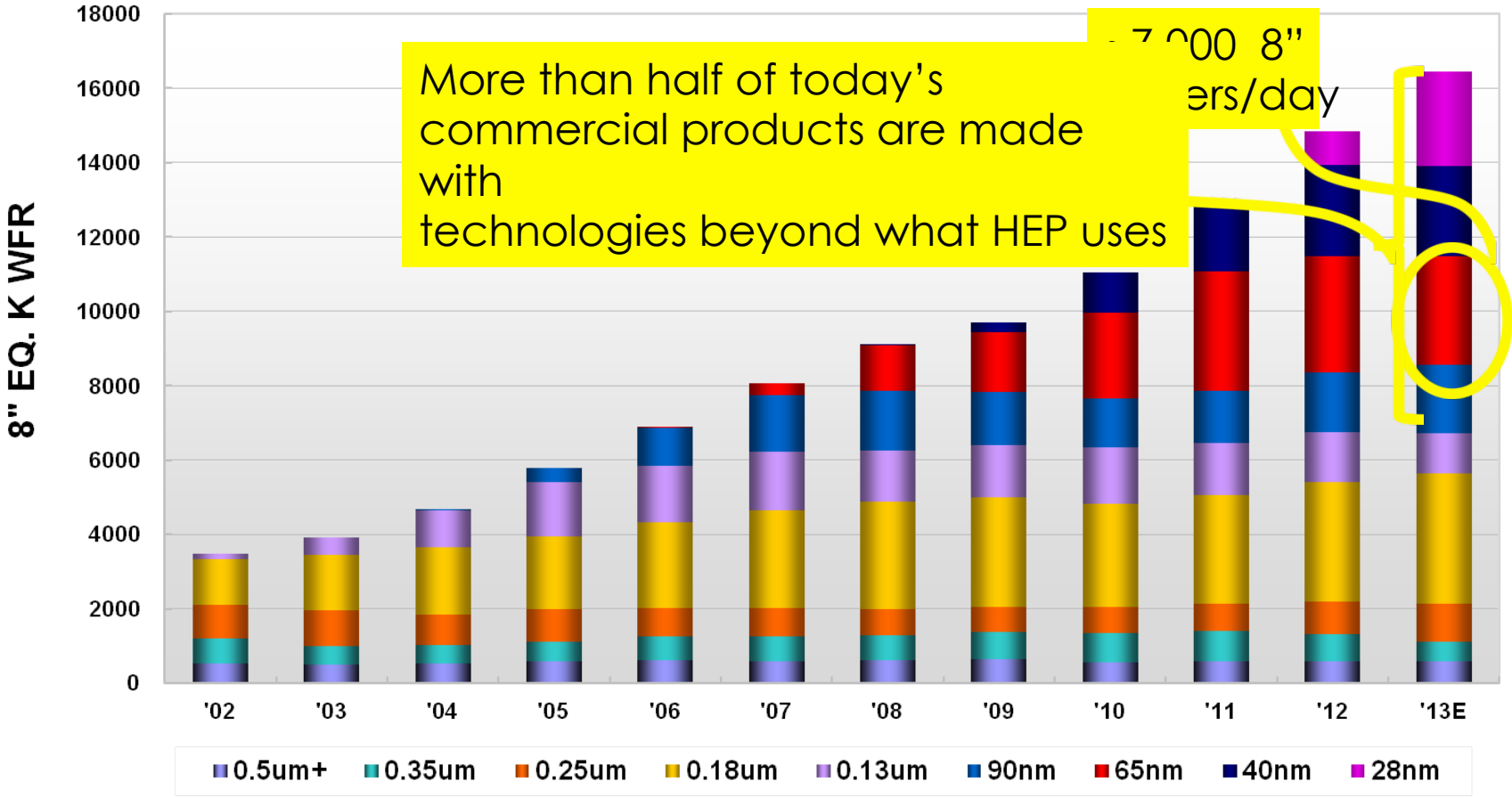
CMS & ATLAS phase 2 pixel upgrades

100MHz/cm^2

400MHz/cm^2

1-2GHz/cm^2

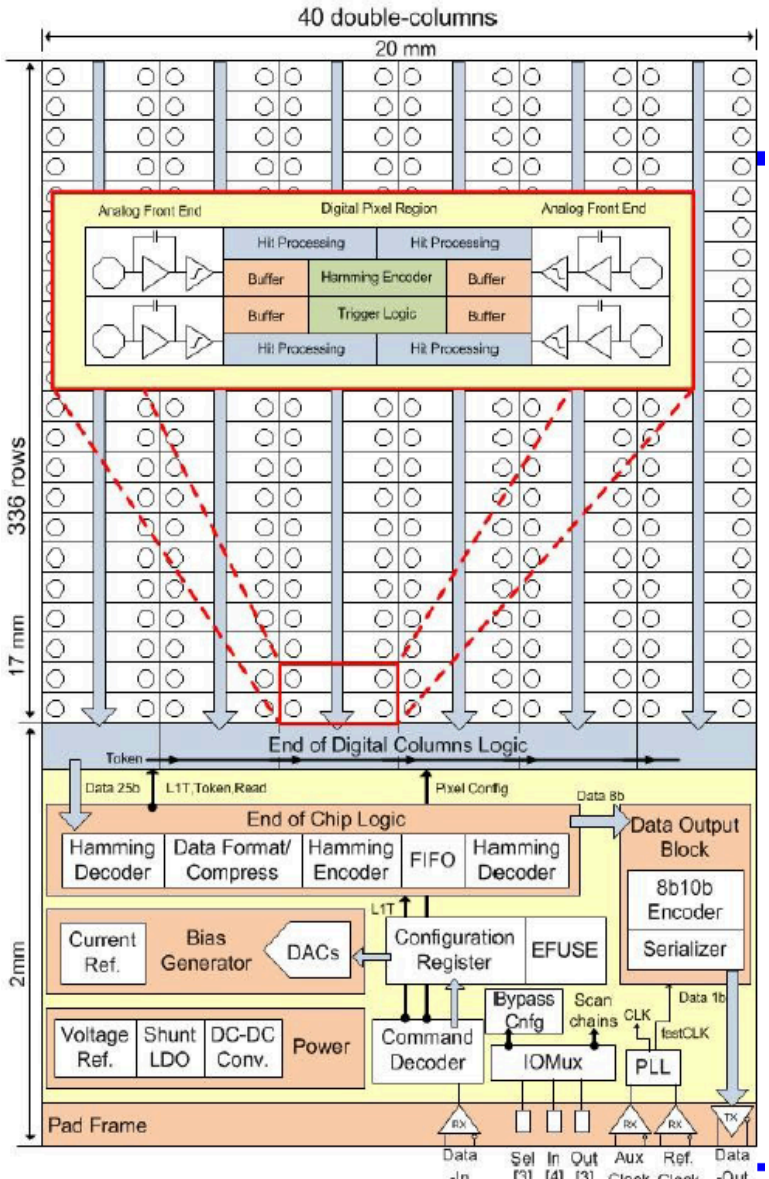
Installed Capacity by Technology



My Note: 0.25 um and 130nm production lines are STILL operational this makes 10-11 years of technology avalability…

Source: TSMC

Example of complex IC: FEI4 chip



Made by 5 institutes (Bonn, CPPM, Genova,LBNL, NIKHEF)

Team of 14 designers

Design responsibility split in several parts (or IP-blocks):

- Shuldo
- DC-DC
- Vref
- Cref
- ADC
- Efuse
- Cal Pulse
- Alt. SEU
- Alt. Comp
- CapMeas
- ConfSR
- PLL
- DAC
- Config.Register
- Command Decoder
- **Front End**
- Digital Double Column
- End of Digital Column
- End of Chip Logic
- Data Output Block
- MUX3to1
- LVDS-rcvr
- LVDS-drvr

CHIPIX65 Research Units

Unit		Unit Responsible	FTE Unit	No. of members	No. of designer	Involvements in CHIPIX65
1	Bari	LODDO Flavio	1.65	5	3	WP2, WP3
2	Milano	LIBERALI Valentino	1.0	3	3	WP2,WP3,WP4
3	Padova	BISELLO Dario	1.6	5	1	WP1,WP3
4	Pavia	TRAVERSI Gianluca	1.5	7	4	WP1,WP3,WP4
5	Perugia	PLACIDI Pisana	1.4	5	3	WP1,WP2
6	Pisa	PALLA Fabrizio	1.15	5	3	WP2,WP4
7	Torino	DEMARIA Natale	1.55	5	3	WP2,WP3,WP4
		TOTAL	9.85	35	20	

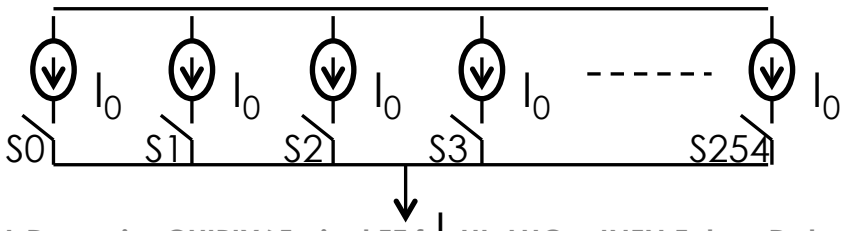
Detailed short description for every unit in following slides: I will not go through all of them in detail, they are there for reference

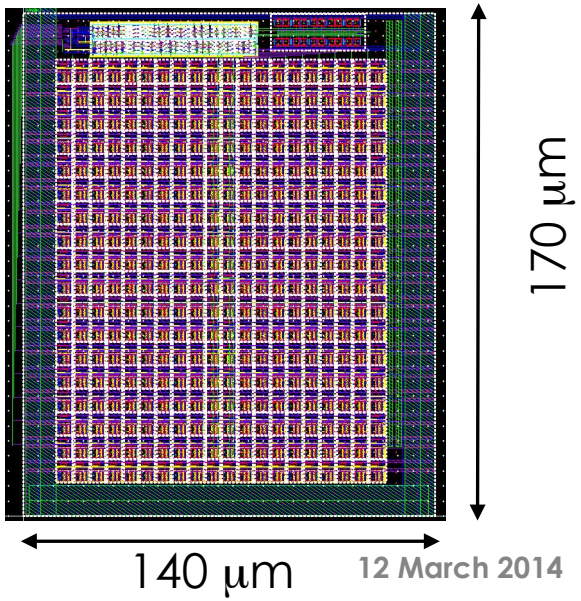
8-12 bit programmable biasing DAC (Ba)

- **Previous** experience of Bari:
  - Rad-hard 8-bit DAC for the slow control of the pixel chip of ALICE (250 nm CMOS)

- **In progress**: VFAT3, a new FE chip for GEM detectors for the upgrade of CMS muon detector (130 nm CMOS). Submission on Feb. 2014
  - **Calibration & Bias circuitry, 8-bit thermometer coded current steering DAC, Constant Fraction Discriminator**

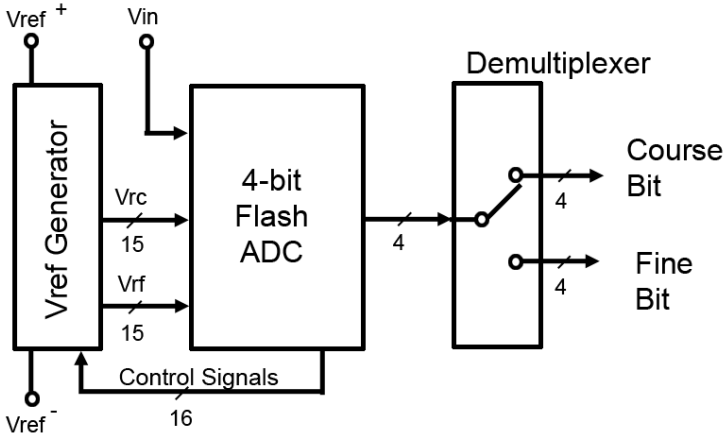
Thermometer coded DAC: 255 "identical" unit current sources connected to output node through switches controlled by a binary-to-thermometer decoder
- **monotonicity is guaranteed**
- **matching conditions more relaxed → common centroid is not required**





10-12 bit slow ADC for monitoring (Ba)

- **Previous** experience of Bari:
  - Two-step 8-bit ADC with max. conversion speed: 20 MS/s (0.35 μm CMOS)

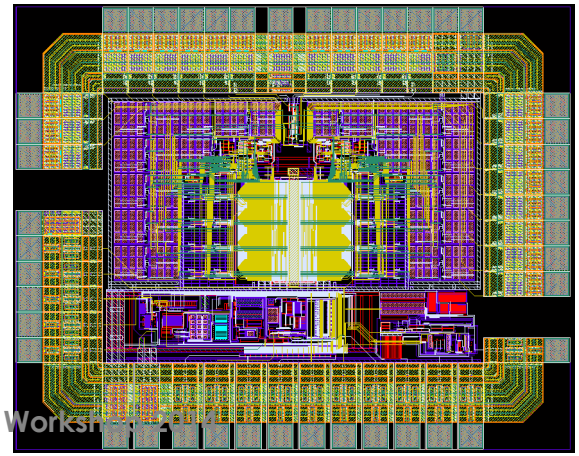


Reference generator: resistor ladder (same as full flash ADC)

"Coarse" (MSBs) conversion phase: the "coarse" refs Vrc are compared with Vin and the "fine" refs Vrf are selected

"Fine" (LSBs) conversion phase: the selected Vrf's are compared with Vin.

- ***Correction logic for both "bubble" errors and wrong "fine" threshold selection***
- ***Boost circuits for the clock phases applied to the CMOS switches***
- ***Final ADC structure: two ADCs, operated in "interleaved" mode***
- ***Total power consumption: 22.4mW***
- ***Maximum conversion speed 20MS/s***



Test chip

(2.18 x 1.74 mm^2)

PLL and VCO design expertise (**Pd**, Pi, To)

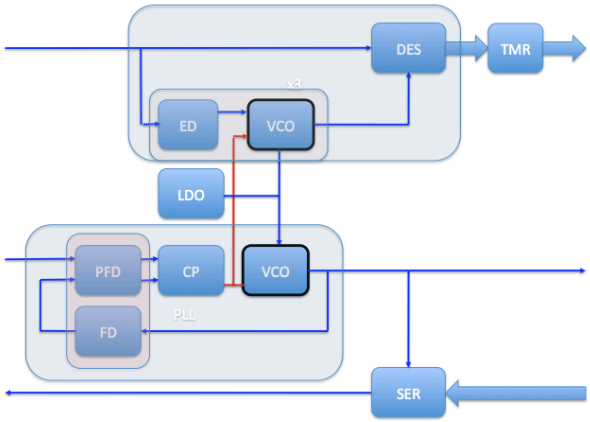
- Padova group (University of Padova – Engineering department)
  - Research group expertise:
    - RF design, Baseband design, Testing and characterization
    - Radiation testing and qualification (Engineering department)
  - Design of a 6.5-18.4 GHz PLL in 65nm CMOS for the local oscillator (LO) generation in a short-range radar front-end (M. Caruso et al., proceedings of ESSCIRC 2013)
  - Design of a 13-15 GHz, LC tank VCO for the local oscillator (LO) signal of a GSM transceiver in 65nm CMOS (S. dal Toso et al., IEEE Journal of Solid-StateCircuits, 2010)
  - Design of an LC tank VCO in 90nm CMOS for a fast-hopping LO generator operating between 6 and 9 GHz based on sub-harmonic injection locking (S. dal Toso et al., IEEE Int. Solid-State Circ. Conf., 2008)
- Pisa has expertise (see later)
- Torino interested too

Serializer (Pi)

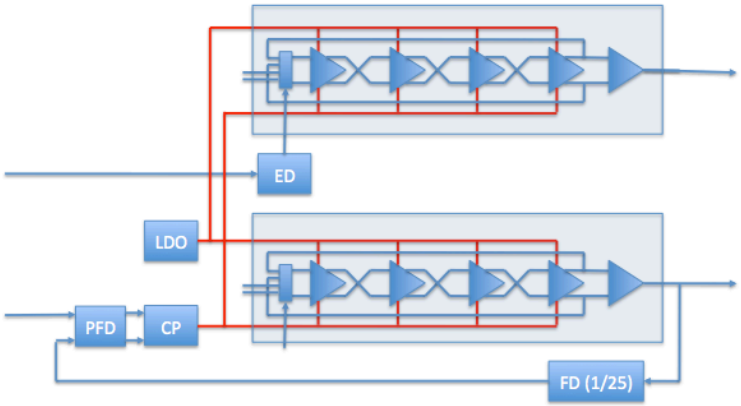
Based on experience on two ASICS designed in the IBM 130nm (2012-2013) Collaboration between INFN-PISA (Guido Magazzu) and UCSB (Physics Department and Electronic Engineering Department): Developments of radiation tolerant IP-cores for high speed serial links :

- UCCF1 (submitted 2012)
- UCCF2 (submission in early 2014)

- **Rescaling** of the IP-**cores into the TSMC 65nm** technology since February 2014 (submission of the first test ASIC foreseen in fall 2014)



- PLL and Clock Data Recovery (CDR) with Triple Modular Redundancy (TMR) to protect against Single Event Effects (SEEs)
- Same Serializer (SER) and Deserializer (DES) modules used in UCFF1



- Clock Data Recovery
- PLL with with x25 frequency multiplication (input frequency = 40MHz => output frequency = 1GHz)
  - Voltage Controlled Oscillator (VCO); Charge Pump (CP) => It provides the control voltage to the VCO module; Frequency Divider (1/25)
  - Phase/Frequency Detector (PFD) => It compares the frequency and the phase of the input reference clock and of the local reference clock and it generates the control signals for the Charge Pump
  - VCO modules (3x) => Same power supply and control voltages used in the PLL
- Low Drop-Out (LDO) regulator (providing power supply voltage to all the VCO modules)

Threshold Timewalk

- Example of FEI4 chip