# ALICE, ATLAS and CMS system architecture

***Marcello Bindi***

*Universita' e INFN Bologna*
*(University of Göttingen)*

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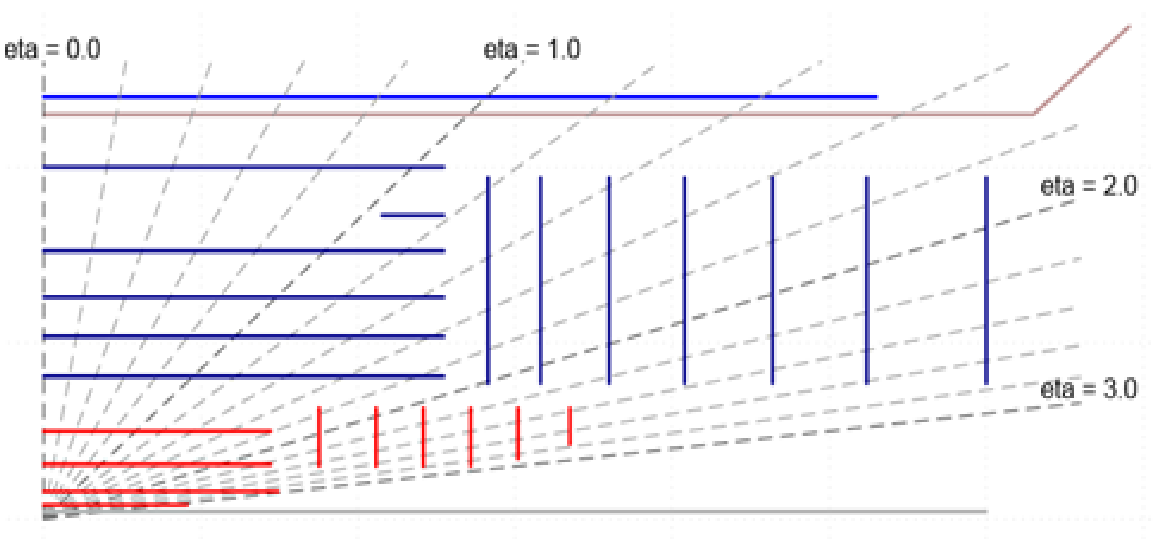
**Trento, March 11-13 2014**



# Outline

- Vertex & Tracking detectors of the 3 experiments: ALICE, ATLAS and CMS
- On detector transmission/GBT
- Off detector architecture/technology.
- Available technologies, R&D already started, R&D to be started.
- Conclusions

# ATLAS/CMS Trackers Upgrade requirements

- **Radiation hardness**
  - Ultimate integrated luminosity considered **~ 3000 $fb^{-1}$** (to be compared with original ~ 300/400/700 $fb^{-1}$)

  →Enhance radiation hardness by one order of magnitude!

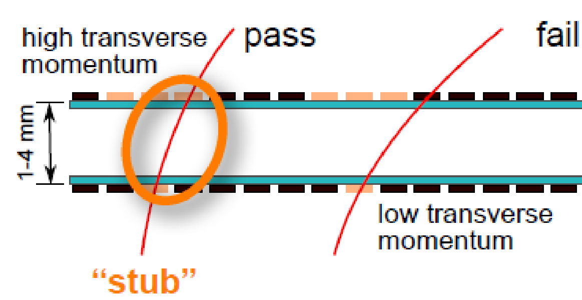
  From $10^{15}$ to **$10^{16}$ $n_{eq}/cm^2$**, 1 Grad for the inner layers of pixel
- **Bandwidth Saturation and Occupancy**
  - Resolve **~140 (up to 200**) of pile-up collisions, (the original design figure for the present trackers was 25!)
  - Maintain occupancy below % level

  →Requires much shorter strips and smaller pixels sizes!

  →Remove limitation between on-detector electronics and the read-out drivers card (ROD)
- **Mechanical constrains (replaceable, removable, retractable)**

# ATLAS/CMS Tracker Upgrade requirements/2

- **Improve tracking performance**
  - Improve performance @ low $p_T$
  - Reduce rates of nuclear interactions, g conversions, bremsstrahlung…
    - **Reduce material in the tracking volume**
  - Improve performance @ high $p_T$
    - **Reduce average pitch**
- **Tracker input to Level-1 trigger**
  - μ, e, jet rates would substantially increase at high luminosity
  - Increasing thresholds would affect physics performance
  - Add tracking information at Level-1
  - Requires changes to detector FE electronics feeding trigger system

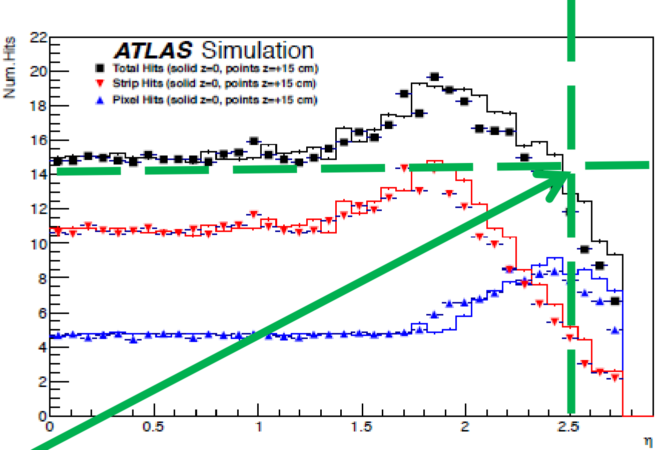



- **Goal for "track trigger":**
  - RoI(ATLAS) or self seeded(CMS)
  - Use info from L0 Trigger to reduce to 500 KHz(ATLAS) to 200Khz
  - Reconstruct tracks PT>2 GeV & ~ 1mm primary vertex resolution (CMS)

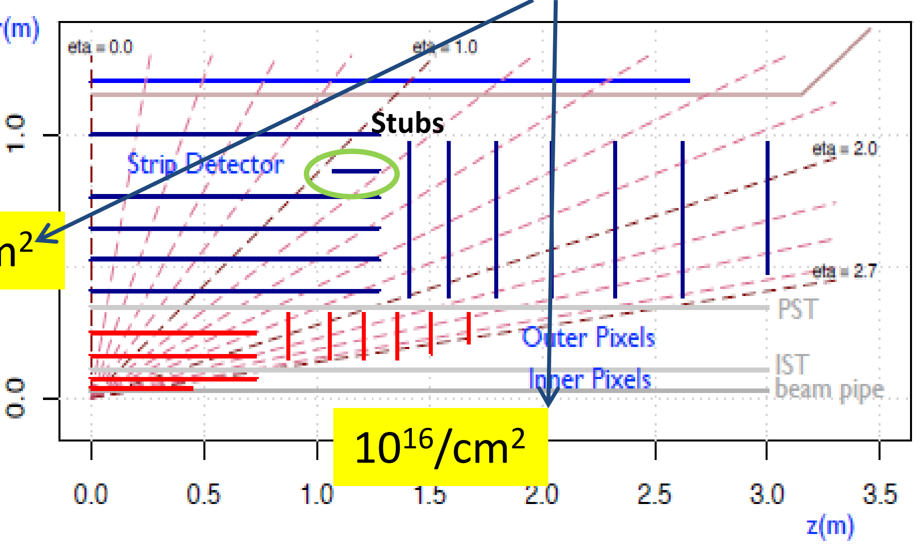
# ATLAS Inner Tracker Layout

- **Inner Pixels:**
  - **2 layers** close to enlarged Phase-2 beam pipe
  - smaller pixel pitch to improve b-tagging (FE-I5)
- **Outer Pixels:**
  - **2 barrel layers** at increased radii to improve tracking
  - pixel endcaps ensure full tracking coverage **to η=2.5**
  - some standalone tracking capability to **η=2.7** (muons)
- **Strip Detector:**
  - maximize momentum resolution (B·dl)
  - 5 barrel layers of double sided strip, 7 disk,
  - shorter strips close to PST to limit occupan
- Overall a 14 hit system down to η=2.5
  - robustness, avoid fakes at high pileup
  - much improved resolution
  - overall much reduced material budget

…..extension to eta=4 under study!

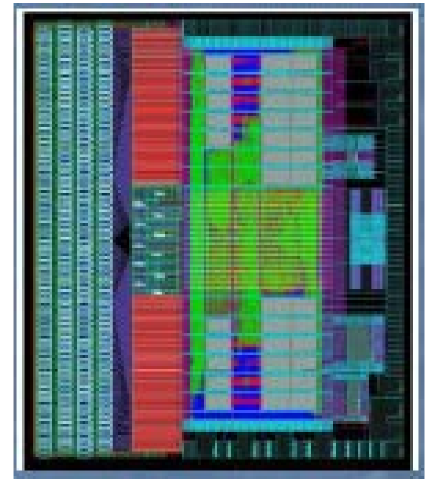



different technology options dependent on r (i.e. fluence)



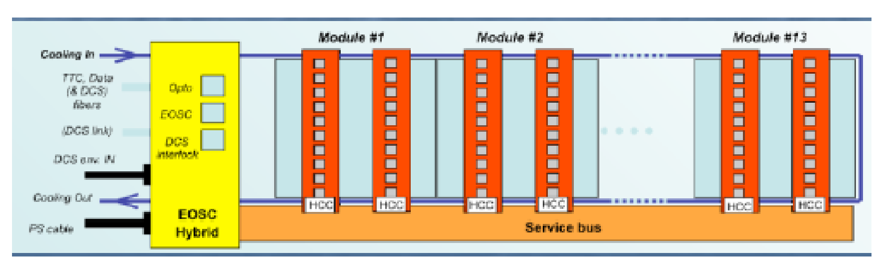
# ATLAS-Strips

- **Detector**
  - Inner: Short strips, Outer: Long strips
  - **~200 m²** (Replace current SCT and TRT)
  - 300k FE chips, ~75M channels
  - Radiation: <25 Mrad
- **Front-end** - Binary
  - Initial 250nm version made and extensively tested on strip modules
  - 130nm 256 channel chip for both short and long strips
  - **Two level trigger with Region Of Interest (ROI) readout**
    - **L0: Rate ~500kHz , Lat. ~6μs, 10% ROI**
    - **L1: Rate ~200KHz, Lat. ~20μs (max 256 events)**
  - **130nm version just submitted: Collaboration between 7 institutes**



ABC: 130nm FE chip

- **Readout**
  - 160 Mb/s e-links on module, 320 Mb/s e-inks from module to end of stave
  - **1 (2) LowPowerGBT** link at end of stave
- **Power -** Two approaches being evaluated:
  - Serial power at module level
  - DC/DC converter per module



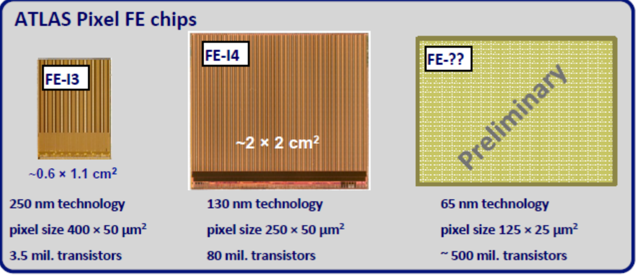

ATLAS strip with opto link per stave

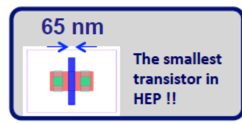
# ATLAS-Pixels

- **Detector:** A clear layout is still to be defined; attempt to improve **η** coverage

  Inner layers (r ~3 to 15 cm): low power; low material budget
  - Development of new sensor materials (planar, 3D-Si, diamond) already well underway
  - IC development based on FE-I4 "working horse" addressed by CERN R&D group RD53 for 65 nm

  → ~ 1 Billion transistors !!




  Outer layers (r>15 cm): low cost, low power

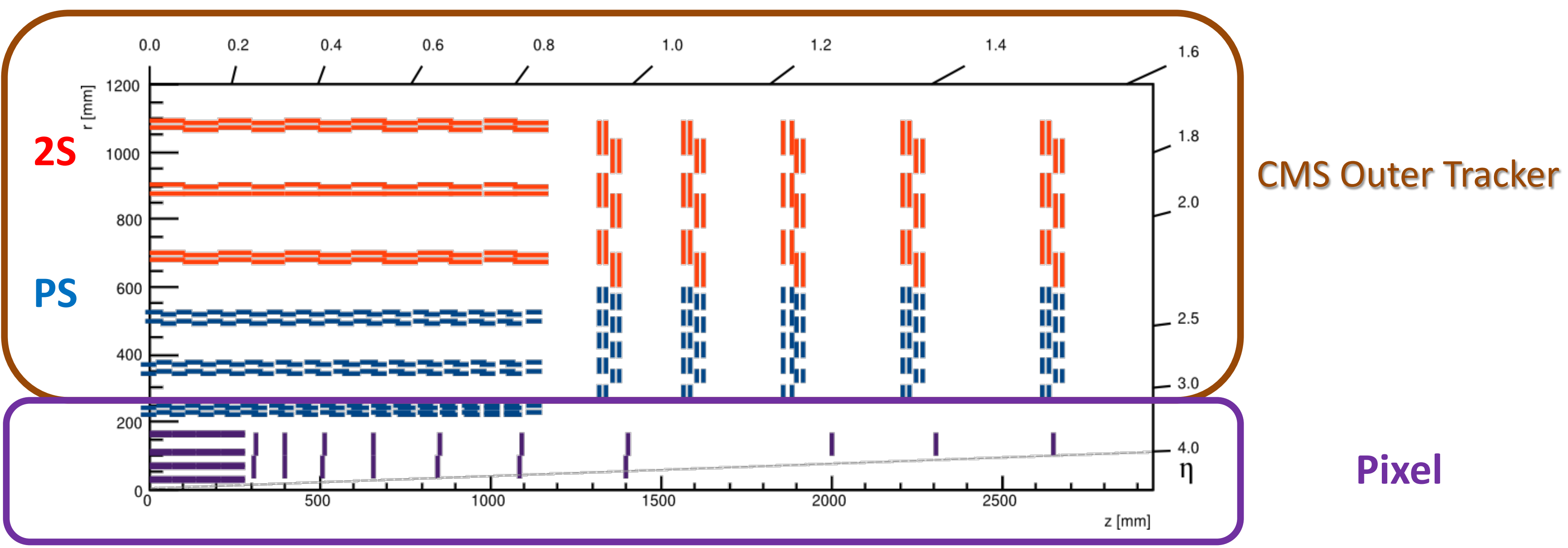
  Possibilities in the context of CMOS pixels (and also strips)... small pixel area/thickness could be attractive for the innermost layer, if radiation resistance allows.

- **Readout:**
  - **100x readout** rate: **~10Gb/s link required per pixel chip (inner)**
  - Opto parts can most likely not survive within pixel volume
  - Low power, low mass cable, high speed e-links to intermediate opto link

- **Power:**

  High power density and hostile radiation environment makes serial powering the most realistic option:
  - Requires R&D and qualification
  - Option: Combination with DC/DC ( e.g. on-chip switched capacitor)

# CMS Tracker Layout



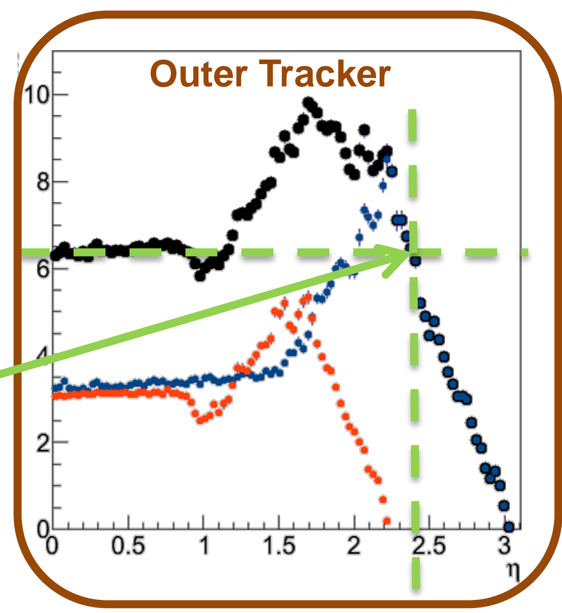

- Main features:
  - Higher granularity (x4 in strip sensors)
  - Radiation hardness (sensors operated at -20°C)
  - Reduced material budget
  - Provide information to Level-1 trigger

# CMS Outer Tracker

## Detector:

**Two-Strip (2S)** and **Pixel-Strip (PS)** modules allow for $p_T$ **discrimination on module level !**

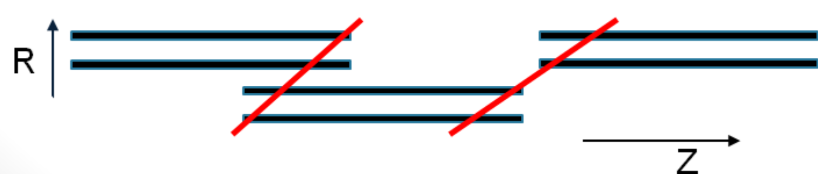
- 4 layers of strips → 2S
- 3 more layers of pixelated sensors → PS
    - Unambiguous 3d coordinates helps track finding in high pile-up
    - 12 hits up to η ≈ 2.4 available at Level -1
- Hermetic surfaces (cylinders and disks) for stub finding
    - Taking into account IP spread




## Front-end: Binary

2S: 130nm 256 channel strip FE chip (CBC) and module controller
2nd version of CBC under test on double strip module
Module controller chip architecture definition and design on-going.

PS: FE pixel chip in 65nm
Architecture defined and design on-going



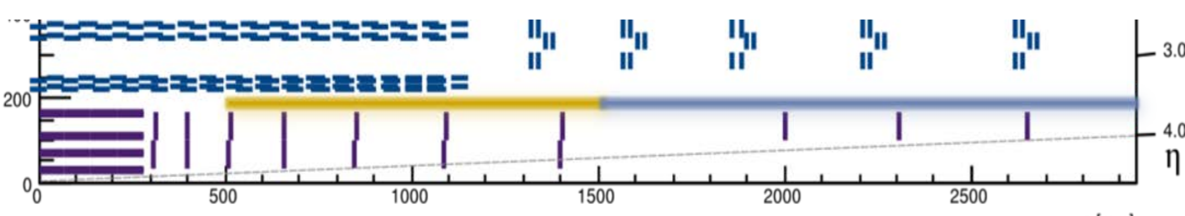

## Readout:

1 link (10Gb/s) per module (high Pt trigger data plus 1MHz trigger)

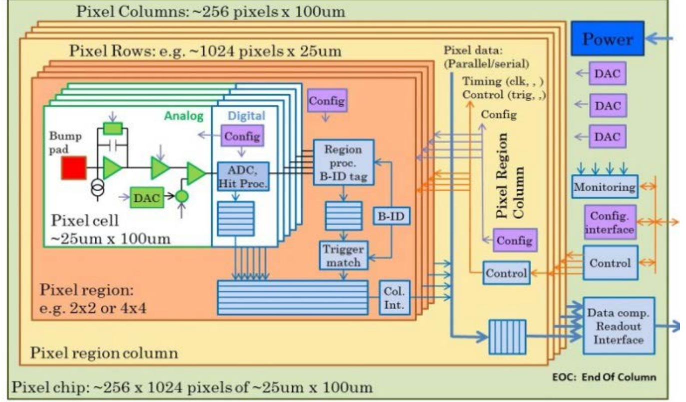
**Power:** Independent DC/DC per module

# CMS-Pixel phase2 "Baseline"

- **Detector**:
  - Phase1 pixel (4 layers) + 10 end-cap disks → extended coverage up to η ≈ 4
  - Opto – Power services on service cylinder: ~2m from the IP




- **Trigger**:
  - 500KHz, (1MHz with 2 x readout links)
  - 10 µs with very low loss (~$10^{-3}$), 20 µs with low loss (~$10^{-2}$)
  - (Option: Pixel participation in first level trigger ?)




- **Front end**:
  - One chip for all layers
    (ATLAS may possibly use FE-I4 for outer layers)
  - RD53: Technology, Basic pixel architecture
  - Pixel size: 25 x 100 µm² or larger
  - Chip size: ~2.5cm x 3cm if appropriate for inner most layer
  - CMS specific: Sensor, Pixel size/aspect, Trigger rate/latency, L1 trigger contribution

# CMS-Pixel phase2 "Baseline"

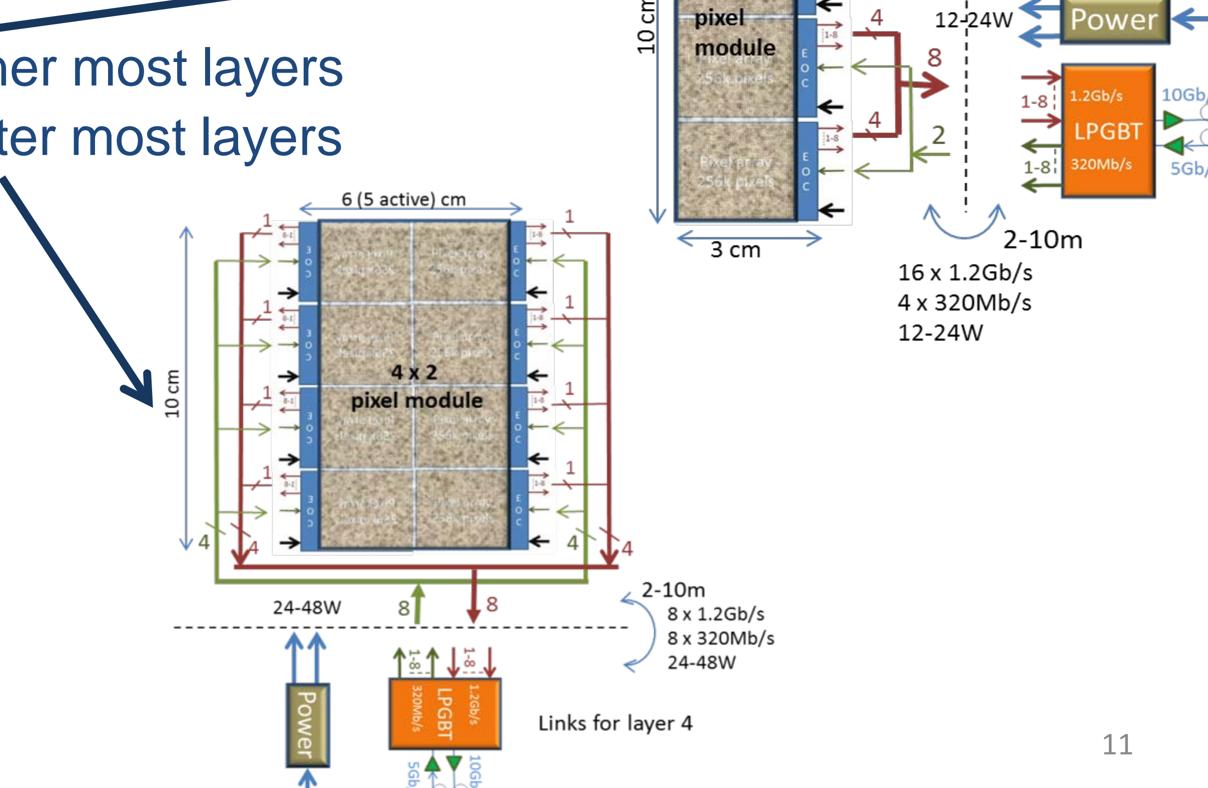
## Readout + Power:

- 1.2 Gbit/s e-links to **L**ow**P**ower**GBT**
- Serial powering, possibly combined with on-chip DC/DC

## Module design:

A: 4 x 1 chips: Two inner most layers
B: 4 x 2 chips: Two outer most layers
Encap disks: ?

## Cooling: $CO_2$



# ALICE fully pixellated Inner Tracking System

- Big pixel camera: > 2 Gpixels, 10 $m^2$.
- Triggered & untriggered operation.
- 100 kHz Pb-Pb event rate.
- 7 layers in 3 groups.

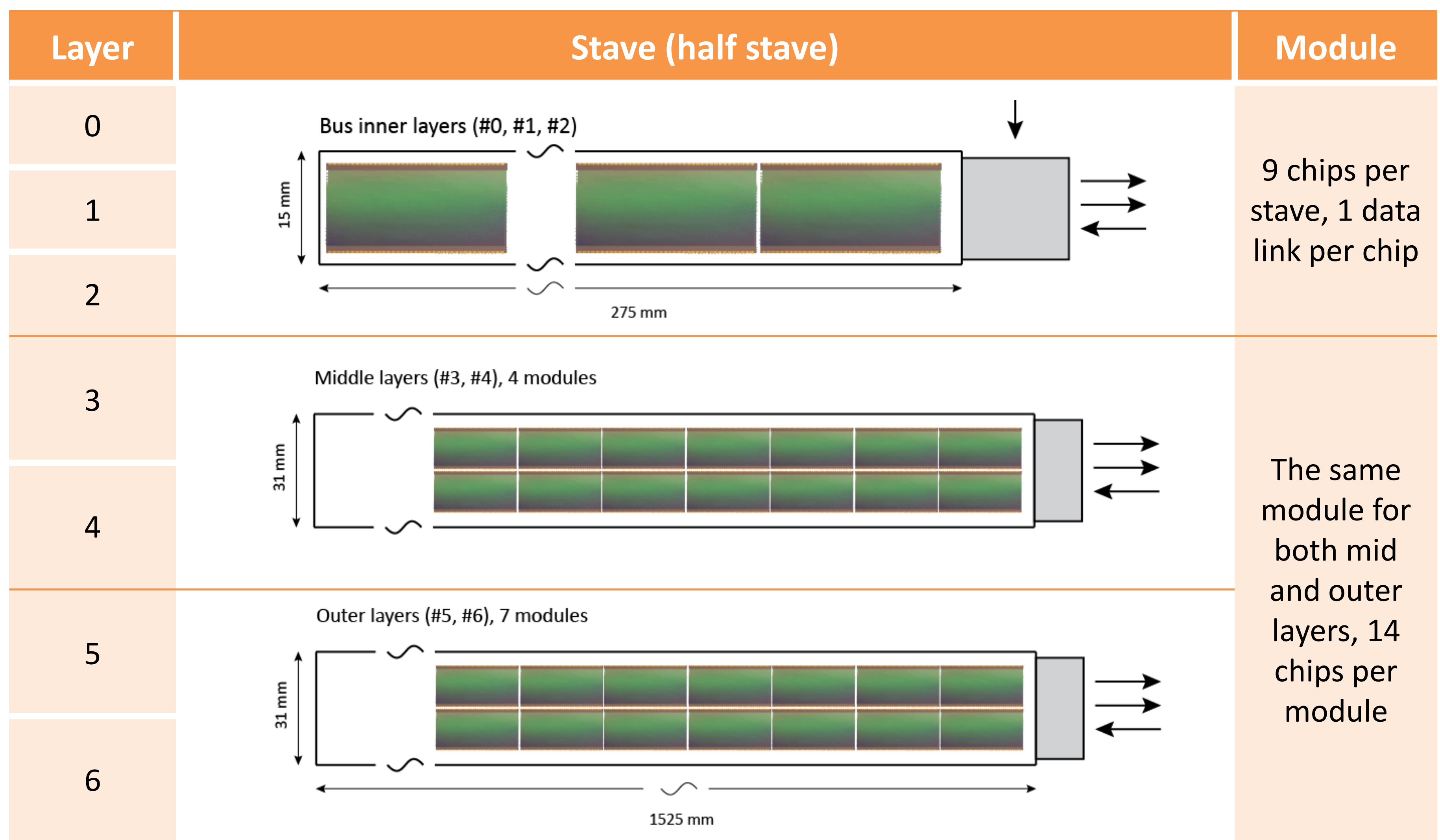
270 mm

1480 mm

- 3 × 1.5 $cm^2$ area, ≈ 28 × 28 $um^2$ pixels.
- Fully integrated readout electronic.
- Low power: < 100 $mW/cm^2$.
- Thinned down to < 100 μm.

- $X/X_0$ = 0.3% per layer (inner layers)

# ITS sensors organized in staves (inner) and modules (outer)



# ITS expected data throughput

| Layer | Chip [Mb/s] | (Half-)Stave [Gbit/sec] | Layer [Gbit/sec] | Nr. e-link | Nr. DDL |
|---|---|---|---|---|---|
| 0 | 348 | 3.1 | 38 | 108 | 12 |
| 1 | 215 | 1.9 | 31 | 144 | 16 |
| 2 | 156 | 1.4 | 28 | 180 | 20 |
| 3 | 16 | 0.8 | 37 | 96 | 24 |
| 4 | 15 | 0.8 | 50 | 120 | 30 |
| 5 | 13 | 1.2 | 107 | 168 | 42 |
| 6 | 13 | 1.2 | 119 | 192 | 48 |
| Total | - | - | 410 [Gb/s] | 1008 | 192 |

Noise dominated

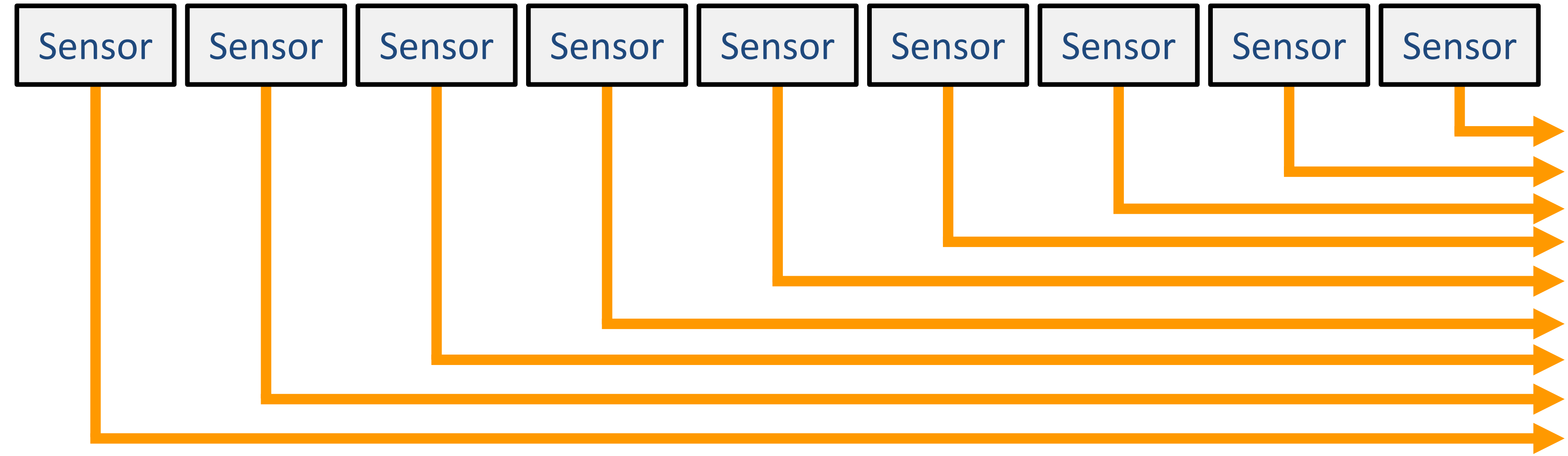
(*) Data rates estimated for:

a. 100 kHz interaction rate
b. QED electrons included assuming an integration time of 30μs
c. 40 bits to encode a hit
d. Fake hit rate $10^{-5}$/pixel per readout frame

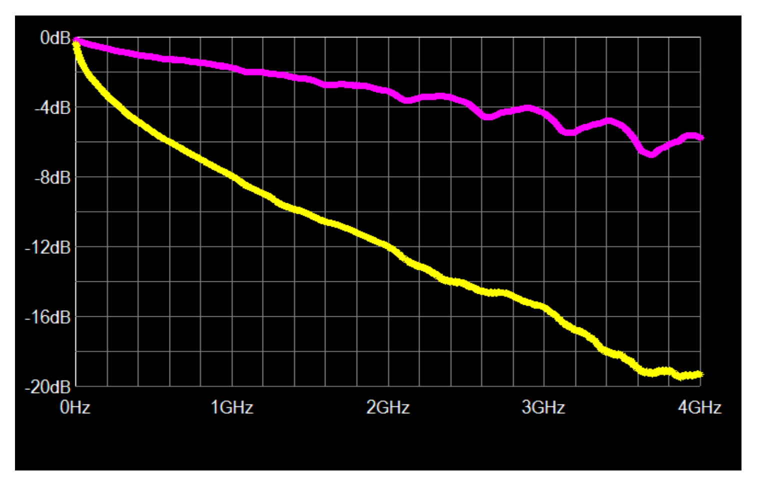
# ITS inner layer: readout scheme

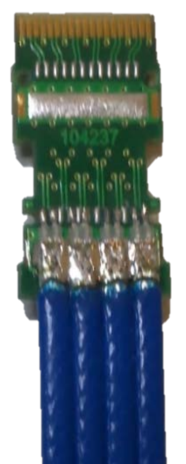
Very simple situation in the three innermost layers:

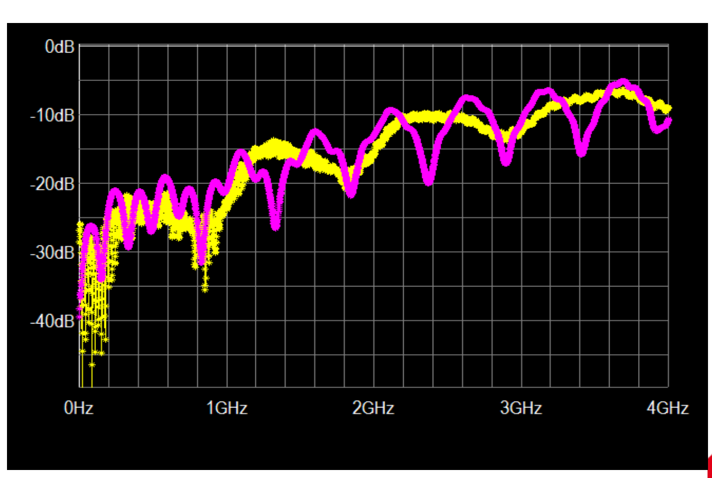
- each sensor drives its own line at full speed (up to 1.28 Gb/s)




- Commercial cables will be employed from the end of the stave to the CRU.

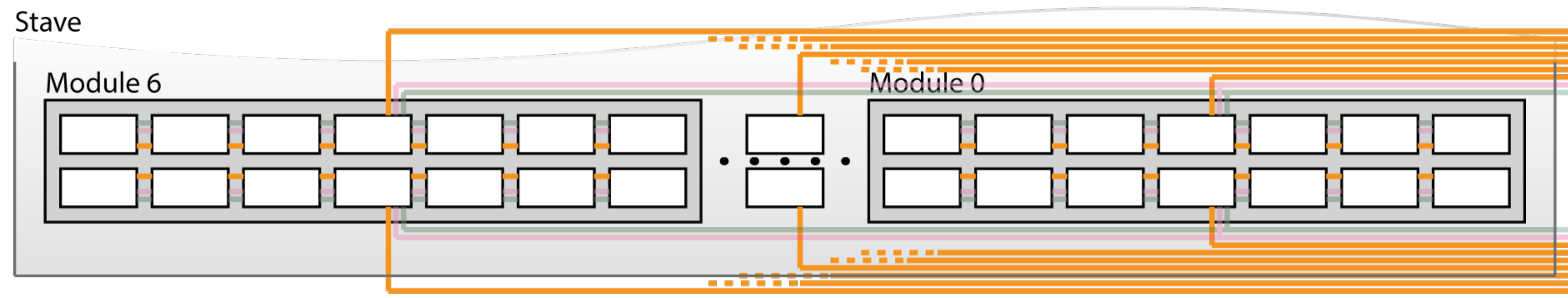




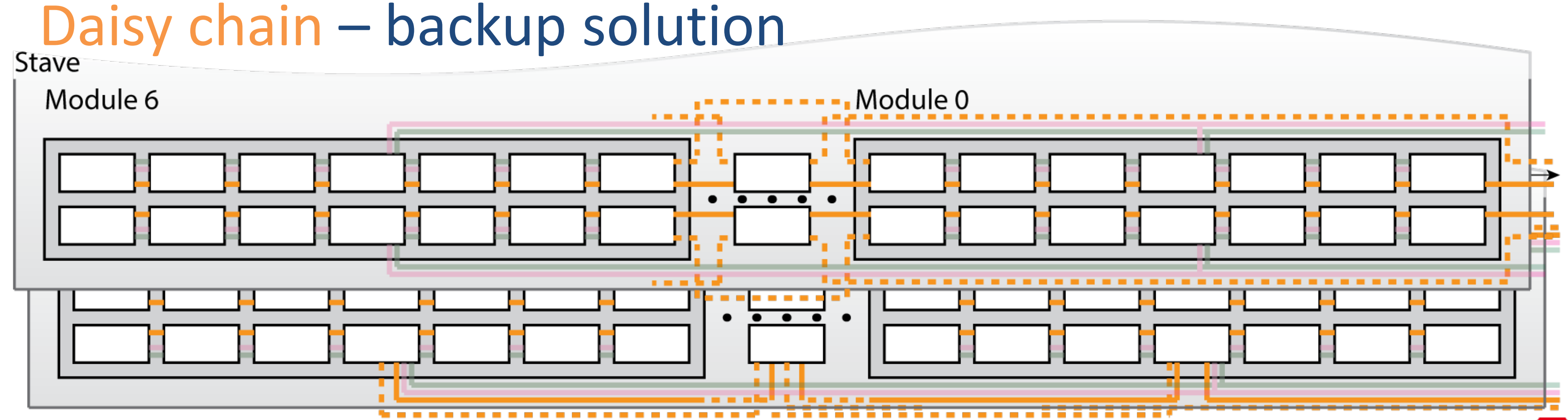
# ITS outer and middle modules: readout scheme

## Masters parallel – preferred solution




- Each master collect data from 6/13 sensor plus itself.
- Data are sent all the way up to the Common Readout Unit (up to 5 m length).
- The only active driver is the one inside the chip: speed up to 320 Mb/s achievable.
- Robust against single point failure, it needs up to 14 data pairs running on the 30 mm wide bus.

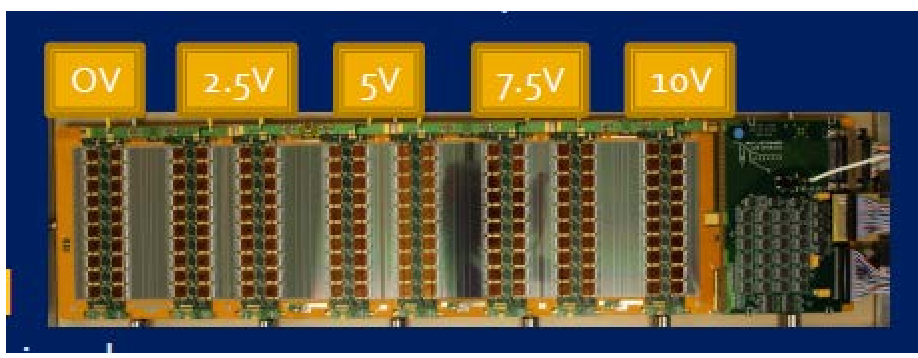
## Daisy chain – backup solution



# Power Distribution

- Two main power strategies being explored for the HL-LHC:
  - Serial Powering
  - DC-DC Buck converters
- In addition:
  - Switched capacitor DC-DC

Ex. Serial Powering: ATLAS Strip staves



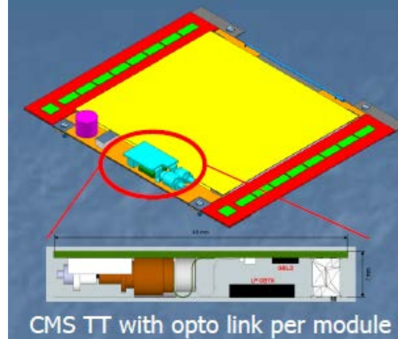

- Necessary to continue work on all

- Continued support is needed to deliver suitable parts in time
  - Bulk supplies
  - Evaluation of larger Serially Powered systems
  - Low mass DC-DC Buck Converters with increased radiation tolerance
  - Identification of "HV" switch transistors for sensor bias applications

Ex. DC-DC buck converter CMS Pixel upgrade

# Data/optical links

- Tracker Requirements:
  - High radiation tolerance: 1Mrad (ALICE ITS), 1Grad (ATLAS/CMS pixels)
  - One link does all: readout, clock, trigger, trigger data, control/monitoring
  - Increased data rates: Hit rates (~10) x Trigger rates (~10) = **~100x** !
  - **Low mass, low power, small form factor, reliable, long-lived, etc.**


CMS TT with opto link per module

→ Use of standardized (very) rad hard links (where ever possible)

  - **Common development with flexibility and support for specific tracker needs**

- **LPGBT ~10Gbits/s in 65nm: To be defined & designed**

- ATLAS & CMS “strip”: < 100Mrad
  - Optical link within tracker volume
  - Collect data from multiple sources (FE chip or modules) and control “fanout”

ATLAS strip with opto link per stave

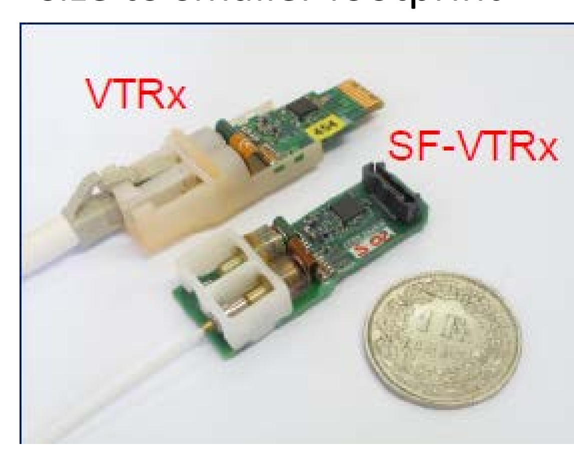
- CMS/ATLAS pixels: ~1Grad
  - Optical link can most likely not survive radiation environment
  - Opto link located few (2-10) meters from pixel modules
  - High speed and low power electrical links critical to get data out of pixel volume!

# High speed link R&D

- Common Projects for Rad Hard Optical Link (Phase-1):
  - GigaBit Transceiver (**GBT**) project (chip-set) & GBT-FPGA project
  - Versatile Link (**V**L) project (opto) & Gigabit Link Interface Board (GLIB)

6 institutes: CERN, FNAL, IN2P3, INFN, Oxford, SMU

Shrinking of GBT package size to smaller footprint




- Meeting the HL-LHC challenge requires:
  - Qualifying new technologies and components
  - Designing electronics, interconnects, packages and perhaps even optoelectronics
  - Maintaining expertise, tools and facilities
  - Investing heavily with a few selected industrial partners
- The community is healthy, but small and fragmented. Manpower is the bottleneck → development time remains very long (~6y) in comparison to industry.
- Si-Photonics might be a valid alternative…On-going collaboration with academic and industrial partners (INFN?) → Assess radiation hardness first!
- High speed electrical data links are not obsolete! (Short distance, on-board serial links, aggregation to high speed opto-hubs, low mass, highly radiation resistant (HL-LHC pixels)

# Optical Link Project Status: GBT

- Project started in 2008
  - GBT (Serializer/Deserializer)
    - GBT-Serdes prototype in 2009
    - GBTx in 2012
    - Packaging in 2013
    - Production in 2014
  - GBLD (Laser Driver)
    - Final iteration (V4.1/V5) in 2013
  - GBTIA (Pin Diode Receiver)
    - Final iteration (V3) in 2012

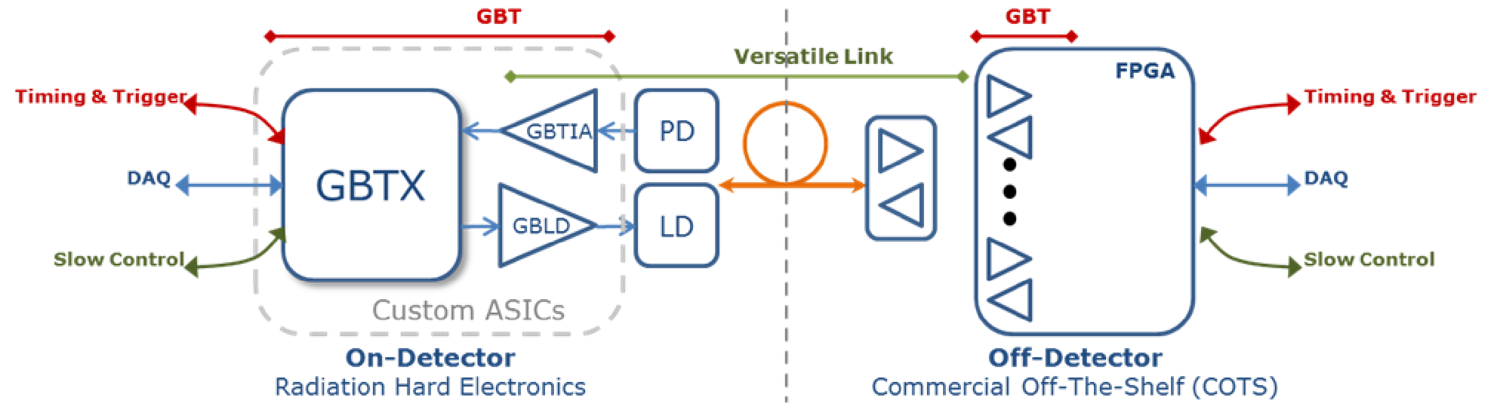
GBTSCA (Slow Control ASIC)

Final version expected in 2014

GBT-FPGA firmware

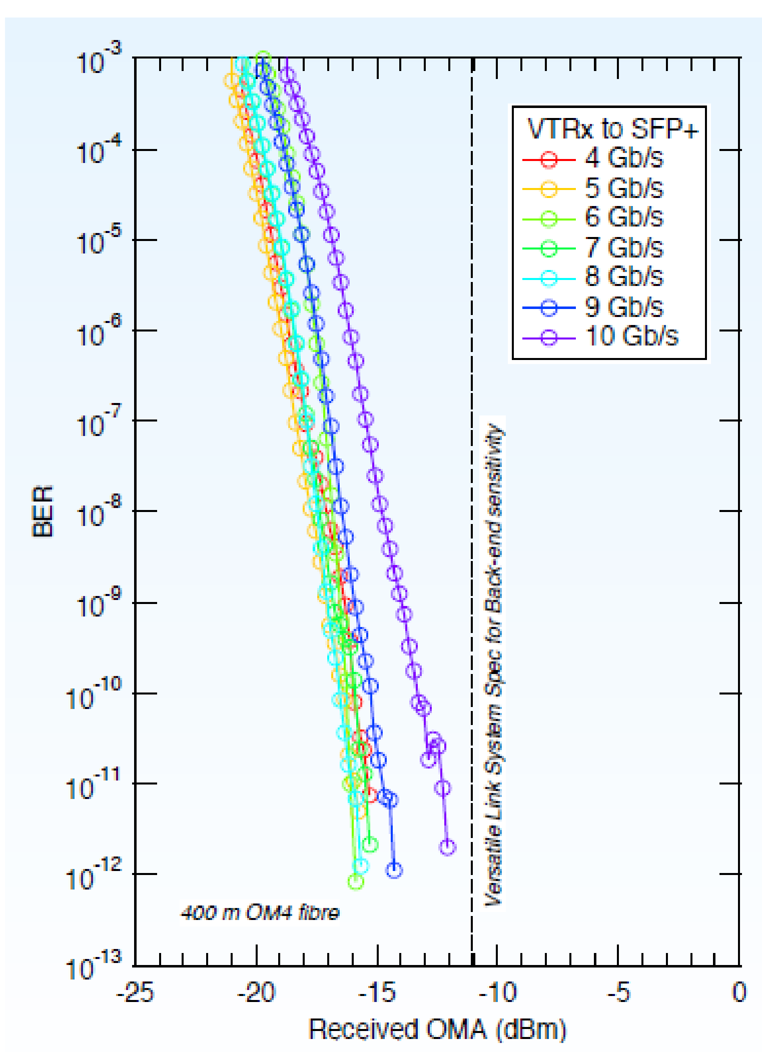
Tracking evolution
of major FPGA families
Available

- Project delivers
  - Chipset for Front-End
  - GBT-FPGA Back-End firmware



# Optical Link Project Status: VL

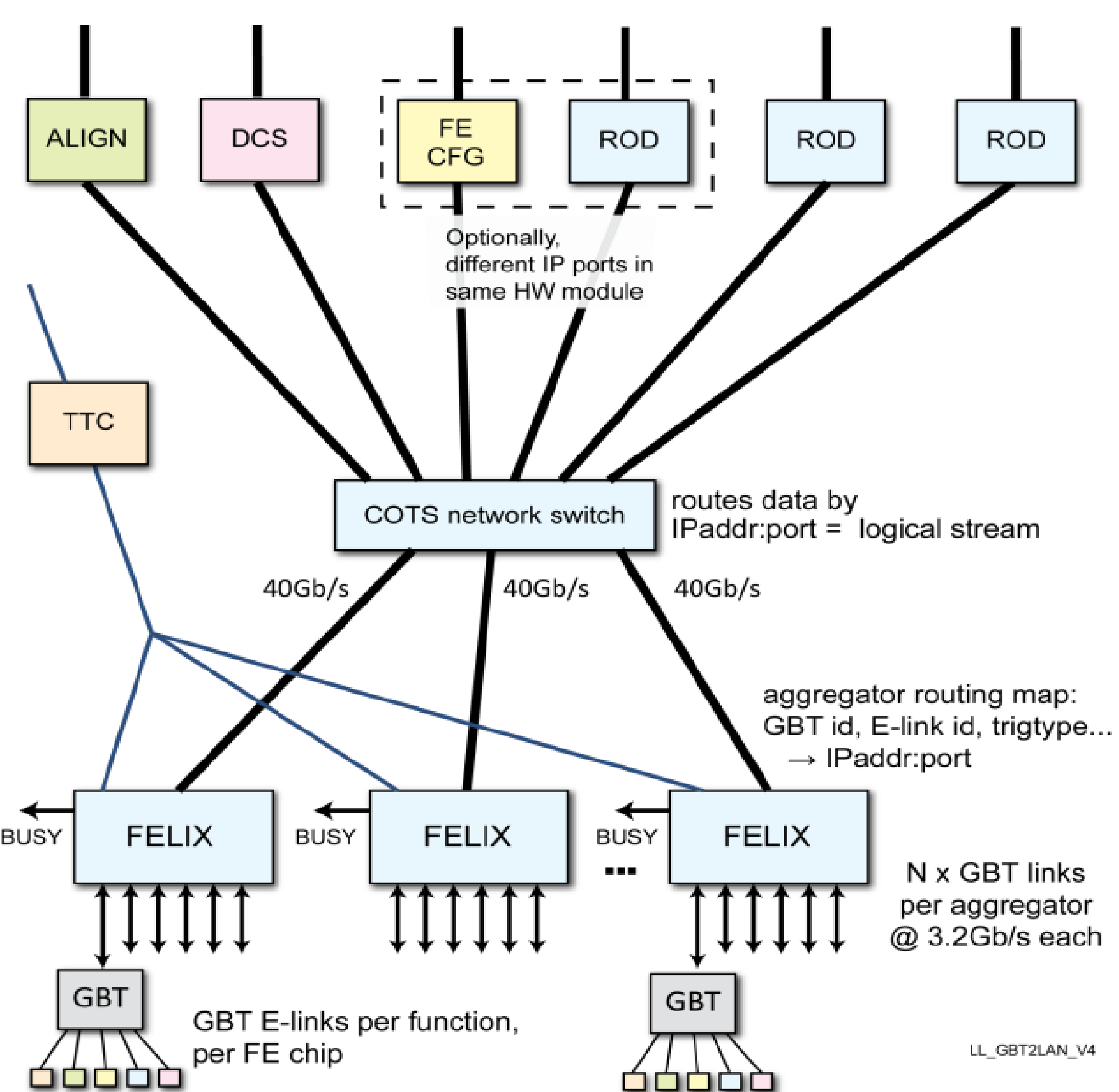
- Kick-off: April08
- Project delivers
  - Custom built Rad Hard VTRx
    - Production readiness: 2014
    - Early delivery of rad-soft VTTX to CMS-Cal-Trig: Dec13
  - Recommendations for
    - Fibre and connectors
    - Backend optics
  - Evaluation Interface boards (GLIB)
- Experiments
  - Design their own system
  - Select passive and backend components based on VL recommendations and on their own constraints



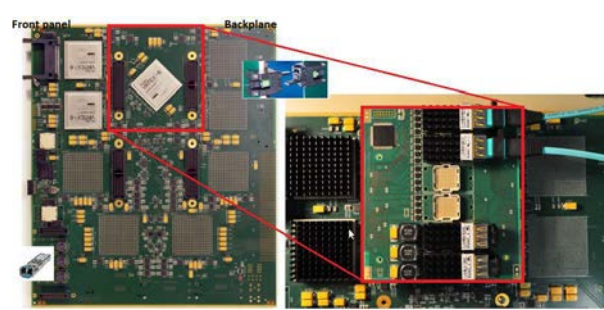
# Front End Link eXchange project (ATLAS)
## (CERN, BNL, Weizmann Institute, Weizmann Institute)

- *"FELIX, a new approach to interfacing on-detector electronics separates the Front End link interfacing from the Front End data processing"*
- It eliminates the static point-to-point connections between the Front Ends and the Read Out system
- Reduce ATLAS dependence on custom electronics and its inherent problems of long term support by experts
- Define an architecture that is scalable and flexible, since we don't know exactly what future requirements will be
- Interface several GBT links to a high bandwidth industry standard network technology – Ethernet (40Gb/s) or Infiniband (56Gb/s) – then route logical data flows to/from different off-detector endpoints

# Integrating GBTs to a LAN



# Off detector: Modular Electronics




- xTCA and its sub-standards:
  - ATCA (2002): ATLAS, LHCb, ILC, …
  - µTCA (2006): CMS, XFEL

- Favoured candidate as successor of VME
- Tight roadmap to define and test common developments

## Next steps:

- Manpower and tools needed to develop common solutions and support them
- Raising the competence of developers community will take time
- Many coordinating actions already started, but lots to be done
- xTCA Interest Group should play a major role

**Alternatively development** of high bandwidth system based on PCIx cards in “commodity” PCs to interface detector specific front-end to DAQ systems on a switched network.

# DAQ for the test beam at DESY (CMS Strips)

**Based on Phase II tracker DAQ developments**

- implemented on CERN GLIBs (µTCA AMCs)

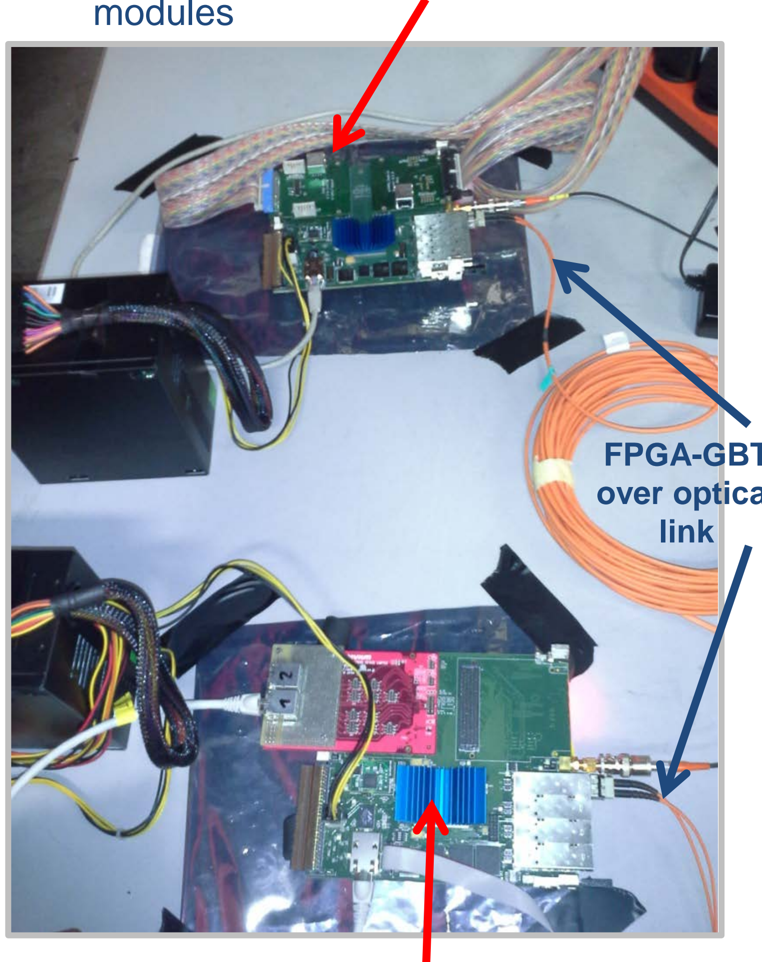
- **'back-end' GLIB** handles external trigger, processes and formats data from front end, configures CBC2s over I2C and issues fast control signals

- **'front-end' GLIB** currently acting as fan-out to modules; but will eventually implement concentrator

- GBT link implemented between front- & back-end GLIBs

- currently working well

'front-end' GLIB + 2 FMC mezzanines to interface with modules



**FPGA-GBT over optical link**

'back-end' GLIB + 1 FMC mezzanine for external trigger

# Summary: Specs and Technologies for the Electronics

## Front-end

Specs:

- Low power / channel
- Low noise
- High-density interconnections
- High radiation tolerance

Technologies:

- Deeper submicron ASICs technologies
- 130 nm for strips, 65 nm for hybrid pixels
- High-density technologies for hybrids substrates
- Coarse bump-bonding for flip chip of ASICs to hybrids, and for large pixels

## Back-end

Specs:

- High processing power
- High interconnectivity

Technologies:

- xTCA standards
- Possibly custom-design ASICs for fast pattern recognition (track trigger)

## Services

Specs:

- High-speed, low-power links
  → special requirements for trackers
- Small-size opto components
- Power conversion
- Rad hardness

Technologies:

- DC-DC conversion, serial powering
- 65 nm ASICS for next generation links
- Low-power low-mass electrical links

# Conclusions

The LHC experiments have conceived viable and highly optimized tracker system upgrades for the extremely challenging HL-LHC conditions:

→ Significant electronics engineering resources will be required to develop, verify and build these trackers.

- **ASICs development:**
  Large, complex, low power, radiation hard, mixed signal ASICs are critical
  - Resources for their development are needed early in the project phase.
  - Manpower must be appropriately organized and trained.
  - Collaborative efforts across multiple institutes and when possible across experiments.
  - Critical to enable small design teams across many institutes to develop such IC's
- **Power distribution and data links:**
  Further developments needed beyond the "phase-1" devices:
  - Must continue as common projects, accommodating specific requirements for trackers
  - These developments are critical for the design of the upgraded trackers
  - Significant efforts will be required to define, develop, test and qualify, support next generation link (LPGBT) appropriate for LS3 tracker upgrades

  → **Radiation tolerance, low power 5 & 10 Gbits/s optical links appropriate for use in tracker!**
- **Off detector electronics: fast and complex, critical for track triggers.**

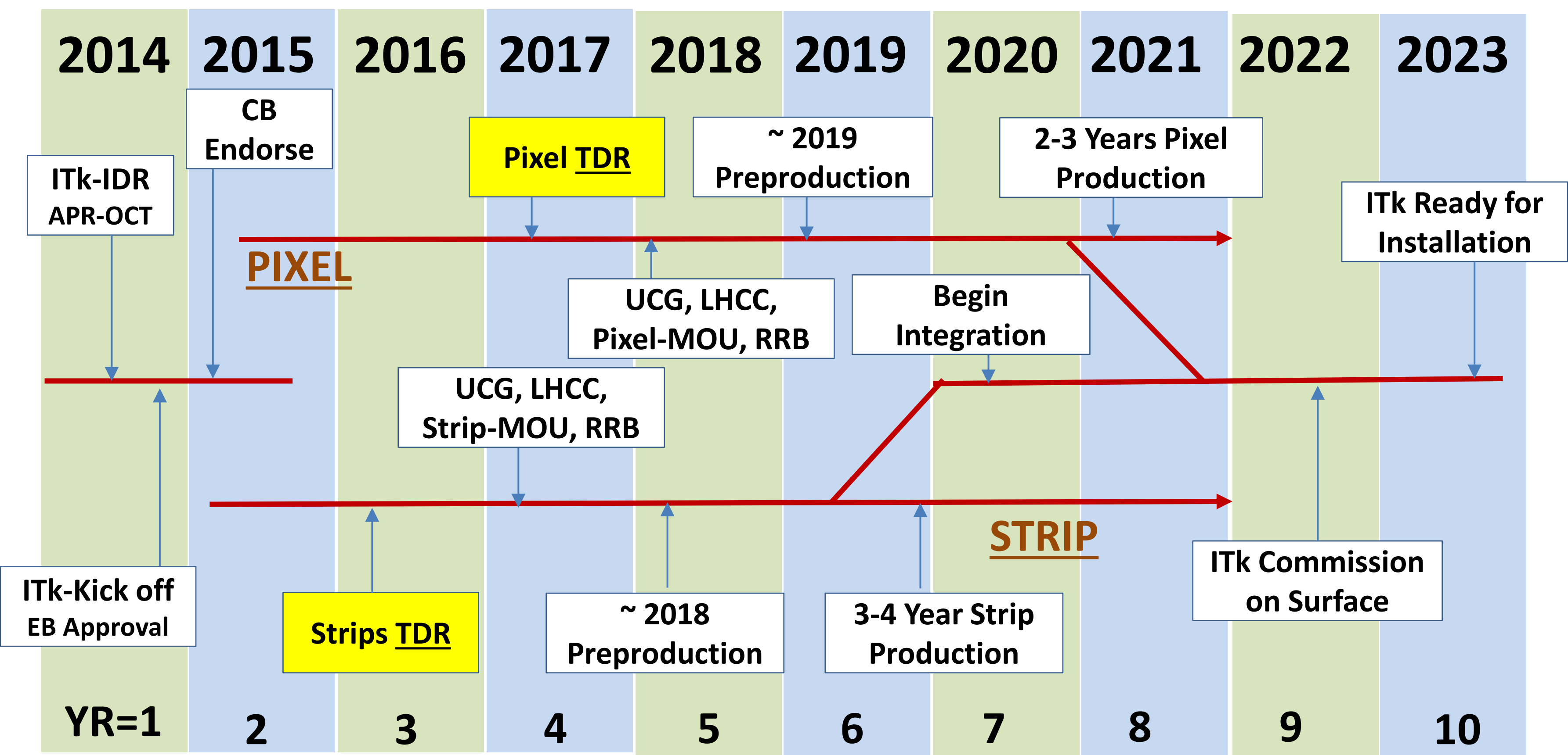
Back Up

# Pixel Chip generations

| Generation | Current FEI3, PSI46 | Phase 1 FEI4, PSI46DIG | Phase 2 |
|---|---|---|---|
| Pixel size | 100x150um$^2$ (CMS)<br>50x400um$^2$ (ATLAS) | 100x150um$^2$ (CMS)<br>50x250um$^2$ (ATLAS) | 25x100um$^2$ ? |
| Sensor | 2D, ~300um | 2D+3D (ATLAS)<br>2D (CMS) | 2D, 3D, Diamond, MAPS ? |
| Chip size | 7.5x10.5mm$^2$ (ATLAS)<br>8x10mm$^2$ (CMS) | 20x20mm$^2$ (ATLAS)<br>8x10mm$^2$ (CMS) | **> 20 x 20mm$^2$** |
| Transistors | 1.3M (CMS)<br>3.5M (ATLAS) | 87M (ATLAS) | **~1G** |
| Hit rate | **100MHz/cm$^2$** | **400MHz/cm$^2$** | **1-2 GHz/cm$^2$** |
| Hit memory per chip | 0.1Mb | 1Mb | ~16Mb |
| Trigger rate | 100kHz | 100KHz | 200kHz - **1MHz** |
| Trigger latency | 2.5us (ATLAS)<br>3.2us (CMS) | 2.5us (ATLAS)<br>3.2us (CMS) | 6 - 20us |
| Readout rate | 40Mb/s | 320Mb/s | **1-3Gb/s** |
| Radiation | **100Mrad** | **200Mrad** | **1Grad** |
| Technology | 250nm | 130nm (ATLAS)<br>250 nm (CMS) | **65nm** |
| Architecture | Digital (ATLAS)<br>Analog (CMS) | Digital (ATLAS)<br>Analog (CMS) | Digital |
| Buffer location | EOC | Pixel (ATLAS)<br>EOC (CMS) | Pixel |
| Power | ~1/4 W/cm$^2$ | ~1/4 W/cm$^2$ | **~1/4 W/cm$^2$** |

# ITk: Rough Draft Timetable

## For Discussion Only




CB= collaboration board, EB=executive board, IMOU=interim memorandum of understanding, UCG=upgrade cost group, RRB= Resources review board, IDR=initial design review (internal), TDR=technical design report (external)

# The ITk Institutes

82 institutes have expressed interest in taking part in building the Itk

Collaboration grown by 6 institutes since November 2013 - ITK-SC. Likely to grow by a few more very soon....

*PLs have started, and will continue, to discuss with the individual institutes their involvement, towards the IDR, TDRs and beyond*

There are currently “significantly” more institutes signed up to work on the pixel detector than strips.

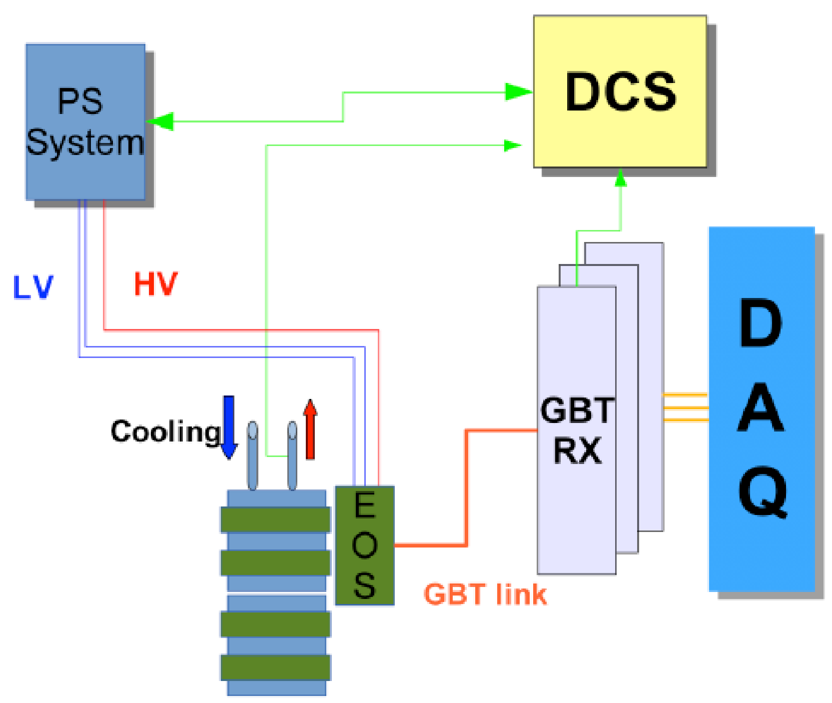
| Country | Number of Institutions |
|---|---|
| Australia | 3 |
| Canada | 4 |
| CERN | 1 |
| China | 1 (cluster) |
| Czech Republic | 3 |
| Germany | 10 |
| France | 5 |
| Italy | 4 |
| Japan | 8 |
| Netherlands | 1 |
| Norway | 2 |
| Poland | 2 |
| Switzerland | 2 |
| Spain | 2 |
| Slovenia | 1 |
| Sweden | 2 |
| South Africa | 1 (cluster) |
| Taiwan | 1 |
| United Kingdom | 12 |
| United States | 17 |
| **Total** | **82** |

# End-of-substructure Card (EoS) (ATLAS Strips)

- First FE-chip in 130nm process (ABC130) test program is ramping up

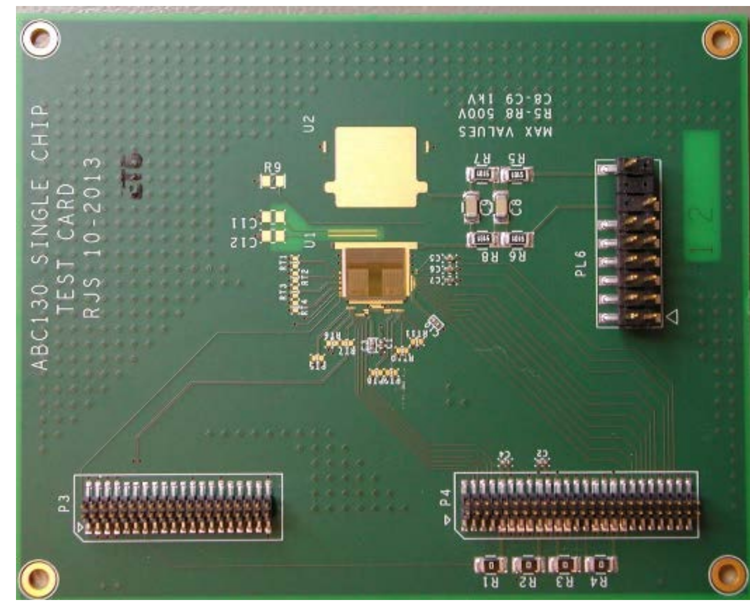
- DESY is leading design effort for EoS
  Design for both Staves and Petals
  PCBs made by DESY
  Close Collaboration with Berkeley & Oxford

- Currently working on EoS system issues
  Power consumption
  Detector Control Systems (DCS)
  Material reduction



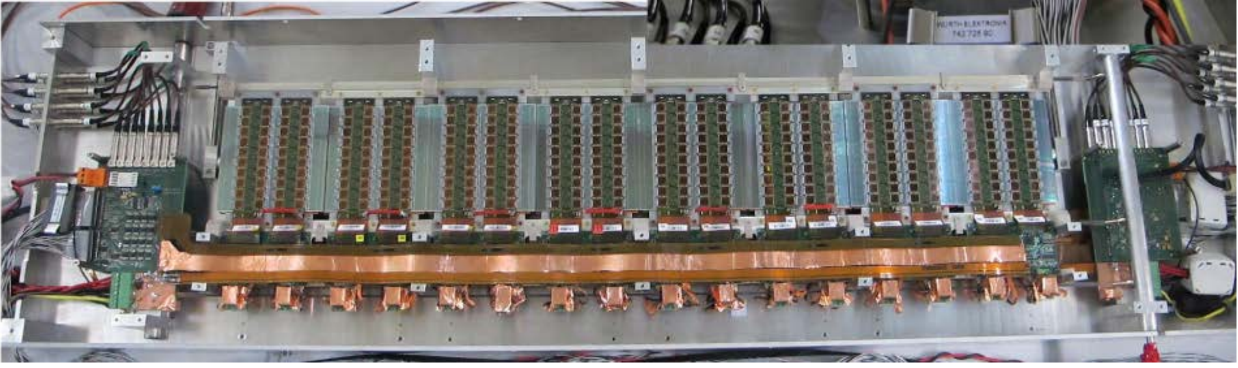

New key features:

- Only interlock relevant DCS lines separated
- **All other DCS information via optical link**
- Less cables




First ABC130 chips
Functional but only after surgery
Will need a re-spin

12 module
250nm DC-DC Stave

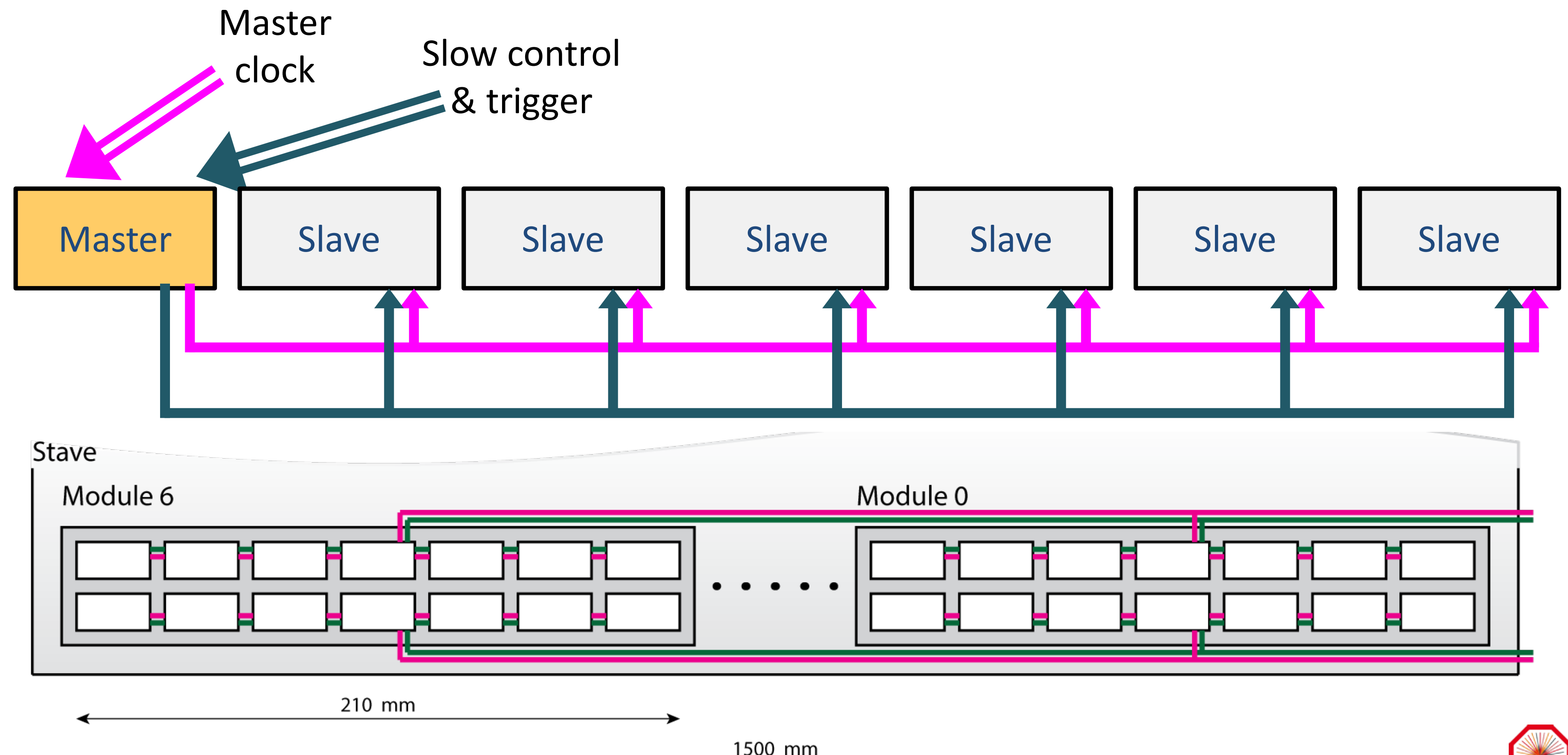


8 module
250nm Super-module

| | Key ITk Dates in 2014 |
|---|---|
| January | 23rd -24th :Mechanics kick off meeting @ CERN<br>29th : ITk-SC @ CERN |
| February | *3rd -7th :Strips meeting in Valencia*<br>18th – 20th : ACES meeting @ CERN |
| March | 13th : ITk-SC @CERN |
| April | 7th – 11th : AUW in Freiburg |
| May | 2nd : ITk-SC @ CERN : Friday |
| June | 2nd -6th : TIPP<br>25th : ITk-SC @CERN<br>30th : Tracker Mechanics Forum (DESY) |
| August | 21st : ITk-SC @CERN |
| September | *Common ITk meeting in first half of the month at CERN*<br>14th – 19th : VERTEX<br>25th: ITk-SC @ CERN |
| October | **ITK-IDR @ CERN**<br>Aix les Bains 22-24 ECFA meeting |
| November | 3rd-11th : AUW a@ CERN |
| December | 4th : AUW a@ CERN |

# ITS clock/slow control/trigger distribution (ALICE)

- For both readout scheme (parallel or daisy chain), the clock, slow control and trigger signals are distributed to master chips only (1 or 2 per module), then locally broadcasted to slave chips.
- Trigger is broadcasted through the slow control lines.



# 2S module

**$CO_2$ cooling**
already used in Phase-1
mass-efficient cooling

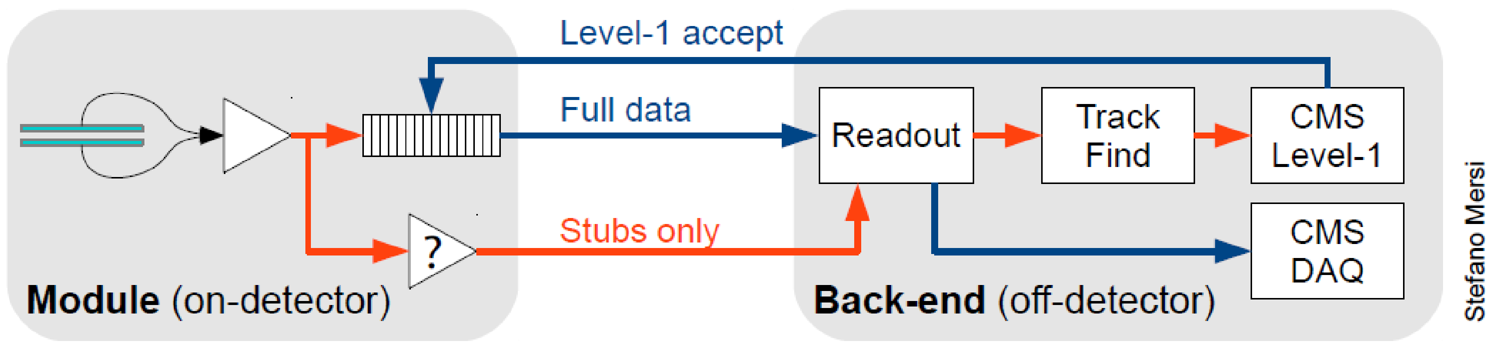
**Binary readout: CBC**
provides hit-matching
(already working prototype)

*Hybrid is the key element*
*for module integration*
***Functional prototypes in hand!***

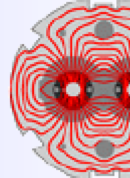
**Data link:**
**Low-power GigaBit Transceiver**
lpGBT currently under development
integrated at module level

**DC/DC converter**
already used in Phase-1
10 V lines: lower current, lower material

# CMS Trigger & DAQ Architecture for HL-LHC



# 2012 ATLAS Trigger & DAQ Architecture



Trigger

DAQ

MHz

cialized h/w
ASICs
FPGA

LVL1

2.5 ms

40 MHz

Calo
MuTrCh

Other detectors

1 PB/

FE Pipelines

DETECTOR R/O

Lvl1 acc = 75 kHz

ROD ROD ROD

Read-Out Drivers

kHz

RoI

RoI data = 1-2%

120 GB/s

120 GB

Read-Out Links

RoI Builder
2 Supervisor

HLT

LVL2

~ 10 ms

ROIB

L2SV

RoI requests

ROB ROB ROB

Read-Out Buffers

ROS

Read-Out Sub-system

L2 N/work
L2 Proc Unit

L2P

L2N

DATAFLOW

~2+4 GB

kHz

Lvl2 acc = ~2 kHz

DFM

EBN

Dataflow Manager

Event Building N/work

SFI

EB

Sub-Farm Input

Event Builder

~4 GB/s

Event Filter
Processors

Event Filter

~ sec

EFP EFP EFP EFP

EFN

Event Filter N/work

EFacc = ~0.2 kHz

SFO

Sub-Farm Output

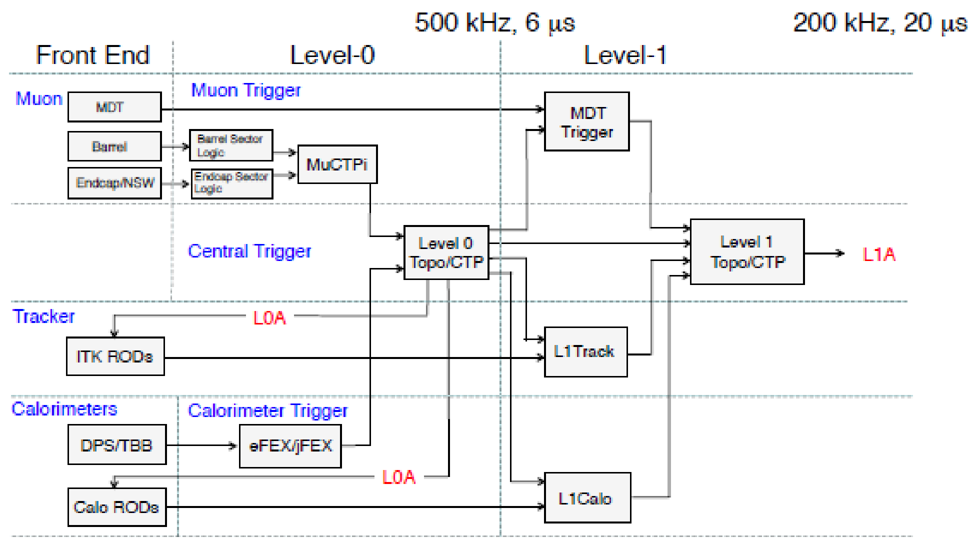
00 Hz

~ 300 MB/

# ATLAS Trigger Scheme

- Split Level-0/Level-1 hardware trigger with a total level-1 accept rate of 200 kHz and total latency of 20 μs.
- Level-0 trigger distributes the Level-0 accept at a rate ~500 kHz within 6 μ s.
- Phase-II Level-0 trigger is ~Phase-I Level-1 system and consists of a feature extractor (FEX) based on calorimeter electromagnetic and jet triggers, and the Phase-I Level-1 muon trigger.
- The Level-0 accept is generated by the central trigger system which incorporates topological triggering capability.

- Level-1 system will reduce the rate to 200kHz within an additional latency of 14μs.
- Accomplished by
  - introduction of track information within a Region-of- Interest (RoI)
  - full calorimeter granularity within the same RoI
  - introduction of a refined muon selection based on the use of the MDT information.
- Increased use of offline-like algorithms in the High-Level Trigger (software trigger) with an anticipated readout rate of 510 kHz.



# Power-cooling-integration

- Power optimized electronics critical for trackers
  - Low power technology: Deep submicron ASICs
  - Architecture optimization: Segmentation, ADC/binary, Triggering, Buffering, Readout bandwidt
  - Circuit optimization: Low power low noise analogue, Low power digital

  Significantly increased performance requirements do not favour low power

- Power densities and cooling
  - Hybrid pixels: 0.5 – 1.5W/cm2 (Extremely high rates) → Uniform high power density over full "small" detector
  - Strips: ~0.05W/cm2 (High rates) → Localized heat sources distributed over large detector
  - MAPS (ALICE ITS): ~0.05W/cm2 (modest rates but high event multiplicity) → Uniform low power density
- Low voltage power distribution critical for trackers.
  - Low power -> Low voltage ASICs ~1V -> High currents -> High cable losses
  - Highly power optimized digital designs have high power transients
  - Associated power control/monitoring and safety systems
- Active power distribution required within detectors
- Power conversion in very high radiation and magnetic fields
  - DC/DC conversion (common development)
  - Serial powering (project specific)

Hard to define/guess power/cooling needs early in project phase

# Trigger Developments

**Tracking Triggers**

- ATLAS: L1 trigger at 500KHz within 20 μs; 'pull path'
- CMS: L1 trigger at 40MHz within 10-20μs; 'push path'

**Challenges:**

- Complex pattern recognition over very large channel counts with short latency and no dead time (clock/event pipelined).
- Highly challenging connectivity and processing problem

**Tools:**

1. **Pattern Recognition Associative Memory (PRAM)**
   - Match and majority logic to associate hits in different detector layers to a set of pre-determined hit patterns
   - highly flexible/configurable
   - Pattern recognition finishes soon after hits arrive

   Challenges:
   - Increase pattern density by 2 orders of magnitude
   - Increase speed x 3 (latency)
   - Use 3D architecture:
     Vertically Integrated Pattern Recognition AM – VIPRAM
2. **FPGAs:**

   Challenges:
   - Latest generation FPGAs create complex placement issues
   - Designs must be heavily floor-planned similar to ASIC layout
   - Embedded Processors, moving tasks from FPGA to SW design

# High Speed Electrical Links

## On-stave Data Links for Innermost Pixel Layers in ATLAS

V. Fadeyev (UCSC), S. Seidel, M. Hoeferkamp (UNM)

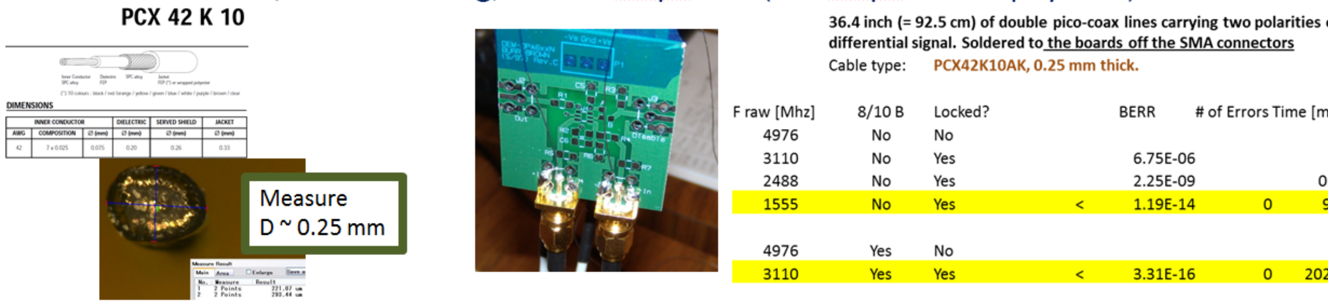
Need: high bandwidth (> 1 Gbps),
low mass (<0.5 mm diameter),
high radiation hardness

→

0.25 mm diameter cable:

- 0.016 % X0 for 1st layer
- 0.168 % X0 for 2nd layer

Investigating dual coaxial cables as a technical solution.
Have shown that cables with non-rad-hard dielectric have high enough BW with proper dimension. With 8/10B encoding, it's 3.1 Gbps raw (2.5 Gbps useful payload).




| INNER CONDUCTOR | | | DIELECTRIC | SERVED SHIELD | JACKET |
|---|---|---|---|---|---|
| AWG | COMPOSITION | Ø (mm) | Ø (mm) | Ø (mm) | Ø (mm) |
| 42 | 7 x 0.025 | 0.075 | 0.20 | 0.26 | 0.33 |

**36.4 inch (= 92.5 cm) of double pico-coax lines carrying two polarities of differential signal. Soldered to the boards off the SMA connectors**

Cable type: **PCX42K10AK, 0.25 mm thick.**

| F raw [Mhz] | 8/10 B | Locked? | | BERR | # of Errors | Time [min] |
|---|---|---|---|---|---|---|
| 4976 | No | No | | | | |
| 3110 | No | Yes | | 6.75E-06 | | |
| 2488 | No | Yes | | 2.25E-09 | | 0.66 |
| 1555 | No | Yes | < | 1.19E-14 | 0 | 900 |
| | | | | | | |
| 4976 | Yes | No | | | | |
| 3110 | Yes | Yes | < | 3.31E-16 | 0 | 20213 |

BUT: After 250 MRad BW is reduced, and mechanical integrity is compromised (not surprising).

The solution is to use cables with correct dimensions with rad-hard materials (kapton is the most likely choice). Axon bid for making them.

In parallel, obtained cable samples with kapton dielectric from 2 other vendors. They were used in proton irradiation run at Los Alamos in September 2013. Assessment of dielectric, impedance, BW changes, and mechanical stability to follow in the near future.

# Many different Link types

- Readout - DAQ:
  - Unidirectional
  - Event frames.
  - High rate
  - Point to point
- Trigger data:
  - Unidirectional
  - High constant data rate
  - Short and constant latency
  - Point to point
- Detector Control System
  - Bidirectional
  - Low/moderate rate (“slow control”)
  - Bus/network or point to point
- Timing: Clock, triggers, resets
  - Precise timing (low jitter and constant latency)
  - Low latency
  - Fan-out network (with partitioning)

- **Different link types remain physically separate, each with their own specific implementation**