UNIVERSITY OF TRENTO - Italy
Department of Industrial Engineering

FONDAZIONE BRUNO KESSLER

INFN Istituto Nazionale di Fisica Nucleare

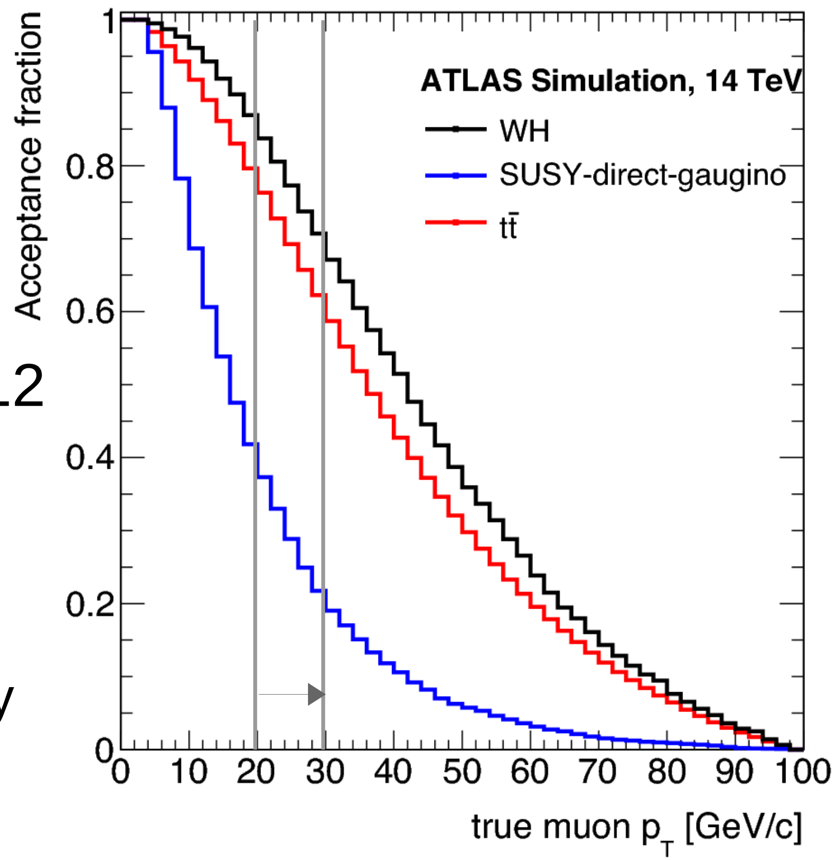
TDAQ@HL-LHC

Trigger/DAQ Session: Introductive Talk

Donatella Lucchesi, Roberto Carlin, Andrea Negri

HL-LHC trigger requirements

- ATLAS&CMS Physics goals
  - High precision Higgs studies
  - EWK and top scale physics
  - SUSY and exotics searches
- Keeping same signal acceptance as 2012
- Trigger thresholds
  - They are already near the energy scale of interesting processes
  - Increasing them will reduce signal efficiency
  - Eg: p_T 20→30 GeV implies an acceptance reduction of a factor 1.3 – 1.8



- T/DAQ base requirements
  - Maintain p_T-thresholds at ~ 20 GeV for single electron and muon trigger to preserve acceptance for W, Z, $t\bar{t}$, H
  - Maintain system flexibility to be able to adapt to new discoveries or changes in background

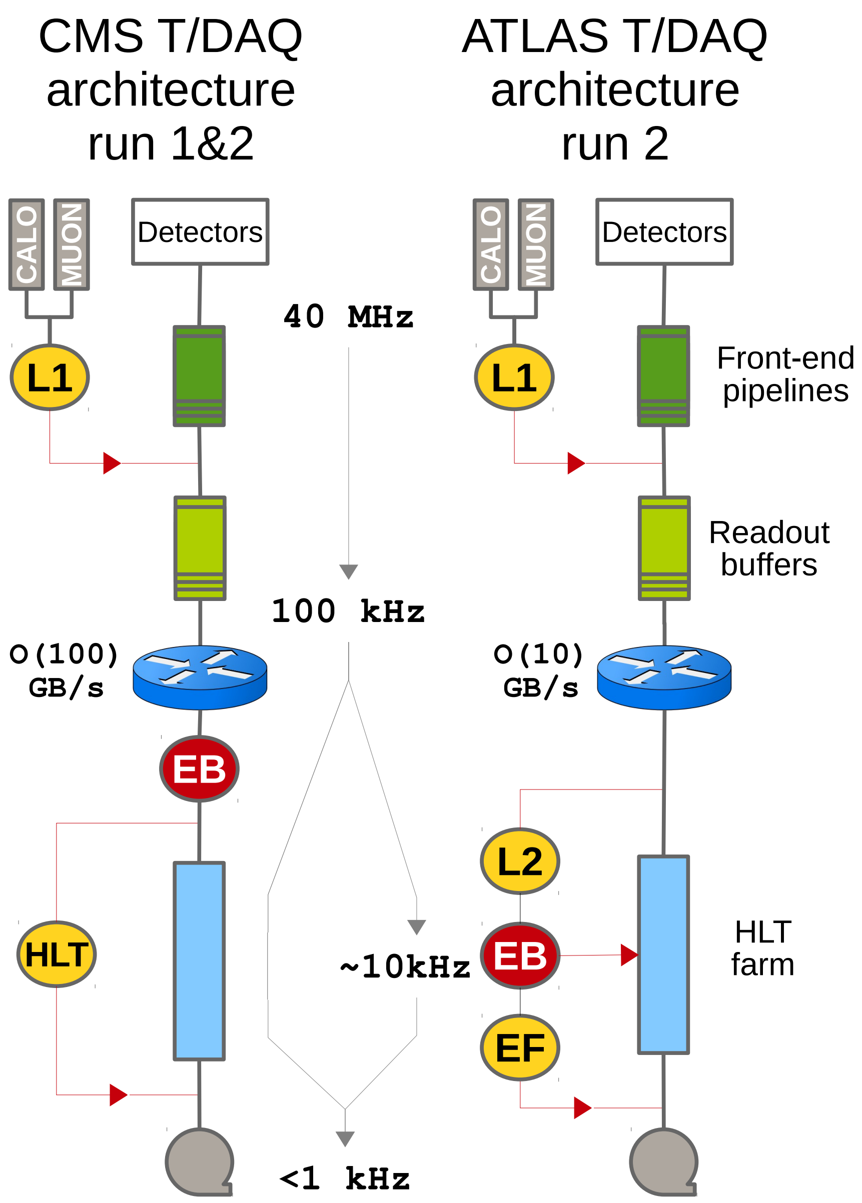
Trigger/DAQ challenges

- Boundary conditions: moving from LHC Run 1 to HL-LHC
  - **E_{CM} x 1.8**: 8 → 14 TeV
  - **Lumi x 7**: 7×10^{33} → 5×10^{34} cm^{-2} s^{-1}
  - **<μ> x 4**: 35@50ns → 140@25ns
- T/DAQ challenge: try to maintain ~loose and inclusive selections w/
  - Higher interaction rates for physics and backgrounds
  - About 10 times more tracks per bunch crossing (in $|\eta|<2.5$)
  - Degraded HLT algorithm performance due to increased hadronic activity
    - Reduced rejection from isolation (electron, photons)
    - Increased fake rates in muon systems
    - Degraded missing E_T and jet triggers cuts
- This implies
  - Increase trigger acceptance rates at each trigger level and at the output
  - Bring more information to L1
  - Much more HLT processing power needed
  - Porting of offline algorithms and techniques to HLT

T/DAQ operations @ run 2

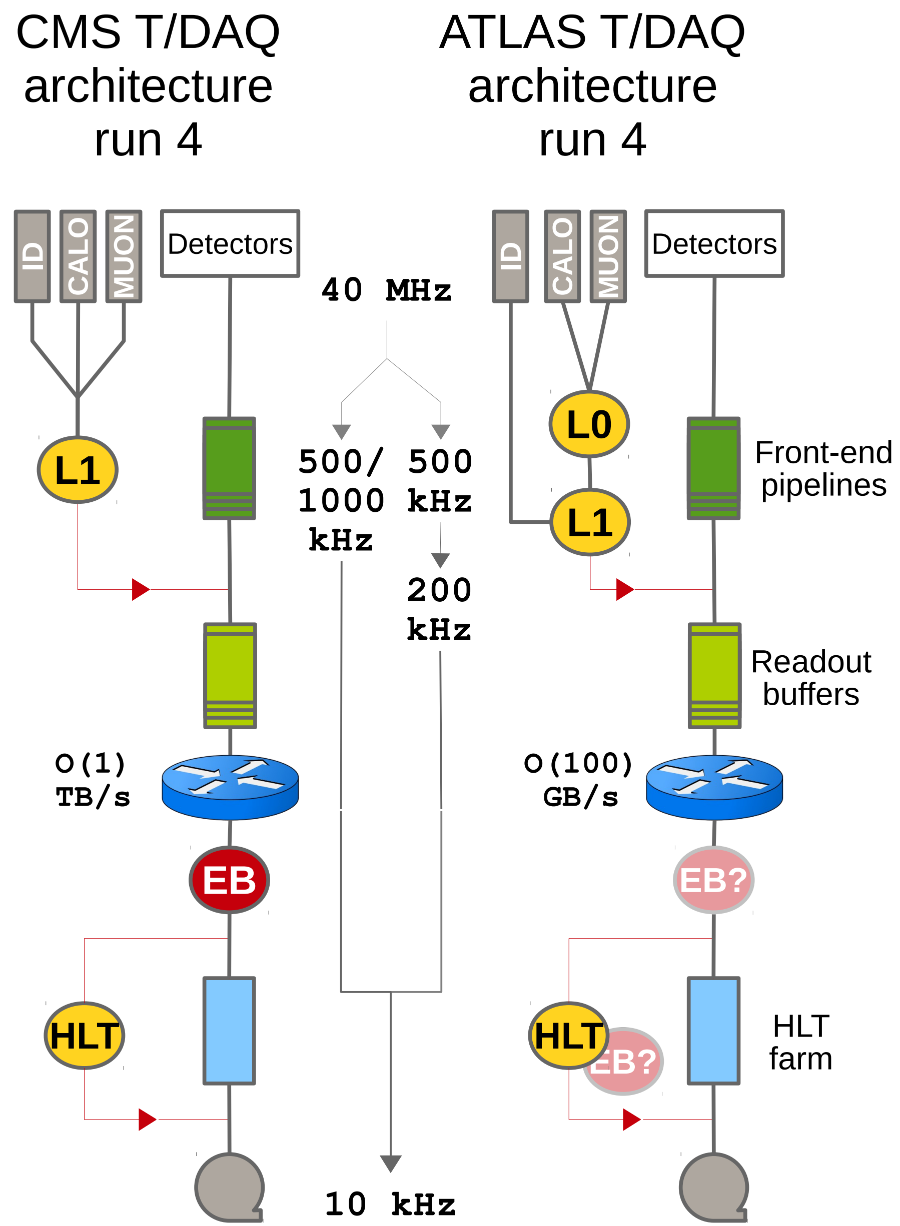
- Current Trigger/DAQ working points for ATLAS & CMS
  - L1 accept ≤ 100 kHz
  - L1 latency: 2.5 vs 4 μs
  - Event Building: 10 vs 100 kHz
  - HLT accept: ~ 1 kHz
- This does not scale up to HL-HLT
  - Relevant trigger objects will sum up to about 500 kHz
    - E.g.: extrapolated L1 trigger rates based on phase-1 HW (ATLAS)

Trigger	Estimated L1 Rate
EM_20 GeV	200 kHz
MU_20 GeV	> 40 kHz
TAU_50 GeV	50 kHz
di-lepton	100 kHz
JET + MET	~ 100 kHz
Total	500 kHz



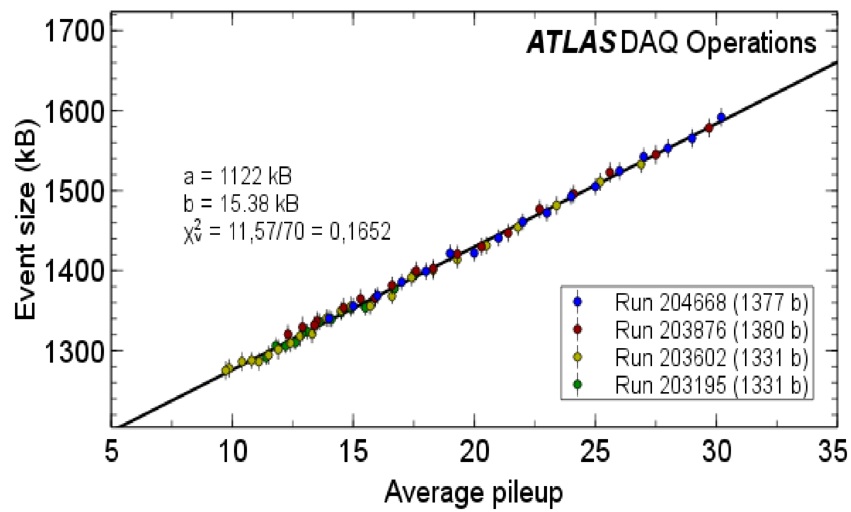
T/DAQ operations @ HL-LHC

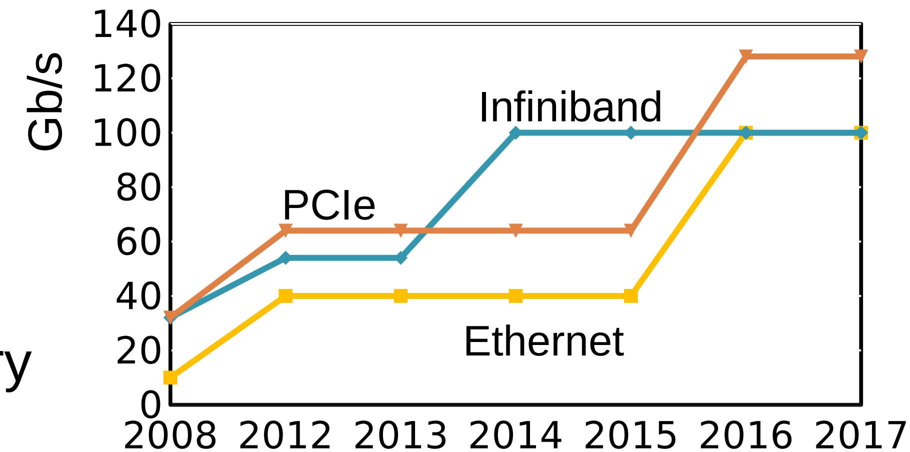
- Readout (RO) constraints
  - CMS: latency ≤ 10 µs
  - ATLAS: latency ≤ 20 µs, RO ≤ 200 kHz
  - Dead material for Inner Detector RO
- L1 output rate raising
  - CMS: L1: 500 – 1000 kHz (20 – 10 µs)
  - ATLAS: L0: 500 kHz (6 µs)
    → L1: 200 kHz (14 µs)
- Bring more information to L1
  - New track triggers
    - In ATLAS after L0 preselection
  - Finer granularity calo & muon information
- HLT output at 5 – 10 kHz
  - Downstream computing limit
  - Rejection factors: CMS ~100
    ATLAS ~40



Read-out requirements

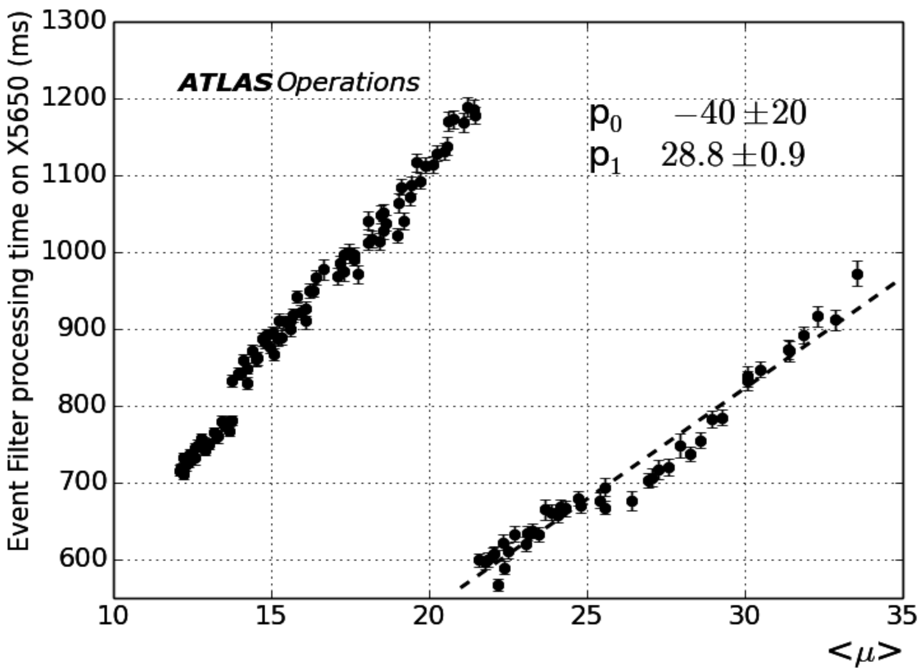
- Event size ~ 4MB
  - Based on linear extrapolation
- CMS: full event building at 0.5 – 1 MHz
  - 4MB @ 1 MHz = ~ 32 Tb/s
- Equivalent to 500 links @ 100 Gb/s
  - By the end of LS2 100 GB/s will be readily available
- Switch capability almost possible today
  - no problem in 10 years
- New packaging and interconnect technologies seems able to provide required performance
  - ATCA, μTCA
- In not radiation environments all network and link needs will be satisfied by industry
  - In radiation hard area moving to **G**iga**B**it **T**ransceiver architecture



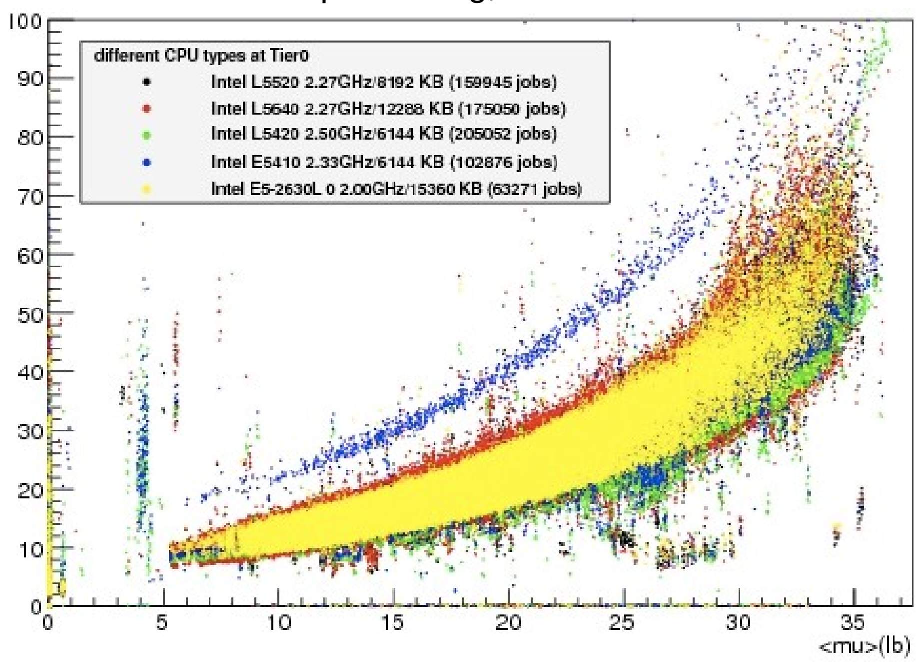


HLT Processing Power

- HLT farm input rate x5 – x10 (0.5 – 1 MHz)
  - Output rate x10, i.e.: same rejection factor as run2
- Moving from 8 to 14TeV will give a ~ x2 rate increase
  - More precise evaluation in run2
- HLT processing time
  - So far, it almost scale with <μ>, but non linearity observed in offline
  - Not obvious how it will scale up to 140

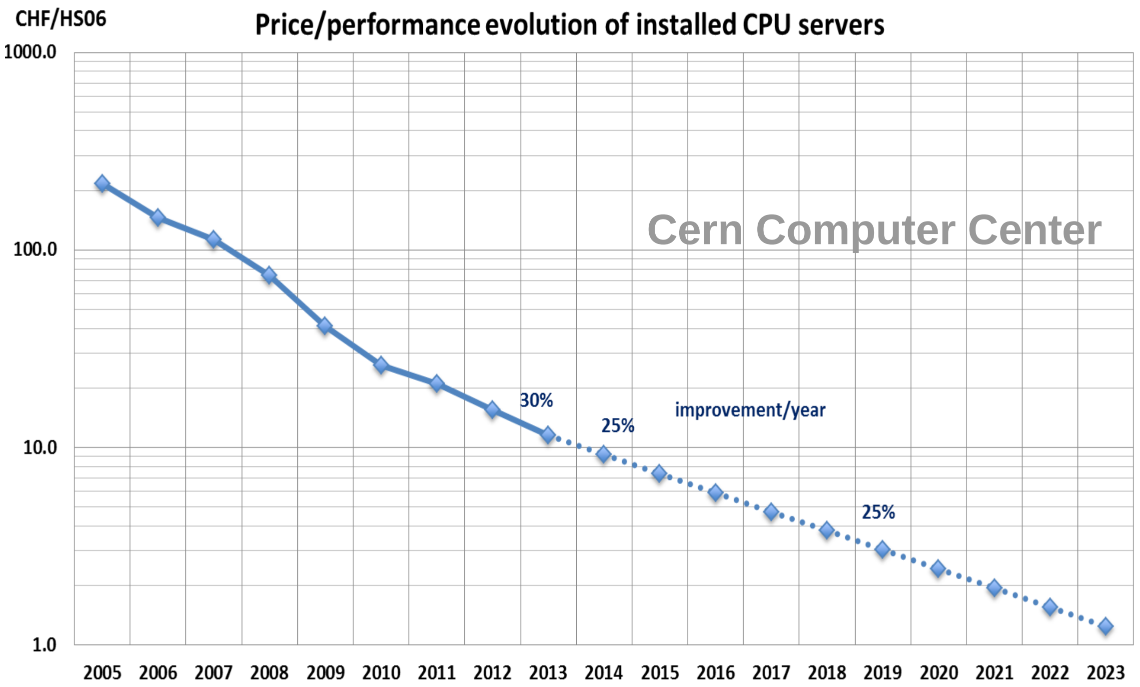


ATLAS: T0 processing, JetTauEtMiss stream



HLT Processing Power

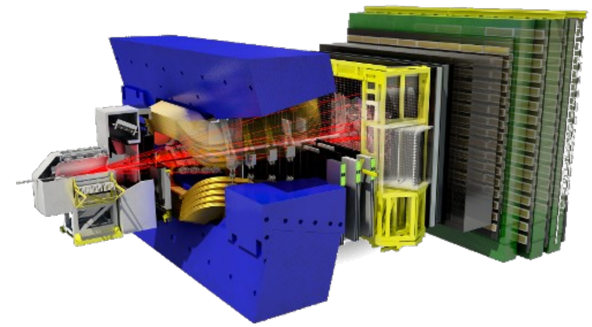
- CMS estimates **x25 – x50** factor increase in needed HLT processing power
  - ~10 M HEP-SPEC-06
- Price performance scaling extrapolation: 25%/year
  - Assuming a flat budget → Factor ~ **x10** for phase-2

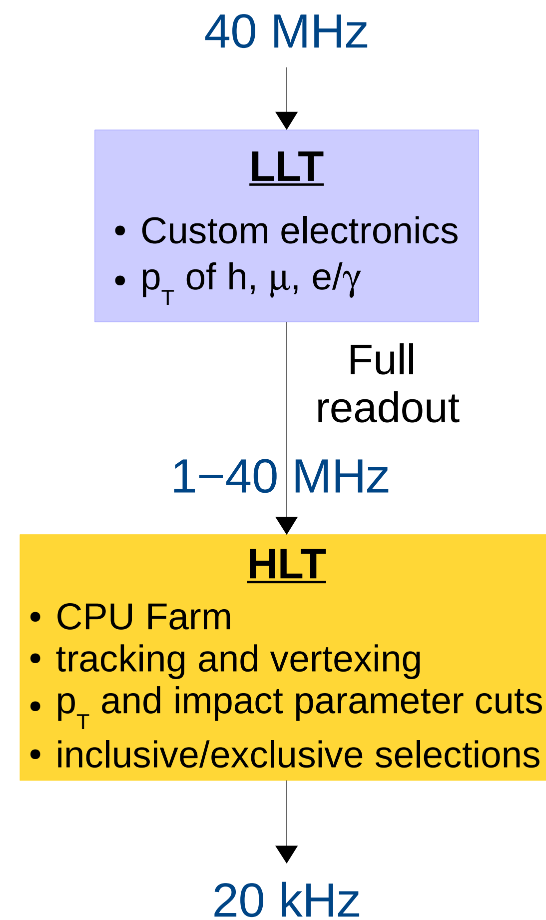


- Deficit factor **x2.5 – x5**
  - Market is providing alternative solutions to optimize performance/costs: ARM, Atom, GPUs, FPGA
  - Possibility to share resources with Tier-0
- But the SW must be able to fully exploit the H/W capabilities
  - This is not the case of the current HEP S/W
  - More parallelism at all levels and large S/W improvements are required

Before Phase 2

- In Phase 1, ALICE and LHC-b are moving to triggerless architectures
  - Eg: LHC-b will execute whole trigger on CPU farm
  - up to 40 MHz input rate and 20 kHz output rate
- They will face in Phase 1 many of the network and HLT processing issues expected for Phase 2
  - LHC-b estimates 8M HEP-SPEC-06
    - Factor ~2000 wrt today
    - Comparable with ATLAS&CMS phase 2
  - LHC-b DAQ bandwidth will be ~ 32 Tb/s
    - i.e. compatible with CMS Phase-2
- Triggerless option for ATLAS&CMS seems unfeasible
  - Aggregate B/W: ~1200 Tb/s (x750 wrt today)
  - HLT Processing power: ~360M HS06 (x2000 wrt today)
  - Too much dead material for tracker readout





Conclusions and hot topics

- In phase 2 the ATLAS and CMS trigger rates will be increased by a factor ~10 at all the levels
- This requires bringing more information at L1
  - Track trigger information at L1 will provide the required trigger efficiency for electrons, muons, taus, MET and jets
    → **Topic of Alberto's talk**
  - The higher rate and the track trigger integration entail major changes in each L1 trigger sub-systems: finer-grain and higher bandwidth. E.g. improved L1 muon triggers
    → **Topic of Nicola's talk**
- HLT will face challenging scalability issues related to rates and pile-up
  - Alice and LHC-b will face those problems already in Phase-1
    → **Topic of Silvia's talk**