ELECTRONICS FOR HL-LHC CALORIMETRY

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Introduction

- Both ATLAS and CMS are planning significant upgrades of their read-out and trigger electronics for Phase II
- Driving factors:
  - *Radiation resistance: replace components with versions more rad-tol (when required) to sustain 3000 fb^{-1}*
  - *Ageing: some components would have ~30 yrs operation (cfr. ~10 yrs by design). Also difficult to maintain and repair.*
  - *Provide highest granularity information and resolution: efficient and selective triggers at high lumi ($L=5x10^{34}$ cm^{-2} s^{-1}/μ=140); Making extensive use of detailed topology of clusters and events; Providing improved Calorimeter Trigger primitives for e/γ/τ/jets, matching with Track Trigger, isolation, etc*

Introduction

- General trend for LHC calorimeter read-out architecture:
  - *Remove all on-detector sums*
  - *the data are not buffered in the front-end, but rather streamed off-detector at LHC bunch-crossing frequency of 40 MHz*
  - *fast pre-processors convert raw-data into calibrated information that feed the trigger system where improved and more complex algorithms are applied*
  - *Off-detector buffers: allow for a much higher trigger latency or purely software-based triggers*
- Changes required on both front-end and back-end systems

Common issues

- On-detector front-end electronics: preamp and shaping, ADC,… with sufficient resolution and large dynamic range (~16-bit)
  - *COTS vs. ASIC development*
  - *Low power, low latency*
  - *Radiation tolerant (in particular SEE)*
- High speed optical data links (≳10 Gbps)
  - *CERN (GBTx) , other developments, COTS,…*
  - *Radiation tolerant (in particular SEE)*
- High performance back-end systems:
  - *x-TCA family: ATCA (ATLAS), μTCA (CMS)*
  - *Alternatively development of high bandwidth system based on PCIe cards to interface detector specific front-end to DAQ systems on a switched network.*
- New electronics → new supply voltages → new power distribution scheme:
  - *High power DC-DC converters*
  - *Local regulation on the front-end element on-detector.*

Upgrade plans

- ATLAS
  - *LAr system: replace all Front End Boards (FEBs)*
  - *LAr hadronic end-cap: studies so far seem to indicate that the HEC cold electronics will survive radiation dose; now performing ageing studies*
  - *sFCAL, mini FCAL: new detector → new electronics*
  - *Hadronic Tile calo: replace all FE electronics (drawers)*
- CMS
  - *ECAL barrel: replace electronics; FE (digital) and VFE (analog)*
  - *HCAL barrel (Phase 1): new electronics (SiPM) and new readout*
  - *ECAL, HCAL endcap: new detector → new electronics*

Radiation estimate (ATLAS)

- Radiation Estimate Task Force: review projected radiation levels and re-evaluate safety factors in ATLAS
- TID and NIEL evaluation in calorimeter region
- Passive dosimeters (~70 TLDs) installed in the crack region of the calorimeters (both barrel and EC), in the LAr crates, near the Tile drawers in the gap between the EC cryostat and the Tile Extended Barrel
- 22 RadMons for neutron 1 MeV Si eq. fluence (and independent TID measurements as well - but with less precision)
- Comparison to FLUGG prediction
- **TID:**
  - ***10-20% agreement***
- **NIEL (worst case in the LAr barrel crates):**
  - *Calculated: Φ [1 MeV Si eq. $x10^9 cm^{-2}/fb^{-1}$] =* ***1.69 ± 0.25***
  - ***Predictions over-estimate measurements***
  - ***Ratio data/FLUGC simulation: x0.74, 0.50, 0.62 [side A,C, combined]***
- **+ Studies performed for SEE**

Radiation estimate

	Simul
TID	3.5
NIEL (neutron DD)	5
SEE (E>20 MeV)	5

Sf_{sim}:

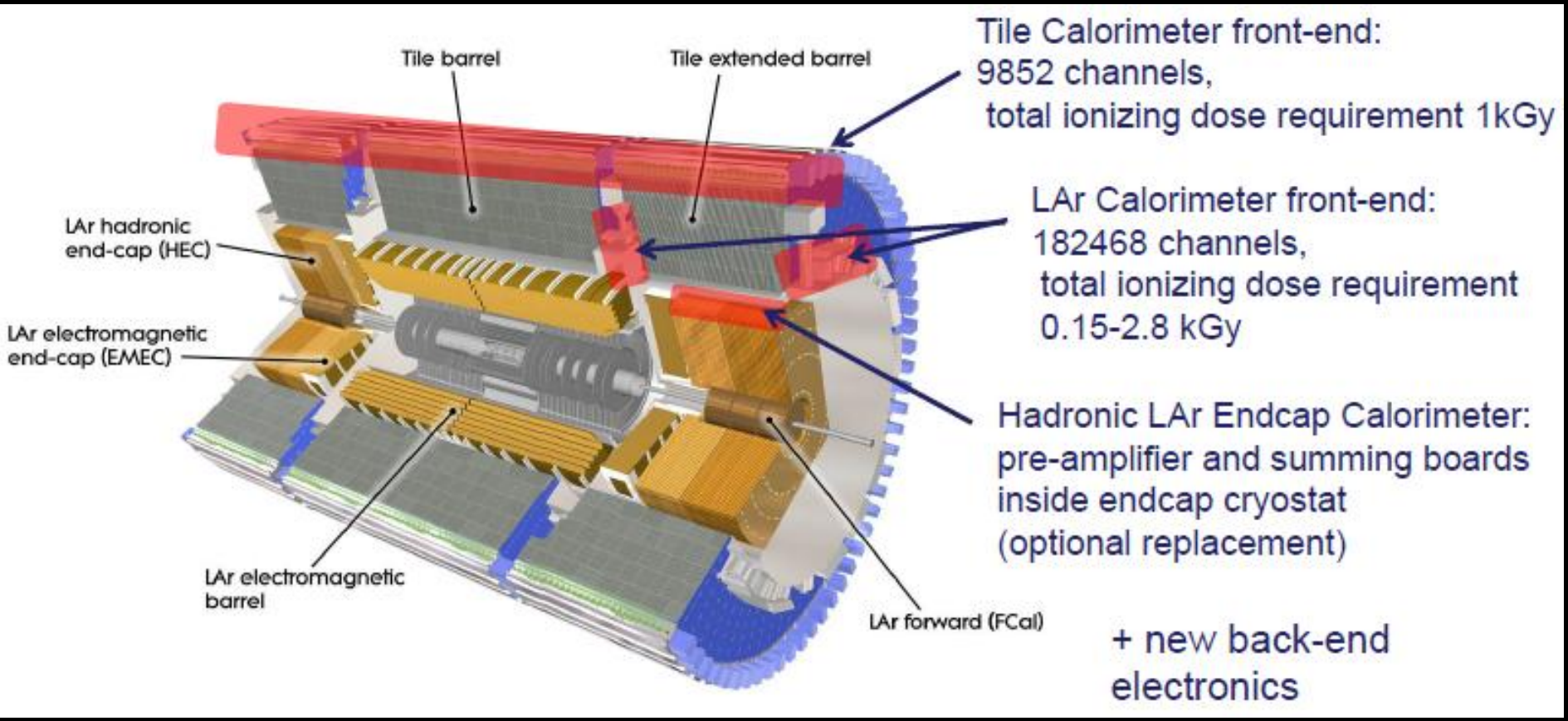
1.5 (everywhere in ATLAS)

1.5 in the Inner Detector/2 elsewhere in ATLAS

2 (everywhere in ATLAS)

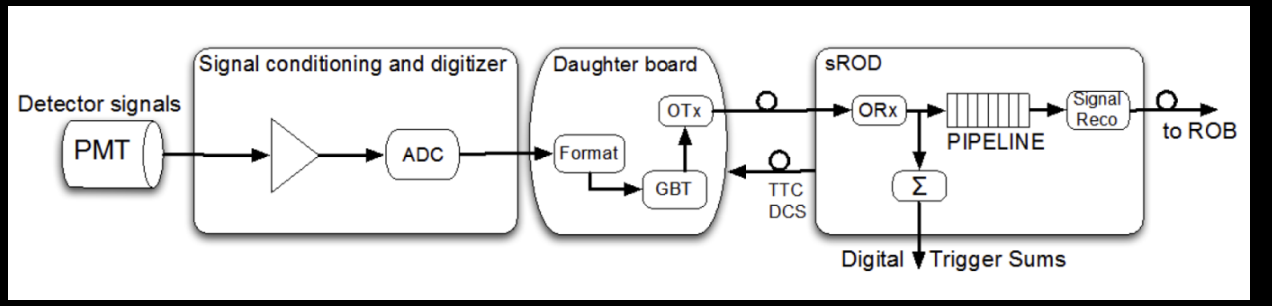
- Less than expected NIEL values in HEC cold electronics region
- GaAs pre-amplifier and summing chips installed inside LAr cryostat
  - *Delicate operation to open cryostat (need time, high radiation levels)*
- In case of replacement:
  - *Cold Si CMOS FET IHP*

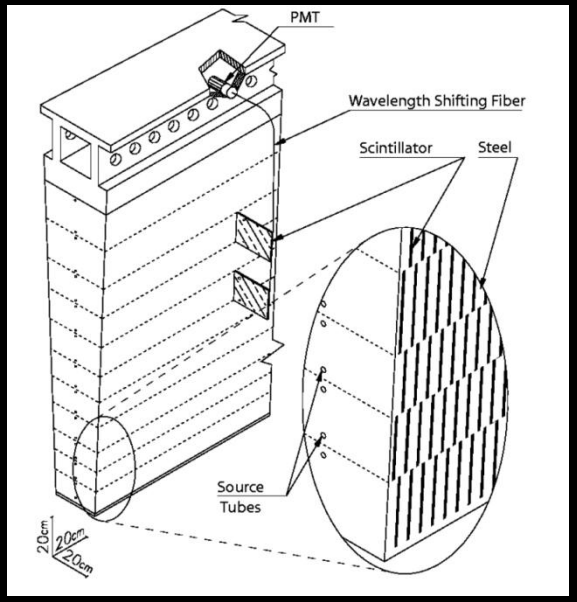
ATLAS



Level-0 with accept rate of 500 kHz and latency of 6 μs
Level-1 with accept rate of 200 kHz and latency of ~20 μs

ATLAS Tile





- Front-end electronics installed in 256 drawers:
  - *To implement free-running design with 40 MHz digitization*
- Main front-end components:
  - *Mixed analog/digital Main Board*
- Front-End Board: 3 alternative developments
  - *evolution of today's 3-in-1 card: shaper, 2-gain amplifier, 3-gain integrator for Cs calibration, discrete (UCHIGAO)*
  - *QIE10 based design (FERMILAB/ARGONNE)*
  - *new ASIC development: FATALIC/TACTIC 130 nm IBM process , 3 gain shaper, 12-bit pipeline ADC (CLERMONT-FERRAND)*

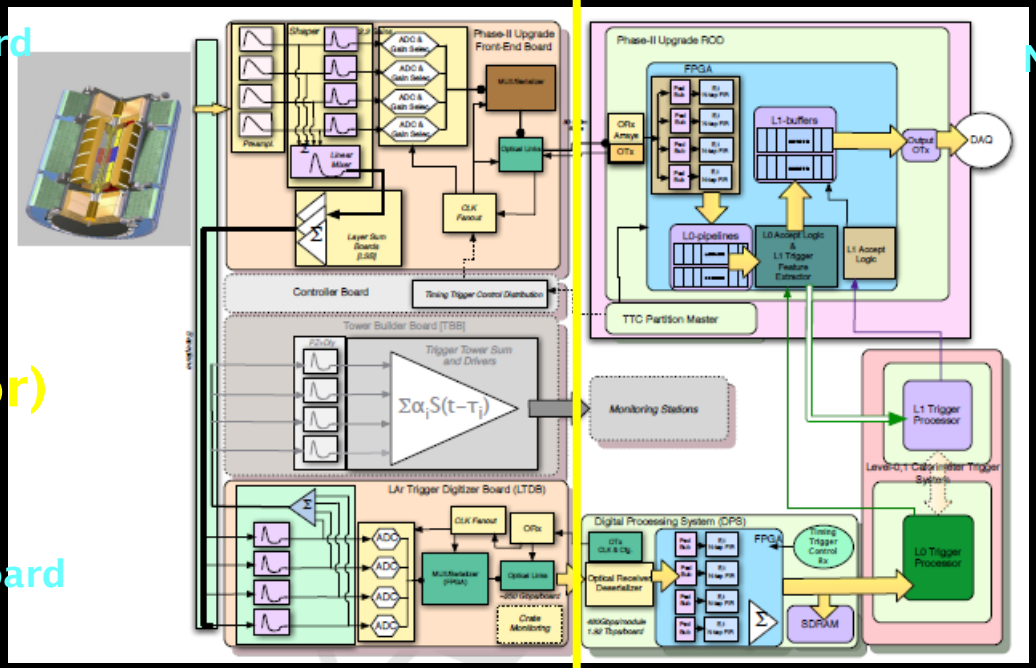
ATLAS Tile

- On daughter boards:
  - *Kintex-7 FPGA and CERN GBTx being studied for data transmission*
- Back-end:
  - *Read-Out Driver in ATCA format*
  - *full custom ATCA blade design with Virtex7/Kintex7 FPGAs*
  - *625 Gbps per Board and 20 Tbps total*
  - *signal extraction, bunch-crossing identification for trigger, pipeline buffer, TTC signal distribution*
- One TileCal drawer is planned to be equipped with a full demonstrator front-end and back-end system in LS 1
- Italian involvement (Pisa):
  - *Expressed interest in setting up a test system to validate the new architecture and compare the different solutions proposed by the Collaboration*

LAr electronics upgrade

New Front End Board (FEB2)

New ROD (sROD)



Front end (on detector)

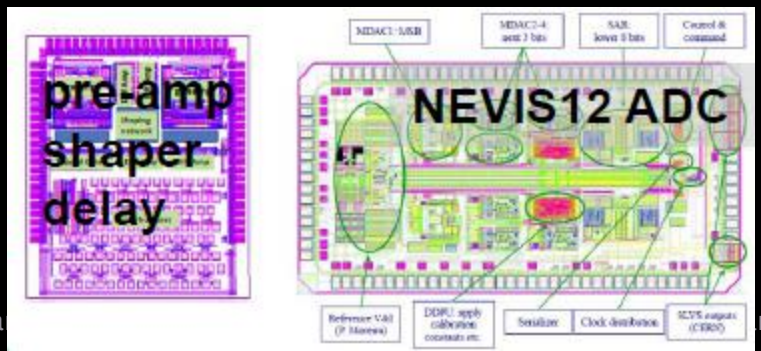
Back end (off detector)

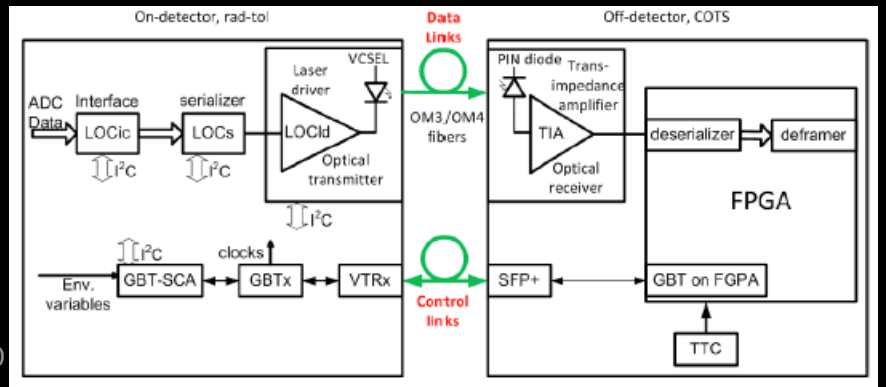
Phase-I trigger board

- Send all data off detector for trigger and read-out at LHC bunch-crossing frequency of 40 MHz (total bandwidth 140 Tbps)
- Need to replace all FEBs and RODs: -> FEB2, sROD
  - *Phase-I new trigger boards (LTDB) will stay to provide a Level-0 low latency trigger*

New Front-End

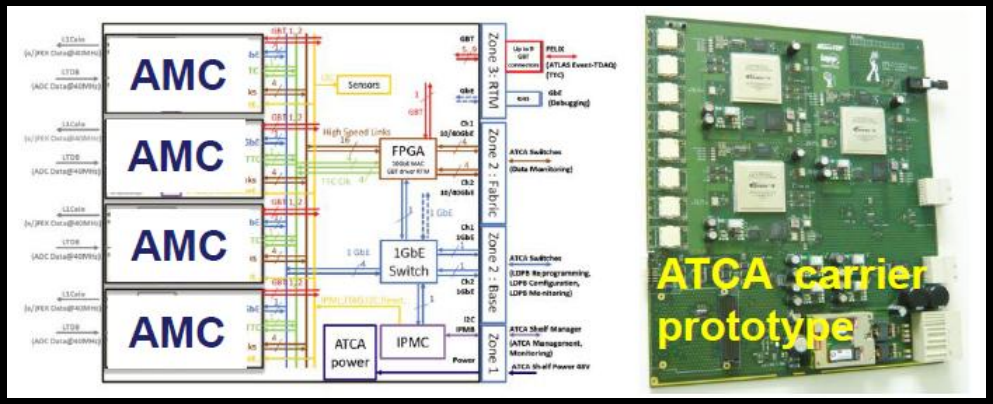
- New pre-amplifier + shaper integrated in a single ASIC:
  - *Low noise, 16-bit dynamic range, followed by low power differential shaping stage*
  - *SiGe BiCMOS technology: Investigations performed with IBM 8WL; test a cheaper process (IHP)*
- New ADC (candidates for Phase 1 than will evolve for Phase II):
  - *Custom NEVIS/PEALL12-bit ADC, IBM 130nm CMOS, low power (30-50 mW/channel), low latency (<90 ns) , radiation tolerance: 12 kGy, 3.3 x 10^{14} n_{eq}/cm^2, 6.3 x 10^{13} h/cm^2*
  - *COTS: 12-bit Texas Instruments ADS5272 performed best → radiation tolerant up to 1 kGy (100 krad), low power (113 mW), low latency (163 ns)*
- Data transfer:
  - *Link-on-chip (LOC) development in Silicon-on-Sapphire (SoS) 0.25 µm ; should allows 8 Gbps design; custom interface and serializer; VCSEL pairs from Versatile Link → Total latency 76 ns (comp. GBTx 220 ns)*
  - *CERN GBTx is used for TTC data*
  - *Phase-II requires 12 x 10 Gbps VCSEL arrays: improved SoS process or a next-generation GBTx*





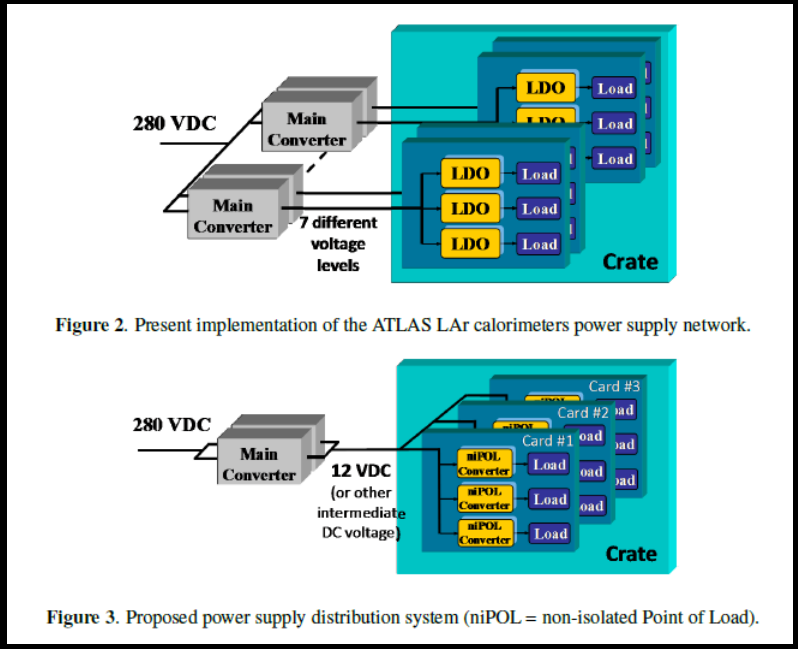
New Back-end

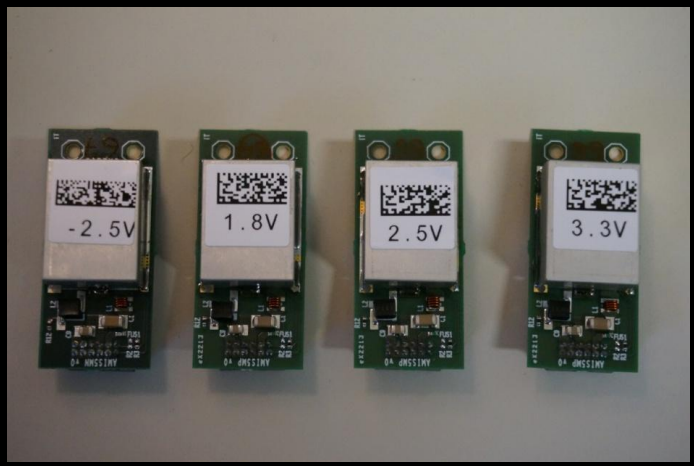
- The data are received using serial optical links on multi-fiber ribbons. The conversion to electronic signal will be performed by commercial components and de-serialization will be handled by fast FPGA transceivers.
- Data planned to be processed by high-bandwidth ATCA Pre-Processor boards
  - *1.2 Tbps input from front-end and ~250 Gbps trigger information to Level-0*
  - *ATCA carrier, AMC boards, FMC, board controlo with IPMI*
- Algorithms to be implemented:
  - *energy reconstruction, bunch-crossing identification, pipeline, trigger sums or more complex algorithms, like the extraction of EM shower shapes*
- Already being studied for Phase I:
  - *will evolve into Phase II solutions*



Power distribution

- Need to re-design the system from the AC-DC converters down to the POLs on the FEB2s
- Same approach as for LTDBs for Phase I upgrade but Powering for Phase II is a much larger effort:
  - More boards, more complex layout, re-design system to start from a single intermediate voltage instead of creating voltages from available lines
- Need to select components rad-tolerant and that can operate in a magnetic field
- CERN POLs (V_{in}=12V, various V_{out}, I_{out}=4A max)
  - Need to be repackaged
  - need more max output current (~10 A)
- All LVPS will need to be replaced with new units generating a single intermediate voltage (eg, 12 V)

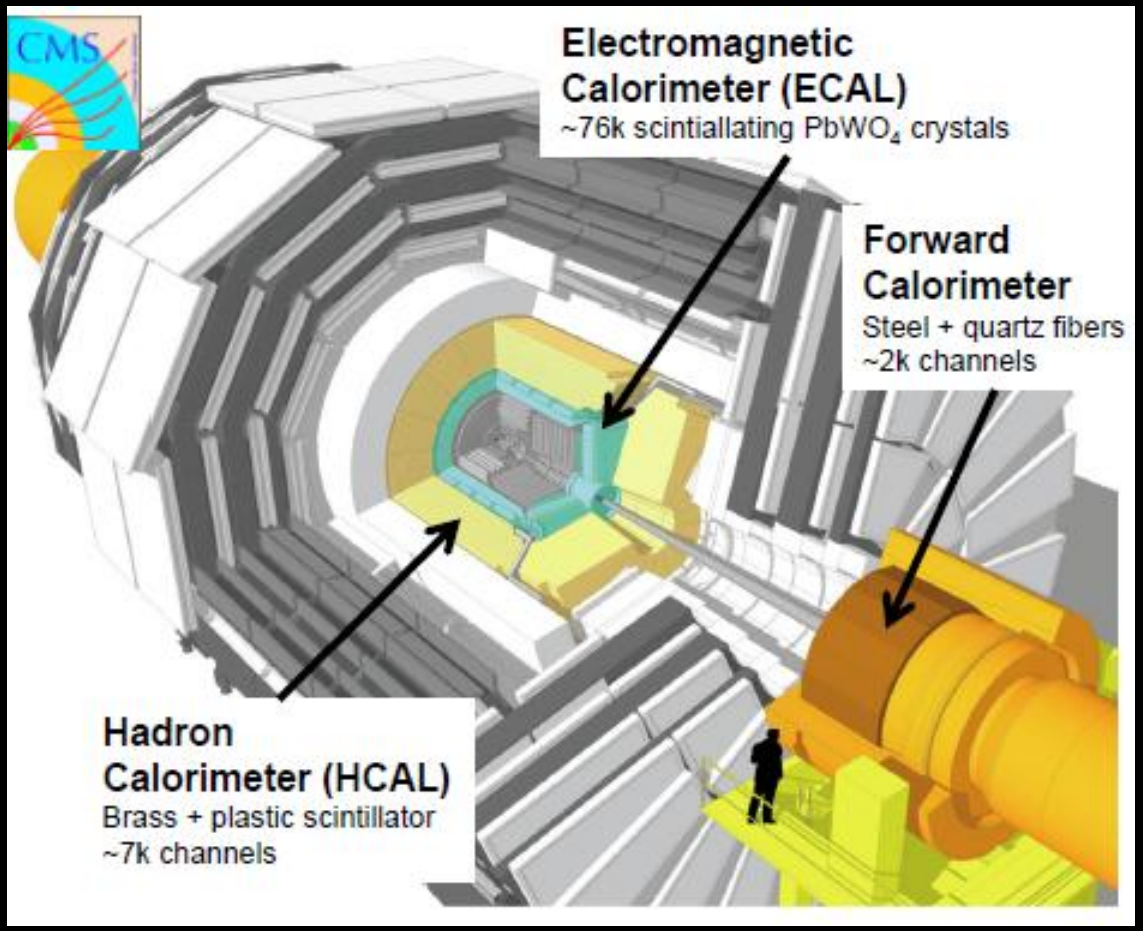




Lar electronics upgrade

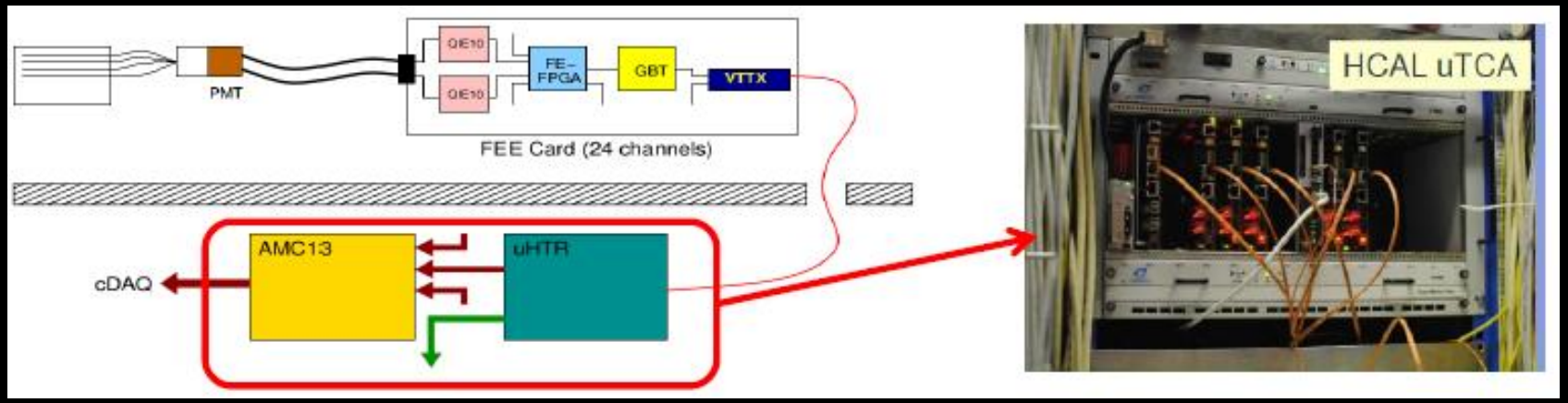
- Italian interests (Milano):
  - *New power distribution scheme (activity started for Phase I and will evolve in Phase II)*
  - *Back end signal processing and triggering:*
  - *implementation of FPGA algorithms on the digitized data from the FEB2*

CMS



L1 requirement of 20μs latency and 1MHz read-out rate

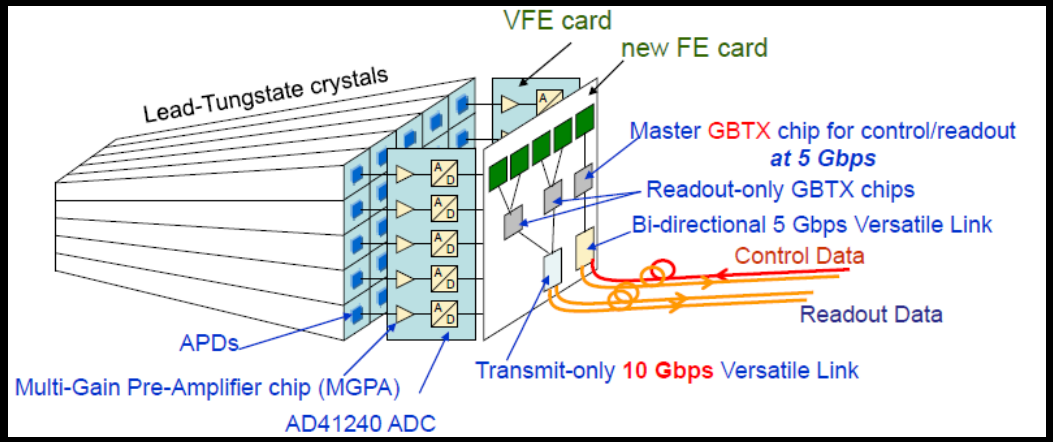
CMS HCAL



- Upgrade during LS1 and LS2
- Silicon Photomultipliers (SiPM) will replace Hybrid Photon Detectors (HPD) in LS 2 in HCAL Barrel and Endcap
- Data will be sent to trigger and read-out at 40 MHz
- HCAL front-end to be equipped with QIE10 chip for charge integration and encoding:
- Radiation tolerant FPGAs
- CERN GBTx/Versatile Link to back-end
- preprocessing and event building in μTCA modules: μHTR (FPGA Virtex 6), AMC13

CMS ECAL Barrel

- Remove all 36 supermodules, replace FE cards + services
- New FE card:
  - Remove all L1 crystal sums, remove buffer, send all data out at 40 MHz
  - CERN GBTx/Versatile link for data transfer to back-end and control
  - will need 10 Gbps rad-tolerant link
- New back-end
  - Evolution of MP7 μTCA board as developed for Phase I trigger based on FPGA Xilinx Virtex 7



CMS ECAL Barrel

- Consider also replacement of VFE
  - *Change preamp, shaper, ADC*
- **Reasons for upgrade:**
  - *Mitigate spikes in APD due to ionization in Si (~1 spike per event at HL-LHC)*
  - *Mitigate noise due APD leakage current increase from neutron damage*
  - *Mitigate pile-up (140 events per crossing, in-time and out-of-time)*
- Lower shaping time would mitigate these effects
- VFE upgrade would also imply upgrade of LV regulator board to provide new voltages
  - *Try also to reduce power dissipation due to present regulators*
- Investigate also the possibility to redesign cooling system to cool ECAL barrel to 8-10^{0}C to mitigate the APD radiation-induced noise
- Italian interest in electronics upgrade:
  - *Milano, Torino (VFE), Roma (APD test)*

Conclusions

- Goal of all LHC calorimeter electronic developments is to meet the challenging pile-up and radiation requirements and to ensure longevity of the systems throughout Phase II
- Examples of common development paths for on-detector and off-detector electronics:
  - *qualification of radiation tolerant commercial components: ADCs, FGPAs*
  - *qualification of custom devices, e.g. QIE10 chip explored by ATLAS and CMS*
  - *CERN GBTx/Versatile Link often implemented : although 10 Gbps radiation tolerant version needed by ATLAS LAr and CMS ECAL*
  - *development and testing of distributed powering components*
  - *ATCA , μTCA processing boards and alternatives like PCIe FPGA boards*
- Several R&D activities have already started

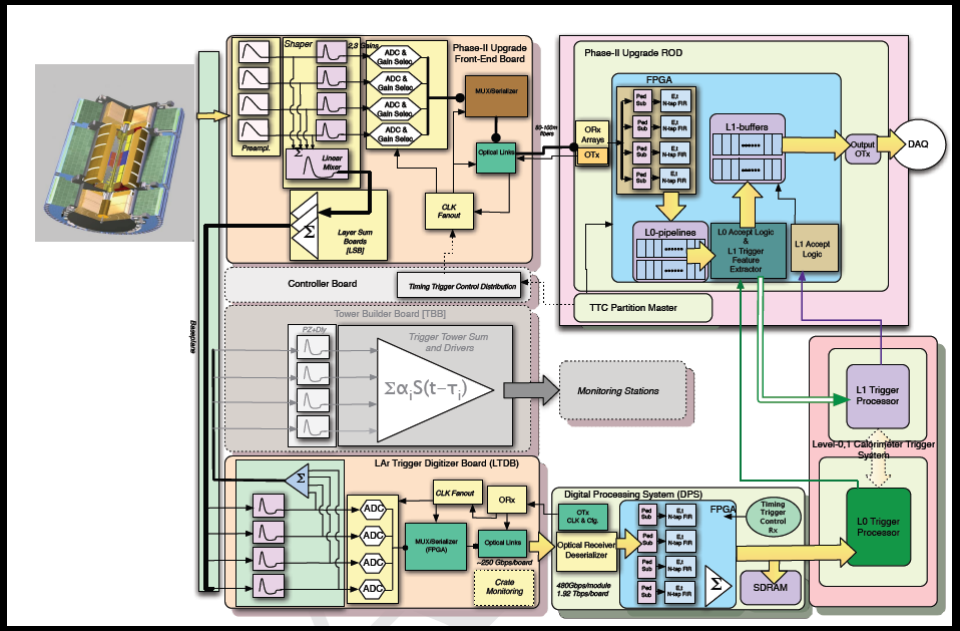
Back-up

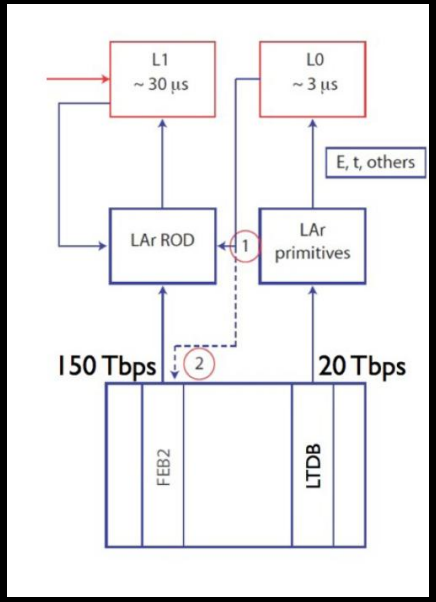
Phase II (Lar)

- LAr has developed four options to progress towards a decision whether to open or not the cryostat:
- **Option 0: No change neither of the HEC cold electronics nor of the FCal detectors.**
- **Option 1: If the HEC cold electronics have to be replaced, the large cold cryostat cover would have to be opened and the irradiated FCal would have to be removed. A newly built cold FCal (sFCal) would then be inserted before closing the cryostat.**
- **Option 2: If the HEC cold electronics do not have to be replaced, the cold FCal would be replaced by a new one of the sFCal type. It is anticipated that only the small cover of the cold vessel, the FCal bulkhead, would have to be removed.**
- **Option 3: If the HEC cold electronics do not have to be replaced, the cold FCal would stay in place and a new small calorimeter (Mini-FCal) would be placed in front of it. In this case only the cryostat warm vessel would have to be opened.**

Phase II

- The Phase I upgrade is compatible with the Phase II
- New FEB2s will be fitted in the existing Front End Crates and will use the same baseplanes built for Phase I:
  - Lar has already acquired all connectors needed for the FEB2s before they disappear from market
- Phase I LTDBs will also stay
  - Can be used to provide a low latency L0 trigger using the supercell granularity
- The full LAr calorimeter granularity will be available to the L1 trigger to further refine the trigger decision, possibly based on refined reconstruction in a region-of-interest determined by L0.





ATLAS

Table 3.4: Radiation tolerance criteria of the LAr electronics for operation at HL-LHC for a total luminosity of 3000 fb^{-1}, including safety factors given in brackets. For ASICs, the pre-Phase-II and Phase-II conditions are compared. For all other electronics components (HEC pre-amplifier and summing (PAS) chips, COTS, and low-voltage power supply (LVPS) electronics) the Phase-II requirements are listed.

	TID (kGy)		NIEL (n_{eq}/cm^2)		SEE (h/cm^2)	
ASICs (pre-Phase-II, 1000 fb^{-1})	0.58	(5.25)	1.7×10^{13}	(5)	3.2×10^{12}	(5)
ASICs (Phase-II)	1.74	(5.25)	5.0×10^{13}	(5)	9.6×10^{12}	(5)
ASICs PAS HEC	5.0	(5)	4.1×10^{14}	(5)	5.1×10^{13}	(5)
COTS (multiple lots)	23.4	(70)	2.0×10^{14}	(20)	3.9×10^{13}	(20)
COTS (single-lot)	5.7	(17.5)	5.0×10^{13}	(5)	9.6×10^{12}	(5)
LVPS (EM barrel and endcap)	1.35	(70)	2.3×10^{13}	(20)	6.0×10^{12}	(20)
LVPS (HEC)	0.1	(5)	6.9×10^{12}	(5)	6.9×10^{11}	(5)

LAr PHASE II upgrade (LS3)

12/12/2015

		it will happen [MCHF]	it might happen [MCHF]	2015 [MCHF]	2016 [MCHF]	2017 [MCHF]	2018 [MCHF]	2019 [MCHF]	2020 [MCHF]	2021 [MCHF]	2022 [MCHF]	total [MCHF]
	LAr electronics											
1	***HV supplies for FCAL***	*0.080*				*0.004*		*0.004*	*0.048*	*0.024*		0.080
	Low Voltage power supplies											
2	LVPS	*3.184*				*0.159*		*0.159*	*1.910*	*0.955*		3.184
3	DC-DC Point of Load Regulators	*2.122*				*0.106*		*0.106*	*1.273*	*0.637*		2.122
4	LVPS for HEC front-end	*0.478*				*0.024*		*0.024*	*0.287*	*0.143*		0.478
5	Cabling, monitoring, testing	*0.424*				*0.021*		*0.021*	*0.254*	*0.127*		0.424
	Calibration system											
6	EM and FCAL	*1.698*				*0.085*		*0.085*	*1.019*	*0.509*		1.698
7	HEC	*0.212*				*0.011*		*0.011*	*0.127*	*0.064*		0.212
	FE ASIC and components											
8	R&D and prototypes	*0.467*		*0.047*	*0.420*							0.467
9	ASIC Production	*4.130*					*0.083*	*2.808*	*1.239*			4.130
10	Other components	*0.424*					*0.008*	*0.288*	*0.127*			0.424
11	Tests	*0.085*					*0.002*	*0.058*	*0.026*			0.085
	FE boards											
12	Prototypes and tests	*0.438*		*0.219*	*0.219*							0.438
13	Materials	*3.608*				*0.180*		*0.180*	*2.165*	*1.082*		3.608
14	Assembly	*1.910*				*0.096*		*0.096*	*1.146*	*0.573*		1.910
	Back end electronics											
15	Links from FEB-2 to ROD-2	*2.335*				*0.117*		*0.117*	*1.401*	*0.701*		2.335
16	Prototypes	*2.122*				*0.212*	*1.910*					2.122
17	Crates, PS and CPU	*0.409*						*0.041*	*0.245*	*0.123*		0.409
18	TTC/Controllers	*0.123*						*0.012*	*0.074*	*0.037*		0.123
19	Transition Modules	*0.344*						*0.034*	*0.206*	*0.103*		0.344
20	Pre-Processor boards (ROD-2) production and testing	*4.401*						*0.440*	*2.641*	*1.320*		4.401
21	***DCS and Monitoring***	*0.212*						*0.021*	*0.127*	*0.064*		0.212
22	***Irradiations***	*0.265*		*0.027*	*0.239*							0.265
23	***System Tests and testbeams***	*2.547*		*0.255*	*2.292*							2.547
24	***Logistic (Infrastructure, shipment)***	*0.106*						*0.011*	*0.064*	*0.032*		0.106
	HEC PAS		*2.3*									
	sFCAL		*8.5*									
	Cryostat opening/closing		*3.8*									
	TOTAL	***32.124***	***14.600***	*0.547*	*3.170*	*1.015*	*2.003*	*4.517*	*14.379*	*6.494*	*0.000*	***32.124***