CHIPIX65

Sviluppo di un pixel chip innovativo in tecnologia CMOS 65nm per altissimi flussi di particelle e radiazione agli esperimenti di HL_LHC e futuri collider di nuova generazione

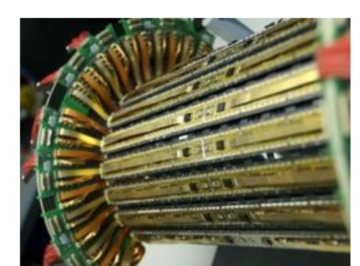
F. Palla, R, Beccherle

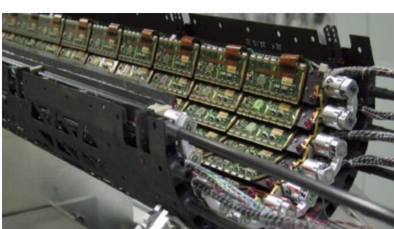
Call CSN5. Responsabile nazionale L. Demaria

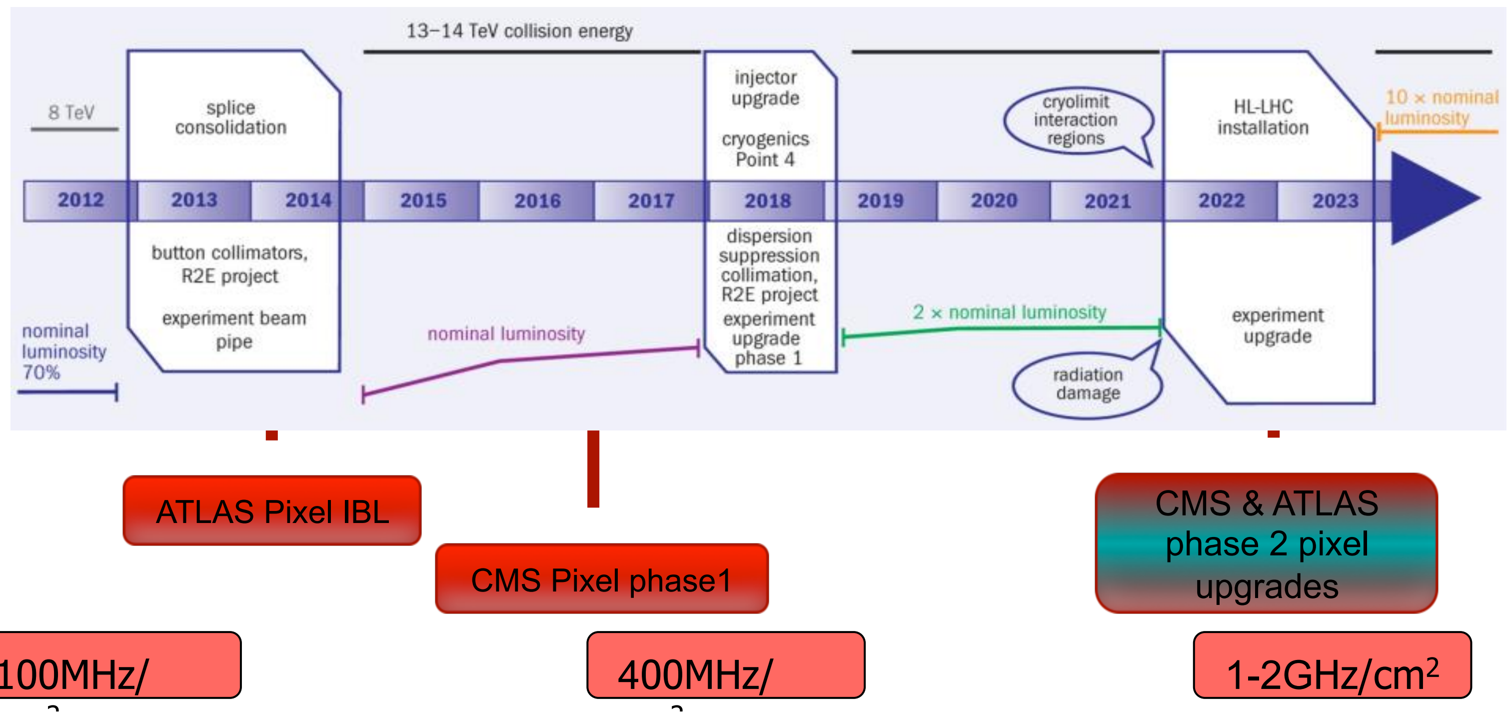
Quadro generale

- Upgrade di fase 1: ~4 x hit rates
  - ATLAS: Addition of inner B layer with new 130nm pixel ASIC (FEI4)
  - CMS: New pixel detector with modified 250nm pixel ASIC (PSI46DIG)

- **Phase2 upgrades**: ~16 x hit rates, 2-4 x better resolution, 10 x readout rates, 16 x radiation tolerance, Increased forward coverage, less material,
  - **Installation: ~ 2022**
  - **Relies fully on significantly improved performance from next generation pixel chips.**







Phase 2 pixel challenges

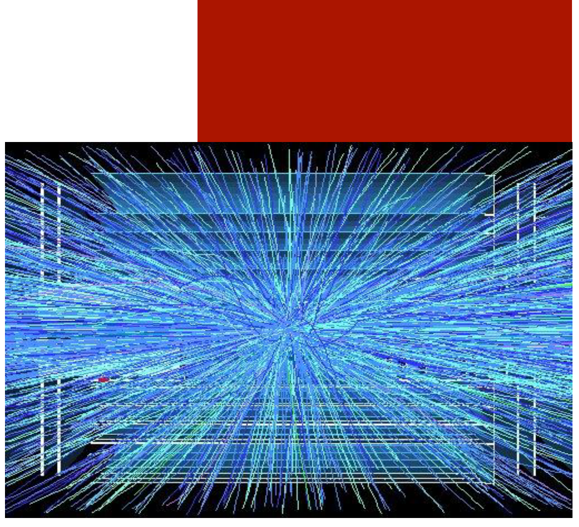
- ATLAS and CMS phase 2 pixel upgrades very challenging
  - **Very high particle rates: 500MHz/cm²**
    - Hit rates: 1-2 GHz/cm² (factor 16 higher than current pixel detectors)
  - **Smaller pixels: ¼ - ½ (25 – 50 um x 100um)**
    - Increased resolution
    - Improved two track separation (jets)
  - **Participation in first/second level trigger**
    A. 40MHz extracted clusters and shape (outer layers) ?
    B. Region of interest readout for second level trigger ?
  - **Increased readout rates: 100kHz -> 1MHz**
  - **Low mass -> Low power**

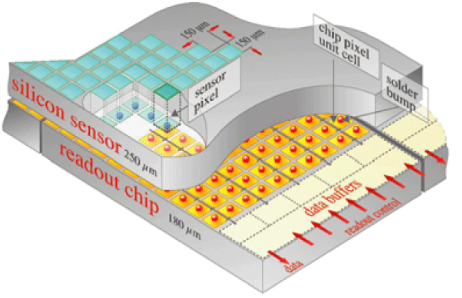
  Very similar requirements (and uncertainties) for ATLAS & CMS

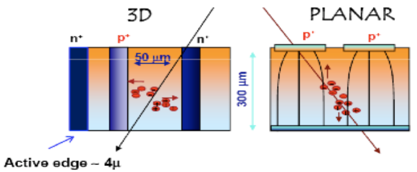
- **Unprecedented hostile radiation: 10MGy(1Grad), 10^{16} Neu/cm²**
  - Hybrid pixel detector with separate readout chip and sensor.
  - Phase2 pixel will get in 1 year what we now get in 10 years

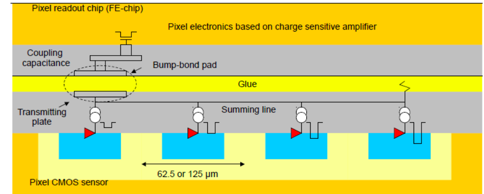
- **Pixel sensor(s) not yet determined**
  - Planar, 3D, Diamond, HV CMOS, , ,
  - Possibility of using different sensors in different layers
  - Final sensor decision may come relatively late.

- Very complex, high rate and radiation hard pixel readout chips required



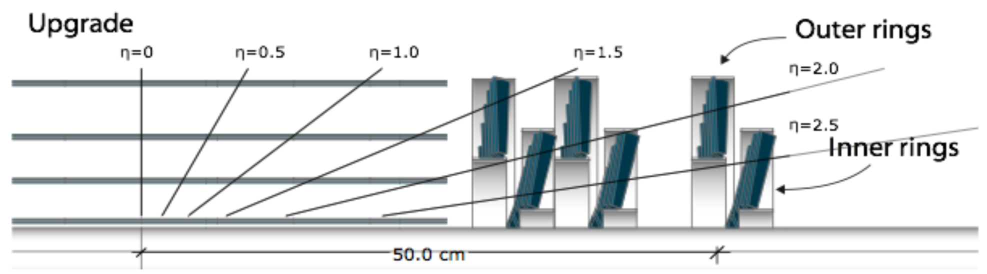




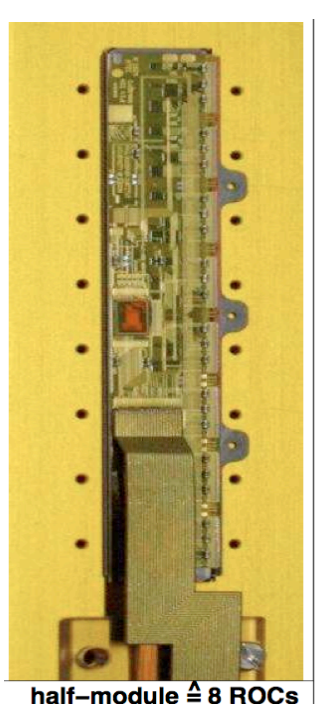


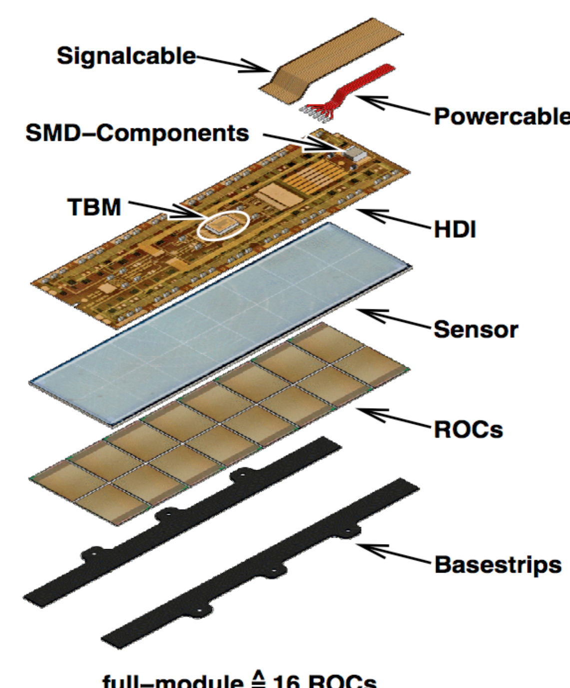
ATLAS HVCMOS program

Vertex identification @L1with pixel detectors



1. Precise information close to the interaction region (3 cm) from small pixel sizes (~100 x 100 μm²)
2. *2D fast clustering, essential to identify specific patterns that identify crossings of interesting tracks*
3. ~2 GHz/cm² hits, clusters of ~4 pixels
   - First data reduction to 500 KHz/cm².
   - Further data reduction ~O(>10) if groups of clusters close-by and with similar shapes.
4. Radiation hardness ~1Grad & $10^{16}{}_{neq}$ (1 MeV)/cm²

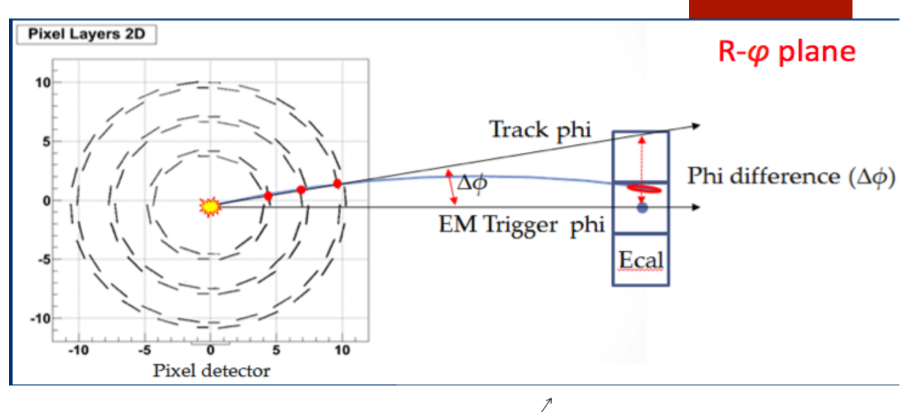

half–module ≙ 8 ROCs

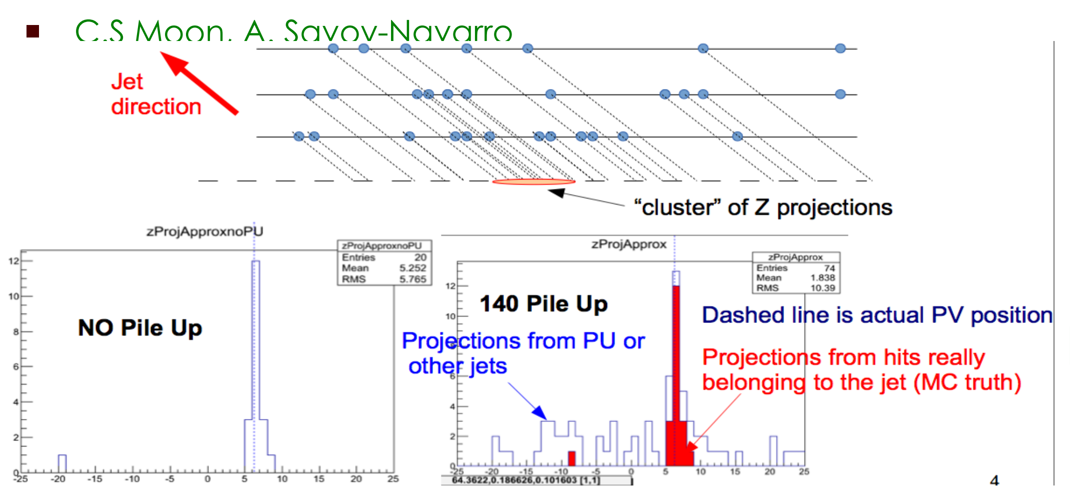


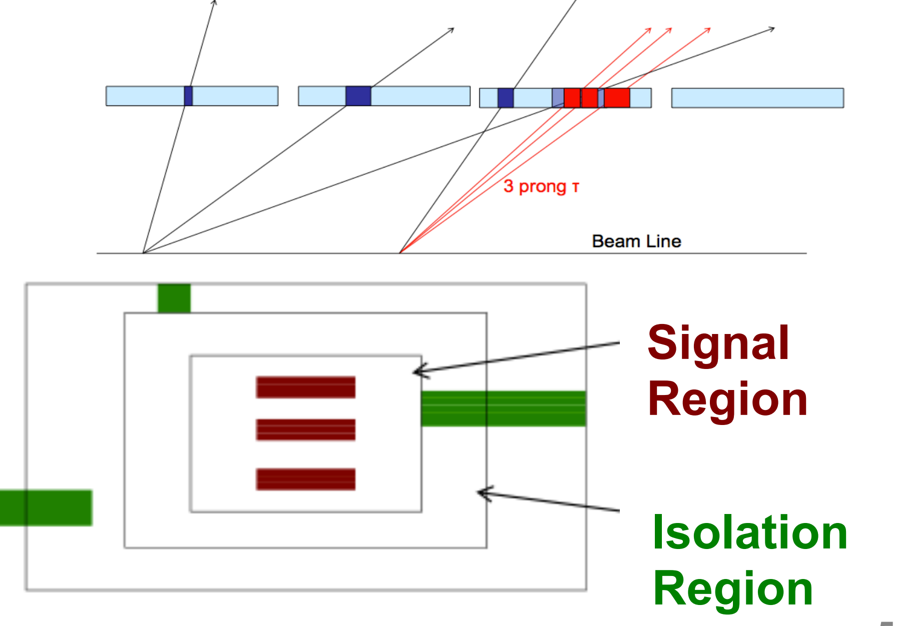
full–module ≙ 16 ROCs

Pixel usage @L1: Fast 2D clustering

- Jet-Vertex identification
  - Assign the vertex to each jet out of ~200 vertices/bx
  - A. Rizzi, S. Donato, J. Bernardini
- Tau→3 prongs identification
  - Compatible clusters in a chip
  - K. Androsov, M. T. Grippo, F. Palla, M. A. Ciocci, G. Bagliesi
- Match pixel hits with ECAL
  - Tracks from pixel layers to identify electrons
  - C.S Moon, A. Savoy-Navarro







RD53 Collaboration

- **Recentemente approvata da LHCC**
- 17 istituti fondanti
  - ATLAS: Bonn, CERN, CPPM, LBNL, LPNHE Paris, NIKHEF, New Mexico, RAL, UC Santa Cruz.
  - CMS*: Bari, Bergamo-Pavia*, CERN, Fermilab, *Padova, Perugia,* **Pisa**, PSI, RAL, *Torino.*
- Collaboratori: 99, ~50% chip designers
- Collaborazione organizzata a livello di Institute Board (IB) con lavoro tecnico nei Working Groups (WG)
- Lavoro iniziale previsto per I prossimi 3 anni con lo scopo di produrre un'ambiente di lavoro per sviluppo di competenze necessarie a produrre I chip di readout di ATLAS e CMS

WG	Domain
WG1	Radiation test/qualification
Qualification of technology to 10 MGy TID, 10^{16} n.eq./cm^2. Transistor simulation models after irradiation. Evaluation of logic cell libraries after irradiation. Expertise on radiation effects in 65nm	
WG2	Top level design
Design methodology, verification and test of ~5 × 10^8 transistor IC. Analog integration in large digital chip. Power distribution Synthesis constraints. Clock distribution and optimization	
WG3	Simulation and verification test bench
System Verilog simulation and Verification framework. Optimization of global architecture/pixel regions/pixel External system and external physics data. Verification of test chips and evolving designs	
WG4	I/O
Definition of readout and control interfaces (e.g. LPGBT). Definition of standardized I/O protocols and performance Implementation of readout and control interface blocks. Standardized interfaces: Control, Readout, etc.	
WG5	Analog design
Evaluate and compare alternate amplifier designs. Evaluate and compare charge ADC techniques vs. number of bits (TOT, shared ADC, etc.)	
WG6	IP blocks
Define common requirements for IP block design. Evaluate, document, and keep library of IP blocks Generate overview and recommendations. Each block will have its own prototyping milestones	

Institute	WG1 Radiation	WG2 Top level	WG3 Sim./Ver	WG4 I/O	WG5 Analog	WG6 IPs
Bari	C		A			A
Bergamo-Pavia	A			C	A	B
Bonn	C	A	A	B	B	A
CERN	B(*)	(*)	A	C(*)	A	B(*)
CPPM	A	B	C	C	B	A
Fermilab	A	B			A	
LBNL	B	A	B	B	A	A
LPNHE Paris	A	B	A			A
NIKHEF		A	A			A
New Mexico	A					
Padova	A				A	
Perugia	B		A			B
Pisa		**B**	**A**	**A**		**A**
PSI	B	A		C	A	A
RAL		B	B		A	C
Torino	C	B	C	B	A	A
UCSC	C	B	C			A

A: Core competency, B: High interest, C: Ability to help

(*): General CERN support for 65nm

CHIPIX65

- Questo progetto di R&D trova una sede naturale di sviluppo in un ambito più allargato di collaborazione internazionale
- RD53
  - Recentemente approvato dall'LHCC
- PRIN 2012 – passato (Tonelli) per finanziare alcuni studi di sintesi di prototipi che possano testare l'architettura e alcune implementazioni specifiche di clusterizzatori online. (in sinergia con Torino per la parte analogica)

- **2014:**
  - **Disegno, sottomissione e test di IP blocks analogici e digitali, ed algoritmi di clustering e data handling WP2/WP3**
- 2015:
  - Qualifica della rad-hardness WP1
  - **Design methodology e verifica WP4**
  - **Ottimizzazione architettura digitale WP4**
  - Architettura del very front-end analogico WP3
- 2016
  - **Integrazione parti analogica e digitale WP4**
  - **Prototipi (MPW, FPGA, eventuale chip) WP4**

Working groups

WG	Domain
WP1	Radiation Hardness
Qualifica della tecnologia per 10 MGy TID, 10^{16} n.eq./cm^2. Modelli di simulazione dei transistor dopo irraggiamento. Valutazione delle librerie logiche dopo l'irraggiamento.	
WP2	Elettronica digitale
Sviluppo architettura digitale e di tool di disegno e verifica per un IC con ~5 x10^8 transistor	
WP3	Elettronica analogica
Sviluppo e confronto di diverse architetture dell'elettronica di very front end e di elettronica analogica in generale. Tecniche di ToT, ADC per la misura della carica.	
WP4	Chip integration
Integrazione dei vari singoli compontenti in un chip completo. Metodologia di disegno e verifica, integrazione di elettronica analogica nel chip digitale.	

Nome	Percentuale
R. Beccherle	***30%***
R. Bellazzini	10% (TBC)
L. Fanucci	20%
F. Morsani	***30%***
G. Magazzù	***30%***
M. Minuti	***30%***
F. Palla	20%
A. Rizzi	10% (TBC)
S. Saponara	20%

L’unità di Pisa intende lavorare all’architettura digitale del chip

In particolare all’utilizzo dei dati per un trigger di L1.

Validazione del disegno del chip con tools industriali complessi.

Interessi e budget (in fase di definizione)

Sezione	WP1 Radiation hardness	WP2 Elettronica digitale	WP3 Elettronica analogica	WP4 Chip integration
Bari		X		
Bergamo-Pavia		X	X	X
Milano	X			
Padova	X		X	
Perugia	X	X		
Pisa		**X**		**X**
Torino	X		X	X

ITEM	KEuro
Sottomissione MPW	300
Studi radiation hardness	75
Prototipo (anno 2016)	200-300
Elettronica varia per test	75
Missioni	60

ANAGRAFICA 2014	Personale	Totale (fte)
Bari	F. Loddo (D) 25% Ciciriello 30%, F. Corsi (D) 30%, G. De Robertis (D) 30% , F. Licciulli (S) 50%, C. Marzocca (D) 30%, C.Tamma (Borsista) 50%, Anonimo (assegno di ricerca tecnologico gia' bandito) 50%	2.95
Bergamo-Pavia	V. Re 10%, L. Gaioni (D) 20%, M. Manghisoni (D) 20%, G.Traversi (D) 20%, S. Zucca (D) 20%, L. Fabris 20%, F. De Canio (D) 20%, C.Vacchi 20%	1.5
Padova	D.Bisello 30%, L.Ding 30%, P.Giubilato 30%, A. Neviani (D) 30%, A.Paccagnella 40%, M. Bagatin 30%	1.9
Perugia	G. Bilei 20%, E. Conti (S,D) 50%, M. Menichelli 20%, D. Passeri (D) 20%, P. Placidi (D) 30%	1.4
Pisa	F. Palla 20%, R. Beccherle (D) 30%, R. Bellazzini 10%, L. Fanucci 20%, G. Magazzù (D) 30%, F. Morsani(D) 30%, A. Rizzi 10%, S. Saponara 20%, M.Minuti 30% (D)	1.8
Torino	N. Demaria 40%, G. Mazza (D) 20%, L. Pacher (S,D) 40%, A. Rivetti (D) 30%, M. Rolo (D) 20%.	1.5
Milano	V.Liberali (D) 30%, A.Stabile (D) 30%, S.J. Jafar (S,D) 30%	0.9

Common ATLAS – CMS R&D

- Pixel readout chips critical for schedule to be ready for phase 2 upgrades
  - Technology: Radiation qualification
  - Building blocks: Design, prototyping and test
  - Architecture: definition/optimization/verification
  - Chip prototyping, iterations, test, qualification and production
  - System integration
    - System integration tests and test-beams
  - Production and final system integration, test and commissioning

- Phase 2 pixel chip very challenging
  - Radiation
  - Reliability: Several storage nodes will have SEUs every second per chip.
  - High rates
  - Mixed signal with very tight integration of analog and digital (digital part will be > 90%)
  - Complex: ~256k channel DAQ system on a single chip
  - Large chip: > 2cm x 2cm, ½ - 1 Billion transistors.
  - Very low power: Low power design and on-chip power conversion

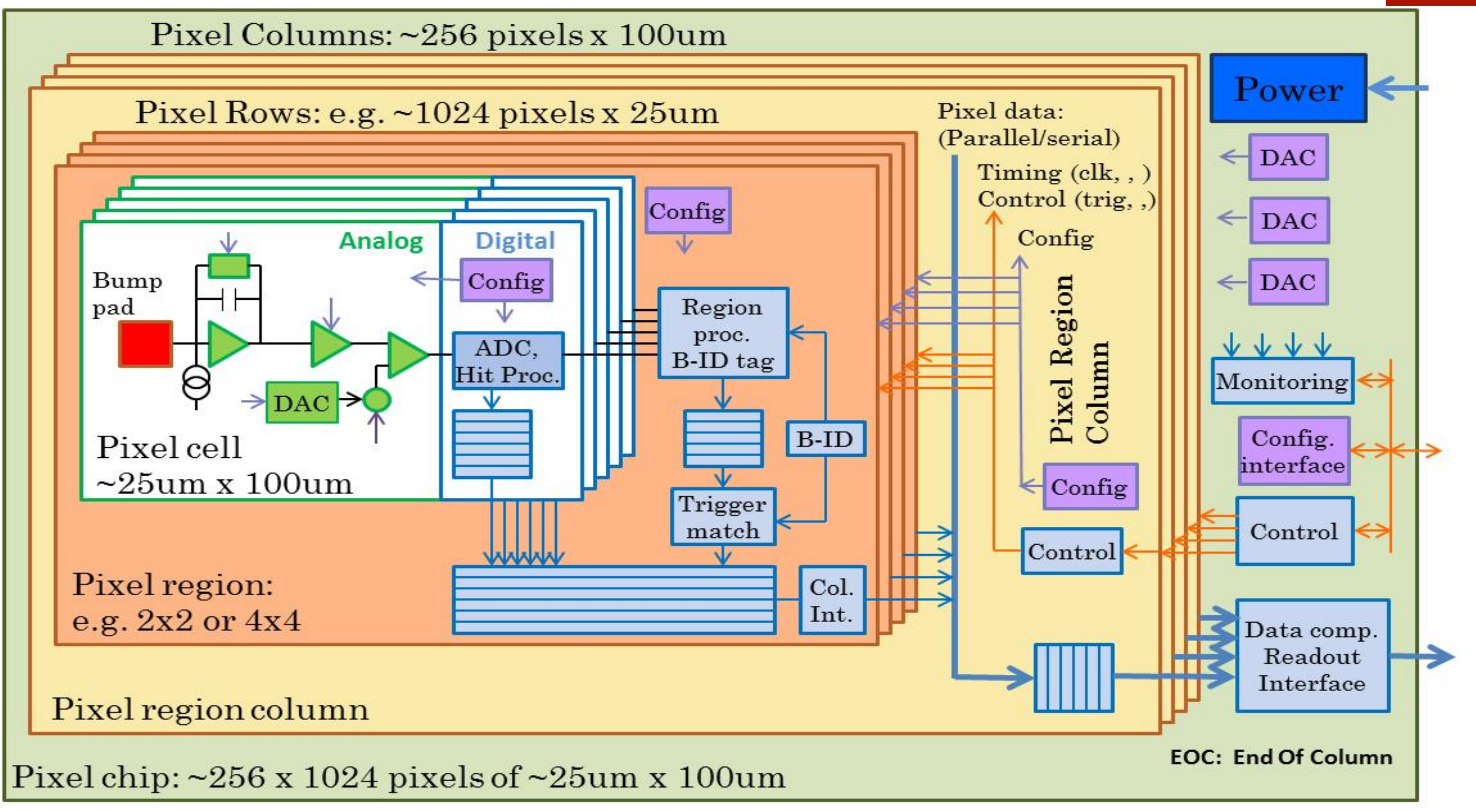
- Both experiments have evolved to have similar pixel chip architectures and plans to use same technology for its implementation.

- Experienced chip designers for complex ICs in modern technologies that most work in a extremely harsh radiation environment is a scarce and distributed "resource" in HEP.

Pixel chip generations

Generation	Current FEI3, PSI46	Phase 1 FEI4, PSI46DIG	Phase 2
Pixel size	100x150um^2 (CMS) 50x400um^2 (ATLAS)	100x150um^2 (CMS) 50x250um^2 (ATLAS)	25x100 um^2 ?
Sensor	2D, ~300um	2D+3D (ATLAS) 2D (CMS)	2D, 3D, Diamond, MAPS ?
Chip size	7.5x10.5mm^2 (ATLAS) 8x10mm^2 (CMS)	20x20mm^2 (ATLAS) 8x10mm^2 (CMS)	**> 20 x 20 mm^2**
Transistors	1.3M (CMS) 3.5M (ATLAS)	87M (ATLAS)	**~1G**
Hit rate	**100MHz/cm^2**	**400MHz/cm^2**	**1-2 GHz/cm^2**
Hit memory per chip	0.1Mb	1Mb	~16Mb
Trigger rate	100kHz	100KHz	200 kHz – **1 MHz**
Trigger latency	2.5us (ATLAS) 3.2us (CMS)	2.5us (ATLAS) 3.2us (CMS)	6 – **20 us**
Readout rate	40Mb/s	320Mb/s	**1- 3 Gb/s**
Radiation	1MGy (100Mrad)	3.5MGy (350Mrad)	**10 MGy (1Grad)**
Technology	250nm	130nm (ATLAS) 250 nm (CMS)	**65 nm**
Architecture	Digital (ATLAS) Analog (CMS)	Digital (ATLAS) Analog (CMS)	Digital
Buffer location	EOC	Pixel (ATLAS) EOC (CMS)	Pixel
Power	~1/4 W/cm^2	~1/4 W/cm^2	**~1/4 W/cm^2**

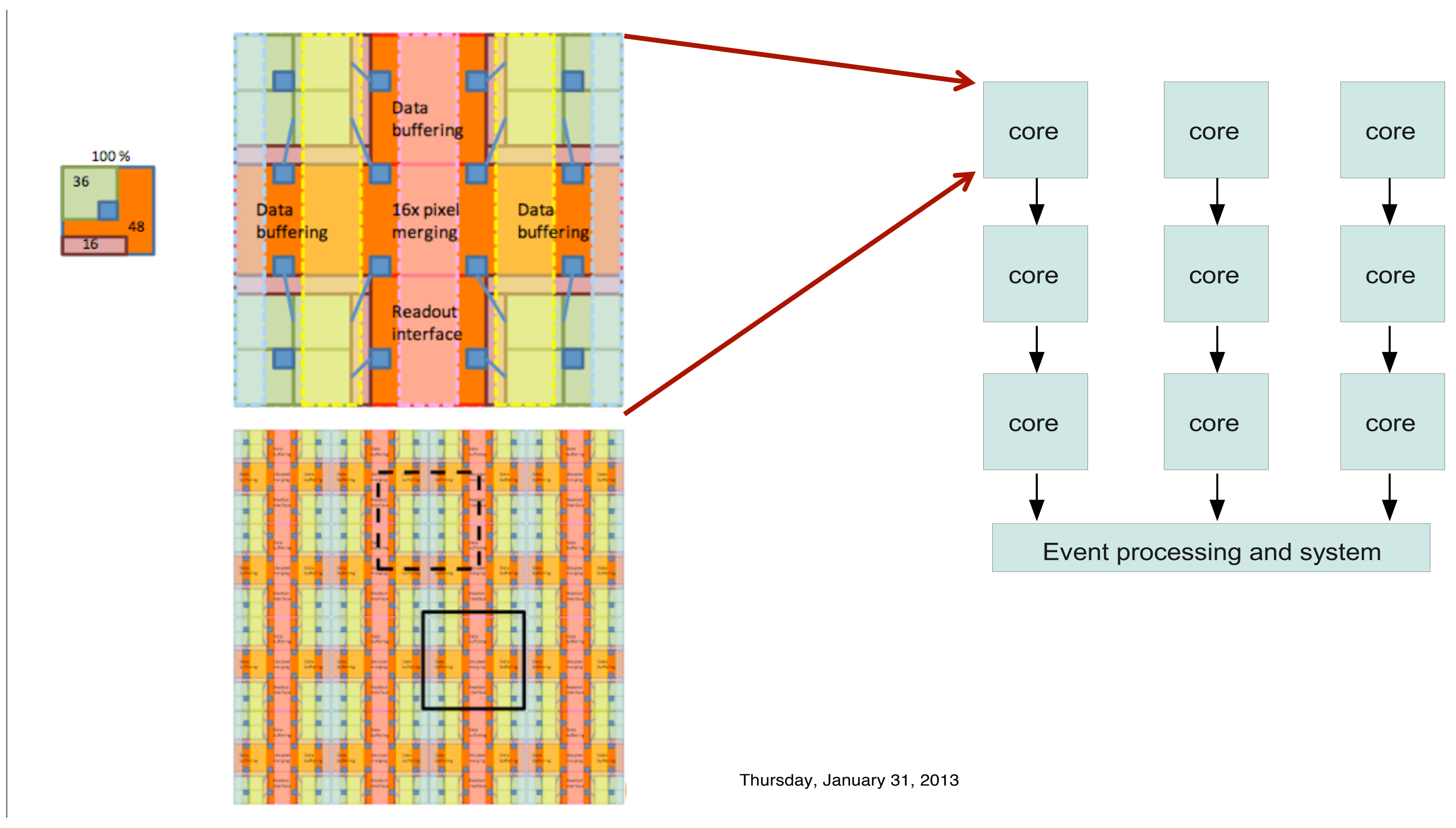
3rd generation pixel architecture



- 95% digital (as FEI4)
- Charge digitization
- ~256k pixel channels per chip

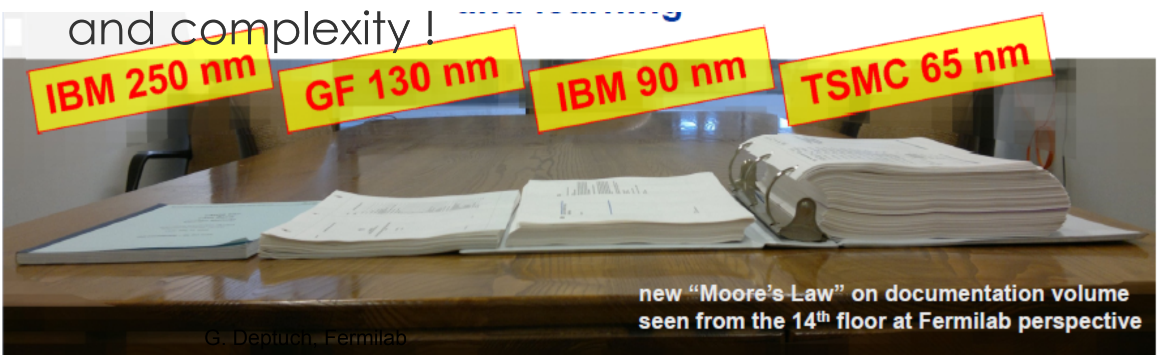
- Pixel regions with buffering
- Data compression in End Of Column

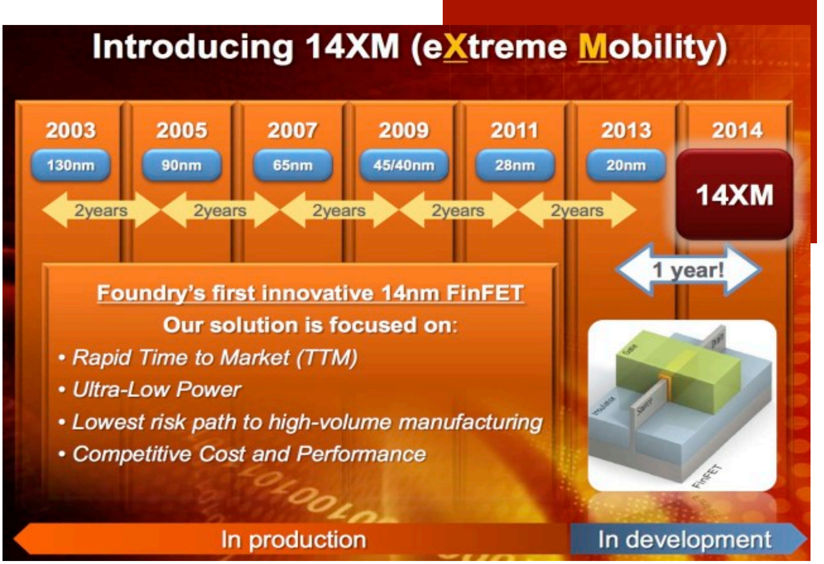
Possible pixel architectures and core communications

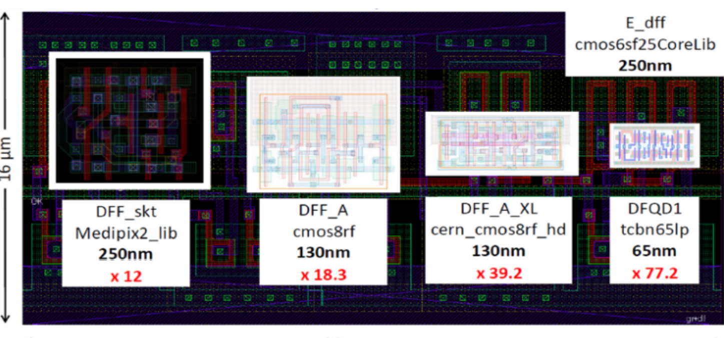


Why 65nm Technology

- Mature technology:
  - Available since ~2007
- High density and low power
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Access
  - CERN frame-contract with TSMC and IMEC
    - Design tool set
    - Shared MPW runs
    - Libraries
    - Design exchange within HEP community
- Affordable (MPW from foundry and Europractice, ~1M NRE for full final chips)
- Significantly increased density, speed, , , and complexity !



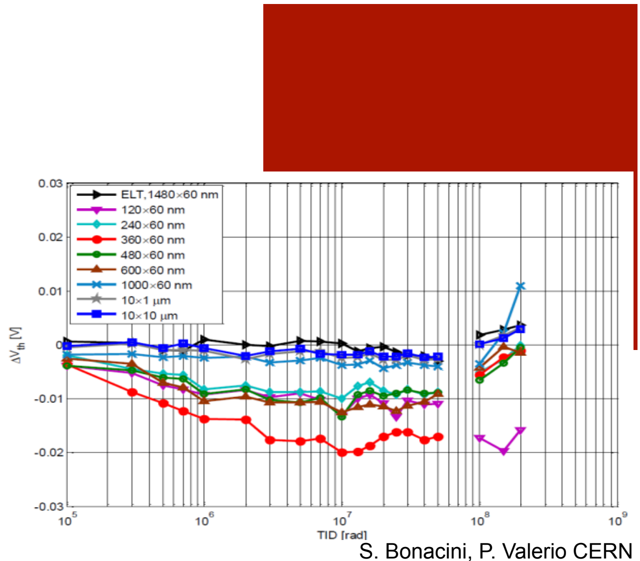




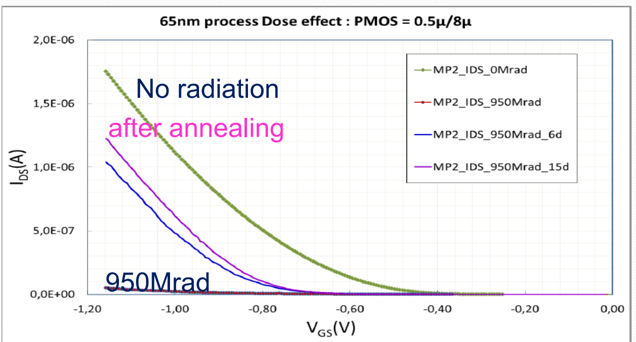
X. Llopart CERN

65nm Technology

- Radiation hardness
  - Uses thin gate oxide
    - Radiation induced trapped charges removed by tunneling
    - More modern technologies use thick High K gate "oxide" with reduced tunneling/leakage.
  - Verified for up to 200Mrad
  - To be confirmed for 1Grad
    - PMOS transistor drive degradation, Annealing ?
    - If significant degradation then other technologies must be evaluated and/or a replacement strategy must be used for inner pixel layers
  - CMOS normally not affect by NIEL
    - To be confirmed for 10^{16} Neu/cm^2
    - Certain circuits using "parasitic" bipolars to be redesigned ?
  - SEU tolerance to be build in (as in 130 and 250nm)
    - SEU cross-section reduced with size of storage element, but we will put a lot more per chip
  - All circuits must be designed for radiation environment (e.g. Modified RAM)



S. Bonacini, P. Valerio CERN



M. Menouni, CPPM