# Test experiment to study the digital pulse shape using nTD Si with PACI at PLF Mumbai

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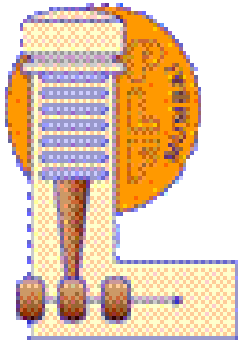


# Plan of the talk

- PLF Mumbai
- Experimental facilities
- Test expeiment
  - Setup
  - FPGA based indigenous developed digitizer card
  - Results
- Summary & outlook

# Pelletron-LINAC Facility, Mumbai

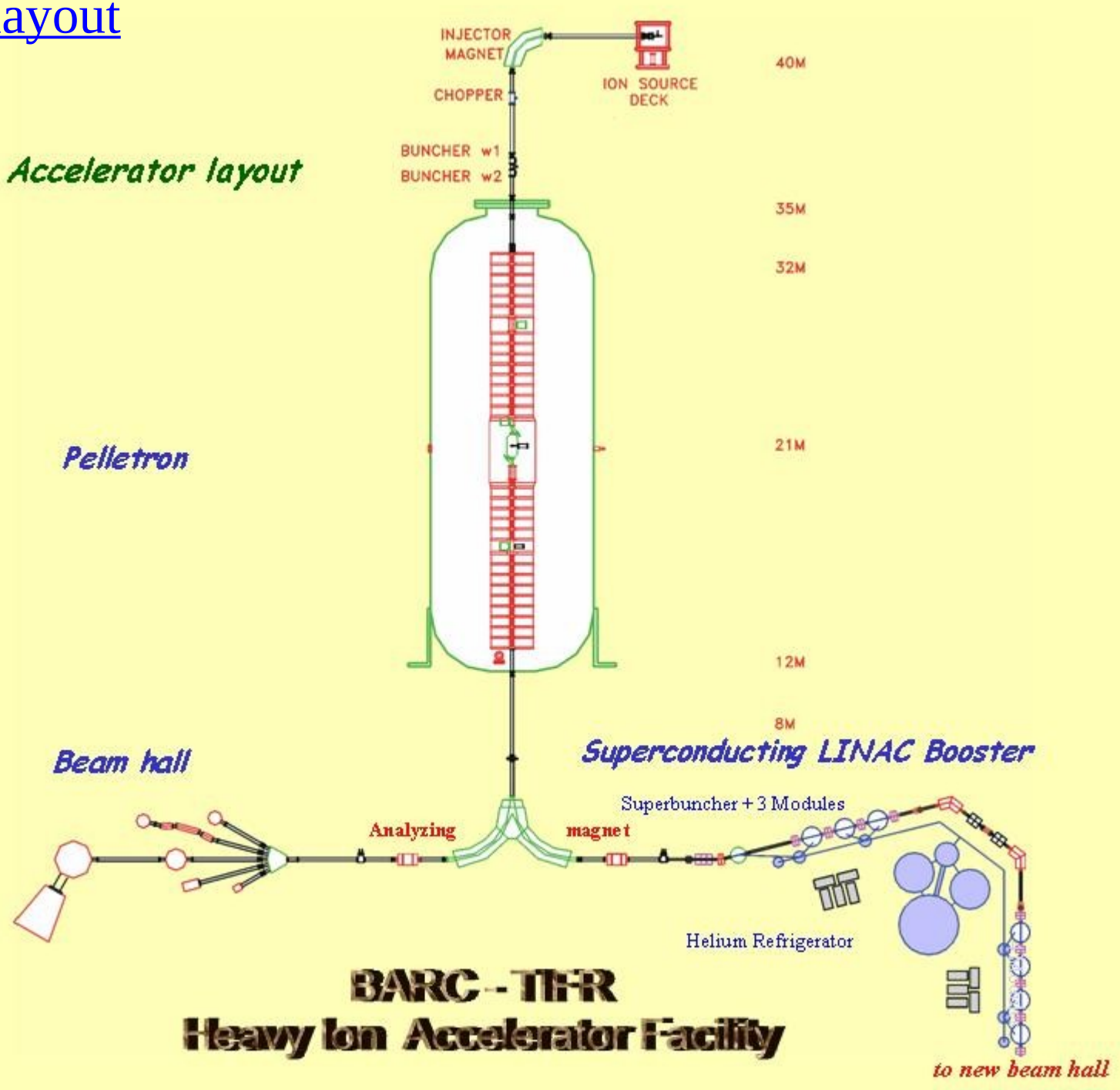

## Ongoing Research activities

- Nuclear Structure
- Reaction studies near barrier
- Fission studies
- Radio Chemistry studies
- Atomic Physics
- Condensed Matter studies

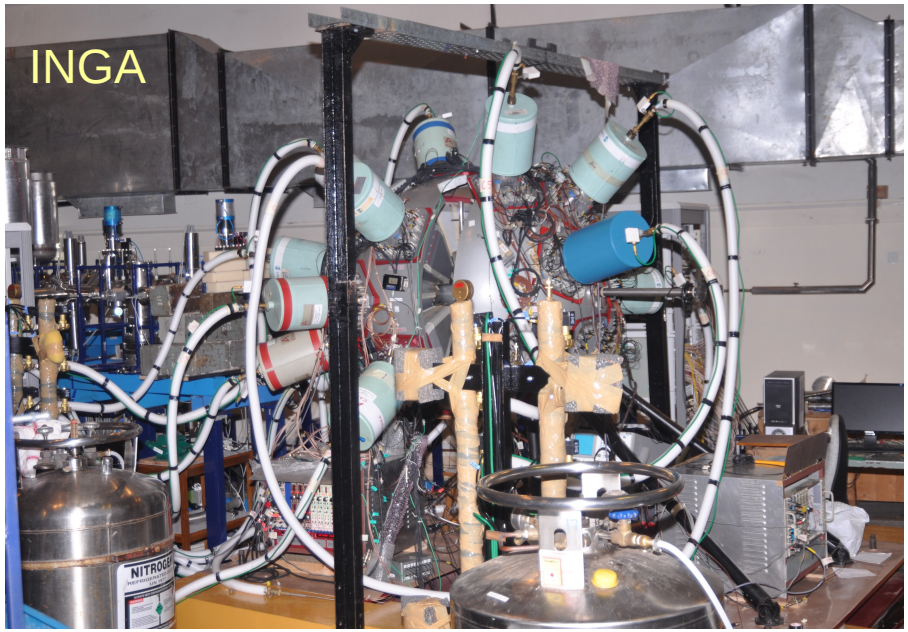
## Applications

- Bio-environmental studies
- Radiation damage studies
  (reactor materials, space application chips)
- Radiation biology (proteins, DNA)
- Accelerator Mass Spectrometry (36Cl/Cl)
- Track etched membrane (ultra-fine filters)

# Facility layout

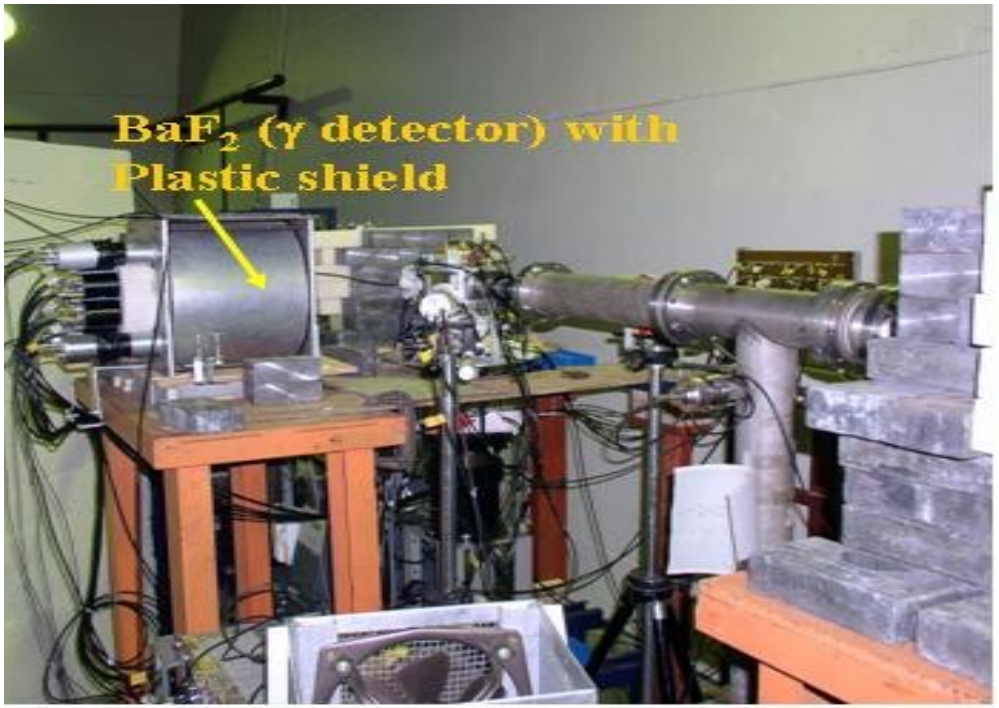


# Low energy γ-ray detector array




- 100 MHz & 12-bit ADC's
- Data rate: 80 MB/sec
- Handle high count rate with good E,T.
- Particle ID in CsI detectors using digital pulse shaping
- Trigger less system
- For in-beam Clover + CsI expts and off-line expts with planar detectors.

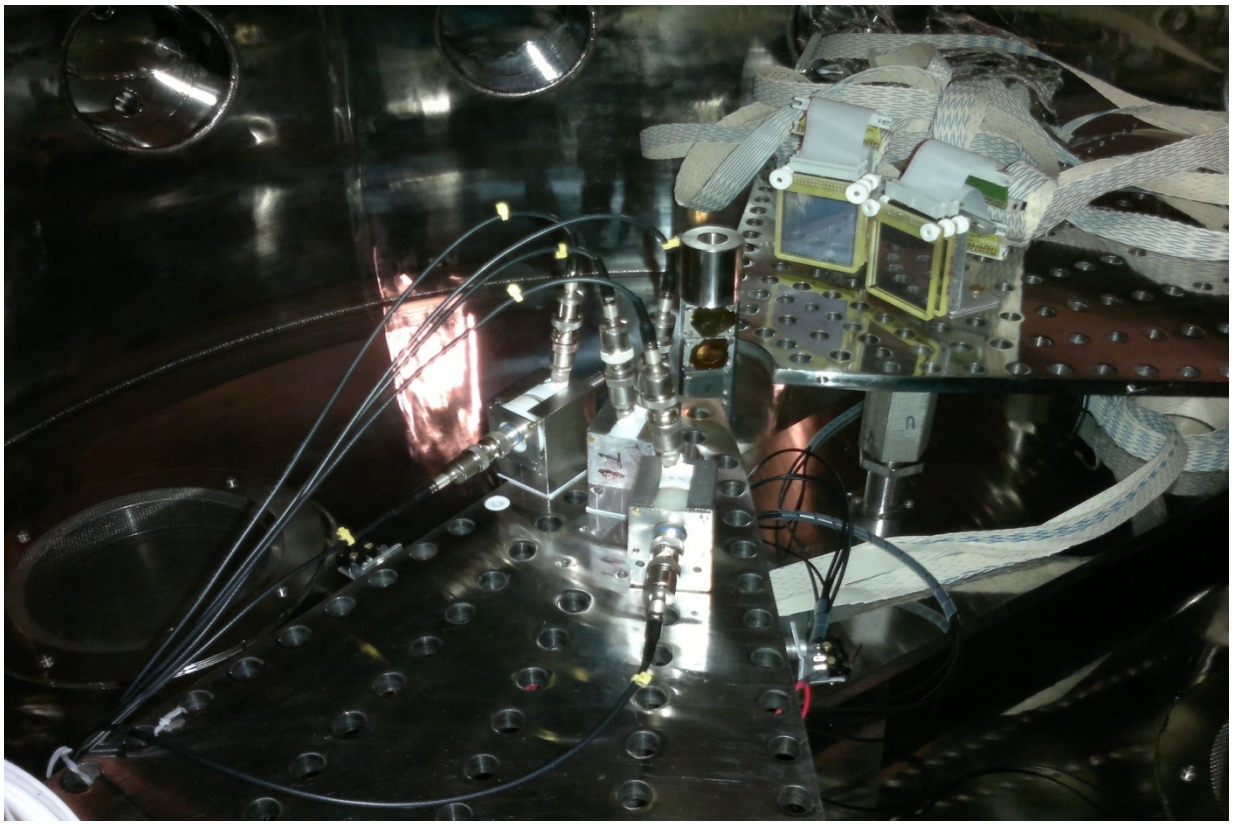
# High energy γ-ray detector array



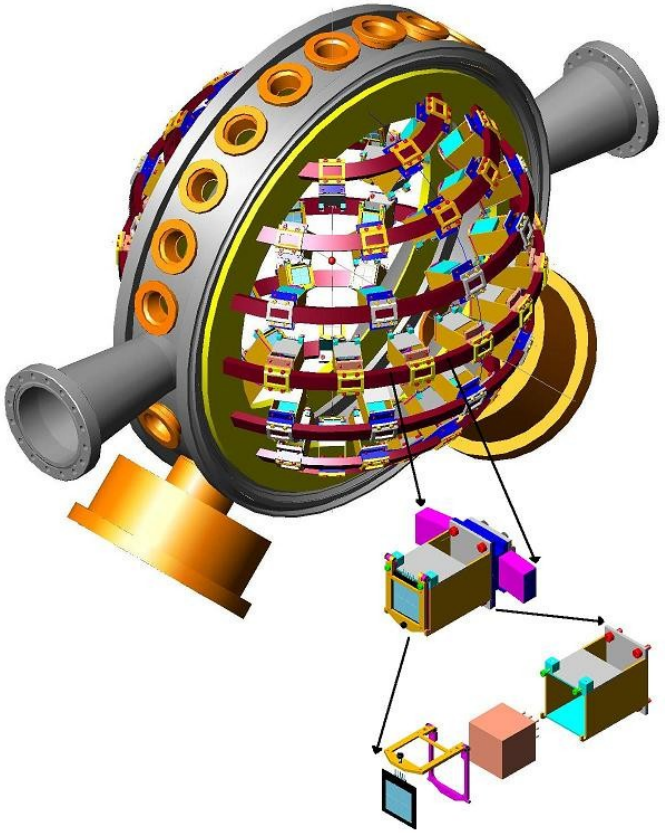

# 1.5 M dia General purpose scattering chamber

- Fully computer controlled rotation of arms and target ladder height and orientation

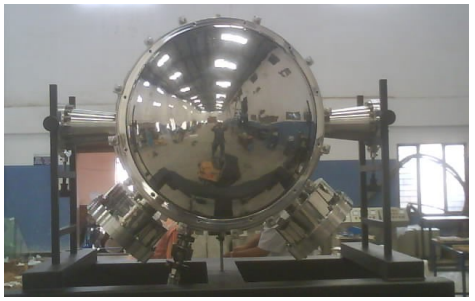
- Used for  angular distribution measurements

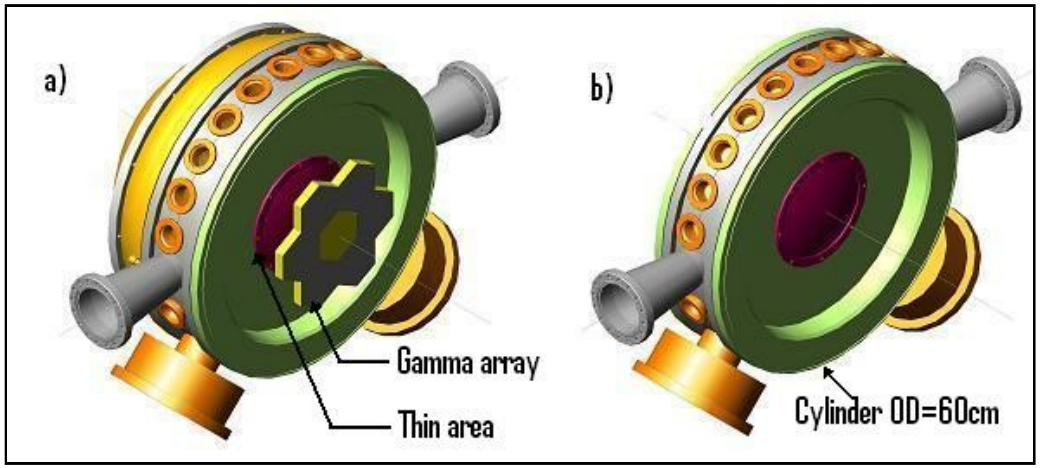


# CPDA for Mumbai LINAC facility – using BEL Si Detector

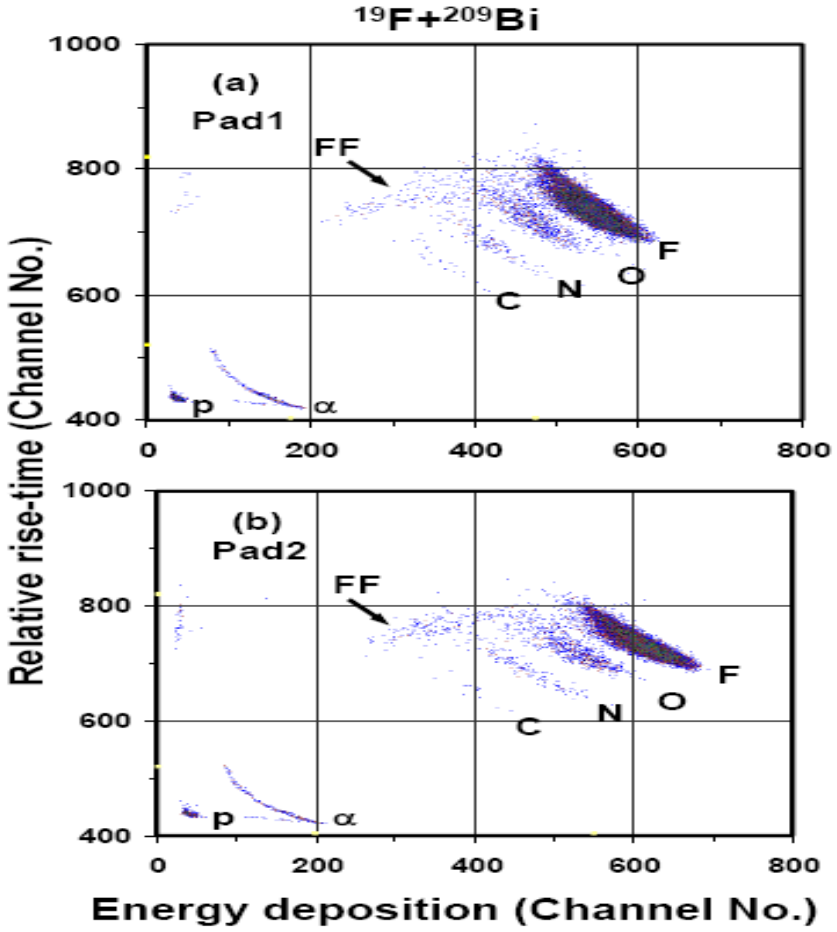


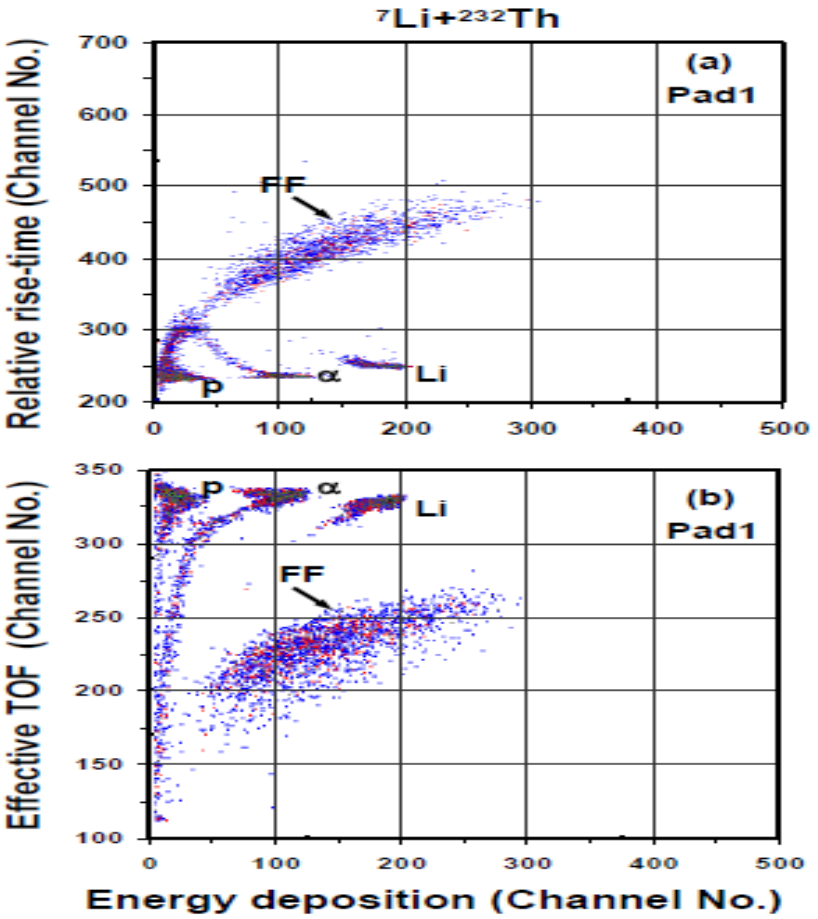
- The module can be fastened at any scattering angle in a pre-fixed wide range (up to 10-170)
- First element is located at a distance of 18.5 cm from the center
- Maximum solid angle – 1520 msr(12% of 4pi)
- 50 modules in the first phase





# Pulse shape discrimination studies with silicon pad detector at the PFL facility

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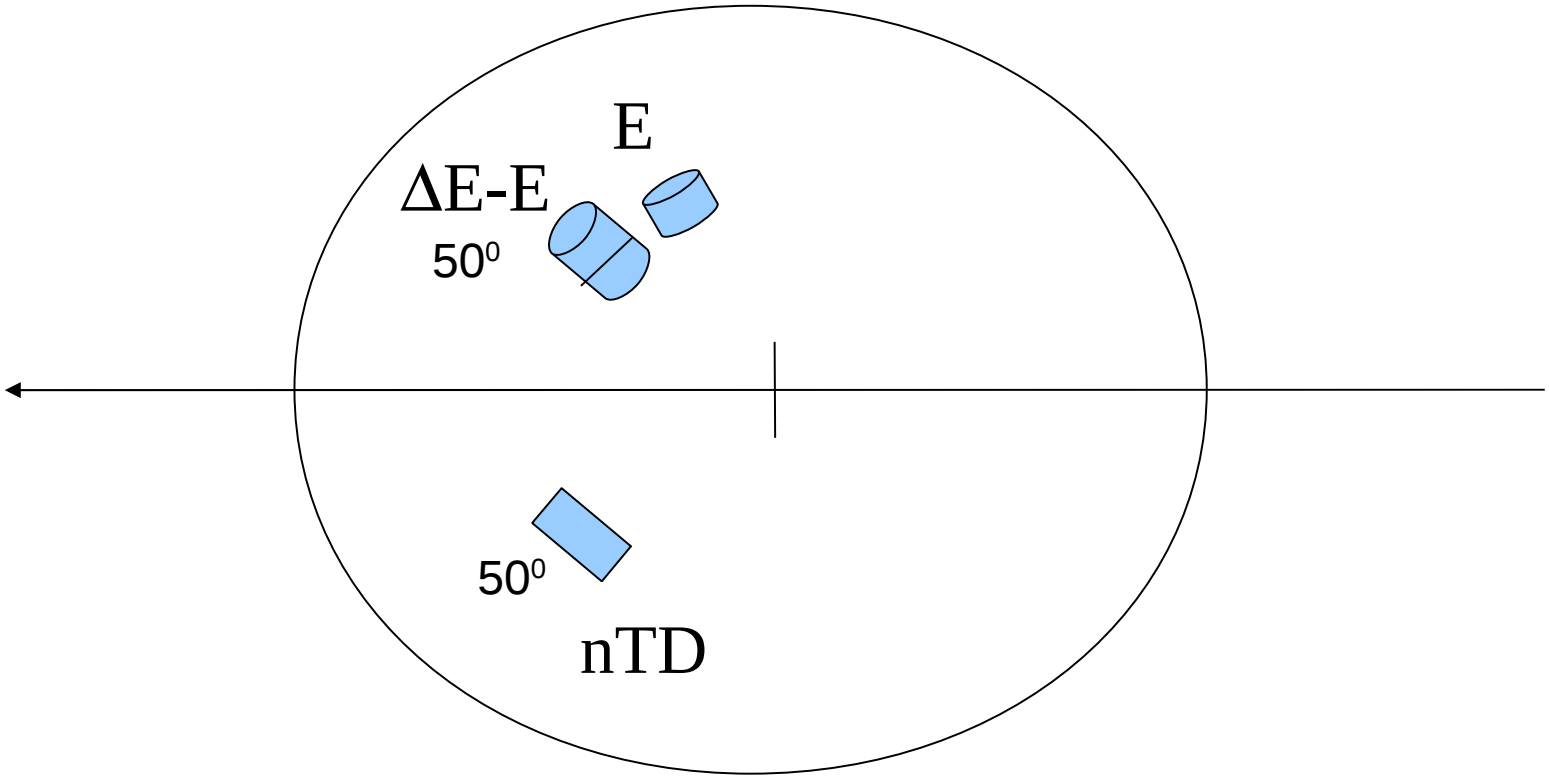
# Experimental Setup for digital pulse shape analysis




- Beam Time: October 14-15, 2012
- Beam: 7Li, 20, 30, 35 MeV
- Target: $^{89}Y$, $^{197}Au$, $^{12}C$
- Signal processing: Digital as well as analog

## Analog Processing

1. MSI-8: Mesytec preamplifier, shaper, timing filter, sum timing

2. PACI with Ortec amplifier

- 13 bit ADC

## Digital Processing

- PACI charge  out put was digitized using indigenously developed FPGA based High speed Data acquisition board

## Card Details

Form factor: 6U.

FPGA:VIRTEX-5 XC5VFX100T

cPCI interface: 32 bit, 33MHz master interface with DMA transfer capability using PCI 9054 from PLX Technology.

Clock: 156.25 MHz clock oscillator for SFP; 40 MHz clock oscillator for PCI; 32 MHz system clock; Clock distribution for ADC and DAC; can accept external clock also.

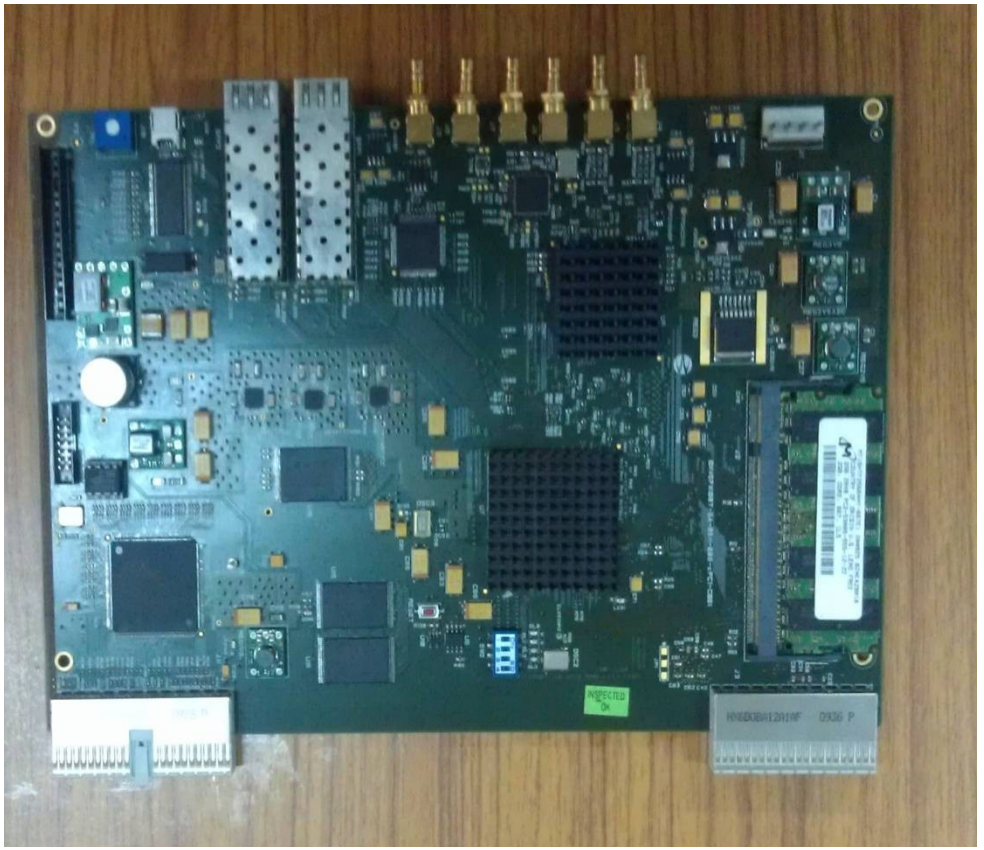
Rocket IO interface: Two SFP connectors are provided for SFP module.

Memory: 2GB DDR2 – SDRAM; 256Mb flash Memory

Analog Input: Two channels using 12 bit, 1.0 GSPS ADC: ADC12D1000 from National Semiconductor

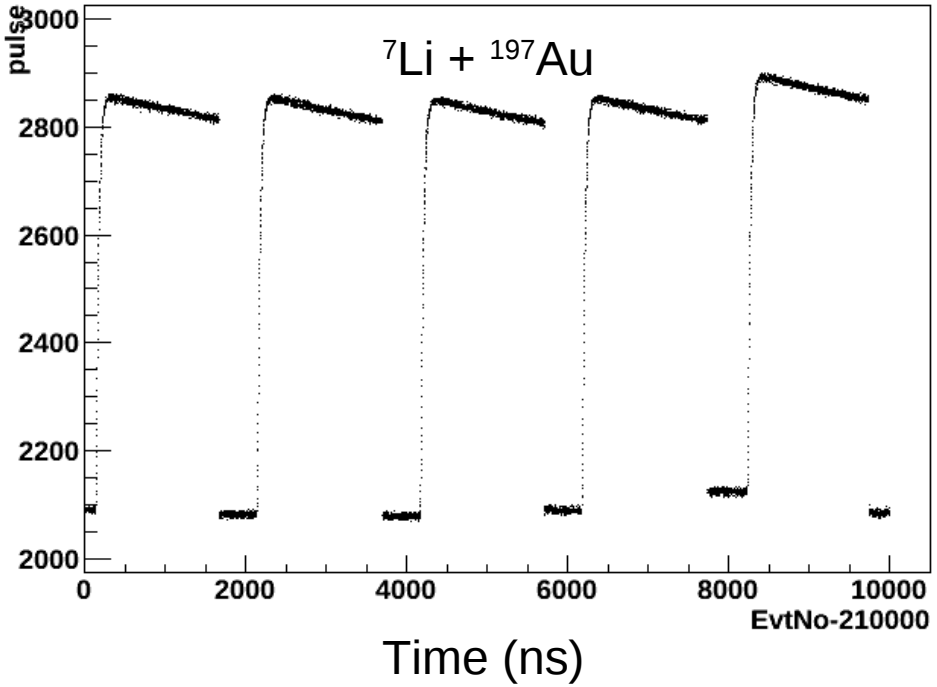
Configuration: JTAG Mode; Using On-board Configuration PROM.

# The card

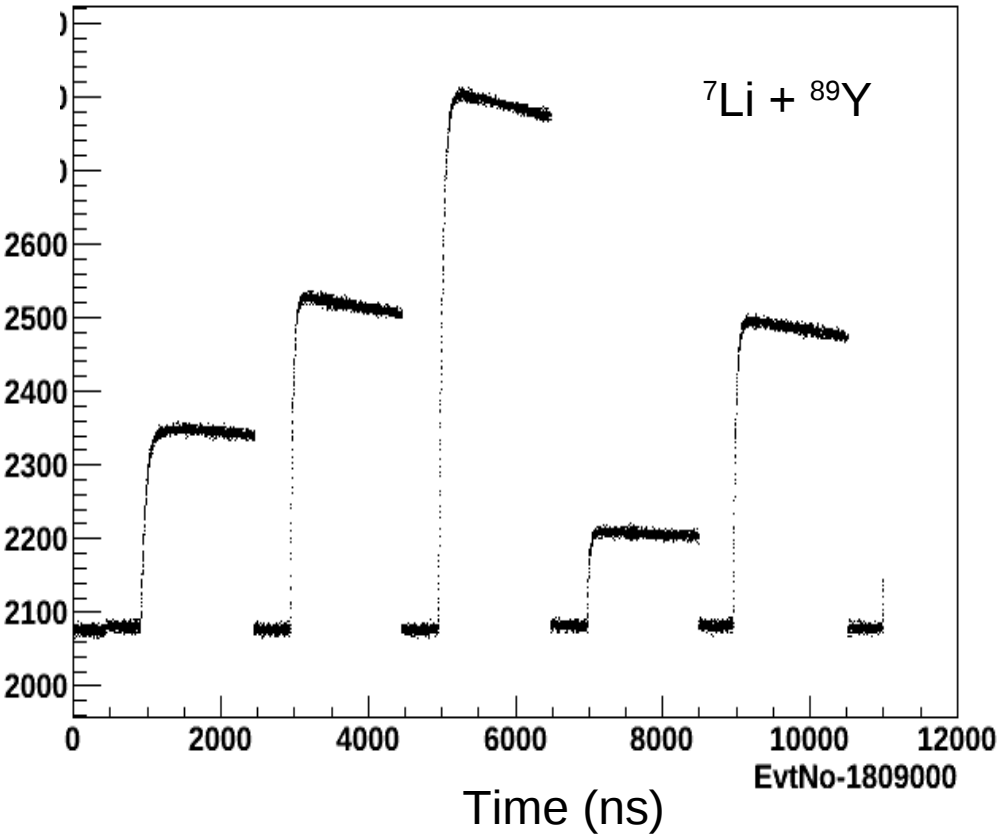


- Single channel, only charge signal recorded
- 8 channel card expected soon

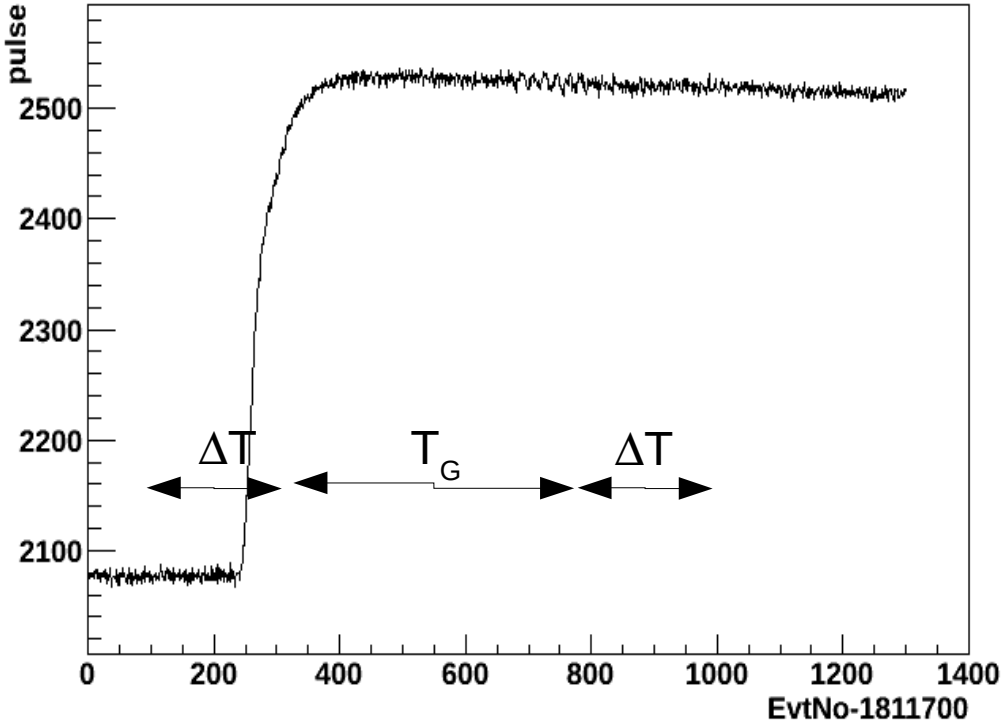
# Typical pulses



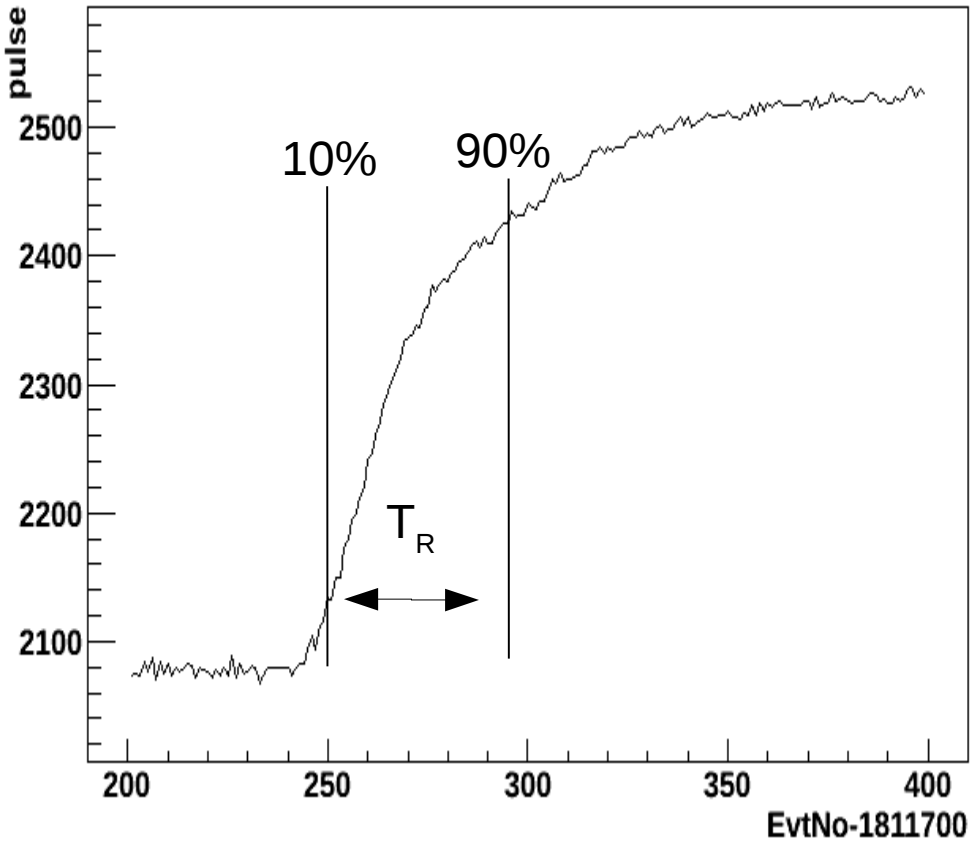

- 500 ns pre-trigger (adjustable)
- 2.5 μs recording interval (adjustable)



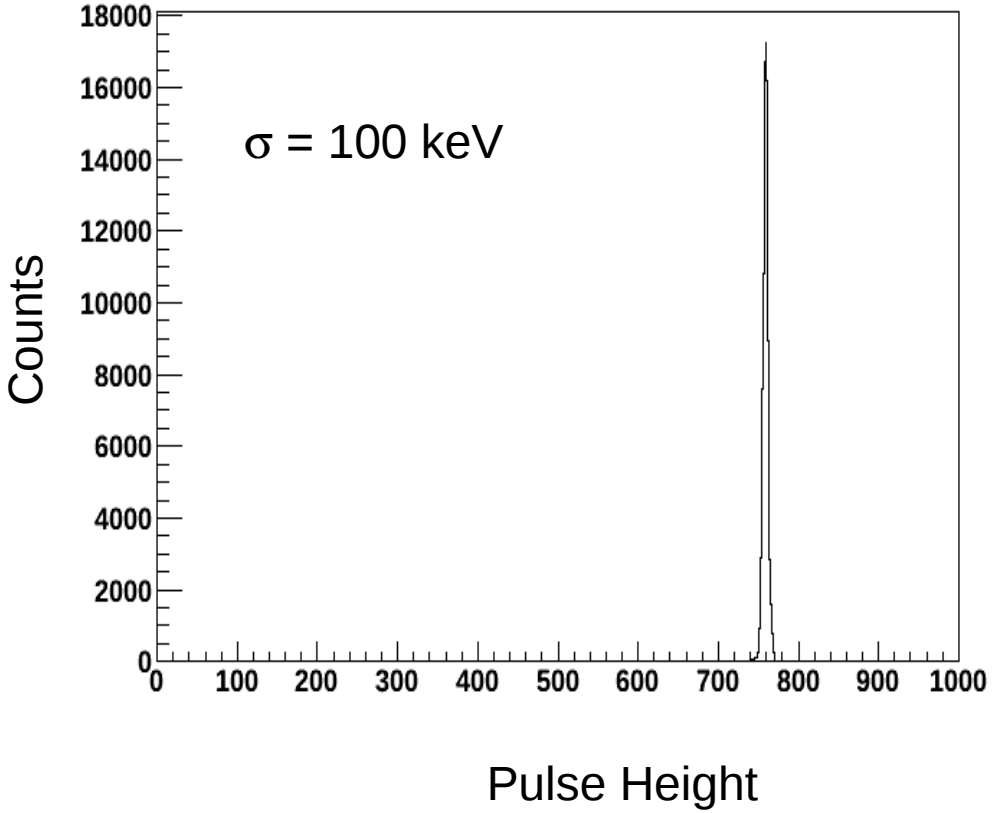
# Trapezoidal Filter

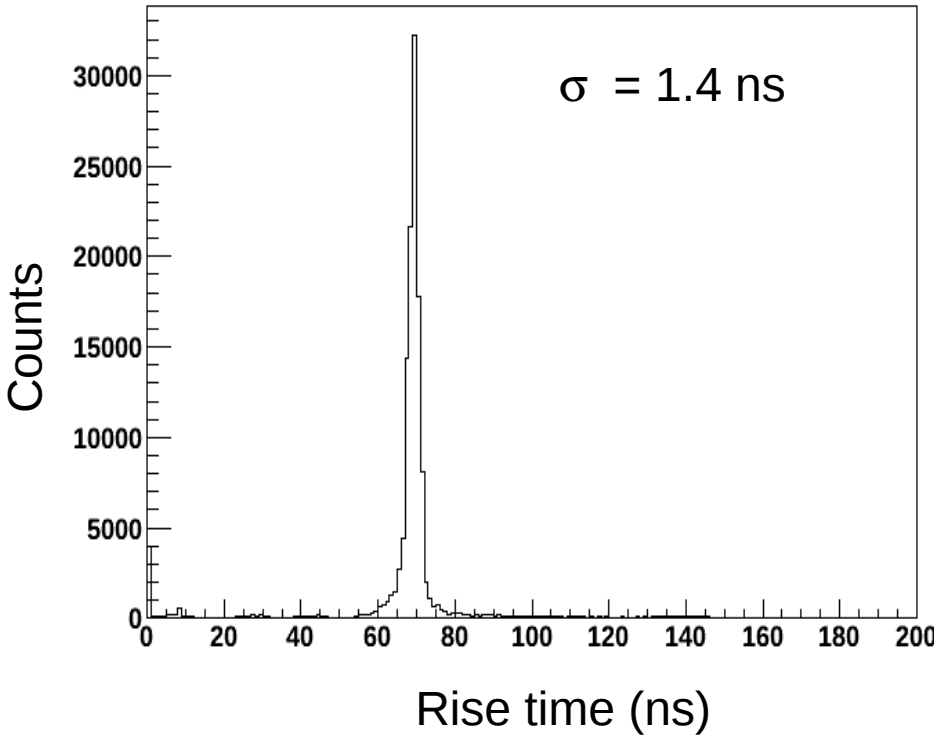



# Risetime

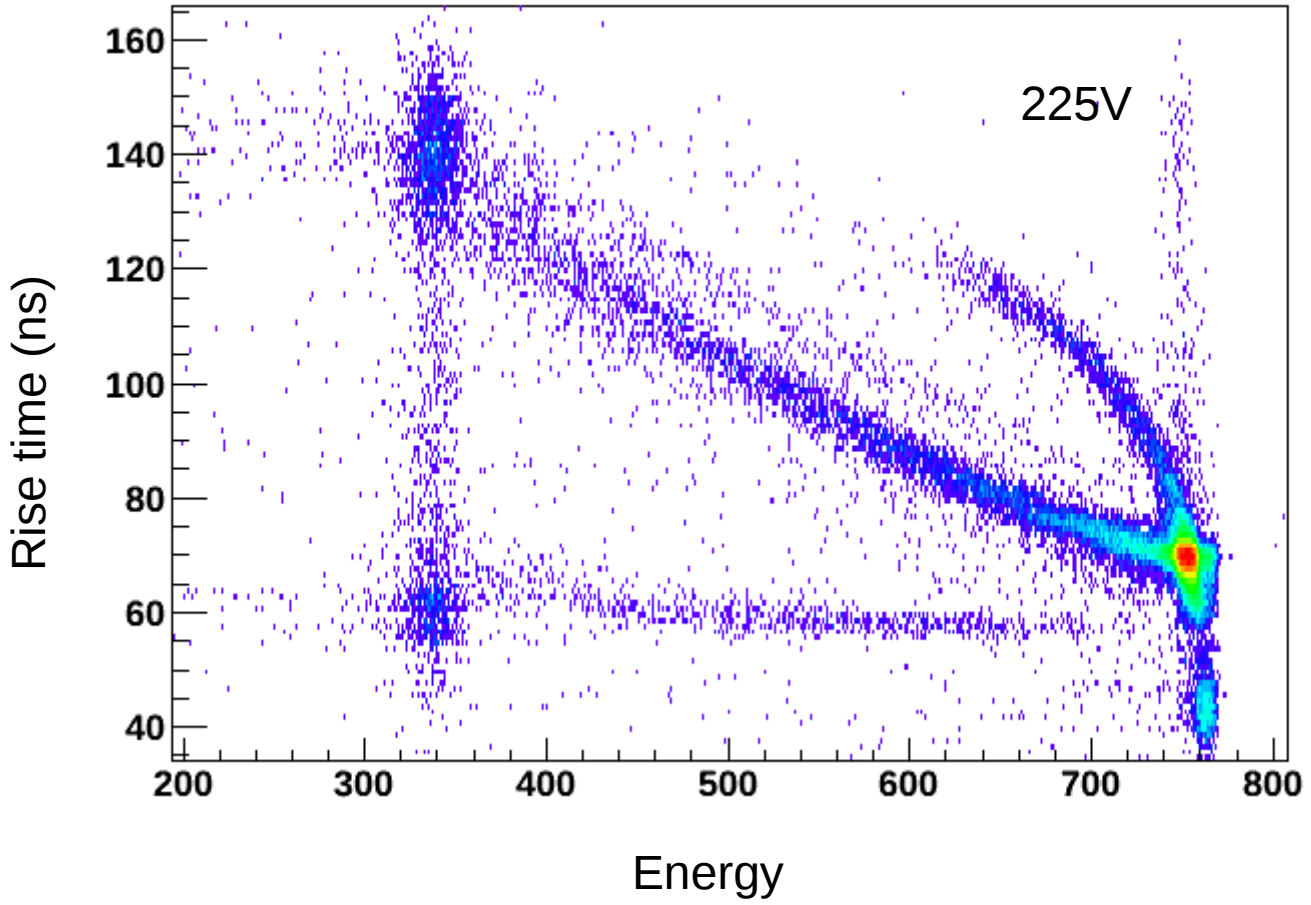


# Energy and Rise time Spectra ($^{7}$Li + $^{197}$Au)

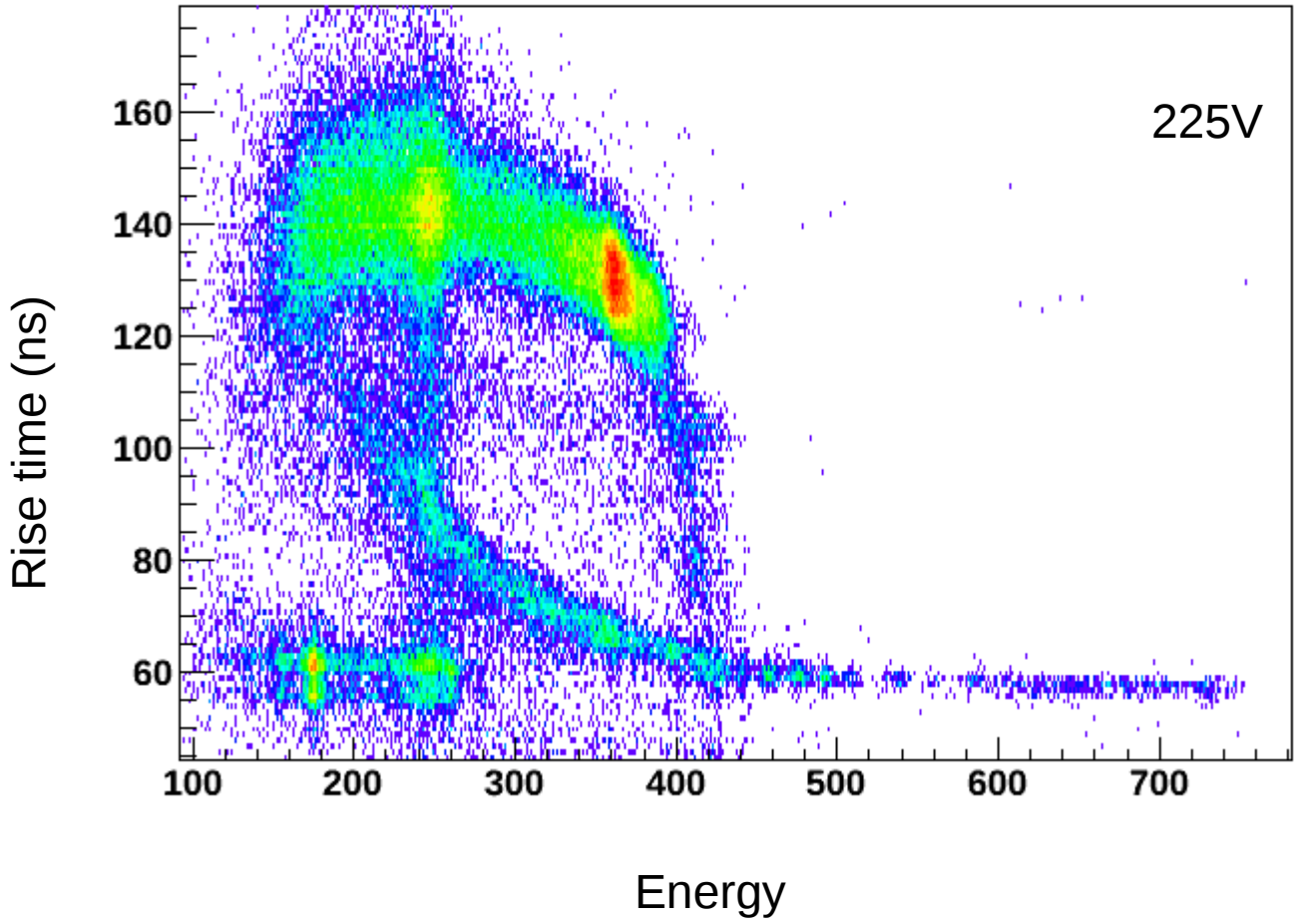


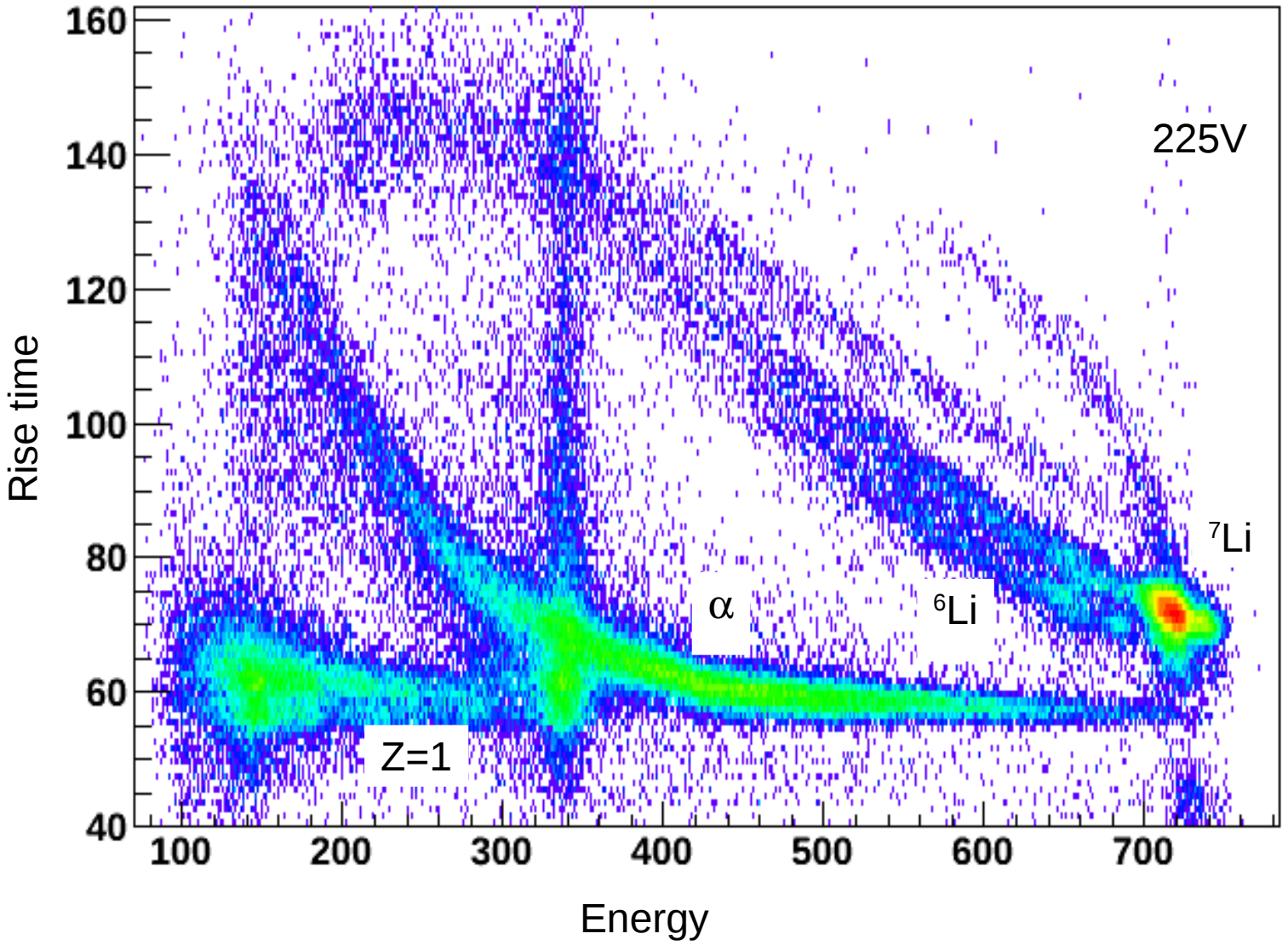
# Energy vs Rise time ($^{7}$Li + $^{197}$Au)



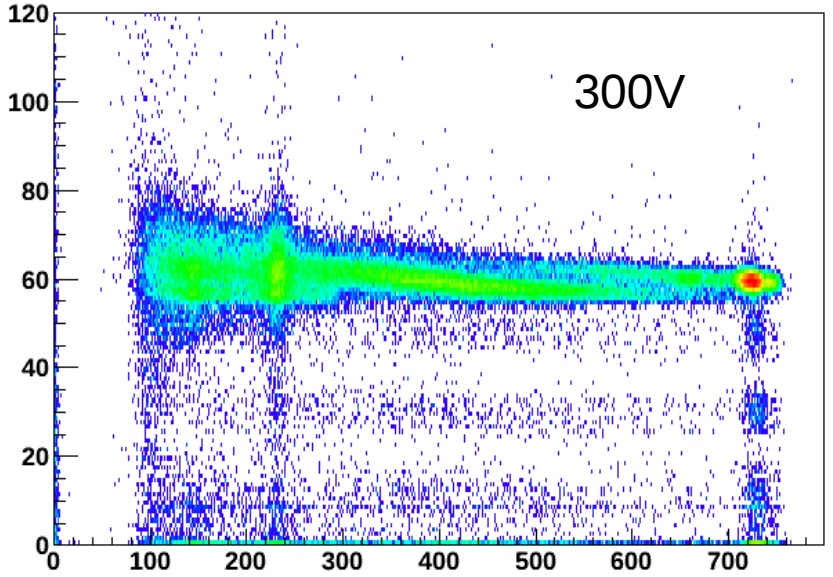
# Energy vs Rise time ($^{7}Li + ^{12}C$)

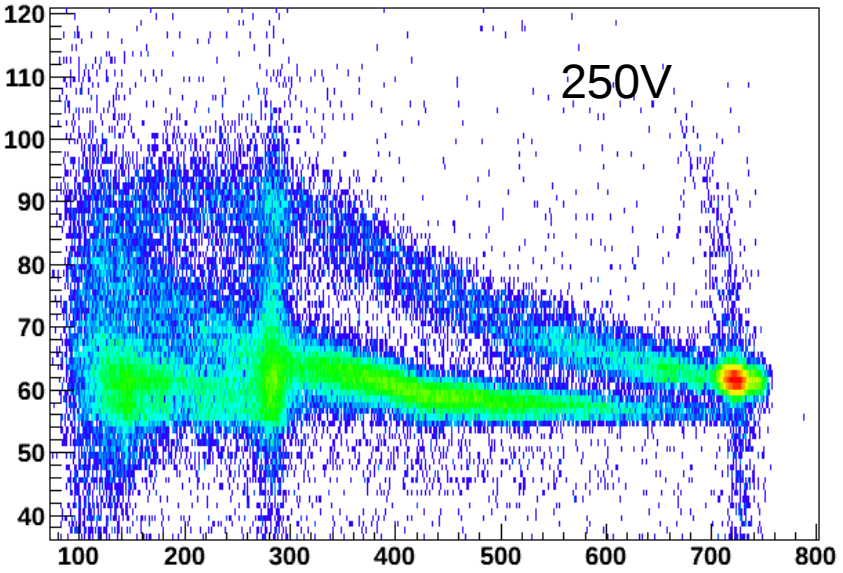


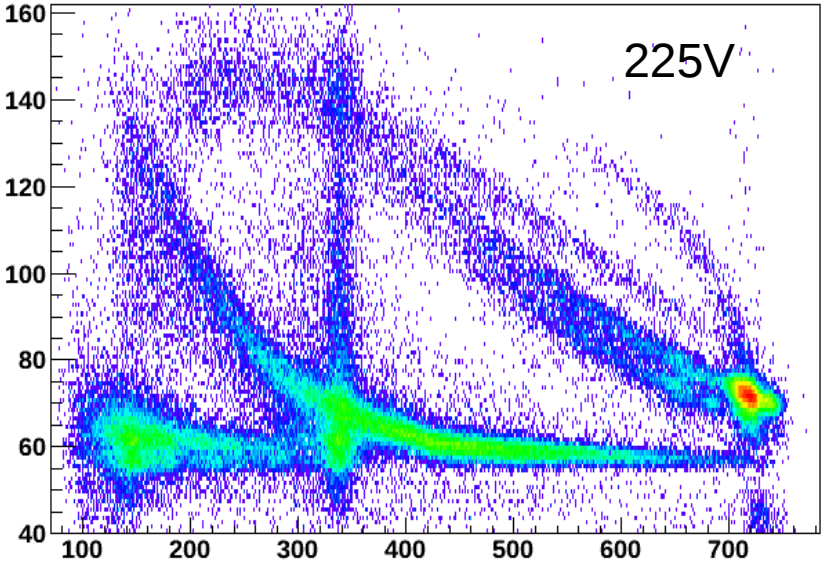
# Energy vs Rise time: ($^{7}$Li +$^{89}$Y)

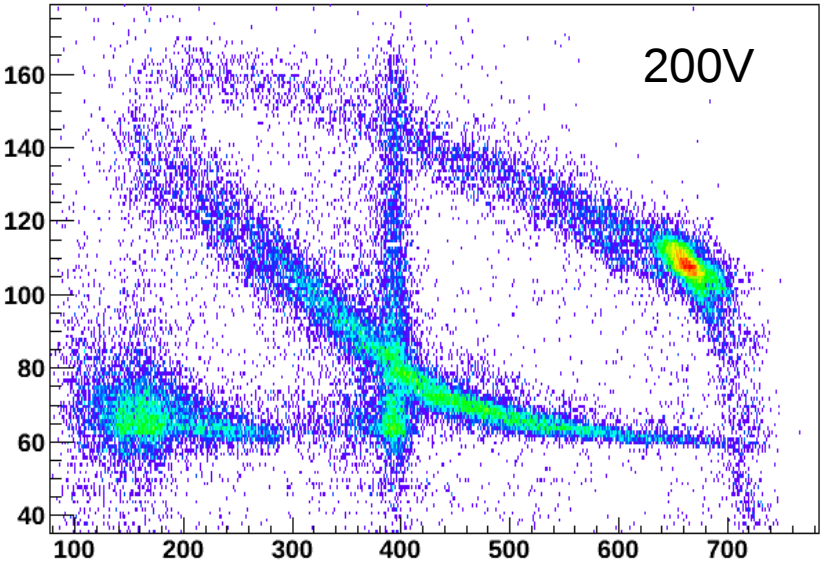


# Energy vs rise time: effect of depletion voltage



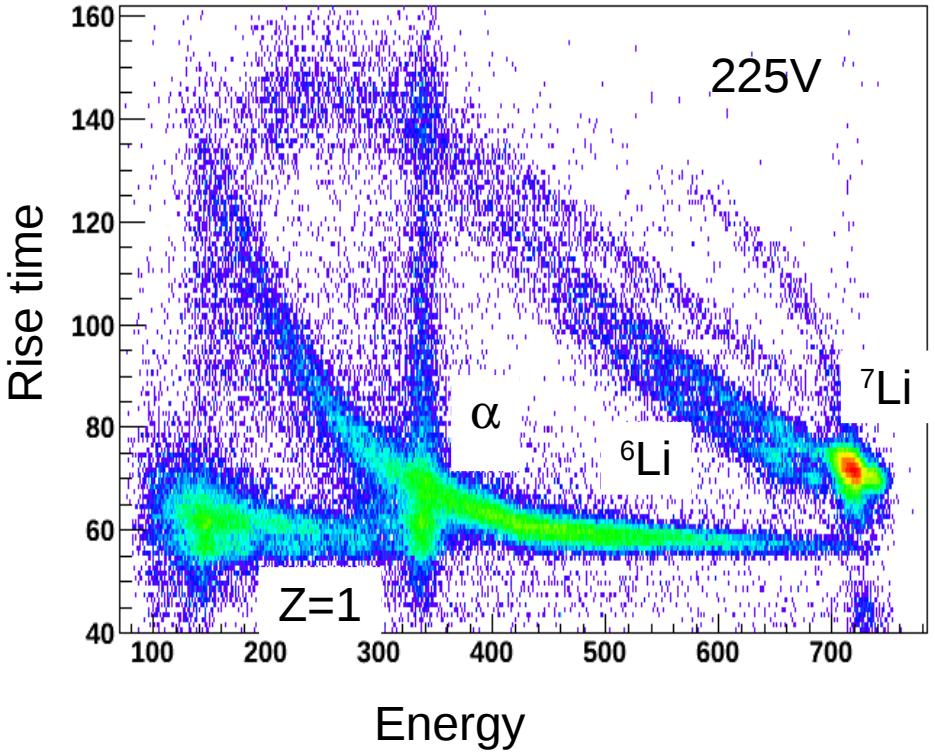



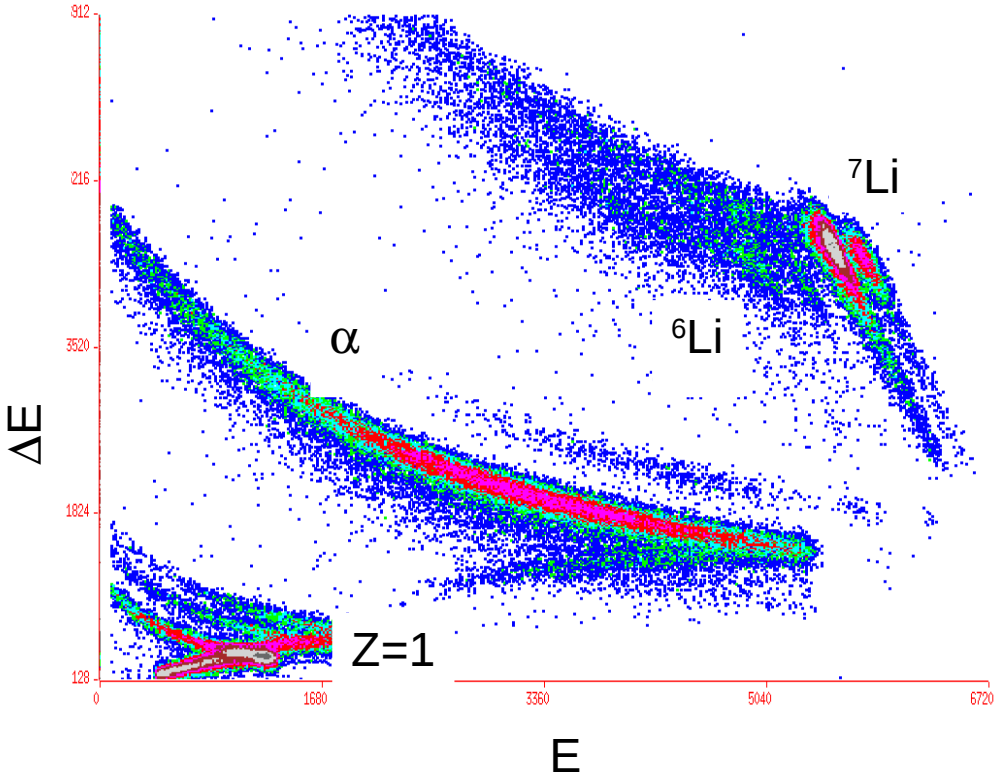




Rise time

Energy

# Energy vs Rise time and DE-E (mass separation)



# Summary and outlook

- A test experiment to study digital pulse shape analysis has been carried out
- Only charge signal have been digitized using indigenously developed high speed FPGA based card
- Effect of depletion voltage has been studied
- Charge as well as mass separation have been achieved
- 8 channel card is under fabrication
- Procurement of CAEN digitizer
- Prototype 64 x 64 strip DSSD has been fabricated and I-V characteristics are being tested

# *Worplan for 2012*
# *(from D Beaumel talk Nov 2011, Mumbai)*

## ORSAY/HUELVA

- Test experiment at IPNO tandem (February)
  3 telescopes with new nTD protos
  1 telescope monocell (Fazia)
  1 telescope of TRACE (pads)
- Data analysis – conclusion
- start detailed design of final detectors

## MUMBAI

- Develop numerical bench
  - ✓ get preamplifiers (PACI)
  - ✓ test cards
  - ✓ choose/purchase digitizer MATACQ (CAEN)
  - ✓ integrate in DAQ
- Delivery of standard DSSDs from BEL (June)
- Test with $\alpha$-source and beam
  - BEL standard DSSD
  - ✓ MICRON sc nTD detectors

Thank you