PId Front End Chip: PIF

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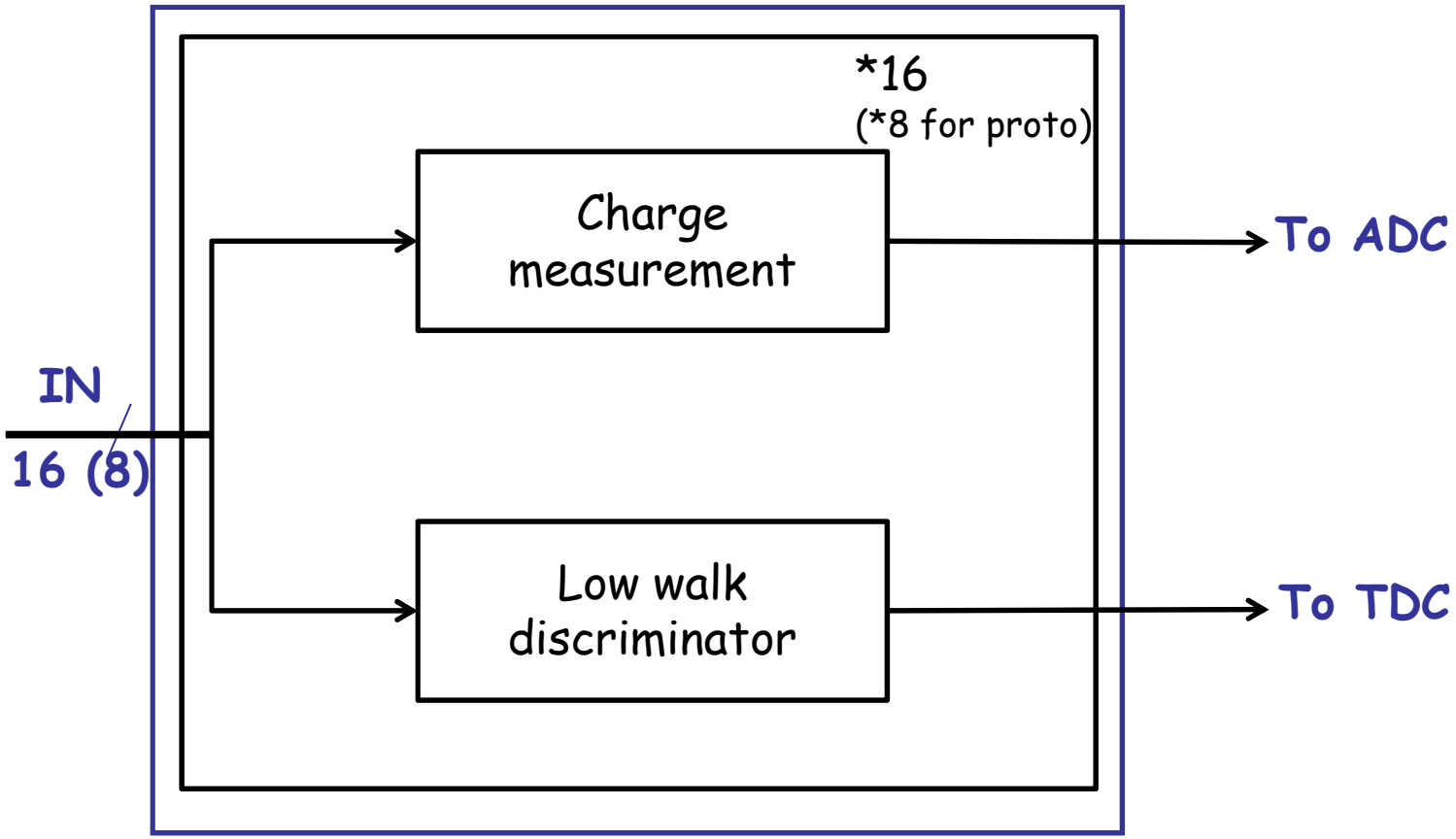
Characteristics & Requirements

- PMT signal characteristics (Jerry's & Bari's meas.):
  - amplitude's:
    - Dynamic around 15
    - Pixel to pixel dispersion: 3
  - time's:
    - rise time: 700ps
    - Fall time: 1,5ns

- Time measurement :
  - 100ps resolution max total
    - Considering 70ps TDC resolution: 50ps for PIF
  - 1MHz background rate max
  - 50ns double pulse resolution min

- Charge measurement :
  - Maximum signal considered to be 100mV
  - 8 bits
  - Time measurement synchronous

PIF: PID FE chip



PIF: FE chip

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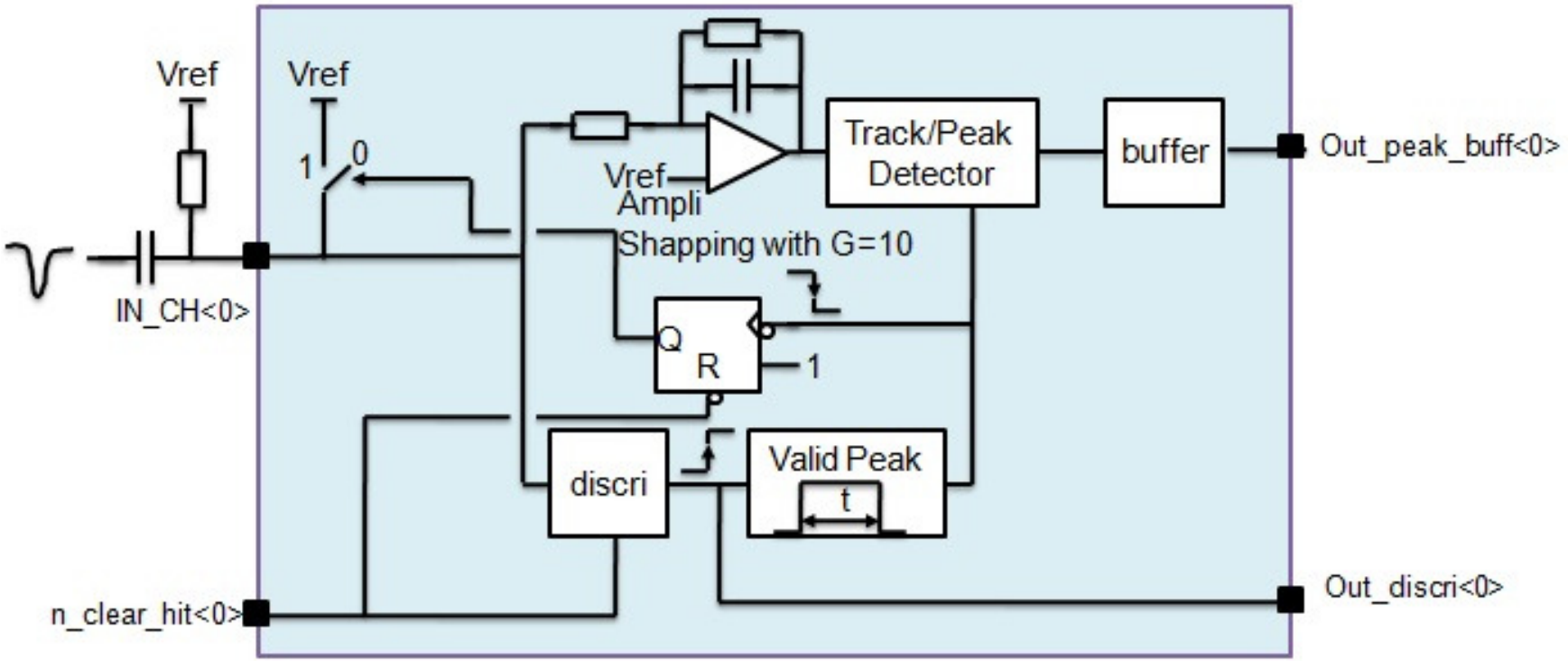
• No walk correction if walk < 50ps (depending on PM dynamics) • Charge measurement to improve resolution	• Need « Time + charge » data synchronization

2 different chips developed:

❶ analog front end -> {PIF }: CFD like and charge measurement

❷ time measurement -> {SCATS}

PIF 1rst prototype architecture

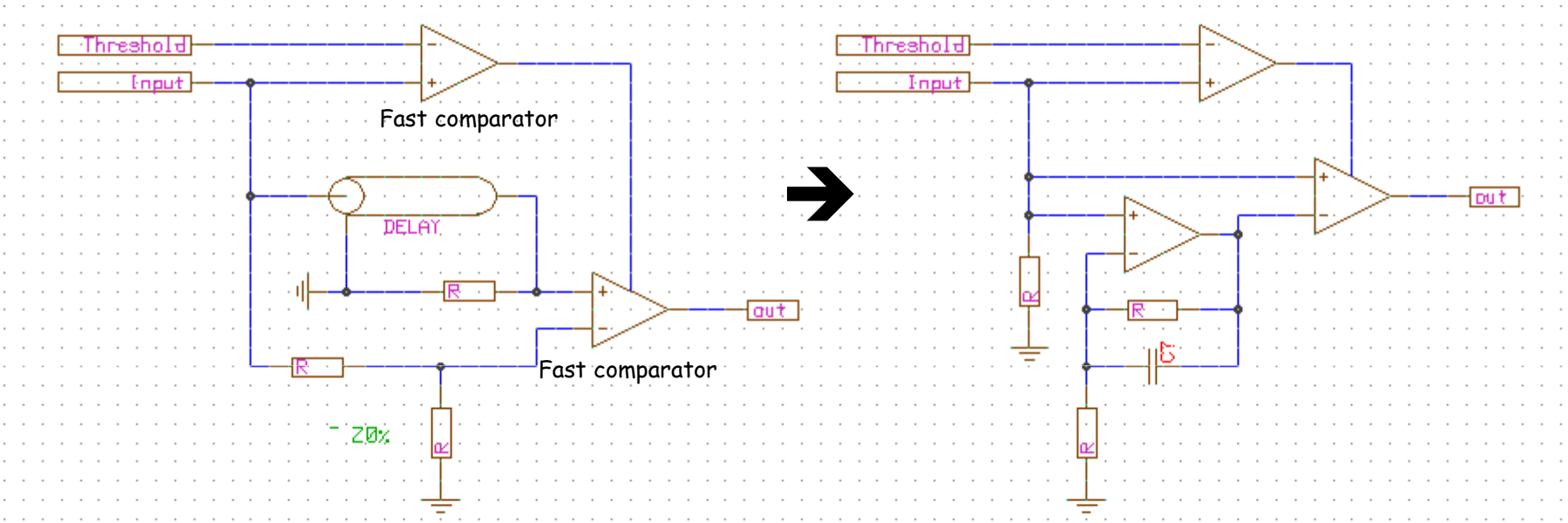


Gain dispersion consideration:

- **Input gain selection**
- **No selection / look up table**

Both solutions need pixel mapping – 2nd solution has been chosen for the 1rst proto.

CFD on silicon

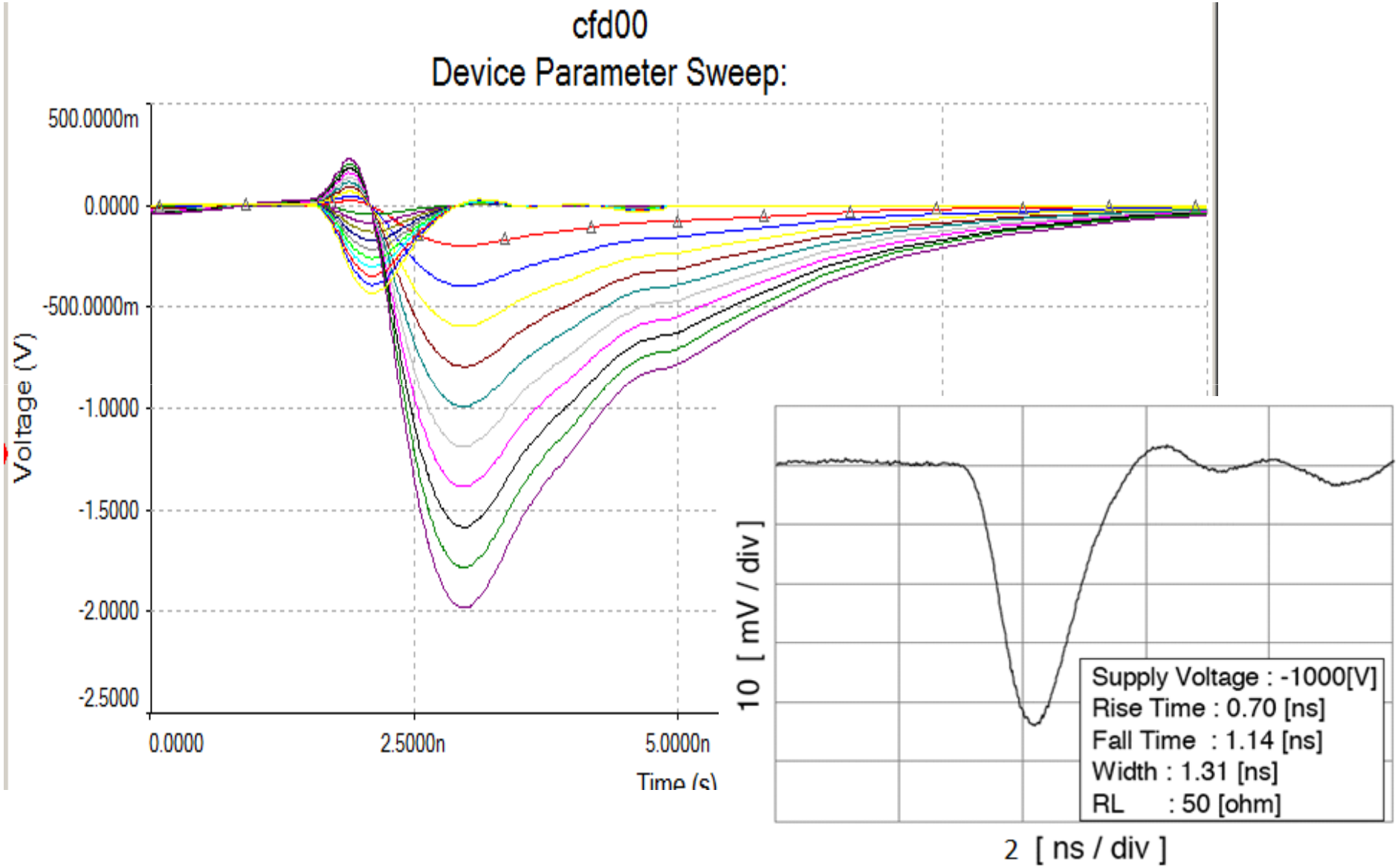


Classical CFD

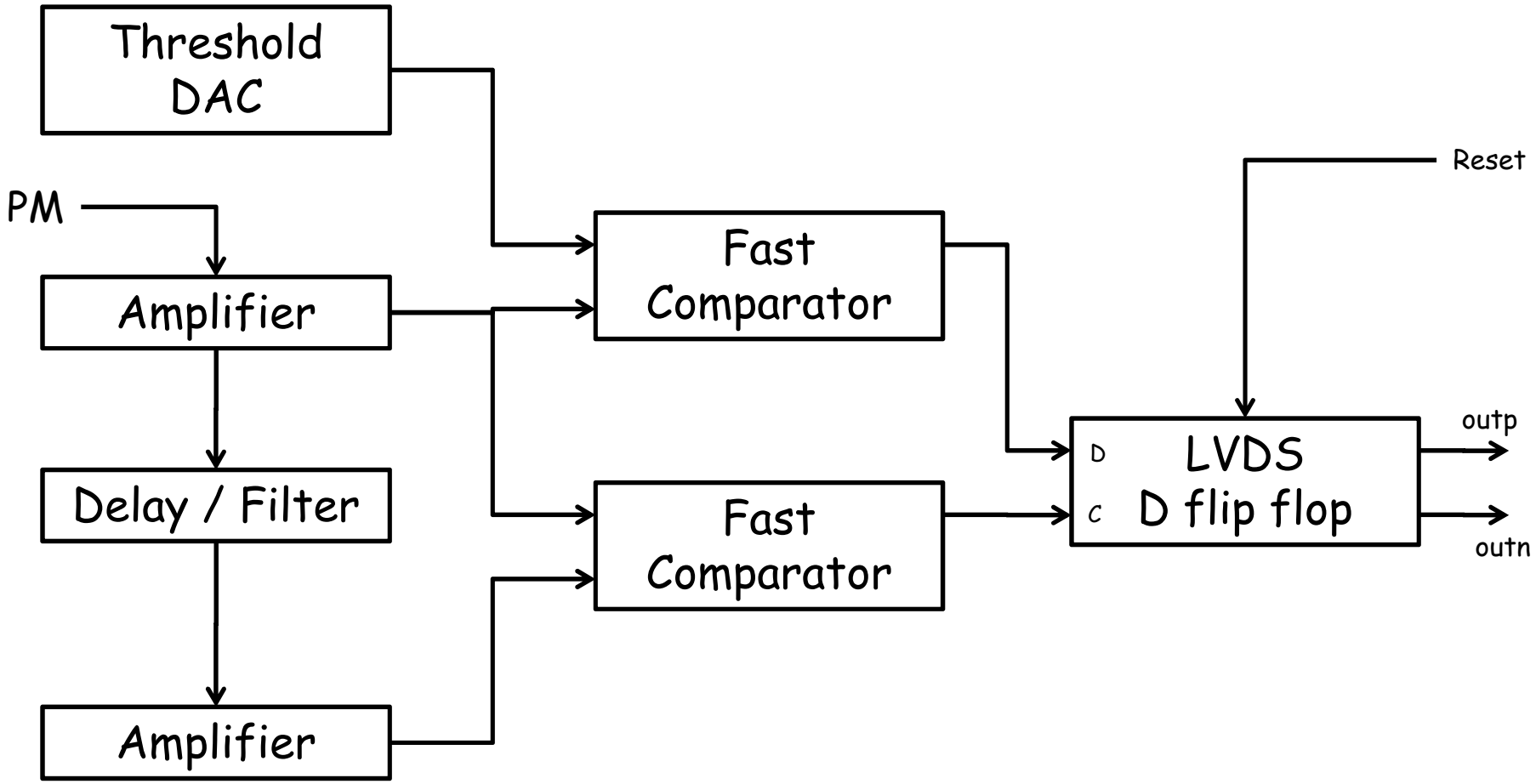
Proposed pseudo CFD

- Delay + Fraction → Gain + Integrators

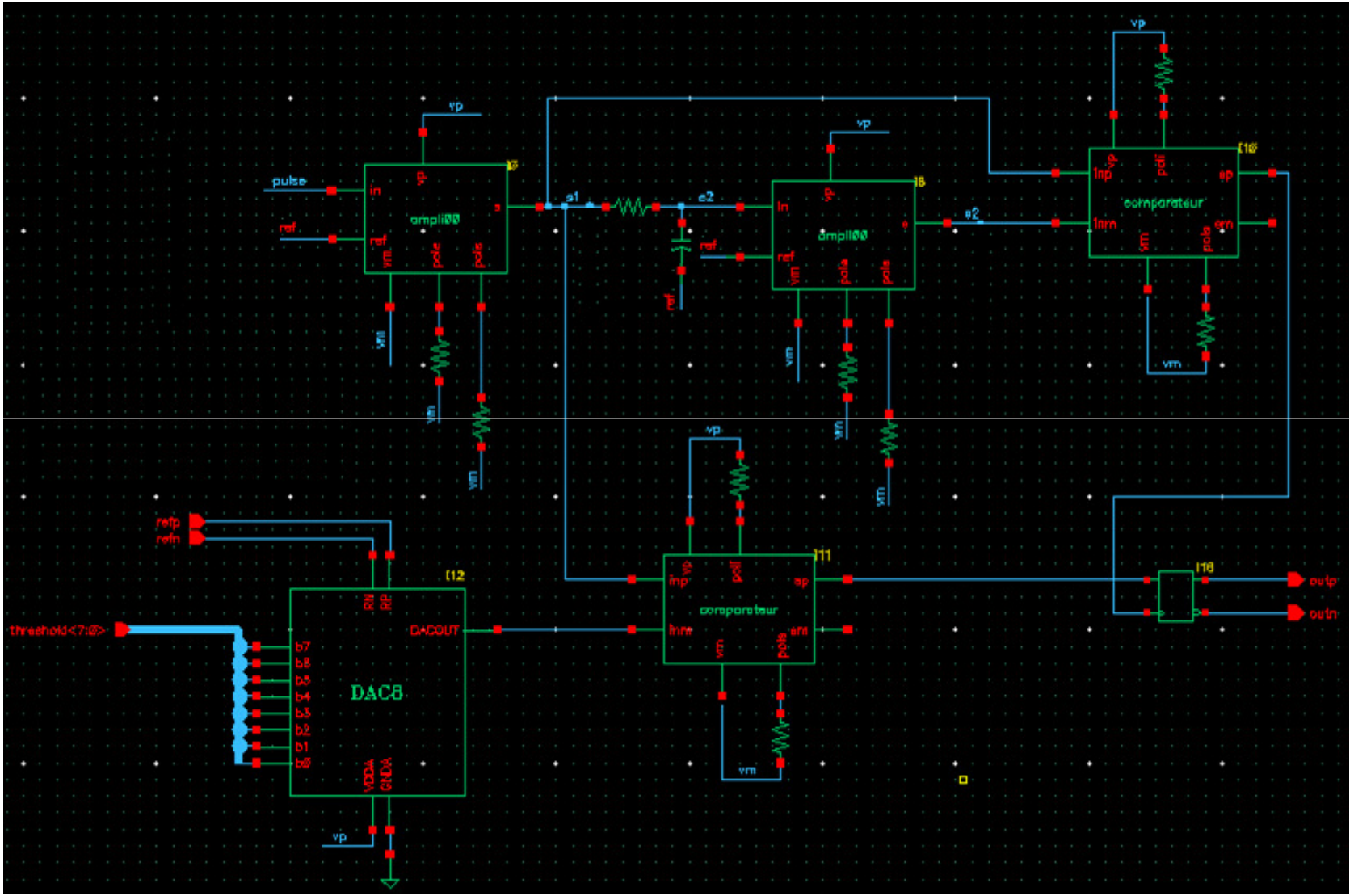
Spice Simulations



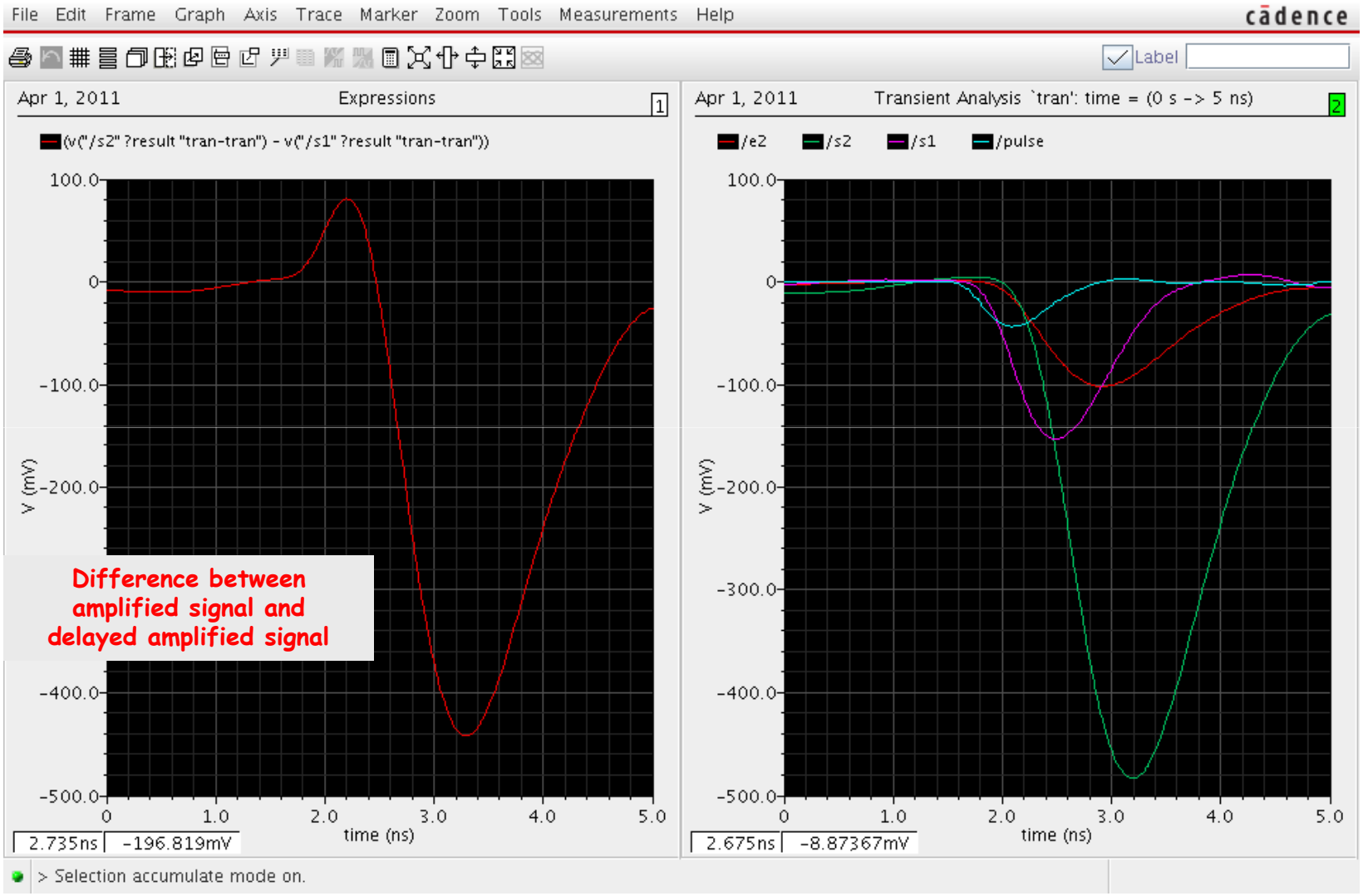
CFD Implementation



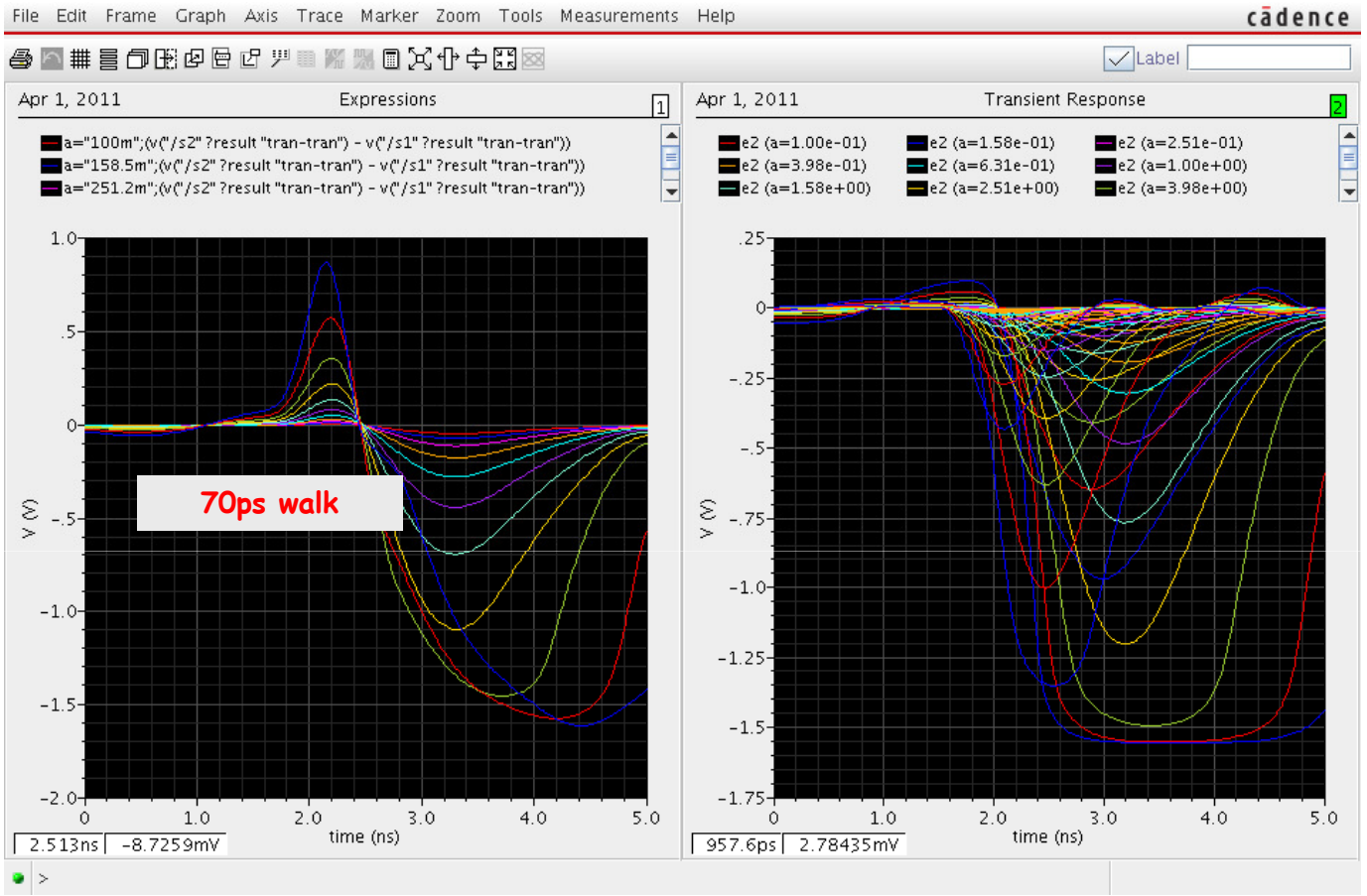
Simulations with AMS CMOS 0.35µ



Simulations with AMS CMOS 0.35µ



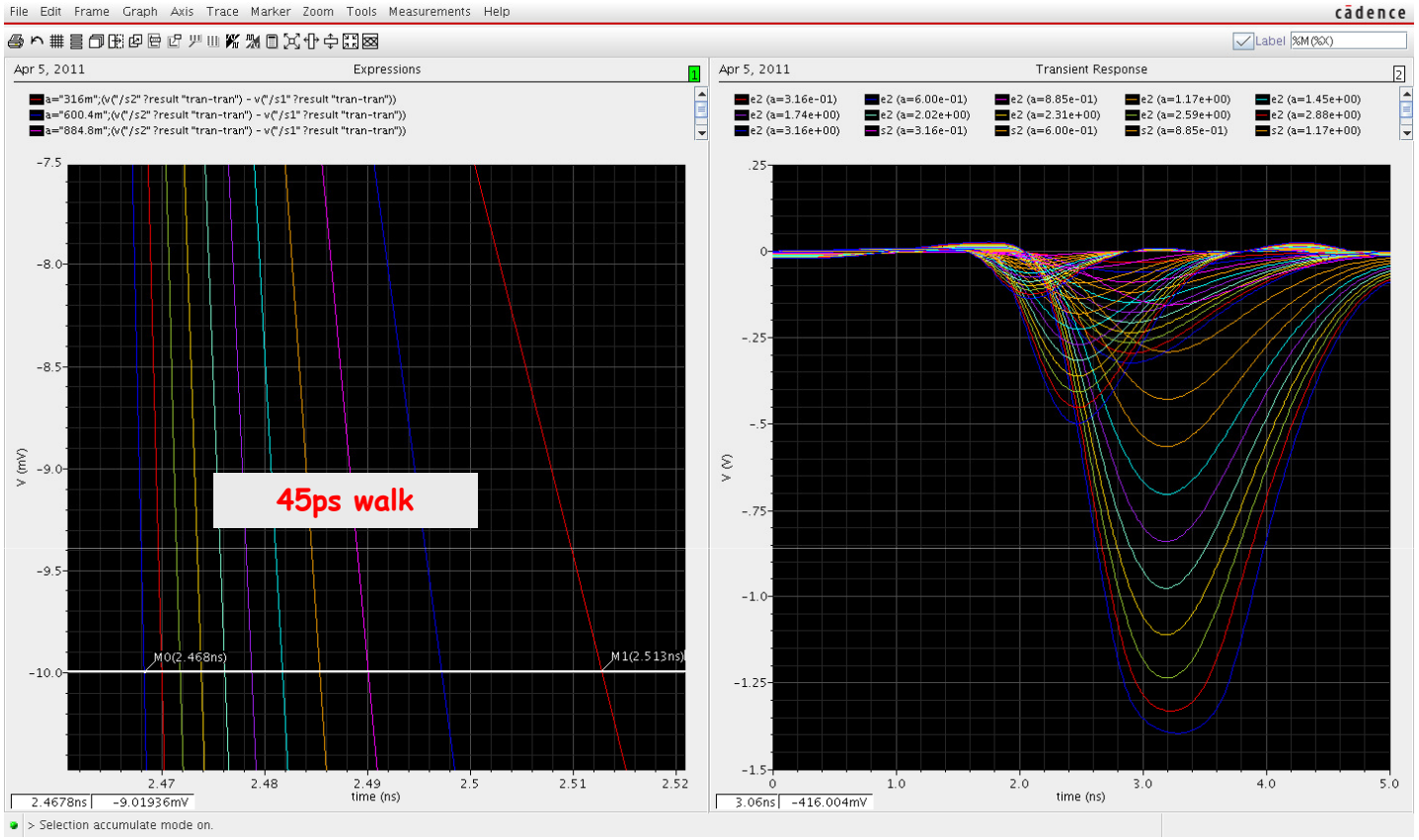
Parametric simulation : amplitude from 1 to 100



Resolution:

- ↳70ps for a dynamic of 100
  - ↳100ps total resolution

Parametric simulation : amplitude from 1 to 10

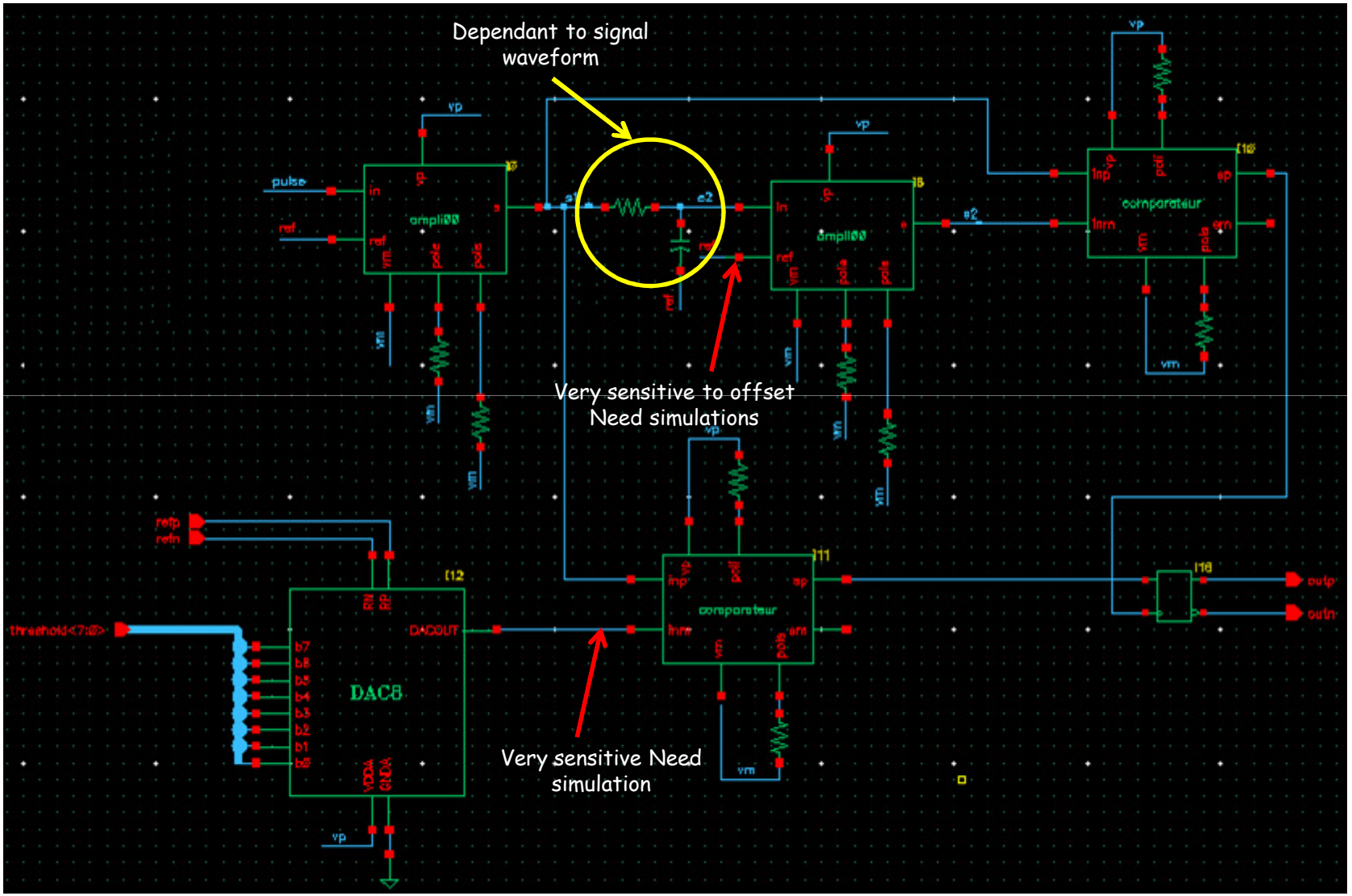


Resolution:

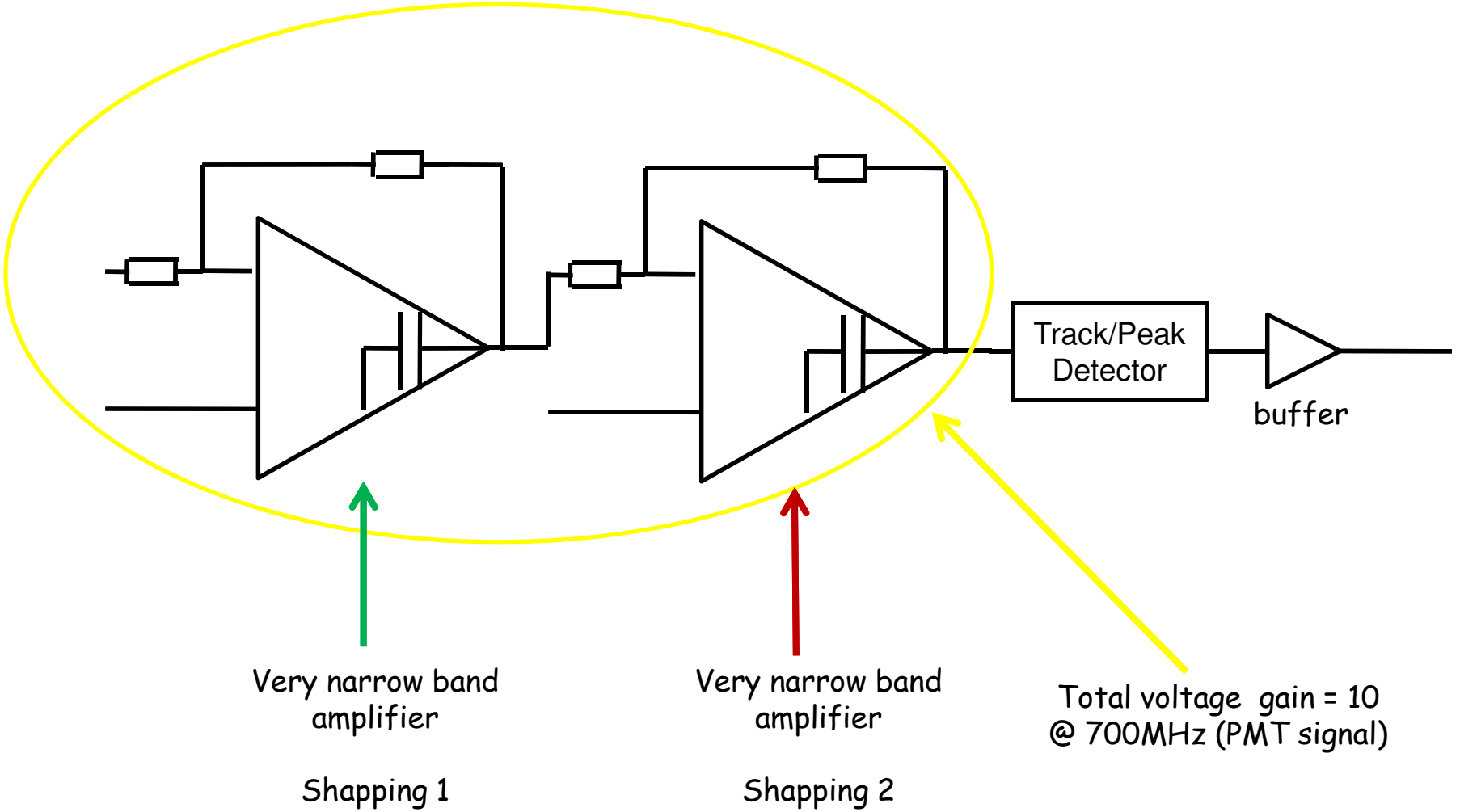
- 50ps for a dynamic of 10
  - 86ps total resolution

V. Tocut, A. EL Berni, SuperB Workshop, Elba 06/2012

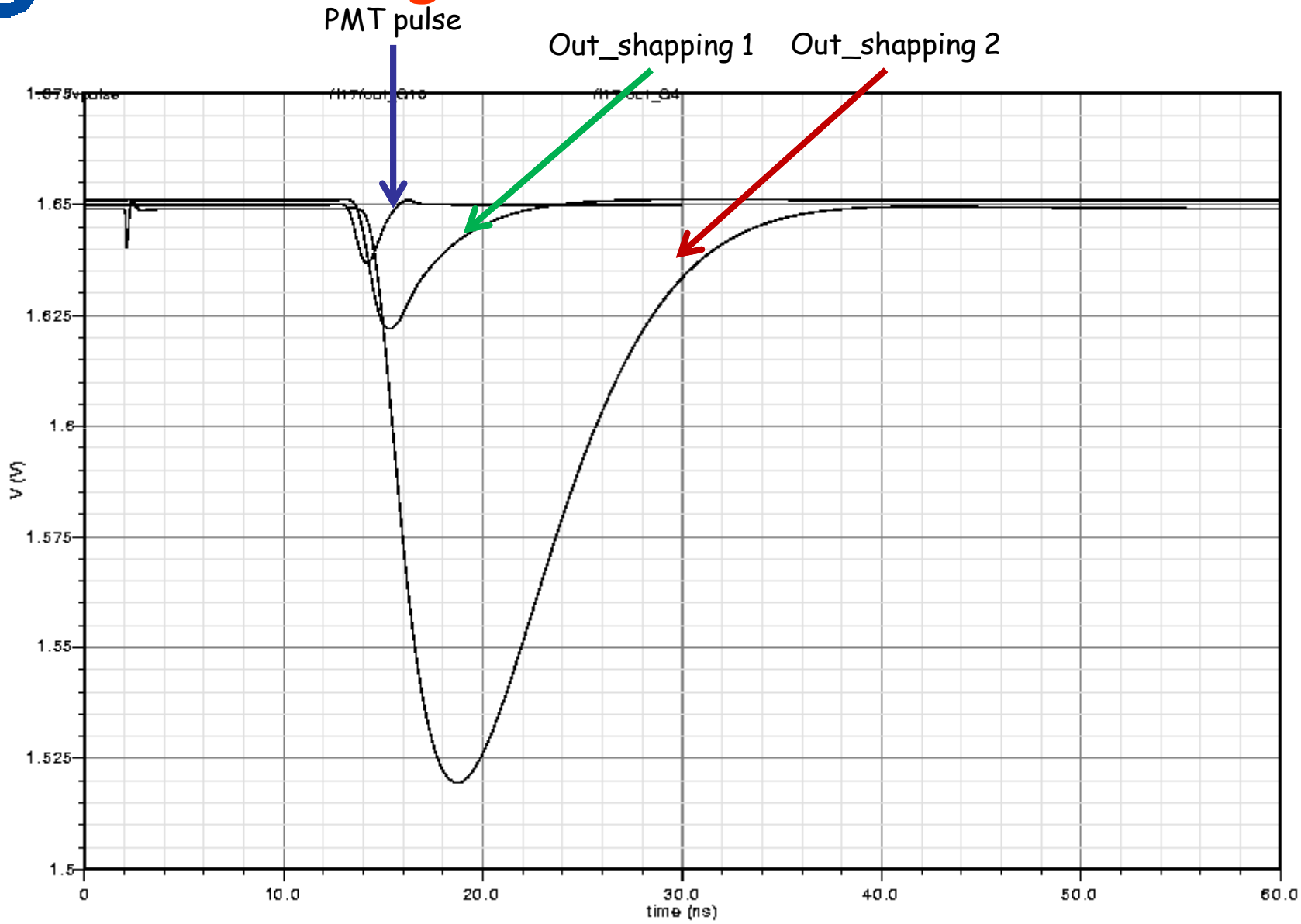
Design challenges



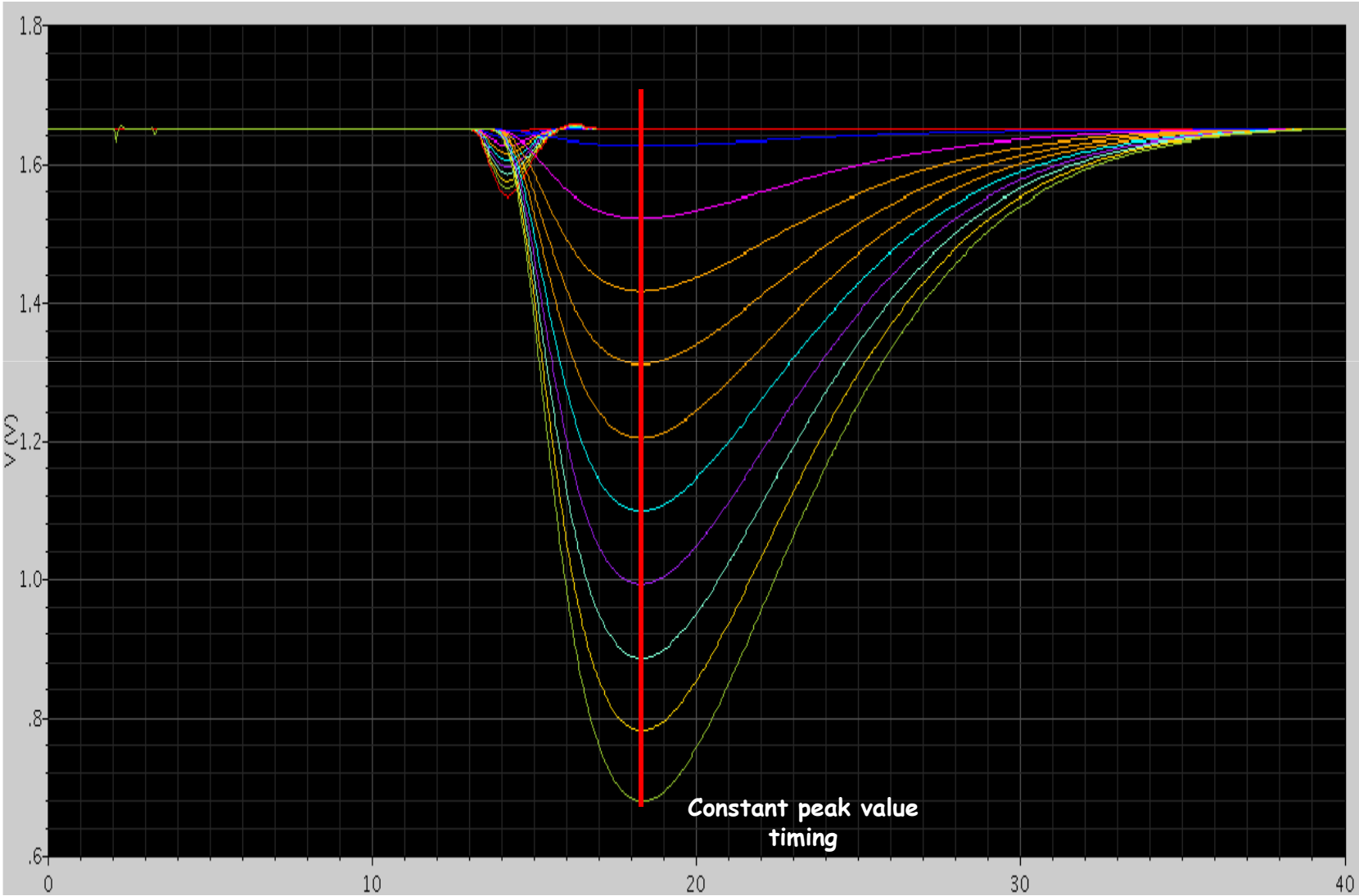
Charge measurement Implementation



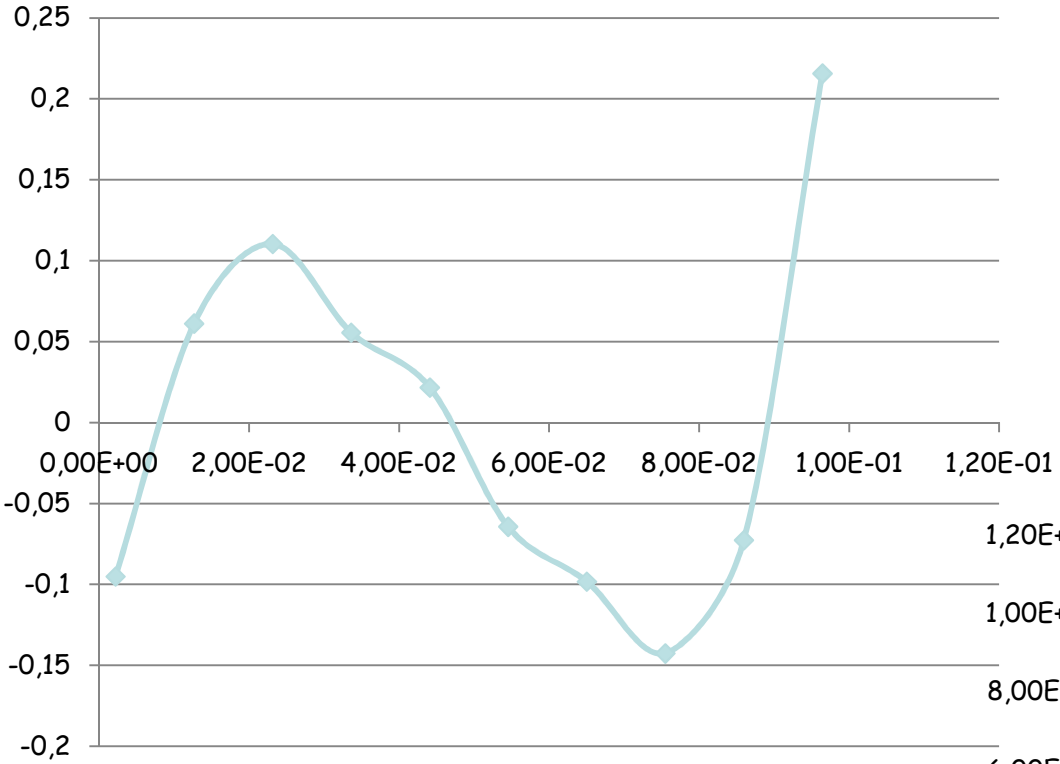
PIF charge measurement simulation



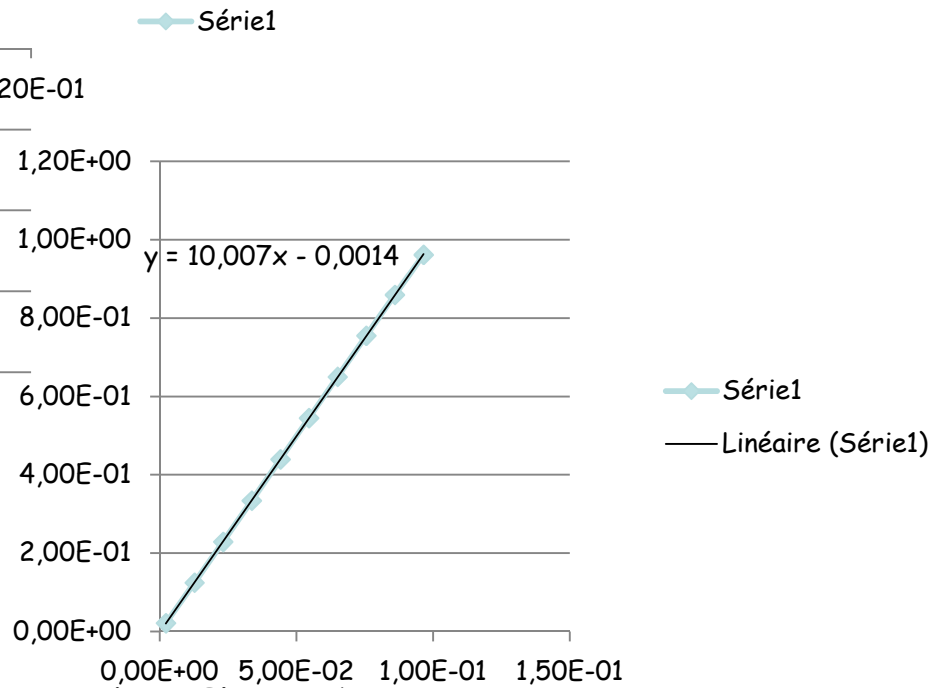
PIF charge measurement simulation



PIF charge measurement simulation



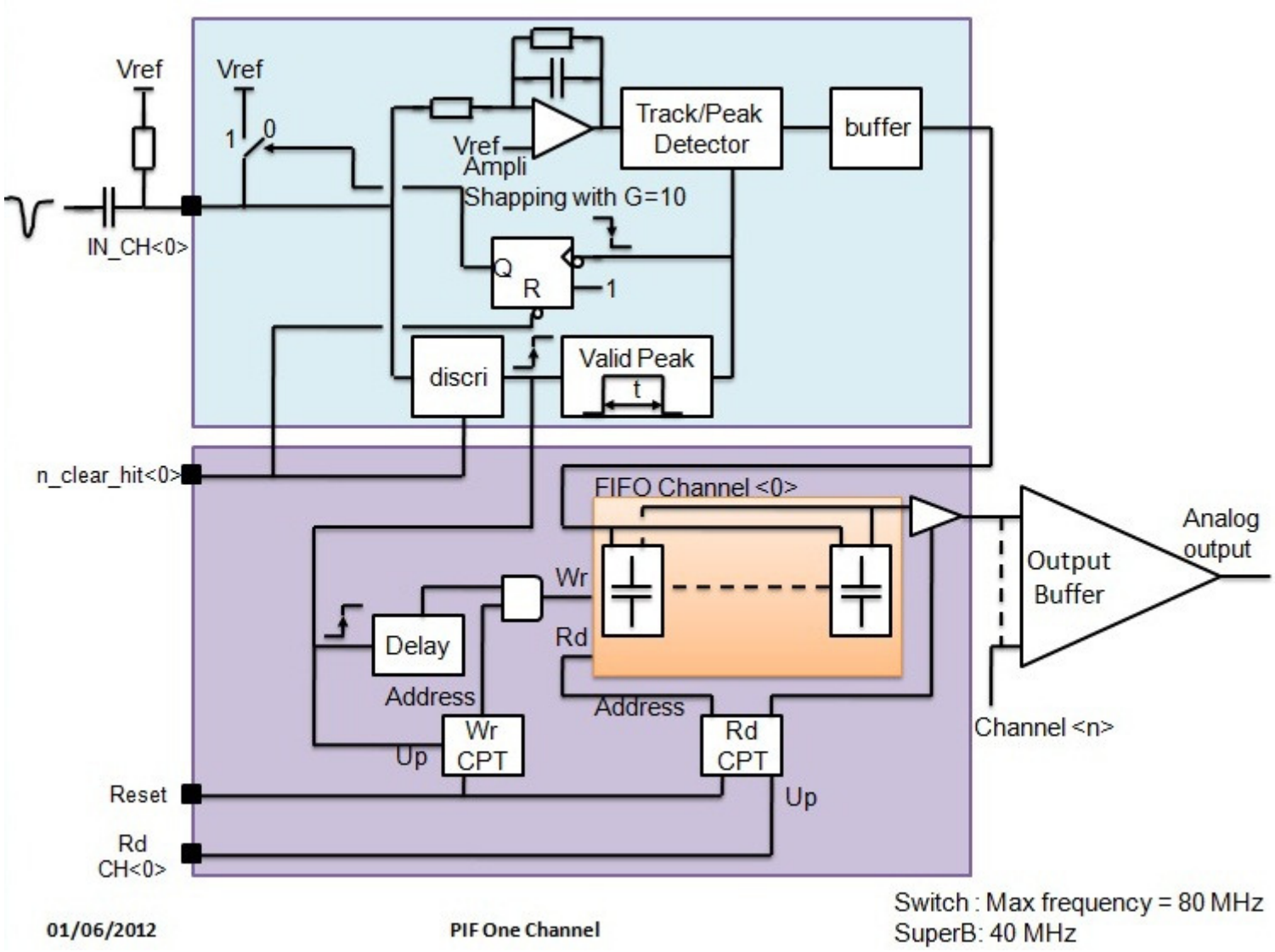
Linearity over the full range 2mV to 100 mV



Milestones

- PIF :
  - Design & Simulations with CMOS AMS 0.35μ (to be 'SCATS compatible')
  - Submission by the end of 2012 (Dec, the 10th). PIF back around the end of feb. 2013

PIF (inside SCATS) final architecture



LAL CRT test bench

D. Breton, C. Beigbeder, A. El Berni, V. Tocut,
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Status

- Operational CRT test bench @ LAL with discri boards.

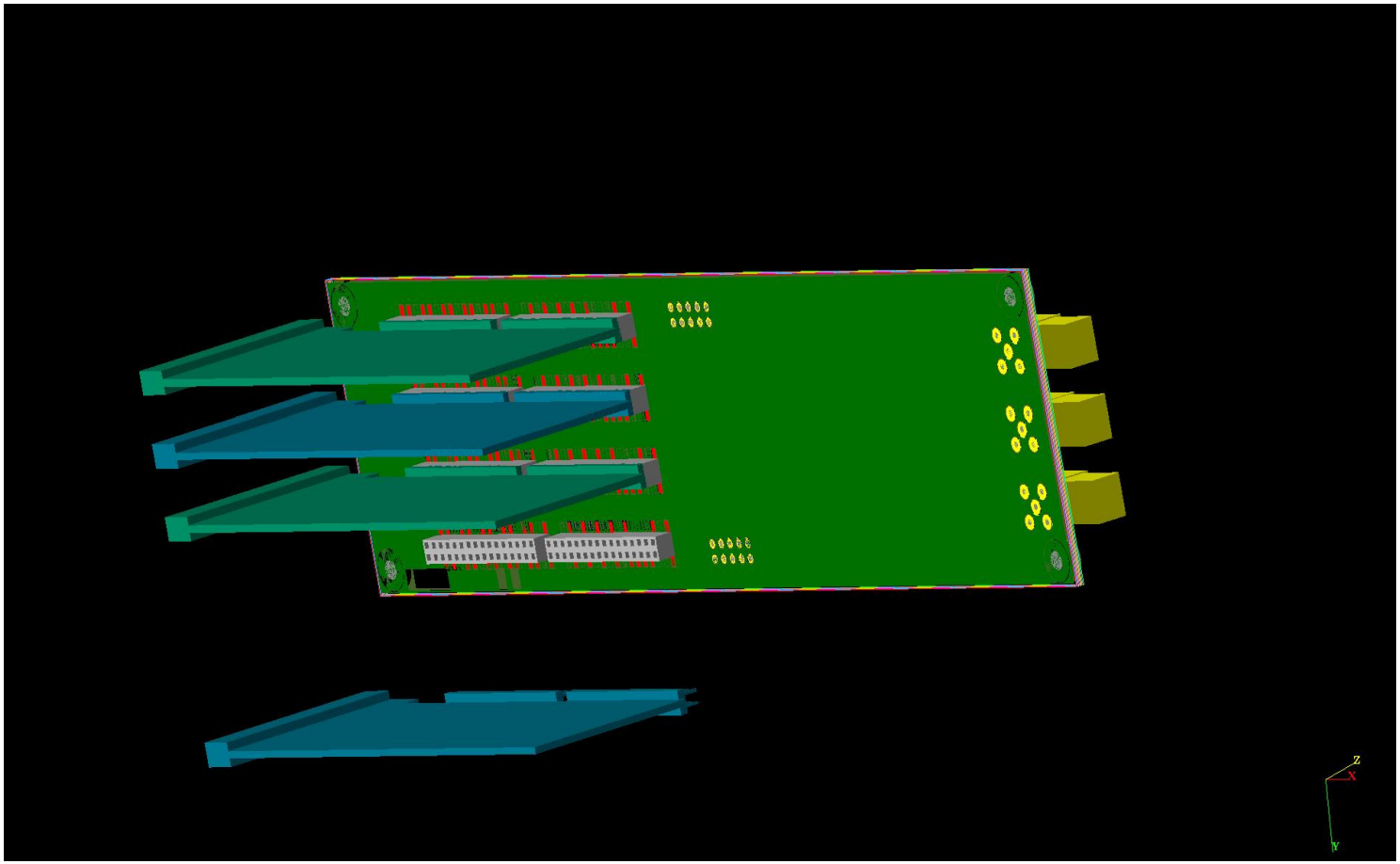
- Sensitivity to fine tuning has been demonstrated: signal shape – signal offset….
  - Manuel tuning 'a la BABAR' has to be avoided!

- Width and amplitude of the discri signal is critical for SCATS (Time measurement):
  - very low amplitude & narrow signal on CRT board
  - discrete solution problem or pseudo-CFD generic problem? Has to be solved.
  - Can we enlarge the signal to be able to deal with SCATS requirements?

- Pseudo CFD walk can be evaluated

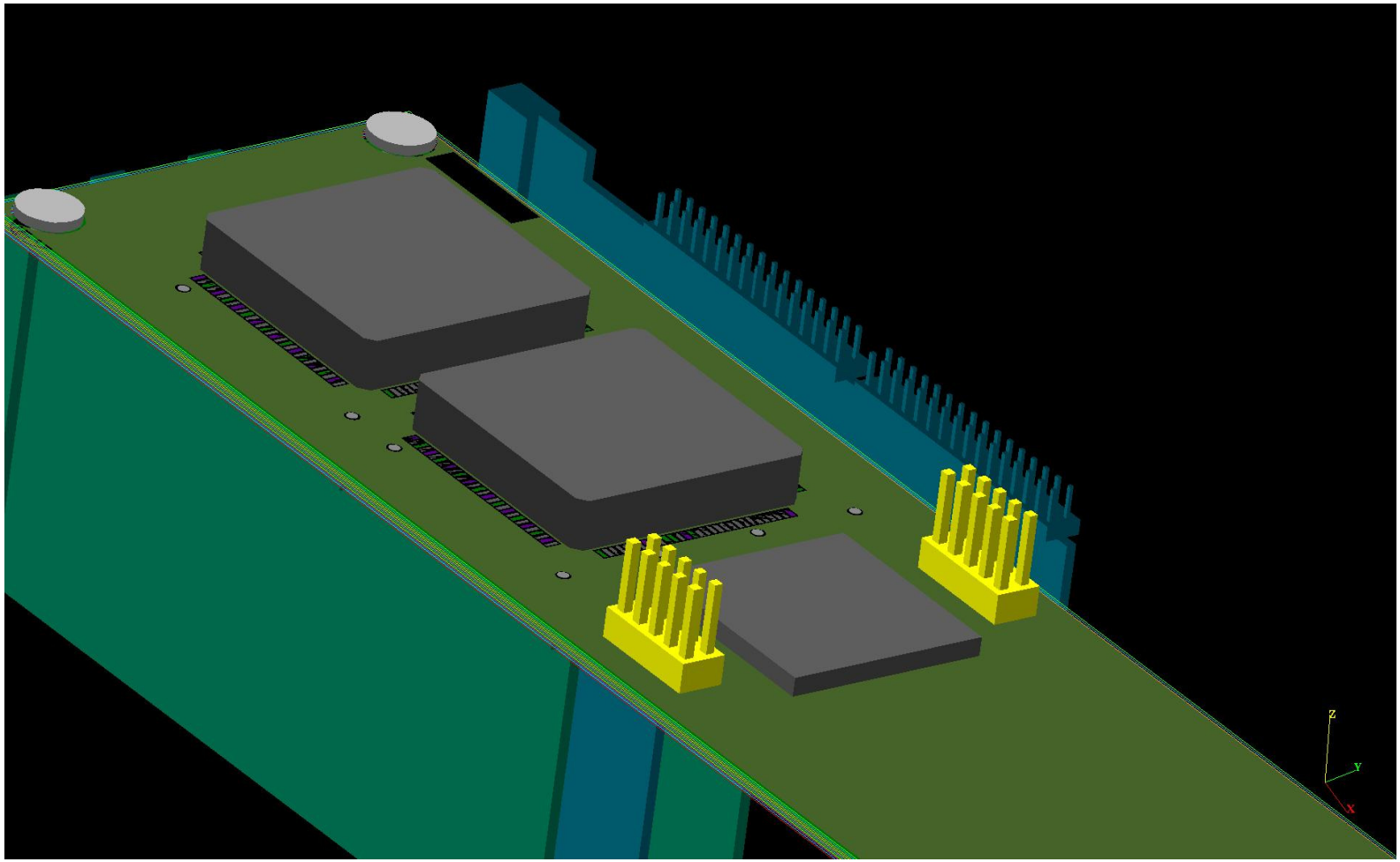
At the same time, another is now under investigation

CRT test board



4 analog boards with the SCATS CRT (bottom view)

CRT test board



- **SCATS CRT board : 2 SCATS, 1 FPGA.**
- **ADC will be added for the new design of analog board with PIF.**
- **Input and ouput connectivity have to be compatible with both designs.**