

## **Arachnid Project**

4<sup>th</sup> SuperB Collaboration meeting, Elba, 2<sup>nd</sup> June 2012

F. Wilson on behalf of Arachnid members:

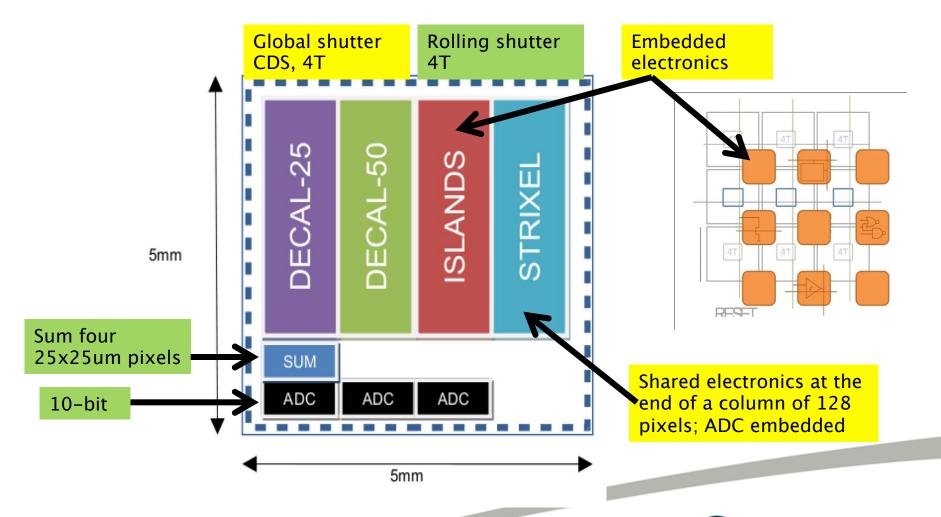
Birmingham, Bristol, QMUL, STFC - RAL, STFC - Daresbury

## **CHERWELL Chip Reminder**

- CMOS MAPS
- Low power, low noise, small inactive area
- Rolling Shutter, Correlated Double Sampling (CDS) and 4T architecture
- Control and readout electronics distributed in active area
- Power pulsing (CLIC/ILC)
- Binary and digital readout
- On-board 10-bit ADCs



### **CHERWELL** demonstrator





## **Progress since March**

- Now have initial firmware for CHERWELL chip.
- Now have readout software for system using inhouse USB-DAQ.
- Investigating replacing USB-DAQ with commercial version (Opal Kelly).
- The 3 variations of the chip (standard and highres) are now bonded onto the carrier board (CoB) and available at 4 institutes for testing.
- Hired designer for next generation of chip.
- Started Fe<sup>55</sup> testing.



#### **Current firmware status**

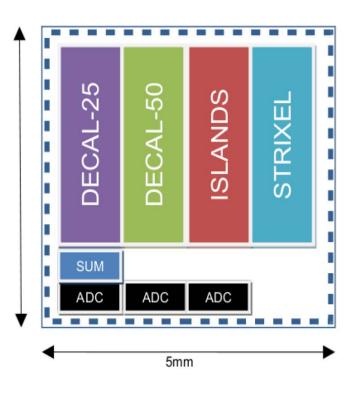
- Rolling Shutter control and external ADC readout of Cherwell and Strixel parts.
- Rolling Shutter control and internal ADC readout of Cherwell, Strixel, and DECAL parts.
- Global shutter implemented but not fully tested.



### **Cherwell CoB**



5mm

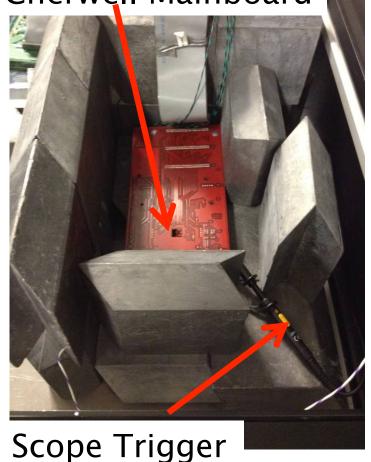


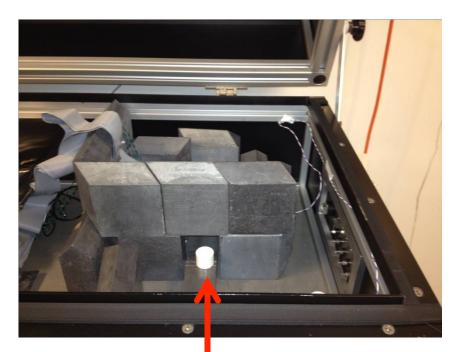
5mm



# Fe<sup>55</sup> Testing - May 2012

Cherwell Mainboard



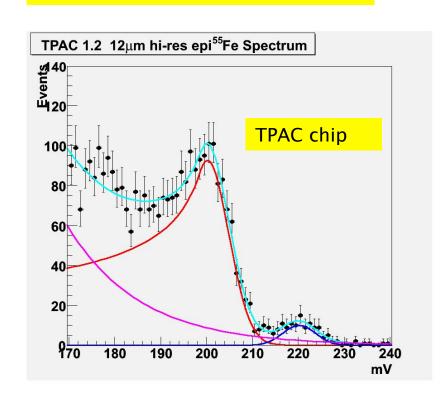


Fe<sup>55</sup> source

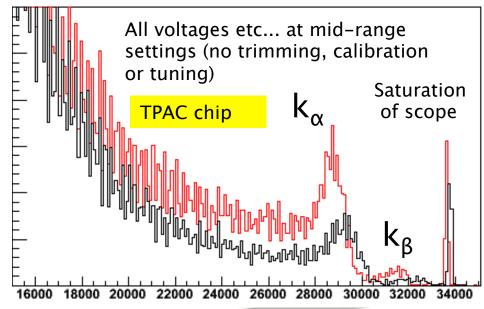


## Resurrecting readout chain

Original results from EUDET testing at DESY 2010



First results with Fe<sup>55</sup> at QMUL 16<sup>th</sup> May 2012



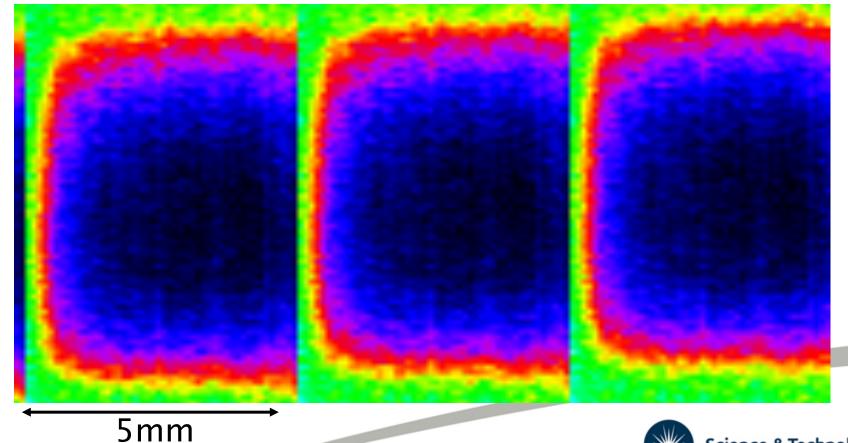


### First results from CHERWELL chip

Response to room light, 16 May

2nd June 2012

All voltages etc... at mid-range settings (no trimming, calibration or tuning yet)

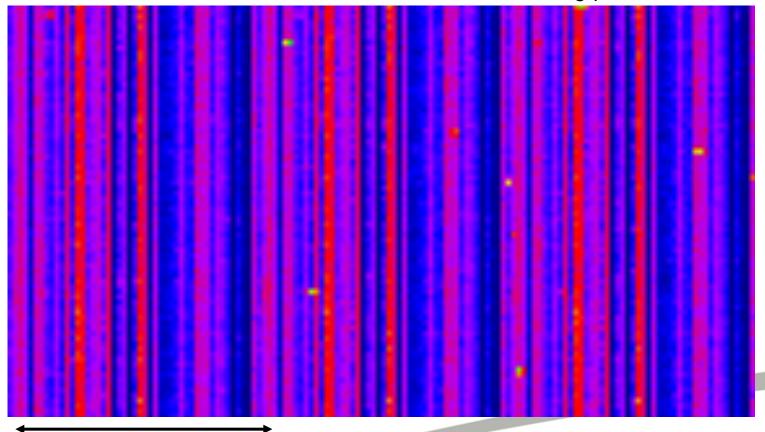


Science & Technology
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### First results from CHERWELL chip

Response to Fe<sup>55</sup> in dark room, 16 May

All voltages etc... at mid-range settings (no trimming, calibration or tuning yet)







#### **Current Plans**

- We are re-commissioning our 2 IR laser systems (Bristol and RAL).
- Fe<sup>55</sup> testing at all sites.
- We are re-commissioning our test beam setup (telescope, trigger, power, readout, etc...)
- Test beam at CERN in November.
- Hope to go to DESY before then.
- We are investigating access to a proton source on RAL campus or at Birmingham.
- Aiming for presentation of results at Pixel 2012 (Sep, Japan)



#### **Current Plans**

- We are designing a next generation chip.
- It will take on-board the needs of SuperB but ...the chip is targeted at ALICE Inner Tracker upgrade due to:
  - Upgrade and CDR/TDR schedules
  - UK funding
  - UK Nuclear Physics priorities and size of group
- There is good overlap between ALICE and SuperB needs
- Main goals are:
  - Prove radiation hardness
  - Identify power requirements
- Possible Schedule:
  - Hope to design, produce and begin first testing by Spring 2013
- Continue to support SuperB access to CMOS foundry.



### Conclusion

- It has taken us some time to get to this stage.
- Testing progress should accelerate from now on.
- Hope to characterize the CHERWELL chip performance over the summer.
- Moving from a demonstrator chip to a new chip design specifically for the needs of Nuclear/Particle Physics.

