INFN/AExxx, LAL-xxx, SLAC-R-xxx

Super$B$ Detector Technical Design Report

Abstract

This report describes the technical design detector for Super$B$.

Contents

11 Electronics, Trigger, Data Acquisition and Online

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11.1 Architecture Overview

SL + DB + UM

The Super$B$ [1] Electronics, Trigger, Data acquisition and Online system (ETD) comprises the Level-1 trigger, the event data chain and their support systems. Event data corresponding to accepted Level-1 triggers move from the Front-End Electronics (FEE) through the Read-Out Modules (ROMs), the network event builder, the High Level Trigger (HLT) to a data logging buffer where they are handed over to the offline for archival and further processing. ETD also includes the hardware and software components that control and monitor the detector and data acquisition systems and perform near-real-time data quality monitoring and online calibration.

The system design takes into account the experience from running *BABAR* [2] and building the LHC experiments [3], [4], [5]. To minimize the complexity of the FEEs and the number of data links, the detector side of the system is synchronous and all sub-detector readouts are triggered by a fixed-latency first-level trigger. Custom hardware components (e.g. specialized data links) are only used where the requirements cannot be met by off-the-shelf components (such as e.g. Ethernet). Radiation levels are significantly higher than in *BABAR*, making it mandatory to design radiation-tolerant on-detector electronics and links. Fig. 11.1 shows an overview of the trigger and the event data chain:

A first-level hardware trigger uses dedicated data streams of reduced primitives from the sub-detectors to provide trigger decisions to the Fast Control and Timing System (FCTS). The FCTS is the central bandmaster of the system; it distributes the clock and readout commands to all elements of the architecture and initiates the readout of the events in the detector FEE. In response to readout requests, the FEE send event fragments to the ROMs which perform a first stage internal event build and send the partially constructed events to the HLT farm where they are combined into complete events and processed by the HLT which reduces the amount of data to be logged permanently by rejecting uninteresting events.

The trigger, data acquisition and support components of the ETD system are described in this chapter, subdetector electronics, power supplies, grounding and shielding and the cable plant are described in the next chapter.

11.1.1 Trigger Strategy

PB + UM + SL

The *BABAR* and Belle [6] experiments both chose to use "open triggers" that preserved nearly 100% of $B\overline{B}$ events of all topologies, and a very large fraction of $\tau^+\tau^-$ and $c\bar{c}$ events. This choice enabled very broad physics programs at both experiments, albeit at the cost of a large number of events that needed to be logged and reconstructed, since it was so difficult to reliably separate the desired signals from the $q\bar{q}$ ($q = u, d, s$) continuum and from higher-mass two-photon physics at trigger level . The physics program envisioned for Super$B$ requires very high efficiencies for a wide variety of $B\overline{B}$, $\tau^+\tau^-$, and $c\bar{c}$ events, and depends on continuing the same strategy, since few classes of the relevant decays provide the kinds of clear signatures that allow the construction of specific triggers.

All levels of the trigger system are designed to permit the acquisition of prescaled samples of

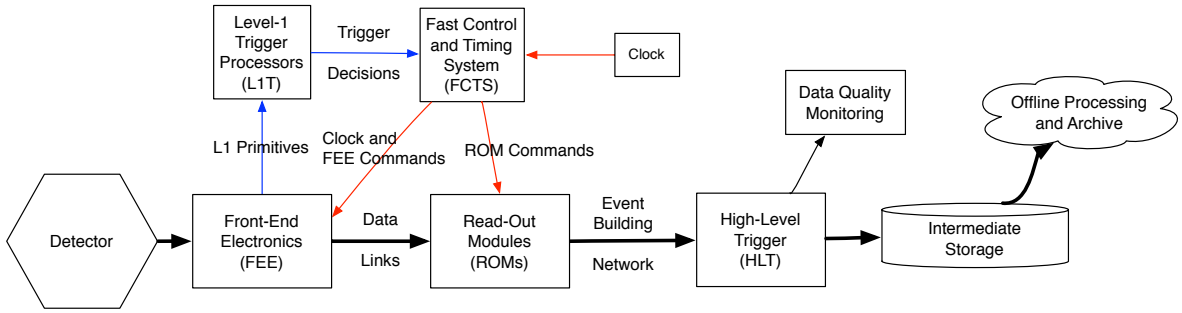


Figure 11.1: Overview of the Trigger and Data Chain

events that can be used to measure the trigger performance.

The trigger system consists of the following components [1]:

Level 1 (L1) Trigger: A synchronous, fully pipelined L1 trigger receives continuous data streams from the detector independently of the event readout and delivers readout decisions with a fixed latency. While we have yet to conduct detailed trigger studies, we expect the L1 trigger to be similar to the *BABAR* L1 trigger, operating on reduced-data streams from the drift chamber and the calorimeter. We will study the possibilities of improving the L1 trigger performance by including SVT information, taking advantage of larger FPGAs, faster drift chamber sampling, the faster forward calorimeter, and improvements to the trigger readout granularity of the EMC.

High Level Triggers (HLT) — Level 3 (L3) and Level 4 (L4): The L3 trigger is a software filter that runs on a commodity computer farm and bases its decisions on specialized fast reconstruction of complete events. An additional "Level 4" filter may be implemented to reduce the volume of permanently recorded data if needed. Decisions by L4 would be based on a more complete event reconstruction and analysis. Depending on the worst-case performance guarantees of the reconstruction algorithms, it might become necessary to decouple this filter from the near-realtime requirements of L3 — hence, its designation as a separate stage.

[1] While at this time we do not foresee a "Level 2" trigger that acts on partial event information in the data path, the data acquisition system architecture would allow the addition of such a trigger stage at a later time, hence the nomenclature.

11.1.2 Trigger Rate and Event Size Estimation

SL + UM

The Super*B* L1-accept rate design standard of 150 kHz is based on an extrapolation from *BABAR* (see the Super*B* CDR [1] for more detail). The *BABAR* Level-1 physics configuration produced a trigger of approximately 3 kHz at a luminosity of 10^{34} cm^{-2}sec^{-1}, however changes in background conditions produced large variations in this rate. The *BABAR* DAQ system performed well, with little dead time, up to rates of approximately 4.5 kHz. This headroom of 50% was very valuable for maintaining stable and efficient operation and will be retained in Super*B*.

In *BABAR* the offline physics filter's output corresponded to a cross-section of approximately 20 nb and included a highly efficient Bhabha veto. We take this as an irreducible baseline for an open hardware trigger design; in fact this is somewhat optimistic since the offline filter used results from full event reconstruction. The accepted cross-section for Bhabhas in Super*B* is approximately 50 nb (Note: to be checked). At the Super*B* design luminosity of 10^{36} cm^{-2}sec^{-1} these two components add up to 70 kHz L1-accept rate without backgrounds. Scaling the beam backgrounds from *BABAR* we assume 30 kHz of background-related L1 accepts, resulting in a total of 100 kHz. Since

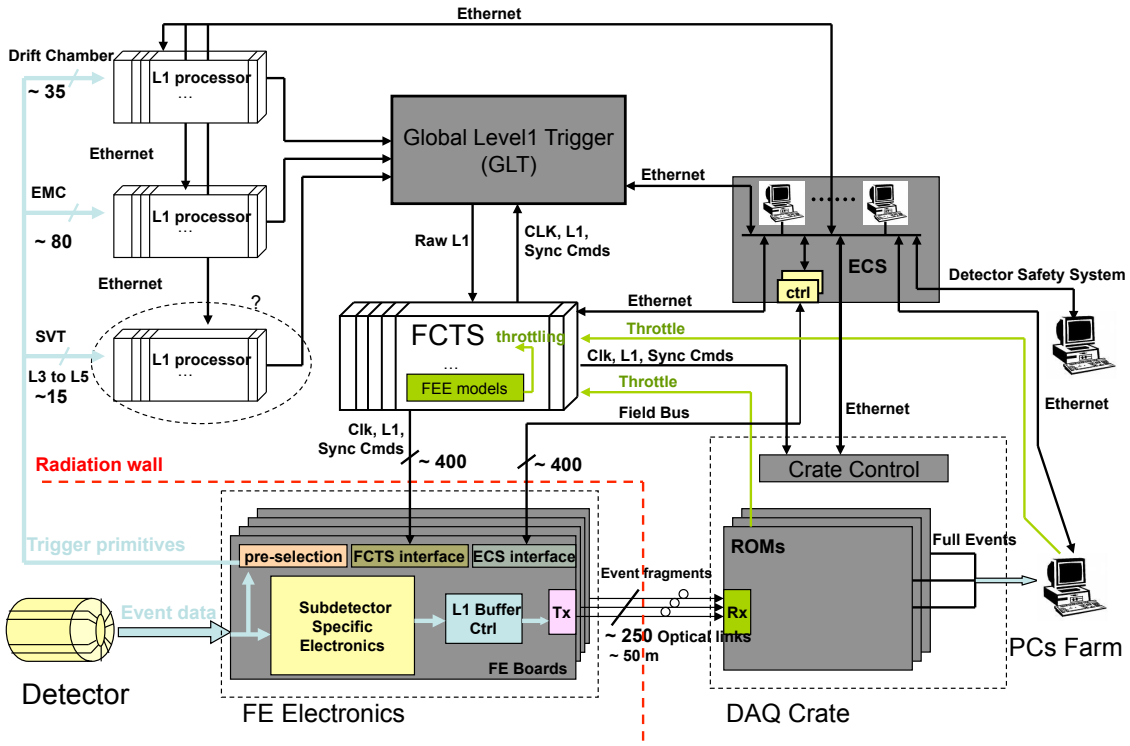


Figure 11.2: Overview of Level-1 Trigger, FCTS, FEE and ROMs. Note: Figure needs to be updated!

a Bhabha veto at L1 is not part of the Super*B* baseline trigger design, this is the minimum rate the readout system has to handle. By adding a *BABAR*-like reserve of 50% to both accomodate the possibility of higher backgrounds then design (e.g. during machine commissioning), and the possibility that the machine exceeds its initial design luminosity, we obtain the Super*B* design rate of 150 kHz of L1-Accepts.

The event size estimates still have some uncertainties. Raw event sizes (between front-end electronics and ROMs) are understood well enough to determine the number of data links required. However, neither the algorithms that can be safely employed in the HLT (or possibly in the ROMs) for data size reduction (such as zero suppression or feature extraction) nor their specific performance for event size reduction are yet known. Based on initial estimates for the SVT and the calorimeter, we assume an event size of 500 kbyte before the HLT that can be reduced in the HLT to 200 kbyte for permanent logging.

11.1.3 Dead Time and Buffer Queue Depth Considerations

SL + DB + UM

The readout system is required to handle the maximum average rate of 150 kHz and to absorb the expected instantaneous rates, both without incurring dead time of more than 1% under normal operating conditions at design luminosity[2]. Dead time is generated and managed centrally in the FCTS based on feedback ("fast throttle") from the FEE by dropping valid L1 trigger requests that do not fit into the readout system's

[2]The 1% dead time specification does not include events that are lost due to individual sub-detector's intrinsic dead times or the L1 trigger's limitations in separating events that are very close in time.

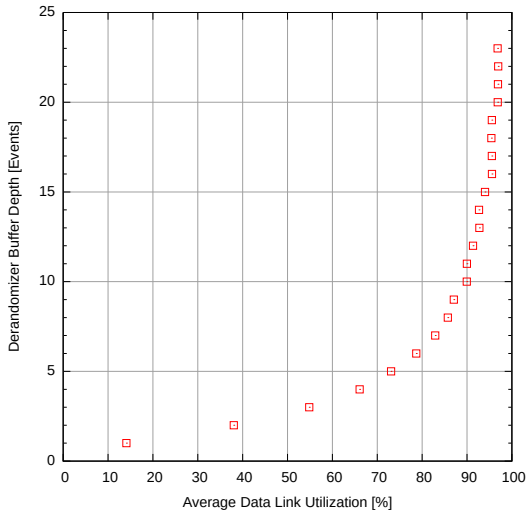


Figure 11.3: Minimum derandomizer buffer depth required to keep the event loss due to "derandomizer full" below 1% as a function of the average data link utilization.

envelope for handling of average or instantaneous L1 trigger rates.

The average rate requirement determines the overall readout system bandwidth; the instantaneous trigger rate requirement affects the FCTS, the data extraction capabilities of the front-end-electronics, and the depth of the derandomization buffers. The minimum time interval between bunch crossings at design luminosity is about 2.1 ns—so short in comparison to detector data collection times that we assume "continuous beams" for the purposes of trigger and FCTS design: The inter-event time distribution is exponential and the instantaneous rate is only limited by the capability of the L1 trigger to separate events in time. Therefore, the burst handling capability of the system (i.e. the derandomization buffer size in the FEEs) is determined by the average L1 trigger rate, minimum time between L1 triggers, and the data link occupancy between the FEEs and the ROMs. Figure 11.3 is based on a simple simulation of the FCTS and FEE of a typical subdetector and shows the minimum buffer depth that is required to keep the event loss due to a full derandomization buffer below 1% as a function of the data link utilization. In the system design, we will target a link utilization of 90% which will require the derandomizer buffers to be able to hold a minimum of 10 events. Additional derandomizer capacity will be required to absorb triggers generated while the fast throttle signal is propagated from the CFEE to the FCTS.

11.2 Electronics in the SuperB Radiation Environment

DB + ?

The high luminosity of the machine and the presence of numerous massive elements close to the interaction region will generate much higher levels of radiation than in *BABAR*, where radiation effects on digital read-out electronics had only been observed after the introduction of FPGAs on the end plate of the drift chamber.

In Super*B* a large flux of charged particles and photons originating from the interaction point and the beam pipes will cross the detector, generate large numbers of secondary neutrons as well.

Therefore a common general radiation policy has been set up at the ETD level.

Long term radiation effects are of two types (ionizing and non-ionizing), while short term effects are linked to instantaneous ionization (Single Events). Radiation levels have been simulated, and Total Ionizing Doses (TID) range from 5kGy down to a few Gy depending on the electronics location. The neutron fluence is required to estimate the effect of the Non-Ionizing Energy Loss (NIEL) and is still under study.

Shielding of the sensitive parts of the detector like electronics is a key point of the design, which has been carefully studied. However, all electronics located on the detector have to be able to handle not only the damages linked to TID and NIEL, but also to present the smallest sensitivity to Single Event Upsets (SEUs), thanks to the intensive use of mitigation techniques like triple modular redundancy (TMR) for the latches and flip-flops and of safety codes (like parity bits) for data stored in memories.

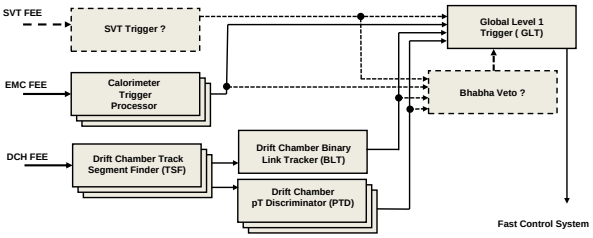


Figure 11.4: Level 1 Trigger Overview

All the components used will be validated for their proven capacity to handle the integrated dose and NIEL foreseen. Power supplies are also designed specifically in order to perform safely in the radiative environment. The architecture of the system has been designed in such a way to reduce as much as possible the risk of failure, especially concerning the critical elements linked to experiment control and readout. In case of failure despite all these precautions, misfunctionning will be detected, experiment control system will be immediately warned, and a fast recovery strategy will be deployed in order to limit as much as possible the dead-time due to these radiation effects.

11.3 Trigger and Event Data Chain

The systems in the trigger and event data chain manage event selection, event filtering and end-to-end data flow from the detector to the intermediate buffer.

11.3.1 Level-1 Trigger

PB (+ SL?)

The current baseline for the L1 trigger is to re-implement the *BABAR* L1 trigger with state-of-the-art technology. It would be a synchronous machine running at 59 MHz (or multiples of 59 MHz) that processes primitives produced by dedicated electronics located on the front-end boards or other dedicated boards of the respective sub-detector. The raw L1 decisions are sent to the FCTM boards which applies a throttle if necessary and then broadcasts them to the FEEs and the ROMs. The standard chosen for the crates would most likely be either ATCA for Physics (Advanced Telecommunications Computing Architecture) for the crates and the backplanes, or a fully custom architecture.

The main elements of the L1 trigger are shown in Fig. 11.4 (see [8] for detailed descriptions of the *BABAR* trigger components):

Drift chamber trigger (DCT): The DCT consists of a track segment finder (TSF) , a binary link tracker (BLT) and a p_t discriminator (PTD). The DCT also extrapolates tracks to the IP; this allows to remove backgrounds that do not originate from the IP.

The layout of the DCT is shown in Fig. 11.5. Track finding is implemented in two stages: In the first stage, the algorithm locally searches for track segments exploiting the data available at the front-end level. The second stage links the track segments and searches for complete tracks.

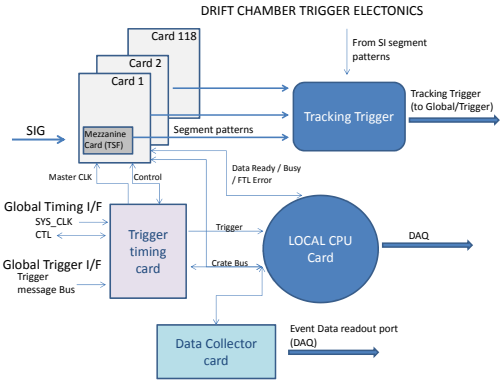


Figure 11.5: DCT Overview

Local Segment Finding: Two options are under discussion as DCH front-end (FE). In the first option time and charge are measured using FADCs and TDCs. A second option is instead based on a cluster counting technique. Granularity is 64 channels per FE in the first case and 16 channels per FE in the second. In the first

case data delivered by the FE will be gathered by a single board on the FE crate and an optical link will connect the crate with the trigger crate. In the other option the DCH electronics has a modularity of 64 channels distributed on 4 contiguous radial planes. This geometry defines the super layer. Table 11.1 shows the super-layer composition for the DCH and the FE cards necessary for its data acquisition. The track segment finder is partially integrated in the DCH front-end.

The TSF will be implemented either at the crate level or at the mezzanine level; the number of optical links and TSFs will be 118 in the case of ADC/TDC-based DCH electronics or equal to the number of DCH front-end crates in the case of cluster counting. With cluster counting, data delivered by the FE will be gathered by a single board in the FE crate and sent to the trigger processor via an optical link.

Each card reads a set of super cell, and each signal will be properly stretched to accommodate at least one drift time. The TSF takes decisions at a programmable rate which can be as high as 59 MHz. A possible track segment is shown in Fig. 11.6.

A pattern needs 3 hits to be taken in consideration. The TSF delivers a bit stream to the following DCH stage, whose dimension depends on sampling frequency. This bit stream represents the ϕ of the segment in the super cell. These data are delivered to the trigger crate. To avoid efficiency losses a small number of contiguous channels is collected by all the neighboring cards. It is relevant in this scheme to optimize the sampling frequency as a function of track efficiency and exploited bandwidth.

Transmission links: We will use high speed serial links to deliver trigger data to the trigger crate. Therefore signal aggregation delivered by the TSF is made possible, and a single card in the trigger crate has all the data from the pertaining superlayer.

Global Tracking: A simple and efficient tracking algorithm is the Binary Link Track Finder (BLT) developed within the CLEO collaboration. This method starts from superlayer (SL) 2 and moves radially outward combining the TSFs if in the following SL one of the three contiguous TSF is active. The track length varies from the first to the last super layer. It is possible to implement a majority logic function of machine background. Track charge does not affect the algorithm and it can be implemented on programmable logic. DCT primitives are received by the DCH L1 trigger box. In this crate the optical links exploited by the DCH trigger lines are collected in such a way that each board stores the information of a single SL. A bus with a switch topology interconnects the single boards where the SL information is present with the master where all the DC TSFs are present.

Particle Counter: The BLT outputs are used to count different tracks using a multiplicity logic exploiting also isolation criteria. To define a track we can use associative memory based techniques so that in one clock cycle a pattern can be identified. The very same ASIC can in principle be used to compute the transverse momentum and the perigee parameters of the track. Track counter takes in consideration 4 SL long tracks.

Transverse Momentum: Using TSF positions and their ϕ angle it is possible to measure track multiplicity above a pre-defined threshold and their perigee parameter. The data are delivered to the GLT which on the basis of the trigger tables asserts the trigger.

Electromagnetic Calorimeter Trigger (EMT): The EMT processes the trigger output from the calorimeter to find energy clusters. From the trigger point of view the electromagnetic calorimeter in the barrel is composed of 24 (8x3) CsI (tl doped) crystal towers.

The EMT layout is shown in Fig. 11.7.

The number of crystals in the barrel is 5760 this implies that the trigger box will handle 240 modules (trigger lines) in the barrel. At the moment we are thinking to divide the end-cap in 5x5 crystal tower this would imply a maximum of 60 towers. Two different strategies are under study. In the first strategy the analogic sum is computed using the information of the

	Sl1	SL2	SL3	SL4	SL5	SL6	SL7	SL8	SL9	SL10	TOT
Planes	4	4	4	4	4	4	4	4	4	4	
Type	A	A	U	V	U	V	U	V	A	A	
n. wires	736	864	496	560	624	688	752	816	896	960	7392
n. TSF	12	14	8	9	10	11	12	13	14	15	118
n. BCD	1	1	1	1	1	1	1	1	1	1	10

Table 11.1: DCH superlayer (SL) and wire readout

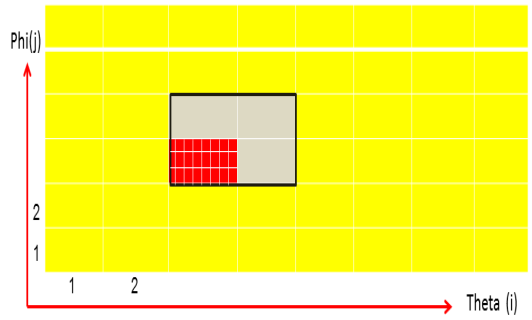


Figure 11.8: EMT trigger tower layout

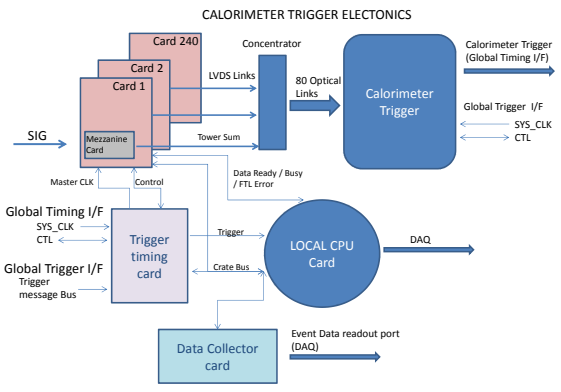


Figure 11.7: EMT Overview

same pre-amp used by the front-end. The other strategy foresees to endow each crystal with independent photon detectors (SiPm). The signal delivered by the SiPm is analogically added up at the tower level. The output can be calibrated using a look-up table and the sum can be encoded and delivered exploiting an LVDS link to an electro-optical converter shielded by radiation.

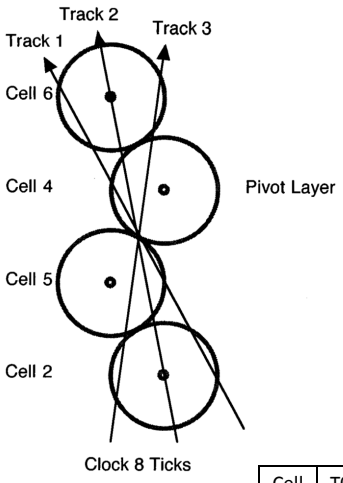
Particle Finders: Global cluster formation The energy can be released on several contiguous towers, therefore, as shown in Fig. 11.8 to assert the trigger signal we'll consider neighboring towers. Towers are scanned and their energy added if a release above a threshold of interest is exceeded in neighbouring towers.

As in Bbar, there will be 3 separate energy thresholds for clusters in the trigger: M cluster (above a low energy consistent with a minimum ionizing), G cluster (above 500-600 MeV) and cluster (electron Bhabha). The thresholds are all programmable. The Bhabha can be vetoed or pre-scaled. This algorithm will be implemented by the L1 EMT processor.

Particle Counters: Since clusters can be dynamically defined this allows to apply isolation cuts on particle definition.

L1 DCT and EMT trigger processors: A crate based on VME or ATCA technology will host L1 processors. These processors will be based on FPGA technology and have the same optical and electrical interfaces. They will differ by the firmware they run. Track finding and dynamic super-cluster definition will be implemented on the L1 processor backplane.

Global Trigger (GLT): The GLT processor combines the information from DCT and EMT (and possibly other inputs such as a Bhabha veto) and forms a final trigger decision that is



Cell	T0	1	2	3	4	T0	1	2	3	4	T0	1	2	3	4
6	0	0	0	1	2	0	1	2	3	0	0	0	0	1	2
4	0	0	0	1	2	0	0	0	1	2	0	0	1	2	3
5	0	0	0	1	2	0	0	0	1	2	0	0	1	2	3
2	0	0	0	1	2	0	1	2	3	0	0	0	0	1	2
	Track 1					Track 2					Track 3				

Cell	T0	1	2	3	4	5	6	7	8	T0	1	2	3	4	5	6	7	8	T0	1	2	3	4	5	6	7	8
6	0	0	0	0	0	1	2	3	4	0	1	2	3	4	5	6	7	0	0	0	0	0	0	1	2	3	4
4	0	0	0	0	0	1	2	3	4	0	0	0	0	0	1	2	3	4	0	0	0	1	2	3	4	5	6
5	0	0	0	0	0	1	2	3	4	0	0	0	0	0	0	1	2	3	0	0	0	1	2	3	4	5	6
2	0	0	0	0	0	1	2	3	4	0	1	2	3	4	5	6	7	0	0	0	0	0	0	1	2	3	4
	Track 1									Track 2									Track 3								

Figure 11.6: Track segment: *BABAR* vs Super*B* output bitstream. In this example we assumed to double babar samplig frequency.

sent to the FCTS. The global trigger receives the information of the detector participating to trigger definition through an optical link. The trigger can be asserted considering the information delivered by the DC and the EMC either separately or combined. This module combines the information of the detectors and compares them to pre-defined criteria. Through the use of an FPGA the trigger can be fully programmable and upgradeable.

Note: This still needs to be updated.

We will study the applicability of this baseline design at Super*B* luminosities and backgrounds, and will investigate improvements, such as adding a Bhabha veto to the L1 trigger. We will also study faster sampling of the DCH and the impact of the forward calorimeter design choice.

For the barrel EMC we will need to study how the L1 trigger time resolution can be improved and the trigger jitter can be reduced compared to BaBar. In general, improving the trigger event time precision should allow a reduction in readout window and raw event size. The L1 trigger may also be improved using larger FPGAs (e.g. by implementing tracking or clustering algorithm improvements, or by exploiting better readout granularity in the EMC).

L1 Trigger Latency: The *BABAR* L1 trigger had 12 μs latency. However, since the size, and cost, of the L1 data buffers in the sub-detectors scale directly with trigger latency, it should be substantially reduced, if possible. L1 trigger la-

tencies of the much larger, more complex, ATLAS, CMS and LHCb experiments range between 2 and 4 μs, however these experiments only use fast detectors for triggering. Taking into consideration that the DCH adds an intrinsic dead time of about 1 μs and adding some latency reserve for future upgrades, we are currently estimating a total trigger latency of 6 μs (or less). More detailed engineering studies will be required to validate this estimate.

Monitoring the Trigger: To debug and monitor the trigger, and to provide cluster and track seed information to the higher trigger levels, trigger information supporting the trigger decisions is read out on a per-event basis through the regular readout system. In this respect, the low-level trigger acts like just another subdetector.

11.3.2 Fast Control and Timing System

DC + CB + DB + SL

The Fast Control and Timing System (FCTS) manages all elements linked to clock, trigger, and event readout, and is responsible for partitioning the detector into independent sub-systems for testing and commissioning. Fig. 11.10 shows how the FCTS is connected to the L1 trigger, FEE, ROMs and HLT. Note: Merge content of Fig. 11.10 and Fig.11.9

The FCTS will be implemented in a crate where the backplane can be used to distribute all the necessary signals in point-to-point mode. This permits the delivery of very clean synchronous signals to all boards—avoiding the use of external cables. The Fast Control and Timing Module (FCTM, shown in Fig. 11.11) provides the main functions of the FCTS:

Clock and Synchronization: The FCTS synchronizes the experiment with the machine and its bunch pattern, distributes the clock throughout the experiment, buffers the clock, and generates synchronous reset commands.

Note: We somewhere need to discuss "synchronization" in more detail, here some potential topics:

- Describe dedicated clock distribution
- Fixed-latency implementation in FPGA (verify) - can't forget this!
- Timing of the various delays during commissioning so that the analog signals are placed correctly within the readout windows. Where is the adjustable delay? On the sender side or the receiver side (i.e. subdetector). DC proposes receiver (it's a per-subdetector thing. Also could potentially adjust latency buffer depth in FEE + adjust phase). What is the hardware support needed in CFEE to measure the offset. Is there a common implementation? Probably not, FEE will have to deal with this problem.
- The ability to reset all clock dividers and state machines in the (C)FEE at system initialization to ensure that divided versions of the 59MHz global clock and state machines are also "in phase". This probably needs some sort of a "reset" or "sync" command to be broadcast to all FEE in a partition via the clock/command link.
- Protocol to detect, report and recover from "loss of lock" in CFEE. Return path of command link (also used for fast throttle) for reporting? Can we recover an individual channel / channel group or do we need to globally reset / resync the detector?

Trigger Handling and Throttling The FCTS receives the raw L1 trigger decisions, throttles them as necessary, generates readout commands and broadcasts them to the FEEs and the ROMs.

Note: We need a discussion of the implementation of a fast throttle. Some issues

- The FCTS needs one bit per subdetector to do the fast throttle
- Aggregation of throttles from different front-end boards within one subdetector is not subdetector-specific

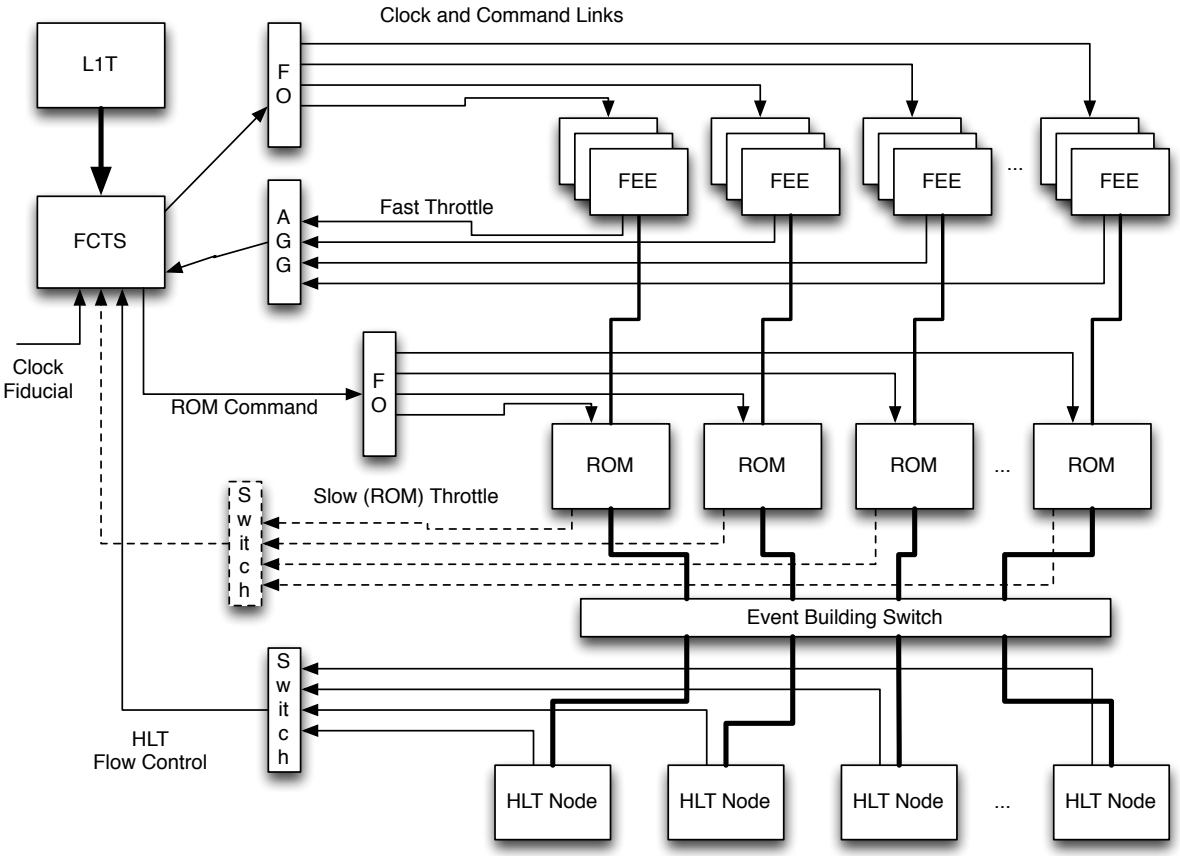


Figure 11.9: Overview of L1T/FCTS/ROM/HLT integration Note: Merge with previous figure

- For diagnostic purposes it is mandatory that we record which front-end board throtteled when ("Logic analyzer on the throttle lines")
- need to define throttle latency (depends on derandomizer depth) - should be as fast as possible to be able to utilize the derandomizer as efficiently as possible (i.e. where do we set the "almost full" level?)

L1-accept Command Format and Distribution The commands broadcast to the FEE have a strict fixed-latency requirement and are as simple and short as possible to minimize the achievable temporal inter-command spacing during transmission and the amount of decoding required in the FEE. We foresee a parity-protected 16-bit command word that contains 8 bits of command code and parameters and 8 bits of an event tag counter. The FEEs are required to include the FEE command word with each event fragment they send to the ROMs.

The commands distributed to the ROMs have no fixed-latency constraint. In addition to a copy of the command word sent to the FEEs they contain at least an event timestamp (56 bits), the full trigger word (32 bits) and the HLT destination node (10-12 bits). Additional information such as a per-run event counter or the time since the last trickle injection pulse in the HER or LER might be included in the ROM command word as well. Since latency is variable, the ROM commands can be derandomized before transmission so that the ROM command links only needs to sustain the average rate (150kHz) of ROM commands.

FEE and ROM commands are sent in the same order (parallel pipelines). Suitable ways of

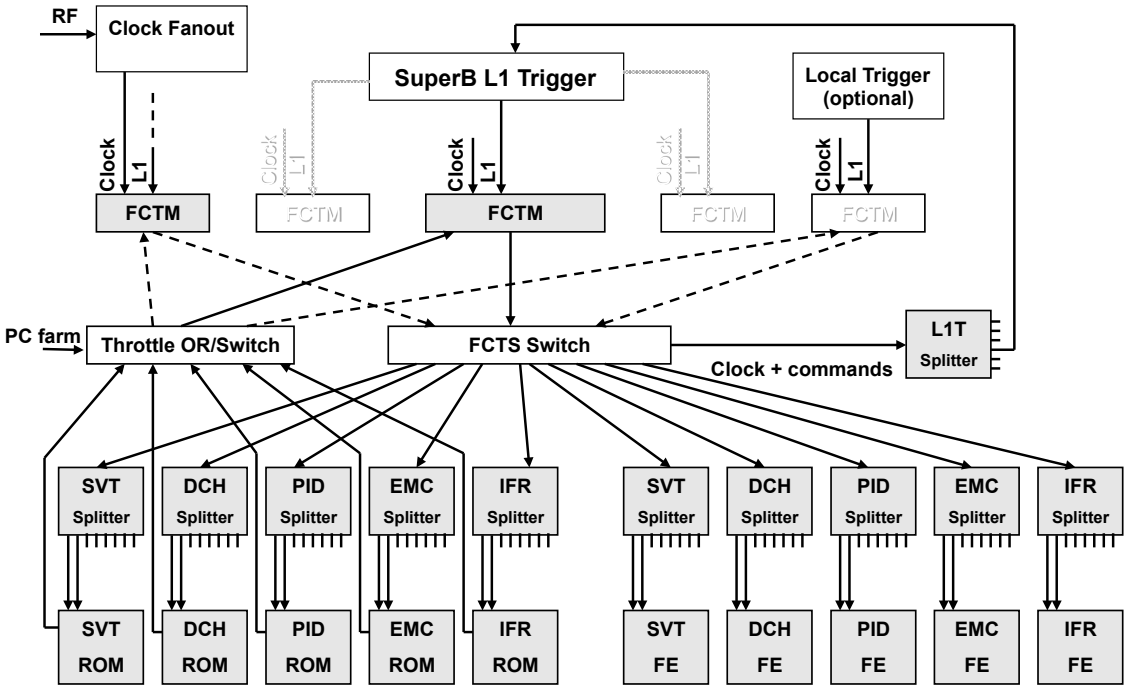


Figure 11.10: Fast Control and Timing System

handling lost or corrupted FEE commands will have to be developed, however this will depend on the detailed failure modes of clock distribution and command links.

Event Management: The FCTS generates unique event identifiers, manages the assignment of events to nodes in the HLT farm and uses a per-node sliding window protocol to load-balance the HLT farm and to stop sending events to unresponsive HLT farm nodes. To do this, the FCTS manages a per-node counter of events it is still allowed to send to this node. A node's counter gets decremented with each event sent to that node. The FCTS determines the next destination node by searching for the next non-zero counter. Every HLT node asynchronously sends generic "event requests" with the number of events it is willing to take — when the FCTS receives such a request from a node it updates the corresponding counter with the value contained in the request. The ROM/HLT/FCTS protocol is described in more detail in the network event builder section below.

For an Ethernet-based event building network it is unlikely that we will need to batch events into multi-event-packets (MEPs), but the system does not preclude the addition of an MEP scheme. This might be required to send overlapping events to the same HLT node or to accomodate a non-Ethernet event building network that would require transmission of data in significantly larger units.

To generate an MEP, the FCTS would simply send the same HLT destination address for subsequent events which would then be packed into the same MEP (the packing can in fact be determined by the individual ROM). Sending a ROM command with a new HLT destination will then close the current MEP and open a new one.

Handling the event distribution with the help of the FCTS minimizes the intelligence required in the ROMs.

The FCTS also keeps track of all its activity, including an accounting of triggers lost due to FEE throttling or other sources of trigger inhibits.

Calibration and Commissioning: The FCTS can trigger the generation of calibration pulses and flexibly programmable local triggers for calibration and commissioning.

Note: How do we handle the EMC source calibration where by definition a meaningful global calibration trigger can not be constructed.

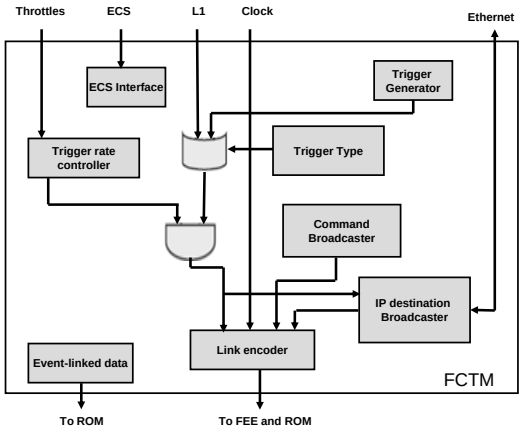


Figure 11.11: Fast Control and Timing Module

The FCTS crate includes as many FCTM boards as required to cover all partitions. One FCTM will be dedicated to the unused subsystems in order to provide them with the clock and the minimum necessary commands.

Two dedicated switches are required in order to be able to partition the system into independent sub-systems or groups of sub-systems. One switch distributes the clock and commands to the front-end boards, the other collects throttling requests from the readout electronics or the ECS. These switches can be implemented on dedicated boards, connected with the FCTMs, and need to receive the clock. To reduce the number of connections between ROM crates and the global throttle switch board, throttle commands could be combined at the ROM crate level before sending them to the global switch.

11.3.3 Control and Data Links

AA et al

Note: This section will contain a comprehensive discussion of the SuperB options for control and data links. An overall discussion of "system integration and error handling" as it pertains to the Super*B* data chain will be in a separate section since it needs to be implemented across multiple sytems, i.e. Clock, FCTS, FEE, Links, ROM and maybe even event builder and HLT.

Requirements

- brief discussion of clock latency, bandwidth, protocol
- request for off-the-shelf solution (no new VLSI design)

Radiation Tolerance Issues

- recall of the SuperB rad environment Note: general aspects should go into ETD rad section
- brief description of tested off-the-shelf components
- most promising devices: National DS92LV18, Xilinx Virtex 5
- discussion of test results normalized to 1 kGy dose due to p@62MeV
- brief discussion of adopted SEU moderation techniques in FPGA (TMR, scrubbing, placement hardening, ...) Note: techniques should go to ETD rad section, specific application in tests goes here

Physical Implementation

- the mezzanine approach
- advantages for design, test, maintenance and upgrade
- link design fully decapled from logic design

Control and Data Links

- very likely based on the same technology
- GOL as a backup solution for Data links

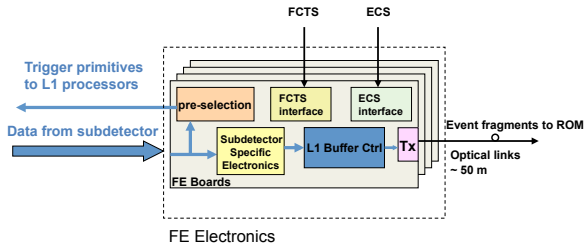


Figure 11.12: Common Front-End Electronics

11.3.4 Common Front-End Electronics

JM + DB

In our opinion it would be beneficial to separate the functions required to drive the front-end electronics by using dedicated independent elements for the implementation of the different functions. These elements could be implemented as mezzanines or as circuits directly mounted on the front-end modules (considered here as carrier boards). For instance, as shown in Figure 11.12, one mezzanine should be used for FCTS signals and commands decoding, and one for the ECS management. Depending on the implementation of the FEE, it could also be useful to decode the FCTS and ECS signals on one mezzanine and to distribute them to the neighbouring boards. This would permit a gread reduction in the number of links. Driving the L1 buffers may also be implemented in a dedicated common control circuitry which may be implmented inside a radiation-tolerant FPGA. This circuitry would have to handle the L1 accept commands and provide the signals necessary to control the reading of the latency buffer and the writing/transmitting of the proper event buffer. The latency buffers could be implemented either in the same FPGA or directly on the carrier boards, and one such single circuit could be able to drive numerous data links in parallel, thus reducing the amount of electronics on the front-end.

Said control circuit would also have to deal with the potential pile-up of events and (if implemented) the possibility to go back in time after a rejected Bhabha event for the subdetectors affected, without forgetting the handling of the fast multiplexer feeding the optical link serializer.

Another important advantage of this solution is that it permits the alternative of implementing an analog L1 buffer inside an ASIC. Then the only (potentially non-trivial) constraint is that the analog output of the ASIC has to be able to drive an internal or an external ADC at a 59 MHz rate in order to keep the synchronization with the rest of the system. It may be feasible to relax this rate constraint by parallelizing slower ADCs.

Serializers and link optical drivers should also reside on the carrier boards, mainly for mechanical and thermal reasons. Figure 11.12 shows a possible implementation of the L1 buffers, their control electronics and the outputs towards the optical readout links. The control electronics may sit within a dedicated FPGA. Both digital and analog buffer types are shown.

Another important requirement is that all (rad-tolerant) FPGAs in the FE have to be reprogrammable without dismounting a board. This could be done through dedicated front panel connectors, which might be linked to numerous FPGAs, but it would be of great help if this could be done through the ECS system without any manual intervention on the detector side.

11.3.5 Read-Out Modules

MB + UM

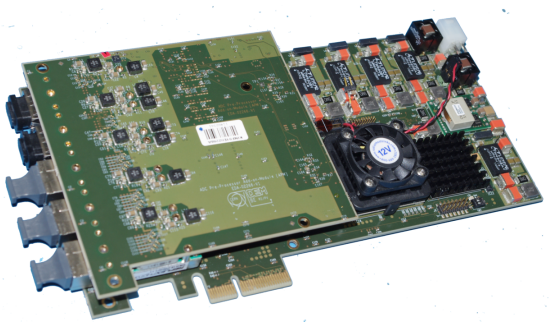


Figure 11.13: Readout Module

The Readout Modules (ROM, Fig. 11.13) are the hardware interfaces between front-end electronics and the (software based) event builder.

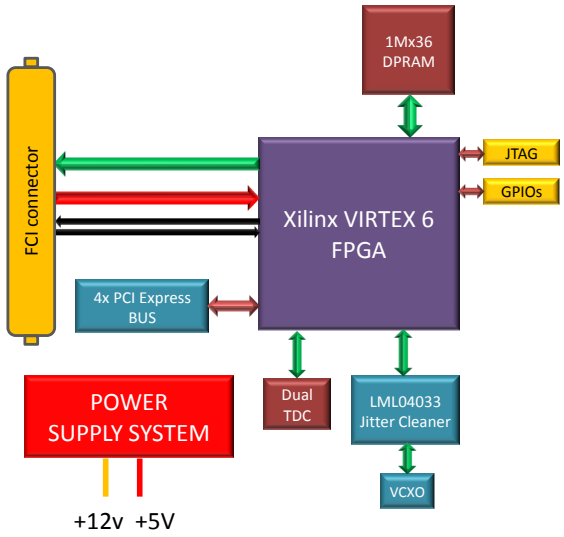


Figure 11.14: ROM block diagram – without optical adapter

ROMs map the synchronous world of FCTS-disciplined hierarchy to the asynchronous domain of the event-building computing farm. Their processing flow starts by receiving event fragments from the sub-detectors' front-end electronics and continues with cross-checking front-end identifiers and absolute time-stamps, buffering them in de-randomizing memories, performing processing (still to be defined) on the fragment data, and eventually injecting the formatted fragment buffers into the event builder and HLT farm. Connected to the front-end electronics via optical fibers, they will be located in an easily accessible, no radiation area. The ROM design will be unique for all sub-detectors and the peculiarities of each sub-detector will be addressed by customization of the ROM firmware. A ROM will have 10 or more optical input channels at a rate of 1 Gbit/s and at least one output channel at 10 Gbit/s. To exploit flexibility and processing power of computer technology, ROM will be manufactured as PCI Express based add-on cards for servers of the event-building farm. This solution will help keeping production costs low (when compared to a field-bus based solution) and opens a new scenario of a mixed hardware-software processing scheme for fragment data; unforeseen changes and upgrades can also be addressed with a low impact on the whole architecture.

A prototype ROM has been manufactured and qualified, in order to assess the suitability of this approach. The prototype ROM is a PCI Express 2.0 based add-on card (Fig. 11.13) based on a Xilinx Virtex6-250T FPGA with 48 high speed serial transceivers. The plug-in module accommodates 3 SNAP12 optical receivers and 2 QSP optical transceivers for a total of 44 receivers and 8 transmitters each operating at max 6.2 Gbit/s. A 8 Mbyte true dual-port ram acts as de-randomizing memory for incoming fragments, while waiting to be streamed to host server memory.

The prototype ROM features a TDC and a ultra-low jitter PLL for the benefit of FPGA (Fig 11.14). A 4x PCIE 2.0 interface with an aggregate bandwidth of 20 Gbit/s per direction allows fragment data to be moved to host memory efficiently. To check worst-case power consumption, the FPGA has been configured with 38 input channels at 2.0 Gbit/s, 38 eight FIR filters for data processing, a 10 Gbit/s PCI-express interface, a scatter-gather DMA engine and a timing unit for a total of 92% occupancy of logic resources; consuming approximately 60W, no precaution has been taken for cooling when housed on a low cost 2U Dell server. By means of a custom developed Linux driver we have exercised the data transfer from the ROM dual-port RAM and the host memory; the driver addresses the custom designed scatter-gather DMA engine in the FPGA to efficiently move the fragment data from the ROM directly into user-space buffers; the driver avoids copying data from kernel address space to user address space by handling the map between Unix virtual memory pages and server physical memory regions, tunneling data from ROM dual-port RAM to user-space declared data vectors. Bandwidth tests show that fragment buffers larger than few tenths of Kbytes can be moved at a rate of approximately 950 Mbyte/s in the aforementioned configuration (4x PCIE 1.1), while almost doubling at 4x PCIE 2.0 (with a 256 bytes PCI-E payload).

Test results of the prototype ROM outperform requirements in the foreseen deployment and this gives us confidence that this approach can be safely adopted.

11.3.6 Network Event Builder

SL

The ROMs receive event fragments in parallel from the sub-detector front-end-electronics, perform a first stage event-build, store the event fragments in memory buffers and combine them with the corresponding ROM command word received from the FCTS (over the dedicated ROM-command links). The resulting event fragments are then encapsulated into UDP datagrams and sent to the HLT node determined by the destination node field in the ROM command word. Thus, all fragments of a given event are sent to the same HLT node. The HLT nodes complete the event building process by combining all fragments of an event and passing the full events to the HLT processes through a queue.

As described above, the FCTS determines the HLT destination node for every event using a round-robin algorithm that is tuned by a simple flow control scheme based on generic requests and sliding windows: Each HLT node maintains a queue of fully built events that is filled by the event building process and drained by the HLT processes. As long as the event building process is running and the number of events in this queue stays below a high-water mark, the HLT node periodically sends "generic" requests for more events to the FCTM active for the current partition. These requests are sent over Ethernet; the aggregate rate of the requests can be limited to a fraction of the L1-accept rate, since each request is for multiple events.

If the HLT processes on a node cannot keep up with the incoming events, the node will stop sending requests and after the FCTM has exhausted the node's window of outstanding events, no more events will be directed to the node. Only after the FCTM receives a new event request from the node, it will consider it as a valid event destination again. No events are lost, since the node will queue the outstanding events. This provides a flow-control and load balancing mechanism for the HLT farm. In case of a complete HLT node failure (or the failure of the event building process) the event loss is less or equal to the number of events last requested.

The event building process is inherently parallel and its rate can be scaled up as needed (up to the bisection bandwidth of the event building network). The baseline technology for the event builder network is standard 10 Gbit/s Ethernet. We will investigate the suitability of end-to-end flow control mechanisms (such as IEEE 802.1Qbb) at the Ethernet layer for avoiding packet loss in the event building network. We will also investigate alternative network technologies and protocols (such as RDMA or Infiniband).

With a L1 trigger rate of 150 kHz and a pre-HLT event size of 500 kbyte, the bandwidth in the network event builder is about 75 Gbyte/s, corresponding to about 750 Gbit/s with network overhead included. To avoid packet loss and to maintain stability, the event building network cannot be operated at an utilization of 100%, so we retain an additional safety factor of ~1.5. Thus, the minimum bisection bandwidth required in the event building network is 1200 Gbit/s. When implemented with 10 Gbit/s Ethernet, this means 120 "source" network interfaces on the ROMs and at least 120 "destination" interfaces on the HLT nodes. Network switches that provide the necessary bandwidth and can host at least $120 + 120 = 240$ 10 Gbit/s Ethernet ports are commercially available at the time of the writing of this document.

11.3.7 High-Level Trigger Farm

SL

The HLT farm needs to provide sufficient aggregate network bandwidth and CPU resources to handle the full Level 1 trigger rate on its input side. The Level 3 trigger algorithms should operate and log data entirely free of event time ordering constraints and be able to take full advantage of modern multi-core CPUs[3]. Ex-

[3] The simplest implementation would be to run multiple identical HLT threads or processes which get their input from a single queue of built events.

trapolating from *BABAR*, we expect 10 ms core time per event to be more than adequate to implement a software L3 filter, using specialized fast reconstruction algorithms. With such a filter, an output cross-section of 25 nb should be achievable. Using contemporary (as of Spring 2012) hardware and taking into account the CPU overhead for event building, logging and data transfer, a suitable farm could be implemented with approximately 150 nodes.

Level-4 Option To further reduce the amount of permanently stored data, an additional filter stage (L4) could be added that acts only on events accepted by the L3 filter. This L4 stage could be an equivalent (or extension) of the *BABAR* offline physics filter—rejecting events based either on partial or full event reconstruction. If the worst-case behavior of the L4 reconstruction code can be well controlled, it could be run in near real-time as part of, or directly after, the L3 stage. Otherwise, it may be necessary to use deep buffering to decouple the L4 filter from the near real-time performance requirements imposed at the L3 stage. The discussion in the Super*B* CDR [1] about risks and benefits of a L4 filter still applies.

11.3.8 Data Logging

SL + ?

The output of the HLT is logged to disk storage. We assume at least a few Tbyte of usable space per farm node, implemented either as directly attached low-cost disks in a redundant (RAID) configuration, or as a storage system connected through a network or SAN. We do not expect to aggregate data from multiple farm nodes into larger files. Instead, the individual files from the farm nodes will be maintained in the downstream system and the bookkeeping system and data handling procedures will have to deal with missing run contribution files. A switched Gigabit Ethernet network separate from the event builder network is used to transfer data asynchronously to archival storage and/or near-online farms for further processing. It is not yet decided where such facilities will be located, but network connectivity with adequate bandwidth and reliability will need to be provided. Enough local storage must be available to the HLT farm to allow data buffering for the expected periods of link down-time.

Assuming that the HLT accepts a cross-section of about 25 nb leads to an expected event rate of 25 kHz at a luminosity of 10^{36} $\mathrm{cm}^{-2}\mathrm{sec}^{-1}$, or a logging data rate of ~5 Gbyte/s.

While the format for the raw data has yet to be determined, many of the basic requirements are clear, such as efficient sequential writing, compact representation of the data, portability, long-term accessibility, and the freedom to tune file sizes to optimize storage system performance.

11.4 System Integration and Error Handling

AA, SC, SL, DC, UM, DB and others

Description of system integration aspects, error-tolerant designs, error detection, fast (downtime-free?) recovery, etc. Participation of multiple sub-systems (Clock?, FCTS, FEE, ROMs, HLT?) is required, so this becomes a separate section.

- evaluation of link failure rate in SuperB assuming 1000 links
- failure IS an option: analysis and recovery strategies
- need for a 'fault-tolerant' DAQ architecture capable to by design to recover from various fault types (mostly SEU-induced) in the FEE and the control and data links.

11.5 Control Systems

A major lesson learned during *BABAR* operations was that achieving high operational efficiency and true "factory-mode" data taking required a high degree of automation and control system

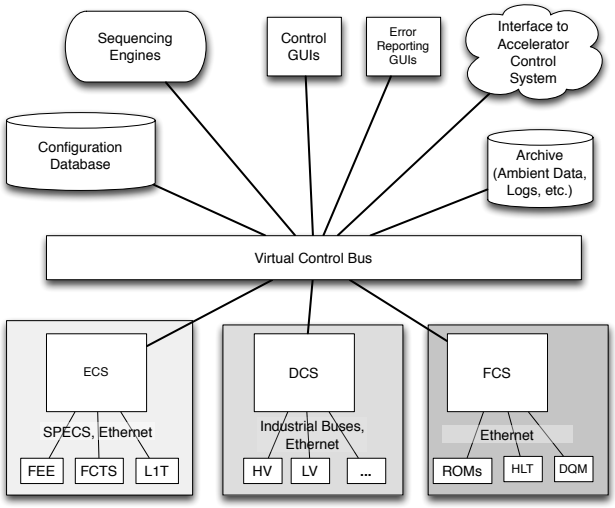


Figure 11.15: The Super$B$ unified control system architecture

integration. The traditional approach of separate control systems for different aspects of the experiment (detector control, run control, farm and logging control) designed and implemented with completely separate tools and very limited capability to communicate with each other, greatly limited the amount of automation and automatic error detection and recovery.

In Super$B$, all routine operations will need to be orchestrated across subsystem boundaries. For example, performing a simple calibration might require high voltages to be ramped to a calibration set-point, the FEE and the FCTS to be configured for calibration, farm nodes to be allocated and configured, the calibration run to be performed, calibration data to be analyzed and after completion the system to be returned to its normal data taking configuration.

For Super$B$ we therefore foresee a unified control system that can automatically perform all routine operations. The system comprises the Electronics Control System (ECS), the Detector Control System (DCS), the Farm Control System (FCS), the configuration database, sequencing engines to implement distributed state machines, an archiving and logging system, operator GUIs and the interface to the accelerator control system. All components are connected by a central virtual control bus ("Global Control System").

All operations are driven by the configuration database and executed under the control of one or more sequencing engine.

A large part of the system, including the central virtual control bus, will be implemented using the !CHAOS [9] control system toolkit which is currently under development for the Super$B$ accelerator. !CHAOS is a state-of-the-art scalable distributed control system framework that combines high-performance data acquisition and archiving capabilities with a plugin architecture to provide low-level controller interfaces and graphical user interfaces (GUIs).

An overview of the unified control system architecture is shown in Fig 11.15; its major components are described below.

11.5.1 Electronics Control System

SL The Electronics Control System (ECS) controls and monitors the FEE, the FCTS and the Level 1 trigger. Its main responsibilities are:

Configuring the Front-ends: Many front-end parameters must be initialized before the system can work correctly. The number of parameters per channel range from a only a few to large per-channel lookup tables. The ECS may also need to read back parameters from registers in the front-end hardware to check the status or verify that the contents have not changed. For a fast detector configuration and recovery turnaround in factory mode, it is critical to not have bottlenecks either in the ECS itself, or in the ECS' access to the front-end hardware.

Calibration: Calibration runs require extended functionality of the ECS: In a typical calibration run, after loading calibration parameters, event data collected with these parameters is sent through the DAQ system and analyzed. Then the ECS loads the parameters for the next calibration cycle into the front-ends and repeats the operation.

Testing the FEE: The ECS is also used to remotely test all FEE electronics modules using dedicated software. This obviates the need for independent self-test capability for all modules.

Monitoring the Experiment: The ECS continuously monitors FEE boards, FCTS and the L1 Trigger to ensure that they function properly. This might include independent spying on event data to verify data quality, and monitoring operational parameters on the boards (such as voltages, currents, temperatures and error flags). By monitoring these parameters, the ECS also participates in protecting the experiment from a variety of hazards[4].

ECS support must be built into all electronics modules that are to be controlled by the ECS – this includes the FEE.

The specific requirements that each of the sub-systems makes on ECS bandwidth and functionality must be determined (or at least estimated) as early as possible so that the ECS can be designed to incorporate them. Development of calibration, test, and monitoring routines must be considered an integral part of sub-system development, as it requires detailed knowledge about sub-system internals.

ECS Implementation: The field bus used for the ECS has to be radiation tolerant on the detector side and provide very high reliability. Such a bus has been designed for the LHCb experiment: it is called SPECS (Serial Protocol for Experiment Control System) [7]. It is a bidirectional 10 Mbit/s bus that runs over standard Ethernet Cat5+ cable and provides all possible facilities for ECS (like JTAG (Joint Test Action Group) and I2C (Inter IC)) on a small mezzanine. It could be easily adapted to the Super*B* requirements. Though SPECS was initially based on PCI boards, it is currently being translated to an Ethernet-based system, as part of an LHCb upgrade, also integrating all the functionalities for the out-of-detector elements. For the electronics located far from the detector, Ethernet will be used for ECS communication. The Super*B* ECS will be implemented using SPECS; an interface to !CHAOS will be developed.

[4] An independent hardware-based detector safety system, which is part of the DCS, must protect the experiment against equiement damage in case the software-based ECS is not operating correctly.

11.5.2 Detector Control System

The Detector Control System (DCS) is responsible for ensuring detector safety, controlling the detector and detector support system, and monitoring and recording detector and environmental conditions. The DCS also provides the primary interface between the accelerator and the detector.

Efficient detector operations in factory mode require high levels of automation and automatic recovery from problems. Here, the DCS plays a key role and a tight integration with the Accelerator Control System (ACS) is hightly desirable. The DCS in conjunction with the ACS manages the accelerator-detector interlocks and beam and detector states and has access to all information from the accelerator and the detector that is needed to fully automate data taking operations.

The DCS-ACS connection is also used to provide the accelerator with beam measurements performed by the detector (such as beam spot positions or bunch-by-bunch luminosities). Operational experience from *BABAR* has shown that mutual access between machine and detector to their respective archived control system data (such as records of background levels, detector currents, trigger rates on the detector side and vacuum pressures, temperatures and stored currents on the machine side) are invaluable for improving the accelerator and detector performance.

The DCS will be implemented with !CHAOS. Due to its distributed nature and modular storage design, !CHAOS will allow us to federate the independent instances of DCS and ACS and provide a unified query interface for data archived by the respective systems.

Low-level components and interlocks responsible for detector safety (Detector Safety System, DSS) will be implemented as simple circuits or with programmable logic controllers (PLCs).

11.5.3 Farm Control System

SL

Processes on the ROMs and on the HLT farm will be started, controlled and monitored by the Farm Control System (FCS) and will be implemented using the !CHAOS framework or a traditional network inter-process communication system such as DIM.

11.6 Other Systems

11.6.1 Data Quality Monitoring System

SL

Event data quality monitoring is based on quantities calculated by the L3 (and possibly L4) trigger, as well as quantities calculated by a more detailed analysis on a subset of the data. A distributed histogramming system collects the monitoring output histograms from all sources and makes them available to automatic monitoring processes and operator GUIs.

11.6.2 Other Components

SL

Electronic Logbook: A web-based logbook, integrated with all major Online components, allows operators to keep an ongoing log of the experiment's status, activities and changes.

Databases: Online databases such as configuration, conditions, and ambient databases are needed to track, respectively, the intended detector configuration, calibrations, and actual state and time-series information from the DCS.

Configuration Management: The configuration management system defines all hardware and software configuration parameters, and records them in a configuration database.

Performance Monitoring: The performance monitoring system monitors all components of the Online.

Software Release Management: Strict software release management is required, as is a tracking system that records the software version (including any patches) that was running at a given time in any part of the ETD/Online system. Release management must cover FPGAs and other firmware as well as software.

Computing Infrastructure Reliability: The Online computing infrastructure (including the specialized and general-purpose networks, file, database and application servers, operator consoles, and other workstations) must be designed to provide high availability, while being self-contained (sufficiently isolated and provided with firewalls) to minimize external dependencies and downtime.

11.6.3 Software Infrastructure

GM + SL

The data acquisition and online system is basically a distributed system built with commodity hardware components. Substantial manpower will be needed to design the software components—taking a homogeneous approach in both the design and implementation phases. An Online software infrastructure framework will help organize this major undertaking. It should provide basic memory management, communication services, and the executive processes to execute the Online applications. Specific Online applications will make use of these general services to simplify the performance of their functions. Middleware designed specifically for data acquisition exists, and may provide a simple, consistent, and integrated distributed programming environment.

11.7 R&D for Electronics, Trigger and Data Acquisition and Online

All

Note: This is copied from the Whitepaper. Needs updating!

The baseline design presented in this chapter can be implemented with technology and components available at the time time of writing of this document. However, we expect that by the times when we have to freeze various aspects of the design to start construction or purchasing, components that are significantly more performant and/or cost effective will be available. In

order to take advantage of these developments, we will need to develop a detailed plan on when we have to finalize the parts of our design.

Data Links: Discuss technology tracking (e.g. LHC Upgrade) here?

Event Builder and HLT Farm: The main R&D topics for the Event Builder and HLT Farm are (1) the applicability of existing tools and frameworks for constructing the event builder; (2) the HLT farm framework; and (3), event building protocols and how they map onto network hardware.

Software Infrastructure: To provide the most efficient use of resources, it is important to investigate how much of the software infrastructure, frameworks and code implementation can be shared with Offline computing. This requires us to determine the level of reliability-engineering required in such a shared approach. We also must develop frameworks to take advantage of multi-core CPUs.

11.8 Organizational Structure of Electronics, Trigger, Data Acquisition and Online

DB + UM + SL

11.9 Conclusions

Copied from the whitepaper. To be reviewed and updated.

The architecture of the ETD system for Super*B* is optimized for simplicity and reliability at the lowest possible cost. It builds on substantial in-depth experience with the *BABAR* experiment, as well as more recent developments derived from building and commissioning the LHC experiments. The proposed system is simple and safe. Trigger and data readout are fully synchronous—allowing them to be easily understood and commissioned. Safety margins are specifically included in all designs to deal with uncertainties in backgrounds and radiation levels. Event readout and event building are centrally supervised by a FCTS system which continuously collects all the information necessary to optimize the trigger rate. The hardware trigger design philosophy is similar to that of *BABAR* but with better efficiency and smaller latency. The event size remains modest.

The Online design philosophy is similar—leveraging existing experience, technology, and toolkits developed by *BABAR*, the LHC experiments, and commercial off-the-shelf computing and networking components—leading to a simple and operationally efficient system to serve the needs of Super*B* factory-mode data taking.

Bibliography

[1] M. Bona *et al.*, *Super*B*: A High-Luminosity Heavy Flavour Factory. Conceptual Design Report*, arXiv:0709.0451v2 [hep-ex], INFN/AE-07/2, SLAC-R-856, LAL 07-15, also available at http://www.pi.infn.it/SuperB/CDR.

[2] B. Aubert *et al.* (*BABAR* Collaboration), *The BABAR Detector*, Nucl. Instrum. Methods Phys. Res., Sect. A **479**, 1 (2002) [arXiv:hep-ex/0105044].

[3] The ATLAS Collaboration, *ATLAS Detector and Physics Performance Technical Design Report*, http://atlas.web.cern.ch/Atlas/GROUPS/PHYSICS/TDR/access.html.

[4] The CMS Collaboration, *CMS Detector Technical Design Report*, http://cmsdoc.cern.ch/cms/cpt/tdr/.

[5] The LHCB Collaboration, *LHCB Technical Design Reports*, http://cmsdoc.cern.ch/cms/cpt/tdr/.

[6] The Belle Collaboration, *The Belle Detector*, Nucl. Instrum. Methods Phys. Res., Sect. A **479**, 117 (2002).

[7] The SPECS Web Page, https://lhcb.lal.in2p3.fr/Specs/.

[8] The *BABAR* Trigger Web Pages, http://www.slac.stanford.edu/BFROOT/www/Detector/Trigger/index.html.

[9] L. Catani *et al. Exploring a new paradigm for accelerators and large experimental apparatus control systems*, ICALECPS 2011, http://accelconf.web.cern.ch/accelconf/icalepcs2011/html/clas013.htm

12 Subdetector Electronics and Infrastructure

Breton/Marconi/Luitz

12.1 Subsystem-specific Electronics

12.1.1 SVT Electronics

The full details of the SVT electronics has been given in chap. **??**. Here we recall the main features relevant for the data collection, trigger distribution, system programming and monitoring.

In the baseline SVT option, the detector will be equipped with double sided silicon strips (or striplets) in all layers. Custom front-end chips will be used to read the detector and transform as soon as possible the analog information of a particle traversing the detector in a digital one, characterized by position (layer, strip), energy deposit (signal time over threshold) and time. At least two different custom chips will be developed to handle separately the first layers (expecially layer 0), characterized by high occupancy and short strips (good signal/noise) and the external layers (layer 4 and layer 5) where the main concern is the length of the strips (worse signal/noise) and not the occupancy. Both front-end chips will have the same digital readout architecture and will present the same interface to the DAQ chain, although with different settings. Possible upgrades of the SVT internal layers might require to move to a pixellated detector, for which a different custom front-end chip will be designed. The digital architecture of the pixel chips, partially already develloped, will be based on the same general readout architecture so that from the point of view of trigger and DAQ system they will share the same interface.

Common characteristics of the chips will be capability to work both in data-push and data-pull mode, the presence of internal buffers to allow for a trigger latency up to 10 μs, the use of a periodic signal to time-tag the recorded hits, the serialized hit output and the chip programmability via (two) digital lines.

The full SVT data chain will therefore be able to provide and distribute all the signals, clocks, triggers, time-tagging signal to all the front-end chips in a system-wide synchronous way.

A sketch of the full data chain is given in Fig. 12.1. Starting from the detector and going to the ROM boards, the chain contains: a) the front-end chips mounted on an HDI placed immediately at the end of the sensor modules; b) wire connections to a transition card (signals in both directions and power lines); c) a transition card, placed about 50 cm from the end of the sensors, hosting the wire-to-optical conversion; d) a bidirectional optical line running above 1 Gbit/s; e) a receiver programmable board (front-end board: FEB).

Each HDI will host from 5 to 14 FE chips servicing a side of the silicon strip module (a so called ROS: Read-Out Section). All the chips will share the same input lines (currently: reset, clock, fastclock, trigger, time-stamp, registerIn) and at least a registerOut line. Programming of the chips can be done individually by addressing

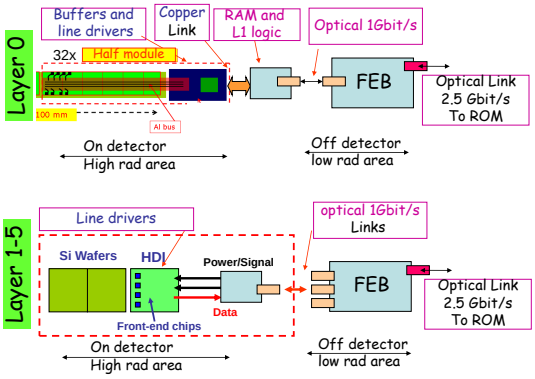


Figure 12.1: SVT Electronics

a sigle chip or via broadcast command sent to all the chips in an HDI. Hits will be serialised on a programmable number of lines (1,2,4 or 6) using the fastclock signal. Each HDI will have a maximum number of 16 output lines running at the fastclock rate.

The role of the transition card is threefold: a) it will distribute the power to the HDI, b) it will receive all the input signals for the front-end chips via the optical line connected to the programmable board and c) it will ship the data to the programmable board for data acquisition. For the inner layers (0-3) there will be a transition card for each HDI. For the outer layers (4-5) it will be possible to group the data of the two HDIs servicing the two sides of the same silicon sensor into the same transition card, reducing in this way the total number of optical links needed.

The received programmable board (FEB) will handle all the comunications with the front-end chips, the FTCS, the ECS and the upper DAQ systems. Each FEB board will be connected to a variable number of transition cards (up to 12 in the current design). Important and critical roles of this board are the clock distribution, the trigger handling and the data collection. The clock-like signals, such as an experiment clock (about 60 MHz), a fast clock (120-180 MHz) and a time-stamping clock (up to 30 MHz), have to be distributed in a system-wide synchronous manner. Special care will be taken to measure at each power-up the latencies of all the serializers and deserializers in the signal and DAQ chain so that the sent signals can be suitably adjusted in phase in order to have a system synchronous at the sensor (or front-end) level. The time-stamping clock will be used to time-tag the hits and can be different for the inner layers, where the high track rate requires short signal shaping times and short daq time windows and outer layers where the long strips and lower track rates allow for a longer shaping times (800 ns - 1 μs) and longer DAQ windows. The estimation of data volumes have been performed assuming a time-stamping of 30 ns period in the inner and outer layers. The acquisition window will be defined in a time window centered around the L1 trigger window and lasting at least 10 time-stamps (300 ns) for the inner layers and 33 time-stamps (990 ns) or more for the outer layers. The trigger request will be sent to the chips via the optical links. The most important function of the board is to collect the data coming out of the front-end chips both for monitoring and for the final daq. The data will be deserialized in the board and the redundant information will be stripped. A possible further data compression can be envisaged in order to reduce the final data volume. Finally the data will be sent-out via an optical link to a ROM module.

Data volumes. As discussed in the SVT chapter, the data rates and volumes are dominated by the background. In the design of the SVT front-end chips and DAQ chain, the latest background Bruno simulations have been considered at the nominal luminosity and a safety factor of 5 has been applied on the simulation results (design inputs). Due to the strong non-uniformity of the particle rate on the sensors, the front-end chip characteristics have been adapted to the peak hit rates, while the data volumes have been extracted from the mean rates for each layer. To evaluate the data rate a 150 kHz trigger rate with 10 μs of maximum latency and 100 ns of time jitter has been considered. An hit size of 16 bits is used as the FE chip output in the calculation that becomes 20 bits during serialization due to the 8b/10b protocol. The bandwidth needed by a layer0 ROS in a data-push configuration is of the order of 20 Gbit/s/ROS. A difficult-to-handle rate that moved us to consider a fully triggered SVT. In table 12.1 for each layer type the mean expected data load is shown.

For events accepted by the L1 trigger, the bandwidth requirement is only 1 Gbit/s and data from each ROS can be transferred on optical links to the front-end boards (FEB) and then to ROMs through the >8 Gbit/s optical readout links.

In total, the SVT electronics requires 18 FEBs and 18 ROMs, 18 optical links at 10 Gbit/s, 172 links at 1 Gbit/s (radiation

Table 12.1: Electronic load on each layer, Readout section and optical link.

Layer	Layer type	chips/ ROS	available channels	Backgnd (MHz/cm^2)	Gbits/trig (per GROS)	FE Boards	Event Size (kB)
0	striplet u	6	768	151	0.99	4	5.3
0	striplet v	6	768	151	0.99	4	5.3
1	strip z	7	896	14.0	0.56	1	2.2
1	strip phi	7	896	16.0	0.64	1	2.6
2	strip z	7	896	9.6	0.54	1	2.2
2	strip phi	7	896	10.3	0.58	1	2.3
3	strip z	10	1280	4.2	0.50	1	2.0
3	strip phi	6	768	3.0	0.36	1	1.5
4a	strip z	5	640	0.28	0.26	1	1.4
4a	strip phi	4	512	0.43	0.38	1	2.0
4b	strip z	5	640	0.28	0.26	1	1.4
4b	strip phi	4	512	0.43	0.40	1	2.1
5a	strip z	5	640	0.15	0.17	1	1.0
5a	strip phi	4	512	0.22	0.24	1	1.5
5b	strip z	5	640	0.15	0.17	1	1.0
5b	strip phi	4	512	0.22	0.24	1	1.5

hard). The average SVT event size is 88 kB, 30% coming only from the layer0.

12.1.2 DCH Electronics

12.1.2.1 Design Goals

The Super$B$ Drift Chamber (DCH) front-end electronics is designed to extract and process the about 8000 sense wire signals to:

- measure the electrons' drift times to the sense wires for the purpose of tracking (momentum of charged particles)
- measure the energy loss of particles per unit of length, dE/dx (particle identification)
- provide hits information to the trigger system (trigger primitives)

Concerning the energy loss measurement two options will be considered. The first one foresees the measurement of the sense wires integrated charge, discarding the highest values to remove the Landau tails (Standard Readout), while the second one is based on primary electron clusters counting (Sampled Waveforms). Because the front-end requirements for the two options are quite different each option will be discussed in a dedicated section.

12.1.2.2 Standard Readout - charge measurements specifications

The method is based on integrated charge measurements thus allowing the use of (relatively) low bandwidth preamplifiers. This makes the front-end chain less sensitive to noise pickup and instabilities, a plus condition in a system with a large number of channels.
The three main specification for charge measurement are: resolution, dynamic range and linearity.

Resolution Charge measurements for particle identification aims to measure, with a precision of the order of 7.5%, the particle most probable energy loss, despite the large fluctuations involved in single measurement.
The goal can be achieved by sampling many

times the collected charge and applying the "truncated mean" method to resolve the distribution peak value to several percent.
Because the Super$B$ DCH design parameters and foreseen working conditions aim to an overall single cell resolution (σ_E) of about 35% and σ_E is mainly driven by the detector contribution, we can set a limit of 15% for the front-end electronics contribution (i.e. $\sigma_{EL} \sim 5\%$) then making it negligible ($\sqrt{\sigma_E^2 + \sigma_{EL}^2} \sim \sigma_E$).
Finally, if we assume that the charge collection due to a m.i.p. crossing orthogonally the cell is about 50 fC ($\sim 2fC/e$ @ 10^5 nominal gas gain) we can infer a limit of the Equivalent Noise Charge (ENC) for the single front-end channel of about 50 $fC \cdot 0.05 \simeq 2.5$ fC.

Dynamic range With 8 bits ADCs the dynamic is $2.5 - 500$ fC, actually even more then system requirements.

Linearity As stated above, the single cell energy resolution is about 35%, therfore a linearity of the order of 2% largely satisfies the system requirements.

12.1.2.3 Standard Readout - time measurements specifications

As for charge measurements we have three main specifications: resolution, dynamic range and linearity.

Resolution One of the Super$B$ DCH requirements is charged particle tracks reconstruction. The measure is carried out by acquiring the first ionized electron arrival time to the sense wire with a negligible error with respect to the quoted value of σ_S ($\sim 110\mu m$).
Limits to spatial resolution are due to primary ionization statistics, electrons diffusion and time measurement accuracy.
Assuming an intrinsic chamber resolution (σ_{SC}) of about 100 μm **(ref DCH)** the upper limit for electronic contribution can be quoted to be $\sigma_{EL} \leq \sqrt{\sigma_S^2 - \sigma_{SC}^2} \simeq 50$ μm. As helium based gas mixtures are characterized by a non saturated drift velocity up to high fields, [1] electrons drift velocity rapidly increase approaching sense wire, thus a 2.5 $cm/\mu s$ (25 $\mu m/ns$) [2] has been used to evaluate the maximum acceptable error in time measurement, that is $\sigma_t \leq 50[\mu m]/25[\mu m/ns] \simeq 2$ ns.
Discarding the bunch length contribution (tenths of ps) there are two main error sources in time measurements: the discriminator jitter (different signals cross a fixed threshold at different times) and the TDC resolution (digitization noise). Signal jitter, in turn, has two main contribution: signal noise and time-walk.
Signal noise contribution is generally small and can be evaluated according to $\Delta t = \sigma_{noise}/(dV/dt) \simeq \sigma_{noise} \cdot \tau / V_{max}$ where τ is the preamplifier-shaper peaking time.
Assuming that a single electron cluster generates a signal of ~ 20 mV, and that noise and peaking time associated to the signal are, respectively, $\sigma_{noise} \sim 3$ $mV(rms)$ and $\tau \sim 5$ ns we get a noise contribution to time resolution of about *0.8 ns*.
The time-walk effect is caused by signal amplitude variation. With a peaking time around 5 ns, a time-walk contribution for a low-threshold leading-edge discriminator of about $1.5ns$ can be estimated.
Finally, the digitization noise is a function of the digitization unit according to $\sigma = \Delta/\sqrt{(12)}$ where Δ is the quantization unit, using $\Delta \simeq 1.5$ ns a digitizing noise of about 0.45 ns is obtained.
Summarizing, without corrections, the time resolution is dominated by the signal time walk and can be estimated to be about 1.8 ns including all contributions. Nevertheless corrections can be applied using digitized signals to minimize time-slewing effects then reducing the time walk contribution (see Front End Boards - Digitization Section).

Dynamic Range The TDC range depends on the drift velocity and on the cell size. A maximum drift time of about 600 ns has been foreseen for Super$B$ DCH cells. Providing some safety factor, a TDC range of about 1 μs is adequate.

Linearity A linearity of the order of 1% fully satisfies time measurement requirements.

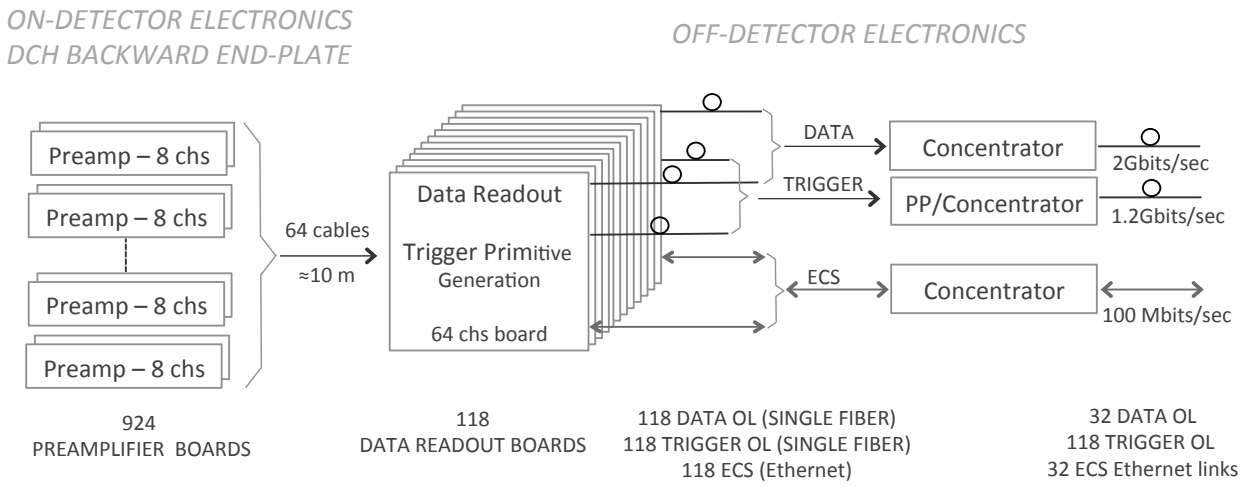


Figure 12.2: DCH front-end block diagram

12.1.2.4 Standard Readout - DCH Front-end system (block diagram)

The DCH FE chain (fig.12.2) is split in two blocks:

- ON-DETECTOR electronics: HV distribution and preamplifier boards located on the backward end-plate to preserve sense wire signal Signal to Noise Ratio (SNR).
- OFF-DETECTOR electronics: Data Readout and Concentrator Boards located on the top-side of the experiment. Trigger primitives are generated on these boards as well.

The connection between ON-DETECTOR and OFF-DETECTOR boards will be implemented by means of micro (mini) coaxial or twisted pairs cables while OFF-DETECTOR Boards output connections will depend on the data path. DAQ chain and Trigger chain data path will use optical links while ECS will use copper links **(see ECS section)**.
In the following paragraphs we will refer to the preamplifier boards as Very Front End Boards (VFEB) to distinguish them from Front End Boards (FEB) containing the digitization and buffer sections located far from the detector.

12.1.2.5 Standard Readout - ON-DETECTOR electronics

Very Front End Boards Very Front End Boards will contain HV blocking capacitors, protection networks, preamplifiers and (possibly) shapers-amplifiers. Because of the small cell dimensions more cells must be grouped in a single, eight-channel preamplifier-shaper board. Output and power supply cables will be connected to the boards by means of suitable connectors.
Besides the requirements on SNR, preamplifier should be characterized by enough bandwidth to preserve signal time information and low power requirement, not more than 20-30 mW per channel, to limit the total power dissipation on the backward end-plate to $160 \div 240\ W$ then allowing the use of simpler and safer forced air cooling system (no risk of leak).

Table 12.2: Preamplifier main specifications

Linearity	$< \%(1 - 100fC)$
Output Signal Umbalance	$< \%(1 - 100fC)$
Gain (Differential)	~ 5.2 mV/fC
Z_{IN}	110 Ω
Z_{OUT}	50 Ω
Rise time	~ 2 ns ($C_D = 24pF$)
Fall time	~ 13 ns ($C_D = 24pF$)
Noise	1350 erms ($C_D = 24pF$)
V_{SUPPLY}	4V
P_D	$\sim$ 30mW

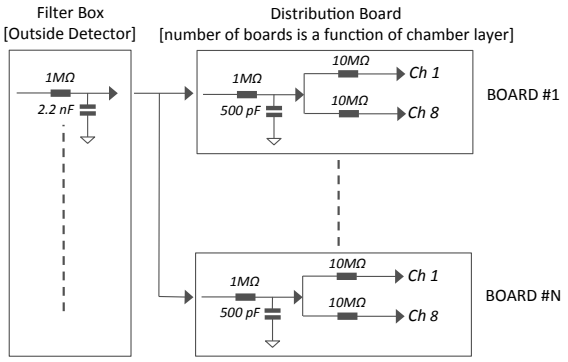


Figure 12.4: Standard Readout High Voltage distribution network

Concerning the circuit implementation, since the channel density is quite low and simple circuit topology can be used, an approach based on SMT technology can be adopted then avoiding dedicated (and expensive) development (ASIC). As an example, a simulation of a three stages

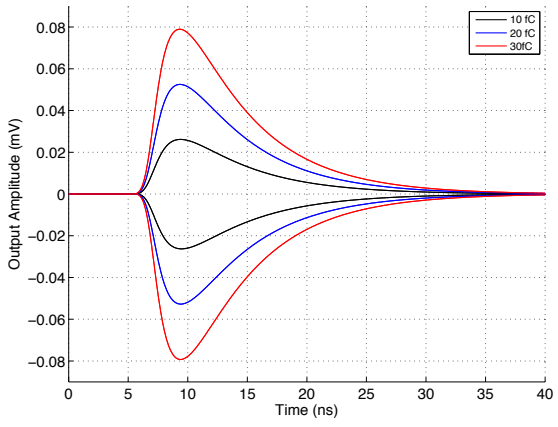


Figure 12.3: Preamplifier output for 10, 20 and 30 fC test pulse ($C_{DET} = 24pF$)

transimpedance preamplifier based on SiGe transistors has been carried out. The first stage dominant pole is around 26 MHz while other stages have been designed with wider bandwidth then obtaining a good separation in terms of cutoff frequencies.
Simulation results are shown in table 12.2 while fig. 12.3 shows the (simulated) output waveforms for 3 different input charges (10, 20 and 30 fC) injected through the test input.

HV distribution boards The high voltage distribution network (fig. 12.4) will be located on the forward end-plate. The distribution board modularity will match the preamplifier modularity while the number of distribution boards connected to a single HV channel will depend on the distance from the DCH inner radius (example: inner layers = 2 boards, outer layers = 5 boards).

12.1.2.6 Standard Readout - OFF DETECTOR electronics

Front End Boards - Block Diagram Front End Boards will host up to 64 channels and will be made of three stages as shown in fig.12.5. The first one receives signals from preamplifiers and generates outputs for digitizing and trigger primitives sections while the second stage provides digitization for charge and time measurements. Digitization stage includes the logic for trigger primitives generation as well. Finally, the third stage contains the Latency and Readout buffers and the dedicated control logic. Boards include an ECS section as well (not shown in the block diagram) for parameters setting/sensing and system test.

Front-End-Boards - Receiver Section Details of the receiving section are shown in fig. 12.6. The preamplifier output signal is amplified and split to feed an anti-aliasing 14 MHz low-pass filter (charge measurements) and a leading edge discriminator (time measurements). Fig. 12.7 shows the simulated analog chain response to a Garfield simulated signal. In the simulations Spice models have been used for both active components and the 10 m twisted pairs cable.

Front-End-Boards - Digitization Section The 14 MHz filter output signal is routed to an eight bits and (about) 28 MSPS FADC whose outputs feed a section of the system Latency Buffer implemented in a FPGA. Thirty-two FADC output samples (corresponding to about 1.14 μs,

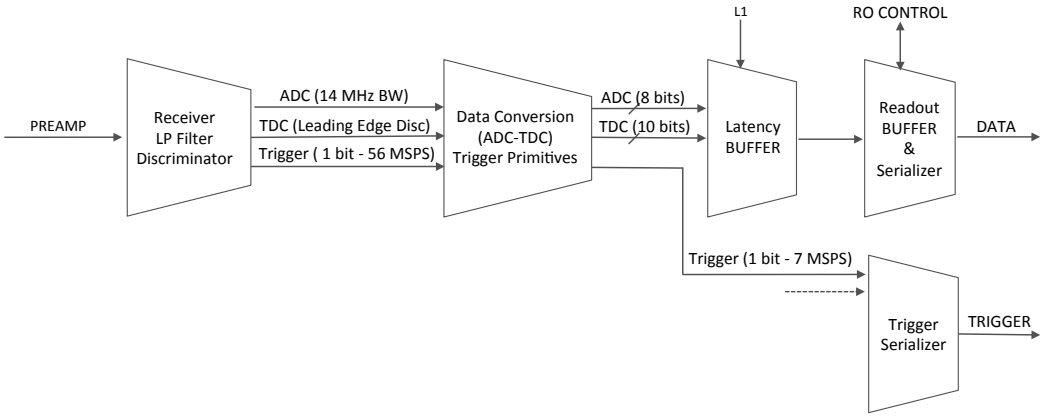


Figure 12.5: Front End Board Block Diagram

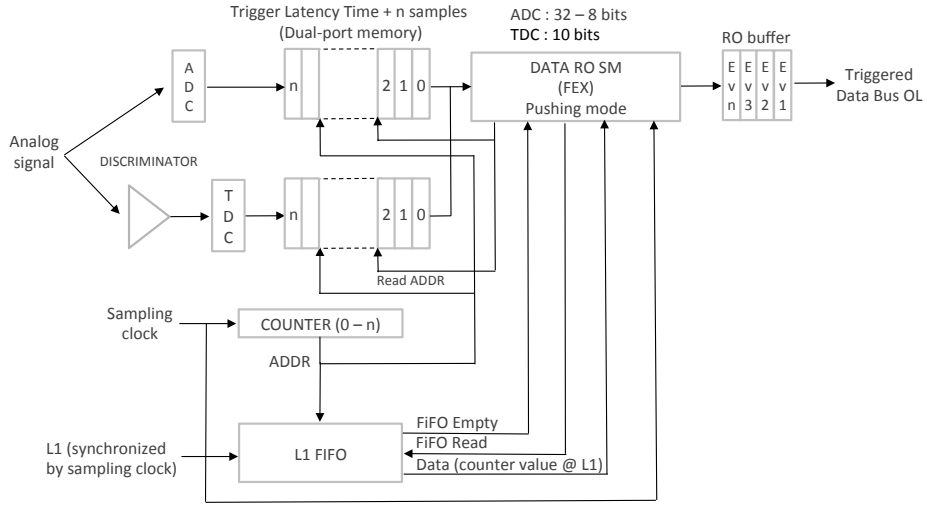


Figure 12.8: Digitization chain block diagram

enough to span the full signal development) will be Read-Out in presence of a Level 1 (L1) trigger and, eventually, stored in a Read-Out Buffer. The comparator output is also routed to the FPGA, where it is spit in two paths. The first one is sent to a TDC (implemented in the FPGA itself using the oversampling method) for arrival time measurement. The TDC outputs feed the second section of the Latency Buffer that, again, will be Read-Out in presence of a L1 trigger signal (fig 12.8). The second one, synchronized with the system clock and conveniently stretched to remove redundant informations is sent to the DCH Trigger Segment Finding modules **(see Trigger Section)**.

The data structure will not have a fixed length as L1 triggers spaced less than single event Read-Out time will extend the time window to include the new event. Nevertheless, the board structure will be also compatible with local Feature EXtraction (FEX) implementation, i.e. the extraction of relevant information from the digitized data. In case of FEX implementation the transferred data stream would have a fixed length; the structure could be similar to that shown in table 12.3.

Table 12.3: FEX based data stream (fixed length structure)

Data stream example
Digitizer Module Address (2 bytes)
Flag (1 byte)
Trigger Tag (1 byte)
Counter (1 byte)
Charge (2 bytes)
Time (2 Bytes)
1st ADC sample (different from baseline) for time walk correction (1 byte)

12.1.2.7 Sampled Waveforms - specifications

The Cluster Counting technique is very powerful as it improves DCH particle identification. The technique is based on primary ionization measurement and, to fully exploit the technique, individual clusters must be identified.
On the other hand the front-end requirements are quite onerous as, despite the use of slow drift velocity ($\sim$1 $\mu s/cm$), high sampling frequency digitizers (at least 1 GSPS) and fast processing (data throughput must sustain the Super$B$ expected 150 kHz average trigger rate) are required. These requirements, at the state of art of technology, result in a huge power requirement and, as a consequence in a low FEB modularity.
As also on the VFEB side fast amplifiers must be used, then power requirements will be higher than in the "Standard Readout" scenario thus envisaging the use of a local liquid cooling system. Moreover the wide bandwidth requirement has also an impact on the type of cable used to interconnect on-detector and off-detector electronics and on the full system noise pick-up sensitivity.
Finally, to apply the cluster counting technique correctly, signal reflection on the sense wires must be avoided by means of termination resistors, and this, unavoidably, sets a lower limit on the system intrinsic noise.
Concerning tracking requirements, if we assume that full efficiency in single electron cluster detection is achieved, Cluster Counting dE/dx measurement already includes information for tracking purpose (it is just required to store clusters arrival time instead of simply counting them).

Specifications for the Sampled Waveforms measurement are the same we defined for the Standard Readout that is: resolution, dynamic range and linearity.

Resolution Digitizers resolution is a function of both the lowest signal amplitude to be digitized and the system noise. Assuming an average delivered signal of $\sim 6fC/e$ @ $3 \cdot 10^5$ gas gain, a preamplifier-shaper gain of $10mV/fC$ and a safety factor of 2 for gas gain fluctuations we get an (average) minimum signal of about 30 mV (single electron cluster).
Preamplifier ENC estimation at the moment it is difficult, nevertheless we can do an estimation of the dominating noise source, that is the termination resistor. Assuming a CR-RC shaping circuit and a 3 ns peaking time we get about $\sim$ 0.2 fC, that is about 2 mV rms for a preamplifier gain of 10 mV/fC.
Thus a LSB of about 2 mV allows good control of system noise and cluster signal reconstruction.

Dynamic range Cluster Counting method requires to find the peaks (corresponding to the clusters) contained in the digitized signals. The expected dynamic range (discarding gas fluctuation) is driven by the cluster size (i.e. the number of primary ionization electrons contained in a single cluster). Signal dynamic range can be,

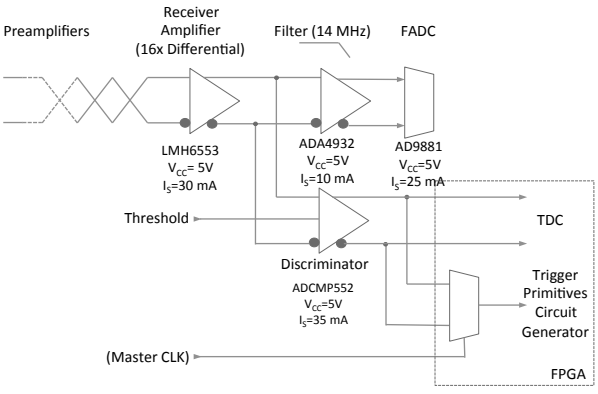


Figure 12.6: Readout board: Analog Section block diagram (40mA@5V/35 mA@3.3 V)

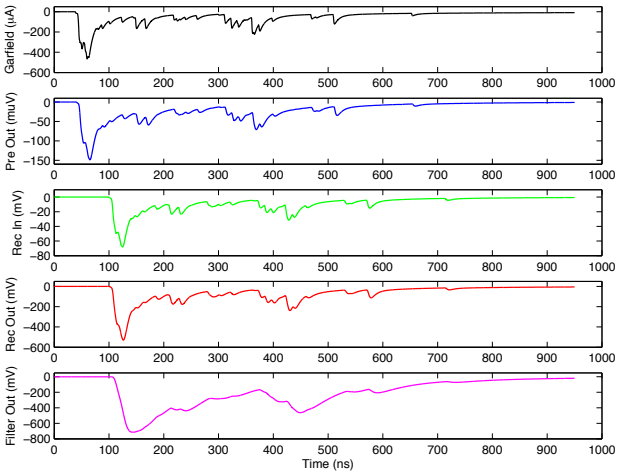


Figure 12.7: Readout board: Analog Chain Response - Garfield output (black), Preamplifier output (blue), Receiver input (green), comparator input (red), FADC input (Cyan)

then, defined (as an upper limit) by the expected total ionization.
Helium based gas mixture have already been well characterized [3]; assuming a 1.2 *cm* square cell and a 90/10 He/Iso gas mixture we expect about 26 electrons for a m.i.p crossing the cell orthogonally, thus an 8 bits ADC dynamic range is fully adequate for CC measurement.

Linearity As we are interested on finding (and tagging) signal peaks, a resolution of 2% fully satisfies the requirements.

12.1.2.8 Sampled Waveforms - DCH front-end system (block diagram)

The Sampled Waveforms DCH front-end chain block diagram is similar to the diagram shown in fig.12.5; also in this scenario we will have ON-DETECTOR and OFF-DETECTOR electronics connected by means of mini coaxial cables, but, because of the lower board modularity both the number of crates and boards will increases significantly (see table 12.4).

12.1.2.9 Sampled Waveforms - ON DETECTOR electronics

Very Front End Boards Because Very Front End Boards will host high bandwidth (500 MHz) preamplifiers both layout and assembly are more tricky with respect to the Standard Readout scenario. In particular special attention must be devoted to ground loops in such a way to minimize both instabilities and external noise pickup.

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Something about preamplifier .....
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HV distribution boards Most of the remarks shown before also apply for Sampled Waveforms scenario. Anyway, because of the sense wire termination resistor the boards layout will be slightly different and, moreover, high quality grounding is required. The HV distribution network is shown in fig 12.9.

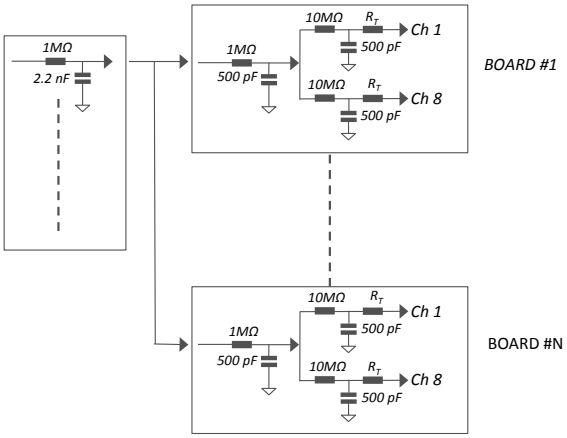

Figure 12.9: Sampled Waveforms High Voltage distribution network

12.1.2.10 Sampled Waveforms - OFF DETECTOR electronics

Front End Boards Front End Boards will be based on high sampling rate ($\geq$ 1 GSPS) digitizer, then a limited number of channels can be packaged on a single board, mainly because of power requirements. At present, up to 8 channels working at 1 GSPS have been packaged in a single VME 6U board. Nevertheless, in the

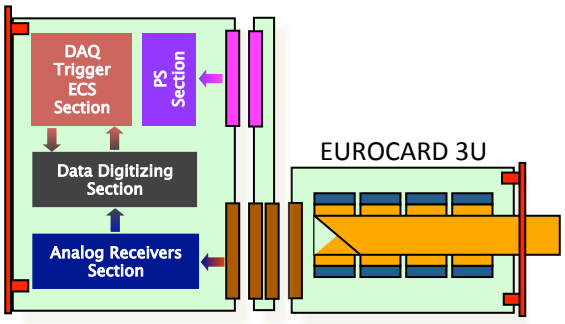

Figure 12.10: VFEB - FEB connections (FEB board - Custom Backplane - Interconnection Board

next future, board modularity could increase to 16 (or 24) still maintaining the current 8 channels board power requirements.
The circuit structure is very close to the block diagram shown in 12.5. Differences arise in digitizing section as no TDC is required for time measurements and also Trigger signals are generated starting from the FADC outputs.
A sensitive issue concerns the FEX. Because of the large amount of data per channel (about 1 thousand of bytes) we can not transfer raw data to the DAQ thus FEX must be implemented in the FEB itself. That is, when an L1 accept is raised all the event samples must be scanned to identify clusters. The time required to implement the procedure is still compatible with the average trigger rate foreseen at the nominal luminosity ($\sim 150\ kHz$), but it could be a limit if the luminosity increases.
Another issue concerns the radiation background, as high performances RAM based FPGA must be used in the design.

12.1.2.11 Front End Crates

Each Front End Crate will host up to 16 FEB, a Power Supply board for VFEB, Data Concentrators and, eventually, Trigger Patch Panel o Trigger Concentrator. Custom backplanes will be designed to distribute power and common signals to FEBs, to allow the use of Interconnection Boards to collect low modularity VFEB cables (fig 12.10) and to route some of the trigger signals to the neighbors boards **(see Trigger Section)**.

12.1.2.12 Number of crates and links

Table 12.4 shows the estimate of the number of links, boards and crates required for both DAQ and Trigger front-end chains (each crate is supposed to host up to 16 FEB). As shown in the table the number of Trigger OL do not change despite the different FEB number the two scenarios. This is because the Sampled Waveform scenario foresees a Concentrator board also for the trigger chain because of the lower modularity. The board will collect Trigger OL coming from several FEBs and will deliver a single OL to the TFS modules.
The estimate has been based on the following assumptions: 150 kHz L1 trigger rate, 7392 sense wires (subdivided in 10 super-layers), 10% chamber occupancy in 1 μs time window and 48 bytes per channel data transfer. Single link bandwidth is 2 Gbits/sec for DAQ data path and 1.2 Gbits/sec for Trigger data path.

Table 12.4: Number of links (Data, ECS, Trig), FEBs and crates for 64 (Standard Readout) and 16 (Sampled Waveforms) channels board modularity

	Mod	Data	ECS	Trig	Boards	Crates
SR	64	32	32	118	118	8
SW	16	32	32	118	462	29

12.1.2.13 ECS

Each FEB will host a mezzanine board to manage ECS communication. Besides the control of the board, ECS mezzanine should provide the capability of data buffer readout for debugging propose. Detail can be found in the ECS section.

12.1.2.14 Cabling

Because the large number of channels involved, DCH cable layout must be carefully designed. The main requirement concerns the possibility of changing, in case of failure, a VFEB without disconnecting output cables from too many boards. Thus, signal and HV cables should leave

the chamber from the outermost layer then minimizing cables overlap. Table 12.5 shows the foreseen number of cables and a rough estimation of cable size. Signal twisted pairs cables are commercially available also with flat shielded assembly (size 16x3 mm^2 for 8 pairs).

Table 12.5: Estimation of the number and dimension of DCH cables (7392 sense wires - VFEB modularity = 8 channels)

	LVPS	HV	Signal (coax)	Signal (twisted)
Quantity	118	32	7392	924
N of cores	16	25	1	16
Cond. area (mm^2)	0.5	0.07		
Overall diam. (mm)	12	12	1.8	6.5

12.1.2.15 Power Requirements

A very preliminary power requirement estimation is shown in table 12.6. The estimation for ON-DETECTOR electronics is based on preamplifier simulation and prototype test, while estimation for OFF-DETECTOR electronics come from the state of art of digitizing board available at the moment. Local (VFEB) voltage regulation is supposed to be implemented by means of linear low-voltage drop hard-rad regulator.

Table 12.6: Power requirement estimation for bot Standard Readout (SR) and Sampled Waveform (SW)

	Channel	Board	Overall
SR VFEB	30 mW		250 W
SW VFEB	150 mW		1.2 kW
SR FEB		40 W	5 kW
SW FEB		40 W	19 kW
SR & CC Data Conc.		30 W	240 W
SW Trig Conc.		30 W	870 W

12.1.2.16 Grounding

As a general rule grounding is supposed to be included in a system/equipment only for safety purpose. Thus, detector equipment should be designed in such a way it should work also without GND connection (GND is not a current return path).
LV power supply should have isolation transformer (AC input/output terminal should be electrically isolated for low frequencies). If the output terminal of HV power supply is not floating a resistor should be connected between GND and the common of HV distribution system to avoid ground loops.

12.1.3 PID Electronics

The electronics for the FDIRC can be seen as an upgrade of the electronics of the *BABAR* DIRC. The new requirements of the experiment (Trigger rate, background, radiation environment) and FDIRC specific requirements (resolution, number of channels and topology) have led to a similar but new design of the electronics chain.

The electronics will equip the 18,432 channels of the 12 sectors of the FDIRC. The electronics chain is based on a high resolution / high count rate TDC, a time associated charge measurement on 12 bits and an event data packing sending event data frames to the data acquisition system (DAQ). The target performance of the overall electronics chain is a time resolution of 100 ps rms. This chain has to deal with a count rate per channel of 100 kHz, a trigger rate up to 150 KHz and a minimum spacing between triggers of about 50 ns.

The estimate radiation level is expected to be less than 100 rads per year. The use of radiation tolerant components or off the shelves radiation-qualified components is mandatory. However, the expected energy of the particles may make the latch-up effect almost impossible. Thus, the design has to take into account only Single Event Upsets. We selected the Actel family FPGA components for their non-volatile flash technology configuration memories, which are well adapted to radiation environment.

Several architectures have been considered which can be summarized as follows:

- All electronics directly mounted on the FBLOCK.
- All electronics mounted next to the detector and linked to the PMTs by cables.
- A part of it on the detector (the Front-end boards) and the other part, called crate concentrator, situated close to the detector, (this board is in charge of interfacing

with the Front-end, reading out event data, packing and sending it to the DAQ.

The first solution has been chosen as baseline for the TDR for two main reasons:

- The cost of the cables (PM to Front-end boards) is estimated to be close to 200 kEuros (1/3 of the price of the overall electronics cost), making this solution too expensive. Moreover, the possible option to have pre-amps on the PMT bases doesn't prevent from having electronics and power supplies on the detector.
- The large amount of data per channel leads to have the L0 derandomizer and buffer on the Front-end boards. The FCTS receiver could be individually located on each Front-end board but the number of cables needed pushes to distribute all the control signals on a backplane. Consequently the board dedicated to receiving and transmitting FCTS signals on the backplane naturally tends to also become the event data concentrator and the link to the DAQ.

The baseline design assumes a 16-channel TDC ASIC offering the required precision of 70 ps rms- embedding an analog pipeline in order to provide an amplitude measurement transmitted with the hit time. Thanks to a 12-bit ADC, the charge measurement will be used for electronics calibration, monitoring and survey purposes. The Front end board FPGA synchronizes the process, associates the time and charge information and finally packs them into a data frame which is sent via the backplane to the FBLOCK control board (FBC). The FBC is in charge of distributing signals coming from the FCTS and ECS, packing the data received from the FE boards to a n-event frame including control bits and transferring it to the DAQ.

12.1.3.1 The TDC chip

A former TDC chip offering the requested performances of resolution has already been designed for the SuperNemo experiment. It provides a time measurement with both a high resolution 200 ps step (70 ps RMS) and a large dynamic range (53 bits). The architecture of this chip is based on the association of Delay Locked Loops (DLLs) with a digital counter, all of these components being synchronized to a 160 MHz external clock.

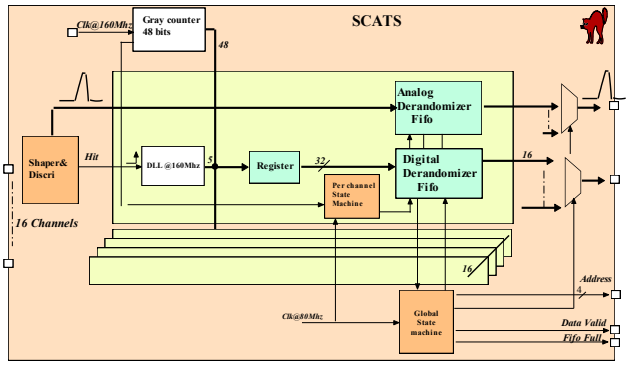

Figure 12.11: Block diagram of the Super*B* FDIRC TDC chip — SCATS —

The Super*B* chip (SCATS, Fig. 12.11) will keep the same philosophy but the high input rate requirement lead to a complete re-design of the readout part, in order to minimize the dead time per channel. Instead of registers and multiplexer which are the bottlenecks of the SuperNemo chip readout, it makes use of an individual FIFO memory per channel in order to derandomize the high frequency bursts of input data

With this architecture, data from the DLLs and the coarse counters are transferred into the FIFO memory within two clock cycles. When the transfer is complete, the channel is automatically reset and ready for the next hit. Simulations of the readout state machine showed an output FIFO data rate capability of 80 MHz. Time ranges for the DLLs and the coarse counter can be easily customized by adjusting the output data format (16, 32, 48 or 64 bits). Therefore, the chip is suitable for various applications with either high count rate and short integration time or low count rate and long integration time.

A FIFO depth of 8 words has been selected after simulation with a exponential distribution

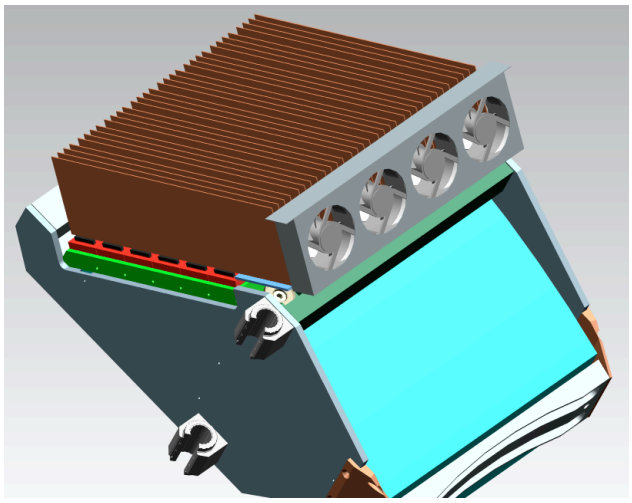

Figure 12.13: The FBLOCK equipped with the boards and fan tray

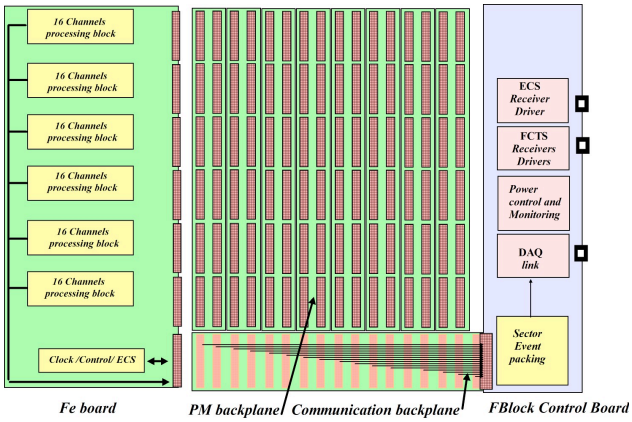

Figure 12.14: The Frontend Crate

model of delta time between hits (mean rate of about 1MHz) applied to inputs. Thus the simulation gives a dead time of approximately 1% with 500 kHz input rate on each channel.

To design this FIFO a full custom RAM has been developed. It permits reducing the size of the chip and consequently its cost. The chip is designed using known and proved mitigation techniques to face single event upset (SEU) issues due to the low-level radiation environment.A first version of the chip without the analog FIFO and the discriminator has been submitted in November 2011 and the test are ... Note: something is missing here.

We plan to submit in 2012 one chip PIF dedicated to the currently missing parts:

- A low walk (approx. 50 ps) discriminator based on a CFD like design.
- A track/peak detector to be able to sample the maximum of the signal.
- An analog pipeline synchronized with the digital FIFO and providing analog output for charge measurement.

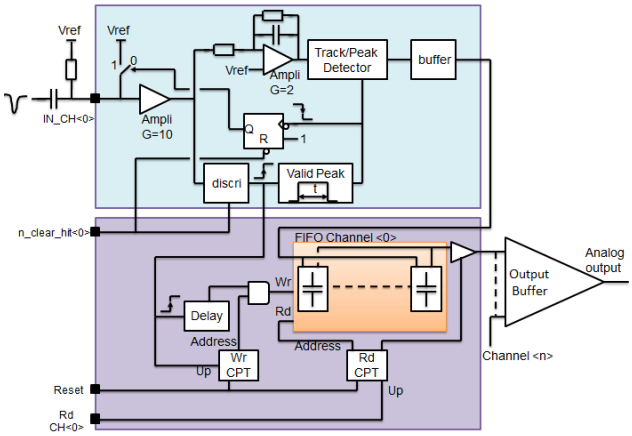

Figure 12.12: PIF One Channel

After testing and validation, it is foreseen to be included in the final version of SCATS taking benefit of sharing the FIFO pointers of the analog and digital parts. The chip will be assembled and submitted end of 2013.

12.1.3.2 The Front-end Crate

The board input will fit the topological distribution of the PM on the FBLOCK. The PMs are arranged as a matrix of 6 in vertical direction by 8 in horizontal direction. Each column of 6 PMs will fit to one FE board. One vertical backplane (PM Backplane) will interface between the 4 connectors of each PM base to one connector of FE board. The PM Backplane is also in charge of distributing the High Voltage, thus avoiding HV cables to pass over the electronics. The FB crate will use as much as possible the elements of a commercial crate, in order to avoid the design of too many specific elements like board guides.

12.1.3.3 The Communication Backplane

Distributes the ECS and FCTS signals from the FBC to the 8 FE boards thanks to point to point LVDS links. Connects each FE board to the FBC for data transfer. A serial protocol will be used between FE board and the FBC in order to reduce the number of wires and consequently ameliorate the reliability. It will also distribute JTAG signal for FPGA board reprogramming and all signals for monitoring and control of the crate.

12.1.3.4 The PMT Backplane

It is an assembly of 8 motherboards, each one corresponding to a column of 6 PMTs. One motherboard receives 2 Fe-board. The 64 channels from 4 connectors per each PMT are merged on the motherboard into two connectors to get into the Front end board to get 16 channels per half PMT, i.e., 6 PMTs correspond to 96 channels per FE-board. It also insures the ground continuity between FE-boards — crate — FBLOCK.

12.1.3.5 Cooling and power supply

The electronics is located on the detector in a place enclosed by the doors. There are 2 major consequences: one is the problem of the cooling which must be carefully studied in terms of reliability and capability and the second is that the location is naturally shielded. Consequently the use of magnetic sensitive components as coils or fan trays is possible.

An estimation of the overall electronics consumption lead to approximately 6 kW, not including the external power supplies. This can be broken down to individual contribution as follows:

- Electronics: 0.325W/channel, 500 W/sector and 6 kW/system.
- HV resistor chain: 0.19W/tube, 9.1W/sector, and 109 W/system.

The cooling system must be designed in order to maintain the electronics located inside at a constant temperature close to the optimum of 30 degrees. The air inside the volume must be extracted while the dry, clean temperature controlled air will be flowing inside. Each FB crate will have its own fan tray like in a commercial crate. Targeting a difference of 10 degrees between inside and outside temperature drives to a rough estimate value of $300m^3/h$ per crate, $4000m^3/h$ can be considered as the baseline value for the whole detector.

12.1.3.6 The front-end board

One Front-end board is constituted of 6 channel-processing blocks handling the 96 channels. The channel-processing block is constituted by one SCATS chip, one ADC, one Actel FPGA and the associated glue logics.

The FPGA receives event data from the TDC and the converted associated charge from the ADC. From one 16 bit bus of the 16 channels coming from the TDC, it de-serializes to 16 data path where events are keeping in a buffer until they are thrown away if there are too old (relatively to the trigger) or sent upon its reception.

The PGA master receives event data from the 6 channel processing blocks and packs the event.The FE board transfers the event frame in differential LVDS to the FBC via the communication backplane.

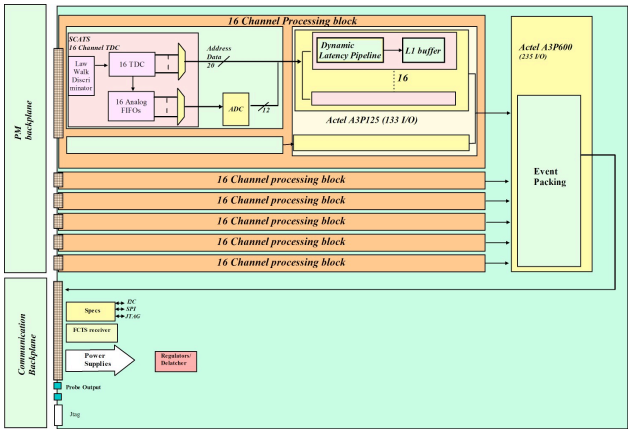

Figure 12.15: PID Front-end Board

12.1.3.7 The crate controller board (FBC)

The FBC is the board which gathers the front-end data, control and monitors the crate. There is one board per crate. The board handles several functionalities:

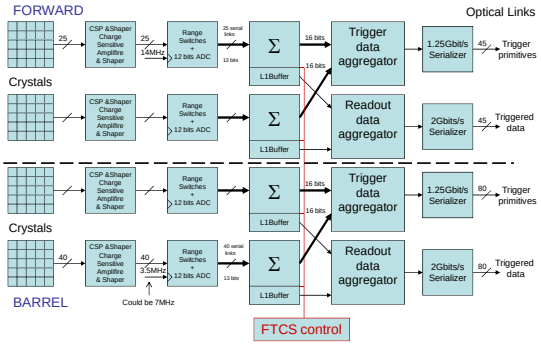

Figure 12.16: EMC Electronics

- Receive the event data from the Front-end boards via the communication backplane, constitutes and event data fram for the DAQ
- Spy data building for monitoring and commissioning purposes
- Distributes the ECS (SPECS) signals to the front end. Distributes the JTAG.
- Deserialize clock and control signals from FCTS.
- Monitor the crate; temperature, power supplies, fans.

12.1.4 EMC Electronics

This is still the version from the Whitepaper!!!

Two options have been considered for the EMC system design—a *BABAR*-like push architecture where all calorimeter data are sent over synchronous optical 1 Gbit/s links to L1 latency buffers residing in the trigger system, or a "triggered" pull architecture where the trigger system receives only sums of crystals (via synchronous 1 Gbit/s links), and only events accepted by the trigger are sent to the ROMs through standard 2 Gbit/s optical links.

The triggered option, shown in Fig. 12.16, requires a much smaller number of links and has been chosen as the baseline implementation. The reasons for this choice and the implications are discussed in more detail below.

To support the activated liquid-source calibration, where no central trigger can be provided, both the barrel and the end-cap readout systems need to support a free running "self-triggered" mode where only samples with an actual pulse are sent to the ROM. Pulse detection may require digital signal processing to suppress noisy channels.

Forward Calorimeter The 4500 crystals are read out with PIN or APD photodiodes. A charge preamplifier translates the charge into voltage and the shaper uses a 100 ns shaping time to provide a pulse with a FWHM of 240 ns.

The shaped signal is amplified with two gains ($\times 1$ and $\times 64$). At the end of the analog chain, an auto-range circuit decides which gain will be digitized by a 12 bit pipeline ADC running at 14 MHz. The 12 bits of the ADC plus one bit for the range thus cover the full scale from 10 MeV to 10 GeV with a resolution better than 1%. A gain is set during calibration using a programmable gain amplifier in order to optimize the scale used during calibration with a neutron-activated liquid-source system providing gamma photons around 6 MeV.

Following the *BABAR* detector design, a push architecture with a full granularity readout scheme was first explored. In this approach, the information from 4 channels is grouped, using copper serial links, reaching an aggregate rate of 0.832 Gbit/s per link to use up most of the synchronous optical link's 1 Gbit/s bandwidth. A total of 1125 links are required. The main advantage of this architecture is the flexibility of the trigger algorithm that can be implemented off-detector using state of the art FPGAs without constraining their radiation resistance. The main drawback is the large cost due to the huge number of links.

The number of links can be reduced by summing channels together on the detector side, and only sending the sums to the trigger. The natural granularity of the forward detector is a module which is composed of 25 crystals. In this case, data coming from 25 crystals is summed together, forming a word of 16 bits. Then the sums coming from 4 modules are aggregated together to produce a payload of 0.896 Gbit/s. In

this case, the number of synchronous links toward the trigger is only 45. The same number of links would be sufficient to send the full detector data with a 500 ns trigger window. This architecture limits the trigger granularity, and implies more complex electronics on the detector side, but reduces the number of links by a large factor (from 1125 down to 90). However, it cannot be excluded that a faster chipset will appear on the market which could significantly reduce this implied benefit.

Barrel Calorimeter The EMC barrel reuses the 5760 crystals and PIN diodes from *BABAR*, with, however, the shaping time reduced from 1 μs to 500 ns and the sampling rate doubled from 3.5 MHz to 7MHz. The same considerations about serial links discussed above for the forward EMC apply to the barrel EMC. If full granularity data were pushed synchronously to the trigger, about 520 optical links would be necessary.

The number of synchronous trigger links can be drastically reduced by performing sums of 4×3 cells on the detector side, so that 6 such energy sums could be continuously transmitted through a single optical serial link. This permits a reduction in the number of trigger links so as to match the topology of the calorimeter electronics boxes, which are split into 40 ϕ sectors on both sides of the detector. Therefore, the total number of links would be 80 both for the trigger and the data readout toward the ROMs, including a substantial safety margin (> 1.5).

12.1.5 IFR Electronics

draft 0.3, May 16 2012, A. Cotta Ramusino

12.1.5.1 Introduction

This section describes first the features of the IFR detector which drive the design of the readout system. It presents then an estimation of the number of electronic channels, of the event size and the data bandwidth at the nominal Super*B* trigger rate. The design constraints determined by the expected background radiation are then reviewed, along with the results of irradiation tests on existing ASICs and off-the-shelf devices suited for the implementation of some functional blocks of the readout chain. This chapter describes, finally, the baseline IFR readout system going from the basic requirements of a dedicated IFR readout ASIC to the proposed locations of the IFR electronics system to the services required in the detector hall.

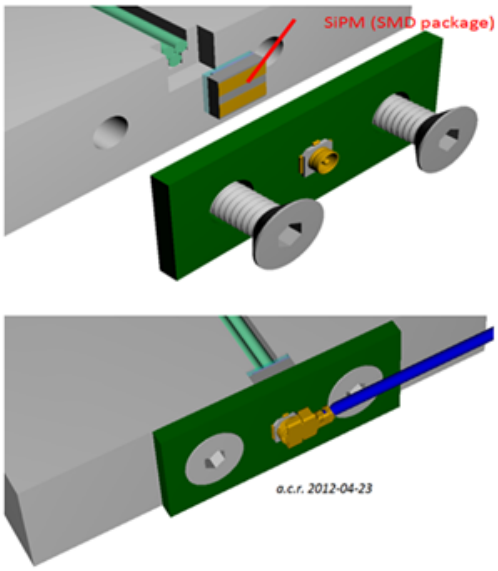

Figure 12.17: details of the three WLS fibers and the PCB for the SiPM

12.1.5.2 Basic features of the IFR detector

The basic IFR detector element exploits an extruded plastic scintillator with WLS fibers applied in machined grooves and "Silicon Photomultipliers" (SiPM) installed as shown in Fig. 12.17. The scintillator bars, fitted with the SiPM carrier PCBs and the signal cables, will be enclosed in boxes made of sheet aluminum which will shield the assembly from the ambient light and will provide it with the necessary mechanical rigidity; the detector assemblies are, in the following, referred to as "modules". The modules will be inserted in the gap between the two steel plates delimiting an "active" layer; nine active layers will be instrumented in the barrel section of the IFR and also nine layer will be "active" in the endcaps. Fig. 12.18 shows a few modules, installed in the barrel section of the IFR, with the aluminum "envelope" removed to show the scintillator orientation. The

LAYER WIDTH	LAYER	No. Modules per layer	LAYER ENABLE	PHI ASSUMING 50MM BARS	ZETA ASSUMING 106MM BARS
1963	1	6	1	13	17
1987	2	6	1	13	17
2050	3	6	1	13	17
2113	4	6		14	17
2176	5	6		14	17
2240	6	6		14	17
2304	7	6	1	15	17
2367	8	6		15	17
2431	9	8		12	17
2494	10	8		12	17
2569	11	8	1	12	17
2641	12	8		13	17
2712	13	8		13	17
2784	14	8	1	13	17
2879	15	8		14	17
2973	16	8	1	14	17
3068	17	8		15	17
3144	18	8	1	15	15
3296	19	8	1	16	15
NUMBER OF MODULES per sextant:		64		TOTAL PER SEXTANT	1940
TOTAL NUMBER OF MODULES	384			TOTAL CHANNELS PER BARREL	11640

Figure 12.19: estimation of the electronics channel count for the IFR barrel

ENDCAP		
top section	horizontal bars per module:	37
	vertical bars per module:	51
center section	horizontal bars per module:	36
	vertical bars per module:	64
bottom section	horizontal bars per module:	37
	vertical bars per module:	51
AVERAGE channel count per module:		92
NO_OF_MOD_PER_LAYER_EC:		3
horizontal bars per layer		110
vertical bars per layer		166
NUMBER OF LAYER PER DOOR		9
NUMBER OF DOORS IN ENDCAPS		4
TOTAL NUMBER OF MODULES IN ENDCAPS:		108
horizontal bars per door:		990
vertical bars per door:		1494
TOTAL HORIZONTAL BARS:		3960
TOTAL VERTICAL BARS:		5976
TOTAL CHANNELS IN ENDCAPS:		9936

Figure 12.20: estimation of the electronics channel count for the IFR endcaps

choice of tightly coupling the SiPM to the WLS fibers is driven by the need of maximizing the number of converted photoelectrons; this choice determines in turn that the coupling between the SiPMs and the first stage of the signal processing chain must be done through coaxial cables and connectors.

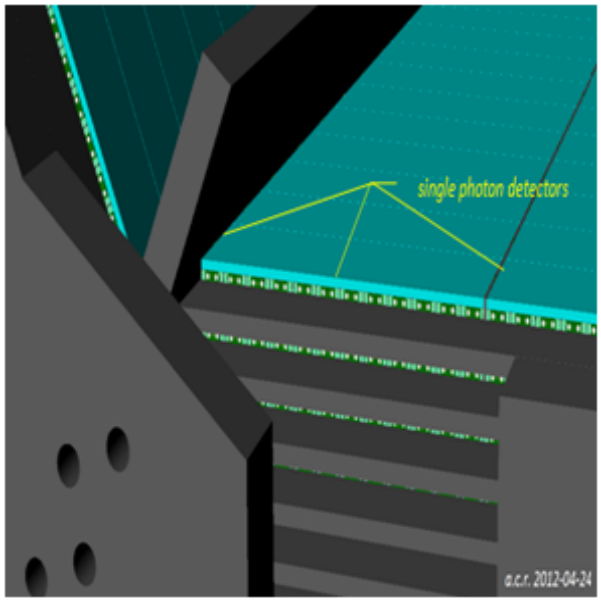

Figure 12.18: detector modules (with the metal enclosure removed) of IFR barrel, layer 0

12.1.5.3 IFR channel count estimation

The active layers of the IFR detectors are equipped with modules in which the detector bars (of different widths for the PHY and the Z views in the barrel) are assembled in two orthogonal layers.

Not all gaps of the flux return steel are equipped with detectors; the "LAYER ENABLE" column in Fig. 12.19 shows the current active layer assignment and the resulting total channel count of 11604 for the IFR barrel.

Fig. 12.20 recalls the distribution of the scintillator bars in an active layer of one endcap door. The total channel count for both forward and backward endcaps amounts to 9540 for 9 equipped gaps.

12.1.5.4 Estimations of the IFR event size and data bandwidth

The IFR detector will be read out in what has been dubbed "binary mode": the output of each SiPM device will be amplified, shaped and compared against a threshold; digitizer modules will sample and buffer the comparators outputs at a rate multiple of the Super$B$ clock and then extract from the latency memories the data selected by the FCTS trigger command. The IFR channels will be processed by functional blocks with a modularity of 32

BARREL		ENDCAP	
Max. channel count per module:	32	Avg. channel count per module	92
Number of MOD32 processing units per module	1	Number of MOD32 processing units per module	3
TOTAL NO. OF MODULES IN THE BARREL SECTION	384	TOTAL NO. OF MODULES IN THE ENDCAPS	108
Total Number of modulo 32 processing units	384	Total Number of modulo 32 processing units	324
Sampling period = 1 / FCTS_clock (ns)	17,86	Sampling period = 1 / FCTS_clock (ns)	17,86
Number of samples in the trigger matching window	10	Number of samples in the trigger matching window	10
BARREL EVENT SIZE (kB)	**15,36**	**ENDCAP EVENT SIZE (kB)**	**12,96**
TRIGGER RATE (kHz)	**150**	**TRIGGER RATE (kHz)**	**150**
TOTAL BANDWIDTH (Gbps) (including 8b/10b overhead)	**23,04**	**TOTAL BANDWIDTH (Gbps)** (including 8b/10b overhead)	**19,44**
Number of data links	24	Number of data links	16
Bandwidth per link (Gbps)	0,96	Bandwidth per link (Gbps)	1,215

Figure 12.22: estimations of the IFR event size and data bandwidth

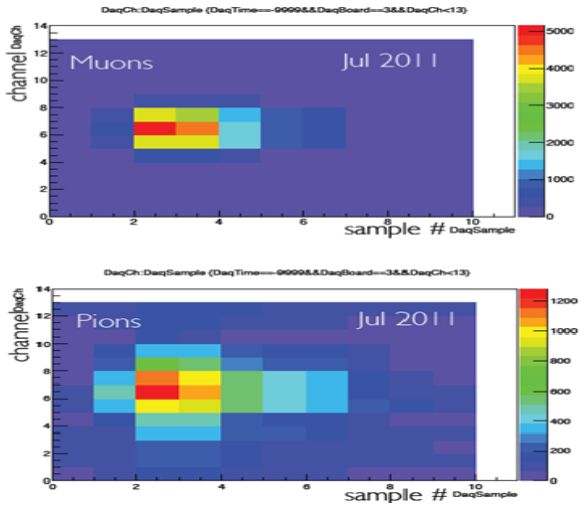

Figure 12.21: time evolution of muon and pions evaluated across the 10 samples taken for each "binary mode" event (plots from [4]). Sampling period was 12.5 ns)

Such a straightforward scheme has been successfully applied to the IFR prototype, which has been tested with cosmic muons and with the beam provided by the Muon Testing Facility of the Fermi National Accelerator Laboratory [4], [5]: the beam tests have shown that the time window for the extraction of data matched to a trigger should be about 120 ns wide (see Fig. 12.21), in order to recover the entire signal from the shower initiated in the detector by an impinging hadron.

The real IFR detector will be read out in the "binary mode" outlined above and the table in Fig. 12.22 reports the expected IFR event size and data bandwidth at the nominal Super$B$ trigger rate.

12.1.5.5 Background radiation and electronics design constraints

The current knowledge on the radiation environment at and around the flux return steel is presented in [6]. This work analyzes the known sources of radiation background in Super$B$ and evaluates the doses in Si at the locations of the SiPMs and at the locations of the front end electronics. The highest fraction of the total dose absorbed by the IFR electronics is deposited by neutrons deriving from the radiative BhaBha and the Touschek processes. The neutron energy spectrum shown in Fig. 12.23 above is quite wide-spread and so different types of interaction processes will have to be considered to assess the effect on the performances of the sensors and of the IFR readout chain. The highest neutron rate, about 5 kHz/ cm^2, is found, according to the plot in the lower left corner, at small radius at the forward endcap; the resulting neutron fluence over 10 years (considering the standard year of 10^7s) would be of about $5*10^{11}$ n/ cm^2.

Fig. 12.24 gives information on the dose (in Si) absorbed at the different locations in evidence. The highest dose is found at the C2 locations of the forward endcap and it is about 140krad/year. Electronics devices and systems which must reliably and durably operate under these radiation conditions must be designed or selected according to guidelines which have already been drawn, among others, by the LHC community; Electronics devices and systems which must reliably and durably operate under these radiation conditions must be designed or selected according to guidelines which have already been drawn, among others, by the LHC community. As an example one could refer to the "ATLAS Policy on Radiation Tolerant Electronics: ATLAS Radiation Tolerance Criteria"

[9] to see that the neutron fluence expected for the Super*B* IFR is of the same order of magnitude simulated for the MDT muon spectrometer. We could then, if not exploiting exactly the same technical solutions adopted there, at least follow the design guidelines established by the cited and by similar documents. A more general approach to the subject of radiation effects in silicon devices is described in other works referenced below [7, 8, 10, 26]. The R&D activity propaedeutic to the TDR has included the evaluation of the radiation effects on SiPM [11, 12, 13, 14, 15] and on electronic devices used to implement the basic functions of the readout system. An irradiation test was performed at the CN facility of the INFN Laboratori Nazionali di Legnaro (LNL) on a sample of the "EASIROC" ASIC developed by the Omega group of the LAL, Orsay, France [16, 17], an ACTEL FPGA and a few samples of low power current feedback operational amplifiers. The CN facility of the LNL has a beam line delivering 4 MeV ^{2}H+ ions to a beryllium target; the energy spectra of the neutrons produced in the ^{9}Be(d,n)^{10}B reaction are shown in Fig. 12.25 where the 4.2 MeV curve is highlighted for convenience.

Fig. 12.25 shows instead the stack of boards carrying the ASIC, the FPGA and the op-amps installed right in front the beampipe, and the thermally isolated SiPM box located right after, at about 4 cm from the beam pipe. Some results of the irradiation tests are presented in the table of Fig. 12.27 below. The OMEGA EASIROC, manufactured in the 0.35 μm SiGe technology of Austria Micro Systems, was exposed to an estimated total of 1.7*10^{11} neutrons, equivalent to a few year's exposition to the Super*B* IFR operating conditions.

The outcome of the test showed that, as expected, while the FPGA configuration memory contents was not corrupted, the on-chip SRAM blocks and the registers in the FPGA fabric were subject to upsets. It follows that any critical part of the FPGA design should include suitable SEU protection functions.

It is worth noticing that no SEU afflicted the EASIROC configuration registers, that no latch-up occurred and finally that no evidence of TID damage was found while comparing the current consumption and the analog performances before and after the irradiation test [15].The op amps to be tested had been fastened to the top of the FPGA and have thus been irradiated with a fluence of the order of 10^{12}neutrons/ cm^2 with no noticeable effect on their current consumption or DC offset.

The results of the preliminary irradiation tests supported the decision on how to build and where to install the front end stages of the IFR readout system. As more neutron irradiation tests on SiPM are planned to assess the radiation tolerance of the latest generation devices, there will be more occasion to test, at the same time, more sample of ASICs built in the AMS 0.35 μm technology at different neutron energies and with different beam orientations w.r.t. to the device under test.

The 0.35 μm CMOS technology from AMS is being tested because it represents the preferred choice for the development of a dedicated ASIC, as described in the next chapter.

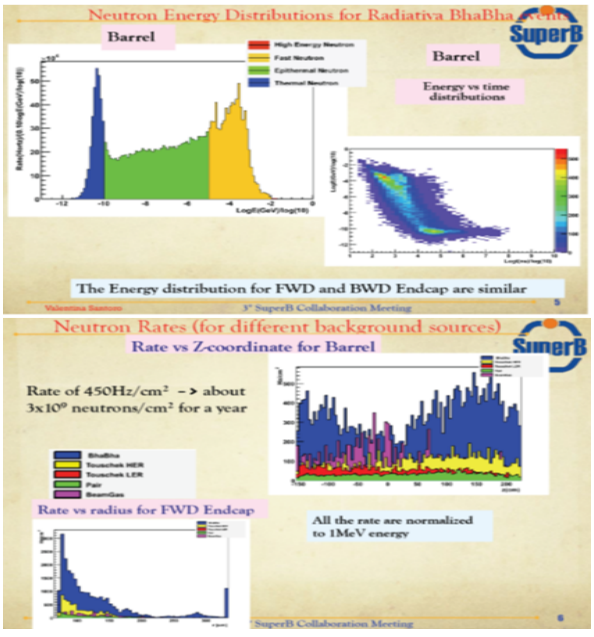

Figure 12.23: background neutrons: energy spectrum and rates (normalized to 1 MeV)

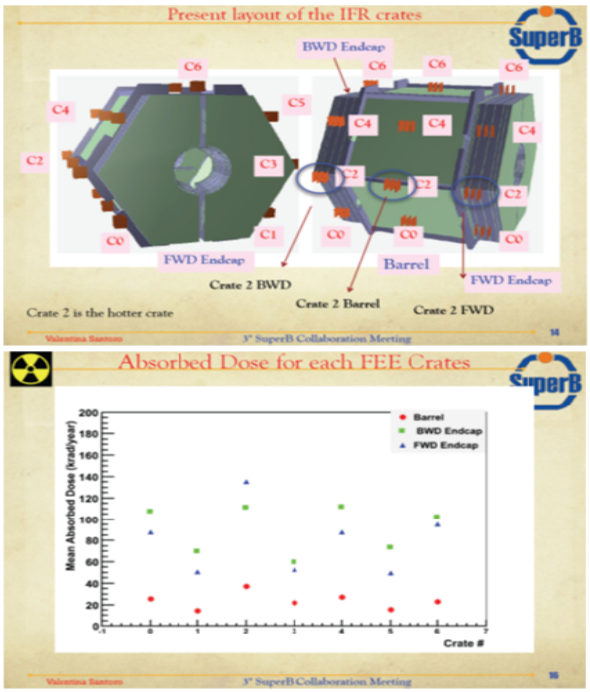

Figure 12.24: background neutrons flux: doses (krad/year) measured at some relevant locations around the detector

12.1.5.6 The IFR readout system

IFR readout basics: outline of the IFR prototype readout The basic principles informing the design of the IFR readout system have been tested with the IFR prototype, which was readout in the "binary" mode described above. For the prototype readout a dedicated front end board, the "ABCD", was built from off-the-shelf components (COTS); Fig. 12.28 shows the "ABCD" block diagram.

The main functions which were implemented on the 32 channel "ABCD" board are:

- individual "high side" regulation (with 12 bit resolution) of the SiPM bias voltage; bias voltage and SiPM signal are carried by the inner conductor of the coaxial cable, whose outer conductor is at true ground potential
- wideband (1,5GHz 3dB frequency) amplification of theSiPM signal
- discrimination of each SiPM signal against an individually programmable (with 12 bit resolution) threshold voltages; the discriminators (two per channel) used A.C. coupled feedback to stretch the output pulse to a width of about 20 ns
- sampling and buffering of the discriminators outputs pending the trigger signal from the experimental trigger system; an ALTERA Cyclone III FPGA was used to sample the discriminated SiPM signals and store them in an internal latency pipeline running at 80MHz.
- trigger processing: with each trigger a set of 10 samples was extracted from the latency pipeline and transferred to an output buffer (along with suitable framing words) from where they reached the "BiRO_TLU Interface board" [19] acting as a crate_wide data-collector and interface to the DAQ PC and to the experiment's TLU (Trigger Logic Unit).
- The DAQ system developed for the IFR prototype readout also performed functions

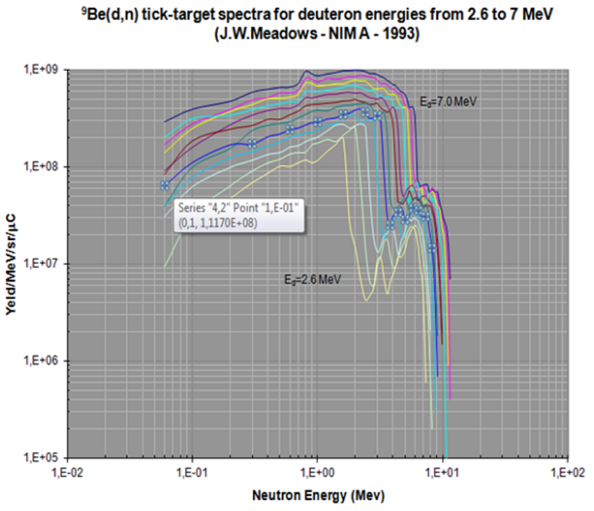

Figure 12.25: energy spectra of the neutron beam delivered by the CN line of the INFN-LNL) measured at some meaningful locations around the detector

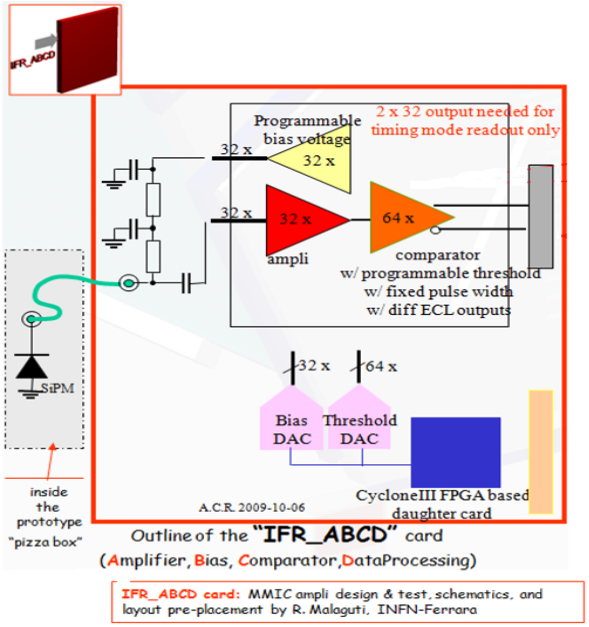

Figure 12.28: basic features of the "ABCD" card designed for the IFR prototype readout

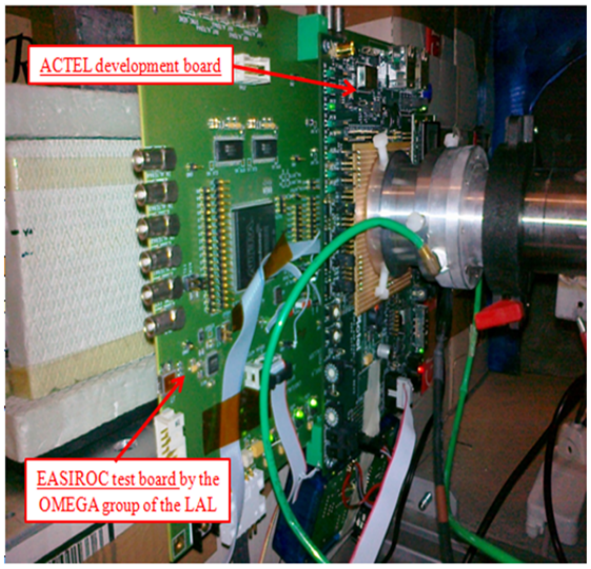

Figure 12.26: irradiation test setup at the CN facility of the INFN Laboratori Nazionali di Legnaro

which would, in Super$B$, be performed by the Experiment Control System (ECS): ambient temperature acquisition, calculation and download to the ABCD DACs of new set points for the bias voltages to stabilize the SiPM gain against the operating temperature variation [4].

- The Fermilab beam tests of the IFR prototype have demonstrated, among other things, that connecting the SiPMs to the front end cards by means of long (4m) coaxial cables, although not optimal, was possible and resulted in a reliably operating system.

total integration time (sec)	60683			
total charge (uC)	4104			
^{9}Be(d,n) thick target yield at 0 angle (YIELD/sr/uC) (ref. 13.5.1_r15)	1,017E+09			
	ACTEL A3PE250-PQ208			EASIROC
distance from source (mm)	7			20
total fluence at the target (neutrons/cm^2)	6,118E+12			1,033E+12
total fluence at the DUT (neutrons)	**4,955E+12**			**1,694E+11**
	CONFIGURATION MEMORY BITS	SRAM BITS	FLIP FLOP	FLIP FLOP
total memory element monitored	N.A.	32768	5824	456
number of SEU detected	**0**	**752**	**26**	**0**
number of SEL detected	**0**			**0**

Figure 12.27: results of the irradiation tests at the CN of the INFN Laboratori Nazionali di Legnaro

- This result supported the current baseline choice of locating the SiPMs near the scintillator bars and far from the front end cards, so that these last can be installed at more convenient locations.

An ASIC based front end readout

The COTS-based design of the "ABCD" card met goals such as short development time and flexibility (especially needed for tuning the parameters of the channels to be read out in the "timing" mode, cfr. the "white book", [20]) but it wouldn't be convenient for large volume production.

A search for existing ASICs suited for "binary mode" processing of SiPM signals was started and a good candidate was found in the "*Extended Analogue Silicon pm Integrated Read Out Chip*" or EASIROC which had many features already suited for the IFR readout application ([16], [17]); Fig. 12.29 shows a block diagram extracted from the EASIROC datasheet. The

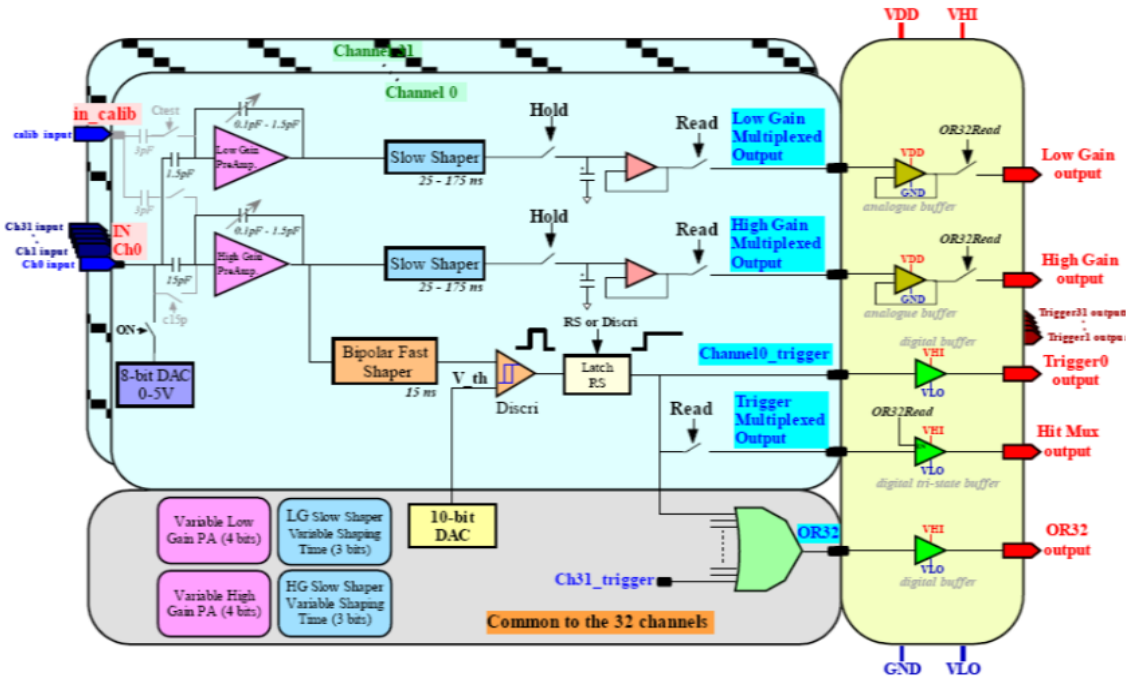

Figure 12.29: EASIROC block diagram developed by the OMEGA group of the LAL, Orsay, France

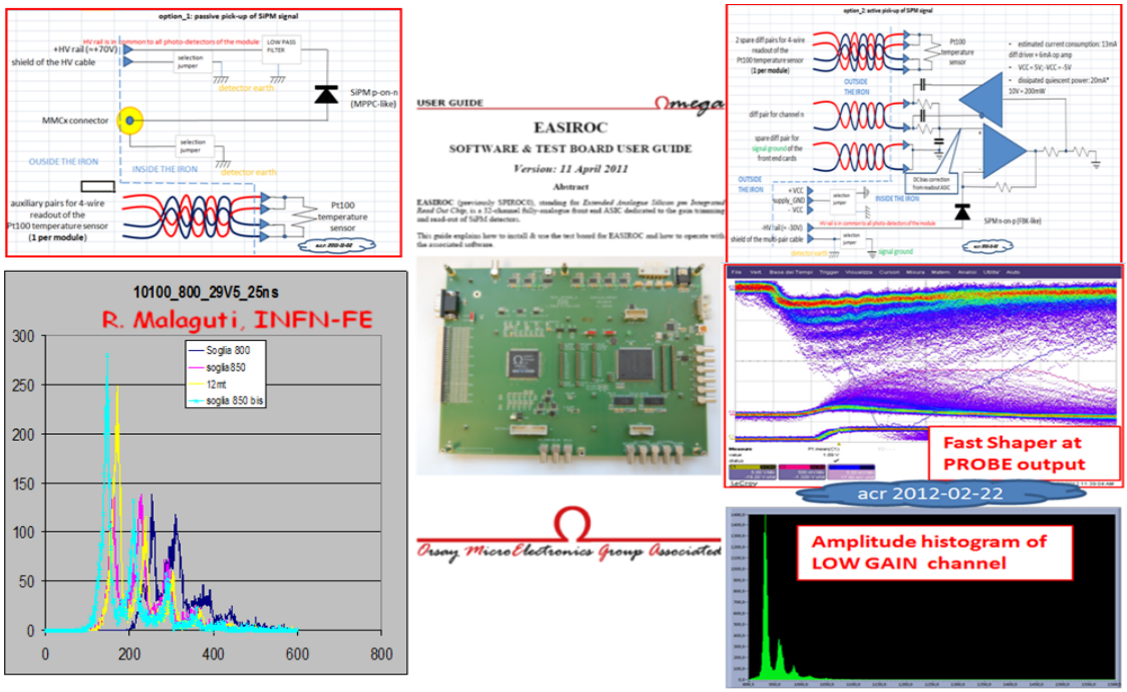

Figure 12.30: Amplitude histograms of signals processed by the EASIROC; SiPM connected with coaxial cables up to 12 m (left option) and with one differential pair of a high density cable 8 m long (right option)

EASIROC has been used, thanks to the test board and utilities provided by the OMEGA group, to test different SiPM technologies and coupling schemes [21]; Fig. 12.30 shows, for instance, pulse height histograms obtained from a 1 mm^2 SensL SiPM connected to the EASIROC via:

- different lengths of coaxial cables, up to 12m (left option)
- one differential pair of a high density, double shielded, multi twisted pair cable 8m long (right option)

The features of the EASIROC which would suite the IFR readout application are:

- the integration of 8 bit DACs, one per channel, for "low side" adjusting the bias voltage of the SiPM
- one fast (15 ns peaking time) shaper stage for each channel driving the "trigger" comparators
- the integration of a 10 bit DAC, common to all channels, for setting the threshold of the fast "trigger" comparators
- the availability of all 32 "trigger" outputs at the I/O pins (with single ended LV-TTL level) of the EASIROC
- low power consumption
- no sign of performance degradation or SEE detected during or after the irradiation tests descried above

The suitable specifications listed above are partially counterbalanced by others features which make the EASIROC not quite usable as it is, the most important of which being the 15ns peaking time of the fast shaper: a lower value is necessary to cope with the increasing dark count rate for SiPMs operating in the Super$B$ radiation environment.

As the IFR collaboration has been growing in the last year to include groups experienced in VLSI design ([22], [23], [24], [25], [26], [28], [29]), the development of an ASIC implementing the front end stages of the IFR readout system has become within reach; the EASIROC and an auxiliary flash based FPGA could still be considered as building blocks for a backup solution.

The new IFR front end ASIC should implement a set of basic features:

- a preamplifier and shaper chain suited for positive and negative input signals characterized by a linear response up to about 100 times the peak amplitude of the signal from a single photoelectron and a peaking time not larger than 10ns to minimize the pulse pile-up effects at high input rates
- individual DACs to set, with a few mV resolution, the DC level of each input and thus the "low side" bias voltage for the DC coupled SiPM; the current drive of the DAC should be designed considering the increase in dark current of irradiated SiPMs
- a fast comparator design, possibly differential to reduce the switching noise; some of the digital outputs should be routed to I/O pads
- one threshold setting DAC with a resolution of at least $\frac{1}{4}$ of the single p.e. signal and a linear range not larger than $\frac{1}{4}$ of the linear dynamic range
- a configurable test pulse injection circuits
- a slow control interface logic: a simple serial protocol should be implemented in order to perform write and non destructive readback to/from all register controlling the ASIC's programmable features
- a clock interface unit: to avoid the need of on-chip PLLs the ASIC will receive an LVDS clock with a frequency multiple of the experiment clock to derive all on-board timing signals; a suitable reset signal should also be foreseen
- a trigger primitives generator: a LUT based block driving two trigger outputs

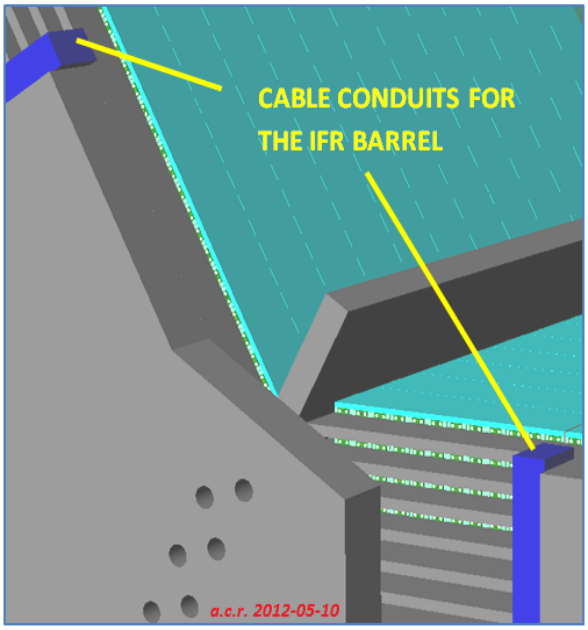

Figure 12.32: The IFR cable conduits for 2 sextants

- SEU protection through TMR or Hamming coding for all key registers and state machines in the ASIC

and a set of application specific features such as:

- a configurable latency buffer: a dual ported memory whose width would be equal to the number of channels and whose depth would be determined by the trigger latency time interval. The constant (but configurable) offset between the write pointer and the read pointer would equal the trigger latency time expressed in terms of clock periods
- a trigger interface: a trigger matching logic would detect a trigger pulse from the experiment, wait for the relevant data to be extracted from the latency buffer and subsequently forward it to the output serializer
- a set of low power serializers clocked by the input clock (which has a pace multiple of the experiment clock) needed to transfer the trigger matched data to the downstream "data collector" units. Serial output data could be 8b/10b encoded to allow the usage of DC-balanced AC coupled transmission links

The features listed above are differentiated into a first set, mainly analog, and a mainly digital second set to point out that it might be convenient to implement the two lists of functions in two different ASICs, to increase the flexibility of the overall system. Fig. 12.31 presents a block diagram of the new IFR readout ASIC and its connection to the SiPMs in the detector module; an IFR ASIC with a modularity of 32 channels would be able to readout all SiPMs in one module of the barrel. As shown in the inlay of Fig. 12.31 a ribbon-coaxial cable, mass terminated to a high density connector, could be used to carry the signals from the sensors to the IFR readout ASICs and the ancillary components on the IFR front end cards. At the right side of the IFR ASIC diagram one can find the input and output ports which would connect the IFR ASIC to the downstream "data merger" cards.

Location of the front end stages of the IFR readout system The SiPMs would be installed, in the baseline design, directly on the scintillator bars and thus distributed at different locations inside the modules. The baseline design foresees, instead, to install the ASIC-based front end stages outside the modules, at close but accessible locations. The reason behind this choice is that even if we were to install the front end ASICs inside the modules we would not still be able to directly connect (in order to minimize the signal/noise ratio) the SiPMs to the ASICs but, in turn, we would make it more difficult to remove the heat dissipated by the front end and we would make it impossible to access the front end cards, to replace faulty ones for instance, without disassembling large parts of the IFR structure. Fig. 12.32 is a detail of the IFR barrel which shows the position of two of the 5" x 3" conduits through which the IFR detector signal and power cables are routed.

The printed circuit board featuring the front end stages of the IFR signal processing chain could be located in these cable conduits; they

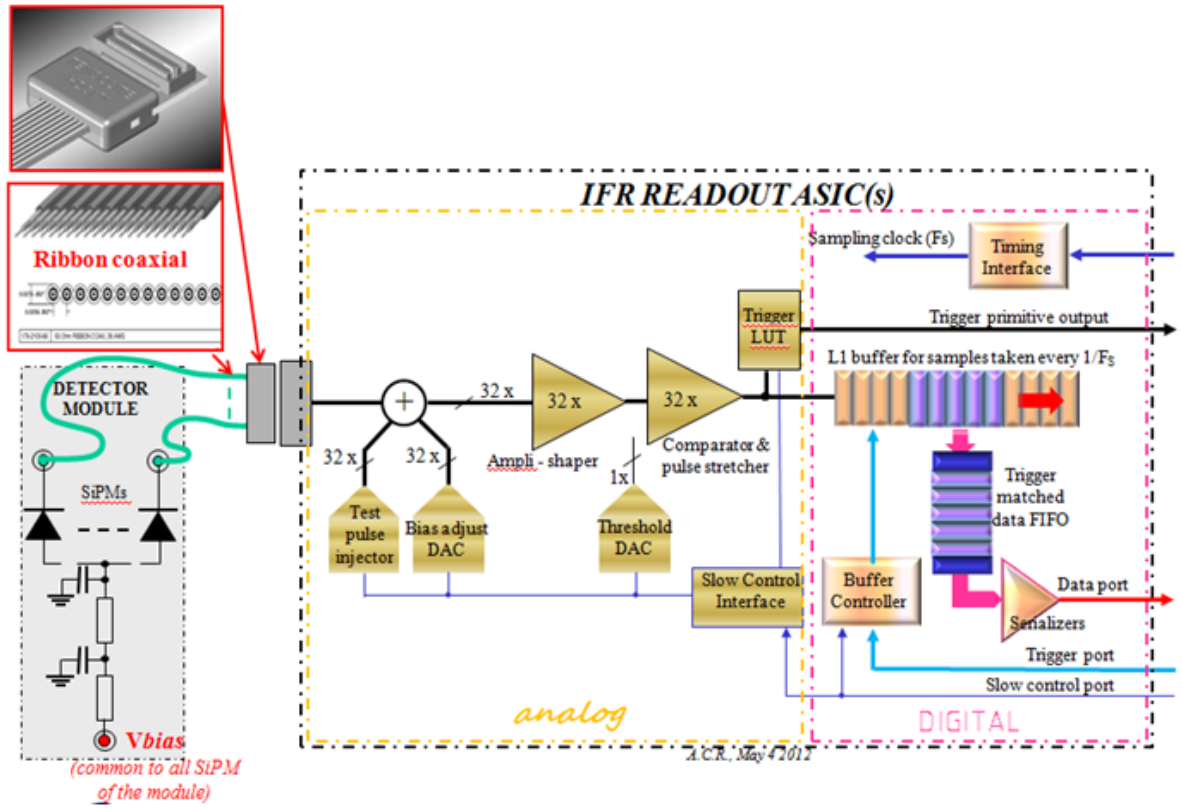

Figure 12.31: Block diagram of the IFR readout ASIC

would be accessible, if needed, without removing structural elements of the IFR magnetic flux return. Fig. 12.33 shows a section of one IFR cable conduit with a stack of 4 boards in evidence. Each IFR front end board could host 2 ASICs with 32 input channels each and since the IFR modules in the barrel are equipped with 32 SiPM at most, a stack of 3 to 4 IFR front end cards can handle all SiPMs installed in an active layer; 9 active layers are foreseen in the IFR detector.

All signals to and from the 2 front end ASICs on a board are coming from the "data merger" cards downstream, physically located as close as possible to the end of the cable conduit emerging from the Super$B$ spectrometer, as illustrated in the next paragraph. The interconnection cables are shown on the right side of the figure: they are double shielded, 17 pair, Amphenol SpectraStrip part number 425-3006-034 fitted with connectors by KEL (part no. KEL 8825E-034-175D); the mating connectors on the front end and the data merger PCBs are KEL 8831E-034-170LD. Not shown in Fig. 12.33 are the power cables for the SiPM bias (one common bias voltage per detector module) and the front end card voltage supply.

The section of the cable conduit can accommodate all boards and cables needed for the 9 active layers of each barrel sextant. Not shown in the picture are also the copper pillars which are foreseen to build a thermal conduction path from the IFR front end card to the IFR steel to which the cable conduit is fastened. In alternative to using ribbonized coaxial cables, the individual coaxial cables carrying the SiPM signals from one module are soldered onto a suitable interface PCB as shown in Fig. 12.34. The multi coaxial assembly shown in this 3D drawing features a SAMTEC QSE-20-01-F-D high density connector which mates to a QTE-020-01-F-D installed on the IFR front end PCB.

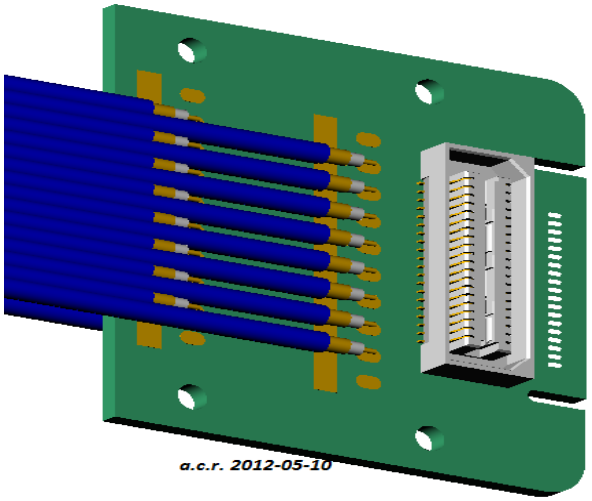

Figure 12.34: Detail of the multi coaxial connector assembly

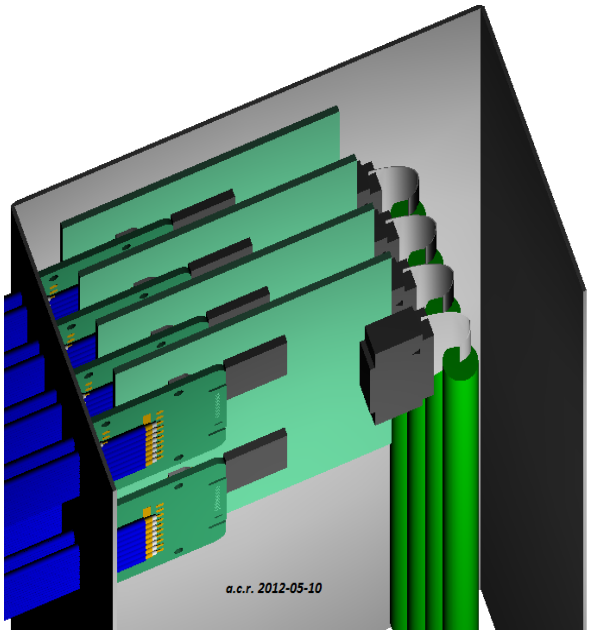

Figure 12.33: Detail of front end cards installed in the IFR cable conduit

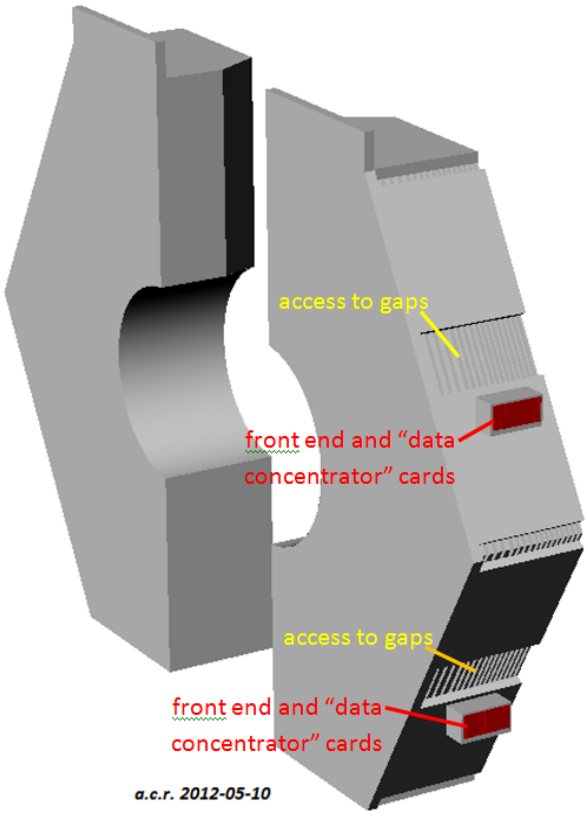

Figure 12.35: Perspective view of IFR endcaps

The description above concerns the instrumentation of the barrel section of the IFR detector. Fig. 12.35 below shows the perspective view of a pair of endcaps: the yellow callouts indicate the openings in the side lining steel through which the signal and power cables for the IFR modules can be routed. The signal emerging from these openings are routed to the crates indicated by the red callouts. For the endcap section of the IFR, the front end cards carrying the IFR read out ASIC could be installed directly in the crate and connected to the "data merger" cards through the crate's backplane interconnections.

The IFR "data merger" crates The IFR front end cards are linked to the "data merger" cards from which they receive the timing and trigger signals and to which they confer the trigger matched data. Fig. 12.36 shows the main functions performed by the units installed in a data-merger crate:

- FCTS interface: the key element of this functional unit is the FCTS receiver module which is linked via optical fiber to the Super*B* Fast Control and Timing System (FCTS). The FCTS interface unit fans out to the IFR front end cards the timing (clock and reset) and the trigger commands decoded by the FCTS protocol receiver

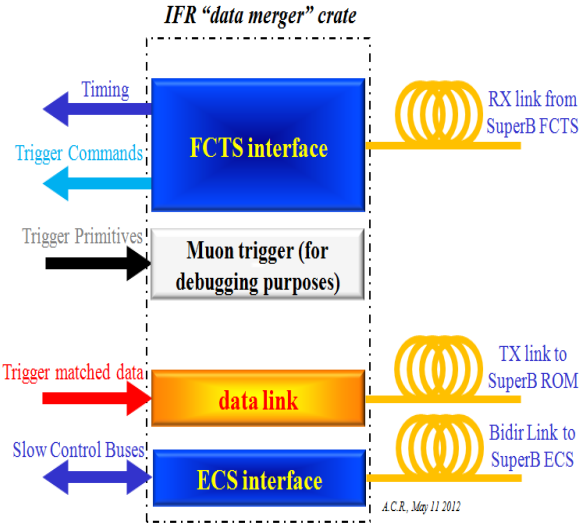

Figure 12.36: Main functions performed by the electronic units in the data-merger crate

- Muon trigger module: this unit receives the trigger primitives generated by the IFR front end cards and combines them to generate a muon trigger for local debugging purposes
- data link: each data-merger crate is supposed, according to the baseline design, to drive a suitable number of data links (4 for the barrel section, 2 for the endcap ones) to the ReadOut Modules (ROM). The data forwarded to the ROMs results from the merging of the trigger-matched data streams produced by the front end cards. A suitable modularity could be of 2 ouput data link per concentrator board; this functional unit will rely on the common TX link driver module to reliably forward data to the ROM even in the radiation environment of Super*B*
- ECS interface: the key element of this functional unit is the ECS receiver module which is linked via optical fiber to the Super*B* Experiment Control System (FCTS). The ECS interface unit controls the whole tree of slow control slave nodes implemented in the front end cards

For the endcap section of the IFR the physical links between the front end and the data merger boards consist of the differential lines provided by the backplane in which the front end and the data-merger units are installed. An ATCA or Micro-TCA crate [26] provide a large number of such interconnection resources and the IFR data merger crates will most likely conform to one of the two above mentioned TCA specifications.

Because of the Super*B* radiation environment it is likely that in the IFR data merger crates the standard "intelligent platform management" controller will be replaced by some ad-hoc interface card hooked to the Super*B* ECS. The power supply units of the IFR data merger crate would have to be radiation tolerant or simply be installed at a larger distance from the crates; the xTCA crates integrated "power entry modules" are fit to both options. The xTCA fans will have to be tested for operation in a radiation environment or replaced with qualified units; the convection cooling specification could be somewhat relaxed, on the other hand, since the data merger crates will most likely dissipate much less than the allowed 150W/200W per slot. Fig. 12.37 shows the proposed location for one of the barrel data-merger crates.

Two other such crates would be placed at 120° on the forward end of the barrel while three crates will be located in a similar arrangement at the backward end of the barrel. Each data-merger crate serves two sextants.

Services needed for the IFR readout in the experimental hall The elements of the IFR readout system, from the detector on, need to be properly powered, monitored and cooled. This paragraph summarizes the main requirements for a readout system built according to the baseline design (which have been described in more detail in the "Super*B* integration questionnaire"):

- SiPM supply voltage: all the SiPMs of a detector module are connected to an ASIC

input with one terminal and to a common bias voltage bus with the other. A total of 492 power supply channels are then needed for biasing the SiPMs; the channel should feature a programmable output voltage ranging from 0 to 100V (value and polarity depend on the final SiPM technology chosen) and should have a compliance of 25mA. The power dissipated by the SiPMs in the whole IFR under nominal operating conditions is of the order of a few tens of Watts

- IFR front end cards: a very coarse estimation of the power consumption for the IFR front end cards could be of 2W at 3.3V. Lower core voltages for the ASIC could be derived from on-board by means of low-drop out regulators; the radiation tolerance of suitable LDO regulators is being characterized. The number of modulo-32 processing units necessary to readout the IFR detector is **384 for the barrel** and **324 for the endcaps**. In the baseline design each front end card carries 2 ASICs in the barrel and, possibly, 4 ASICs in the endcaps, so the number of individually programmable power supply channels would be **192 for the barrel** and **81 for the endcaps** The compliance of these channels should be at least 1A.
- barrel cooling: the power dissipated by the SiPMs and the front end cards in the barrel could be in the order of 700W. Assuming that a cooling system like that designed for the *BABAR* flux return system will also be foreseen for the Super*B* detector, the power dissipated by the front end stages in the IFR steel should be taken into account for properly dimensioning the chiller system

12.2 Electronics Infrastructure

12.2.1 Power supplies, grounding and cabling

Gianluigi Pessina

12.2.1.1 Power Supply to the Front-end:

The voltage supply system is normally composed by a cascade of AC/DC, DC/DC and linear regulators. Depending on the power dissipation and noise requirements some of the above elements can be avoided. The supply system of an accelerator-based experiment has known additional constraints to be satisfied. The large particle fluence and the presence of a strong magnetic field can have an impact on the aging and behavior of the electronic equipment. The first constraint is addressed only by adopting radiation hardened (rad-hard) technology and using suitable layout recipes for the monolithic circuits. This is common to all the devices that sit in the detector area. Magnetic field has generally less impact except for AC/DC and DC/DC converters that need to use inductances and/or transformers, having ferromagnetic cores.

Power Supply outside the detector area: In the following we will describe our solution, able to face the above constraints. The strategy we

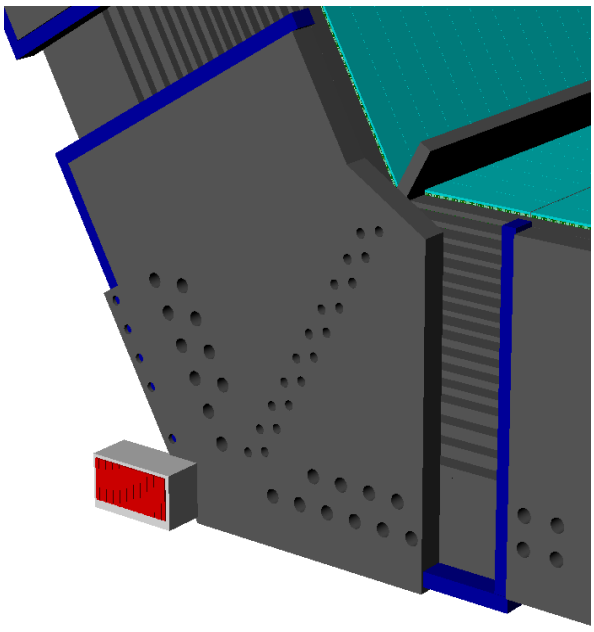

Figure 12.37: The location of one of the 6 data merger crates for the barrel

would adopt is to minimize the number of regulators in the detector area. The distance between the regulators and the front-end can be a few tens of meters. The energy the cable is able to store in its inductive component can be large and attention must be adopted to protect the connected electronic equipment in case of accidental short circuit to ground. Fig. 12.39 shows an example of the recovery from a short circuit of $50\,m$ cable with $4\,mm^2$ section. The short circuit current was limited to $20\,A$. A N-MOS, IPP50CN10NG, with $50\,m\Omega$ ON resistance simulated the short circuit and it breaks down above about $100\,V$ when in open state, that explains the reason of the clipping. The measurement has been taken in the worst condition of no applied load. It is clear from this that an accidental short circuit is very critical in producing possibly destructive damaging.

We have found that most of the cables with 3 or 4 poles and cross-section between $1.5\,mm^2$ and $4\,mm^2$ have an inductance per unit length, L_M, of the order of $0.7\,\mu H/m$, from DC to few hundred of KHz. Calling I_{short} the maximum delivering current available from the power supply and l the cable length, then:

$$E_{nergy} = \frac{1}{2} L_M l I_{short}^2 \qquad (12.1)$$

is the available energy driven to the load in case of accidental short circuit. To limit the voltage at a safe level our straightforward solution is to add in parallel to the load a capacitance able to store such released energy. This can be done if we satisfy that:

$$\frac{1}{2} C_{lim} V_{over}^2 = \frac{1}{2} L_M l I_{short}^2 \qquad (12.2)$$

where V_{over} is the maximum voltage that must not be exceeded and C_{lim} is the capacitance whose value must be chosen to satisfy the eq. with the given voltage V_{over}. As an instance, with $50\,m$ of cable length, $I_{short} = 20\,A$ and $C_{lim} = 160\,\mu F$ the maximum over voltage excursion would be less than $9.5\,V$.

Adopting the introduced technique a hub with a distribution to several shorter cables can be implemented as shown in Fig. 12.40. A large value capacitance, C_H, is at the end of the cable that connects the DC/DC regulators from the outside to the inside of the detector area. In our example we continue with considering $50\,m$ of cable length and $C_H = 160\,\mu F$. From this point several shorter cables, or stubs, connect the various parts of the detector or sub-detector front-end. To save space, the sections of these last cables can be smaller since they have each to manage a smaller current. At the end of each of these stubs, $5\,m$ in our present example, a smaller value capacitance, C_{Fx}, $(33\,\mu F)$ is connected. In case of short at the end of a stub all the current flows into it. But as soon as the short is opened capacitance C_H absorbs the energy of the longer cable, while the energy of the shorted stub is managed by the corresponding capacitance C_{Fx}. Fig. 12.41 shows that the signal at the end of the $50\,m$ cable has an over voltage of only about $10\,\%$. The maximum current was $20\,A$ and it can be seen that the baseline before the short is released is about $2\,V$, the dropout generated by the $20\,A$ current across about $0.1\,\Omega$ given by the sum of the stub (as a

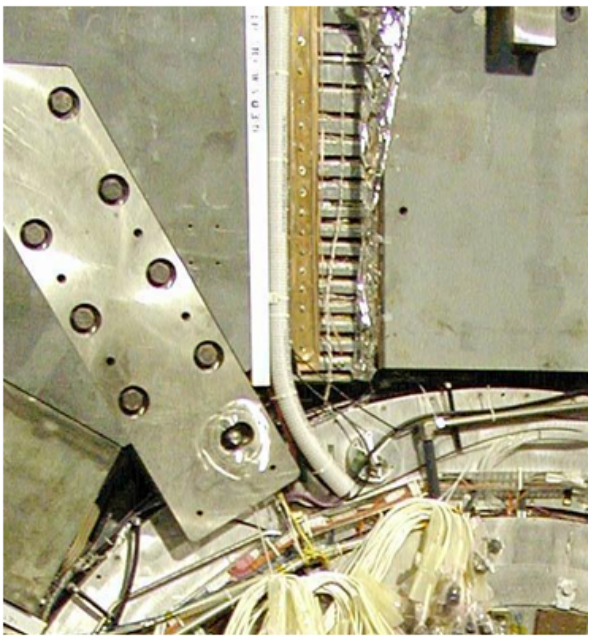

Figure 12.38: A picture from *BABAR* showing one of the elements of the cooling system for the IFR steel

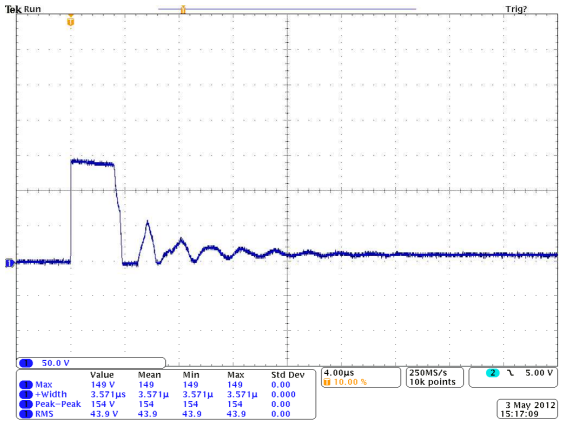

Figure 12.39: Signal at the end of a 50 m cable after a short circuit. The clipping at 150 V is due to the breakdown of the MOS switch used.

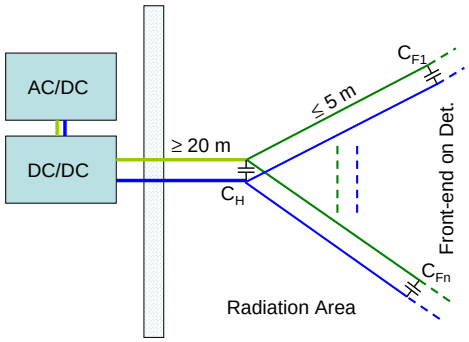

Figure 12.40: Possible layout for a sub-detector for what concerns voltage supply.

reference a section of $1\,mm^2$ has an impedance of about $16\,\Omega/Km$) and the ON resistance of the N-MOS. Fig. 12.42 shows the over voltage present at the stub end where the short is generated and released; again the over voltage is contained within about 10 %. As it can be appreciated, the baseline that precedes the release of the short is about $1\,V$, namely $20\,A$ developed across the about $50\,m\Omega$ ON resistance of the N-MOS. In the test setup of the laboratory we implemented 2 stubs and Fig. 12.43 is the signal at the stub end where the short circuit was not present. Again the over voltage is respecting the safety conditions. The principle applies well also if a low regulated voltage is considered and Fig. 12.44 is an example of release from a short of more than $25\,A$ on a $5\,m$ cable ($2.5\,mm^2$ of cross-section) loaded with $160\,\mu F$ capacitance.

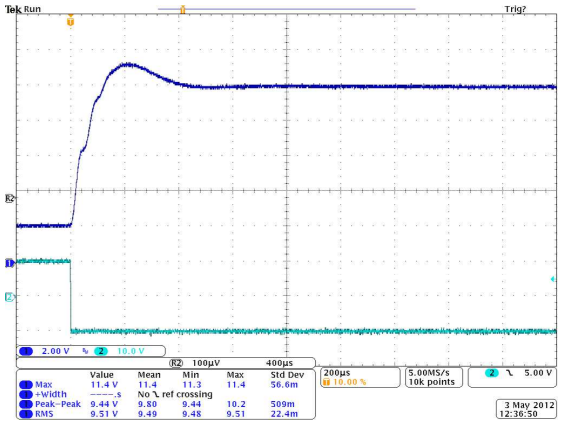

Figure 12.41: Signal at the end of a $50\,m$ cable (blue line) after that a short circuit is generated at one end of a stub. The $50\,m$ cable is loaded with a $160\,\mu F$ capacitor and the short current is $20\,A$; the supply voltage is $10\,V$. Every stub is loaded with $33\,\mu F$. The green line is the voltage driver at the gate of the switched N-MOS.

The suppression capacitance must show a very small series resistance and inductance. Capacitors with plastic dielectric such as Metalized Polypropylene Film satisfy this condition. As an example the $160\,\mu F$ we have adopted for the test has only $2.2\,m\Omega$ of series resistance, but, being big in volume, it shows a series inductance of a few tens of nH. To compensate for this last effect a smaller value (and volume) capacitance ($1\,\mu F$) is put in parallel, able to account for the fast part of the rising signal. Metalized Polypropylene Film capacitances have a range of values limited to a few hundreds of μF. As a consequence, a limited value of current per cable, $10\,A$ to $20\,A$, results in a good compromise. Many commercial regulators, also in the form of the so called bricks and half-bricks layouts, are available on the shelf at low cost. This strategy is particularly usefully for minimizing the

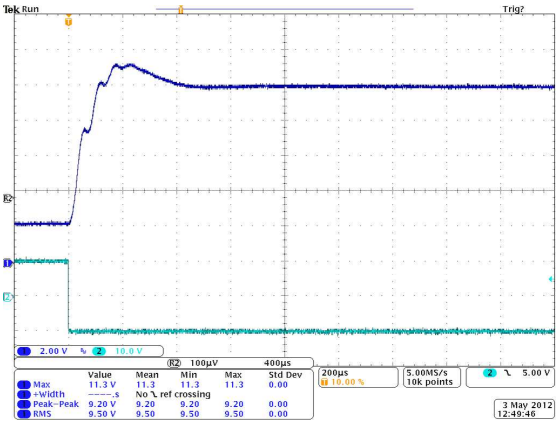

Figure 12.43: Signal at the end of a stub of Fig. 12.40 after a short circuit (blue line) happened at another stub. Two stubs were present in the test setup. C_H is $160\,\mu F$, the C_{Fx} are $33\,\mu F$ and the short current is $20\,A$; the supply voltage is $10\,V$. The green line is the voltage driver at the gate of the switched N-MOS.

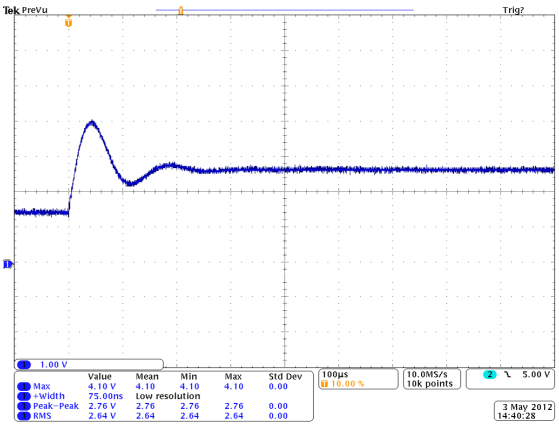

Figure 12.44: Short circuit release on a $5\,m$ cable with $2.5\,mm^2$ cross-section.

dropout along the cable and it is of particular concern when a low voltage is needed.

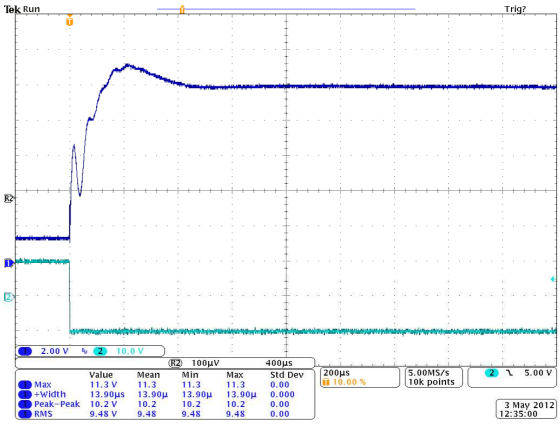

Figure 12.42: Signal at the end of a stub of Fig. 12.40 after a short circuit (blue line). Two stubs were present in the test setup. C_H is $160\,\mu F$, the C_{Fx} are $33\,\mu F$ and the short current is $20\,A$; the supply voltage is $10\,V$. The green line is the voltage driver at the gate of the switched N-MOS.

We cannot forget that an over-voltage can happen due to a possible malfunctioning of the regulator. To reject rapidly and with good precision this effect a stack of fast diodes is a good choice. For instance with a voltage supply of $10\,V$ the series connection of about 20 diodes allows to maintain the safe operating condition provided that they are in contact with a heat sink in case the problem persists for a while. The location of the stack of diodes can be close to the regulator and space occupation would not constitute a problem.

Noise cabling and shielding: The combination of the inductance component of the wires and the suppression capacitance has a twofold utility as it behaves also as a low pass filter. Fig. 12.45 shows the noise at the end of the $50\,m$ cable plus $2 \times 5\,m$ stubs when $160\,\mu F$ plus $2 \times 33\,\mu F$ capacitances load the combination. The applied supply voltage was $10\,V$ and the load $3.3\,\Omega$. In this case a standard commercial regulator has been used. Very low noise DC/DC regulators have been designed [30] and Fig. 12.46 shows the noise performance under the same conditions. Even better performances can be obtained by cascading the DC/DC to a linear regulator of very good quality [31].

Low noise results are obtained if care is considered on the type of cables adopted. In all the measurements described so far cables used

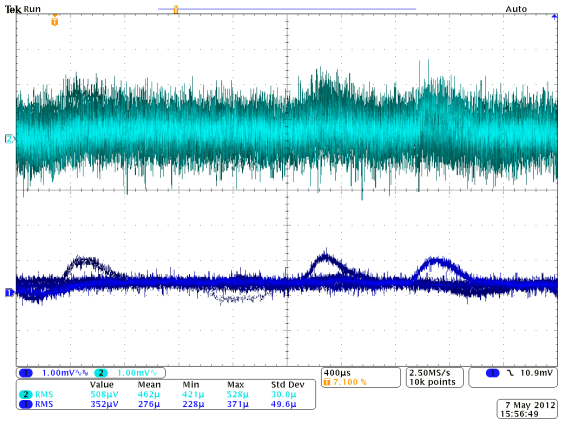

Figure 12.45: Noise after $50\,m$ cable loaded with $160 + 2 \times 33\,\mu F$ capacitance at $10\,V$ and with $3.3\,\Omega$ load. Upper noise is with the full $350\,MHz$ bandwidth of the oscilloscope, Lower noise has the scope bandwidth limited to $20\,MHz$.

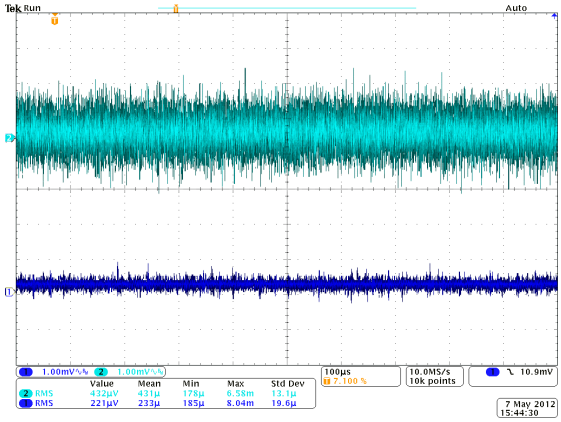

Figure 12.46: Very low noise DC/DC regulator [30]. Measurements condition and setup as for Fig. 12.45

were all armored. This precaution allows to shield the supply voltage from outside disturbances but also to avoid to create disturbances to the outside world. We intend to adopt this kind of layout solution for the final experimental setup. In addition, where needed, we intend to add a double shield by inserting the cables inside a tubular copper mesh.

The connection scheme of Fig. 12.40 is, in a natural way, suitable to route ground. Let's suppose that the ground of every detector or sub-detector to which the cables are routed have their ground isolated. Then, we can route a tinned copper wire (or a copper bar) very close to the power supply cables so as to suppress area sensitive to EMI interferences. Such a routing scheme allows a 'star' connection with only one ground contact node (we remember that AC/DC and DC/DC regulators are floating), that is the standard requirement.

Shielding is considered for whose region were the electric or magnetic field can affect the performances. The shields can be considered for the whole sub-detector or individually on a channel by channel basis. This is particularly true with the effect of magnetic field on those detectors that extend on a large volume, such as photomultiplier tubes (PMTs). Past experience showed that in these cases a local shield implemented with mu-metal around every PMT is essential.

Power Supply in the detector area: We are considering the opportunity to use both DC/DC and linear regulators inside the detector area. Inductances and transformers cannot be based on a ferromagnetic coil. As a consequence they are limited in range of values and the switching speed of the DC/DC must be very large. This is the case for the monolithic DC/DC regulator we are considering [32], developed in $0.35\,\mu m$ CMOS technology based on rad-hard layout and components, and having a switching frequency of the modulator of a few MHz, which allows the use of a coil-free inductance. Based on the same technology a linear regulator is also available [33].

12.2.1.2 High Voltage Power Supply to the Detectors:

High voltage power supplies suffer of similar problems as AC/DC and DC/DC regulators. As a consequence these regulators must be located outside the detector, sub-detector area (we do not know about any commercial rad-hard high voltage regulator). The energy released to the load in case of accidental short circuit would be not an issue thanks to the fact the, normally, such regulators have their driving current lim-

ited to a few hundred of μA. As an instance, if we load the line with a $1\,nF$ high voltage capacitor and considering $1\,A$ the short circuit current we expect an over-voltage of about $0.2\,V$. Finally, commercial over-voltage protectors based on gas discharge tubes are very efficient and fast.

12.2.2 Grounding and Shielding

This section has been incorporated in the Power Supply section

12.2.3 Cable Plant

This section has been incorporated in the Power Supply section

Bibliography

[1] A. Sharma, F. Sauli, Nucl. Instr. and Meth. A 350 (1994) 470.

[2] C. Avanzini et Al. Nuclear Instruments and Methods in Physics Research A449 (2000). 237-247.

[3] P.R.Burchat and John Hiser Studies of helium gas mixtures in drift chambers SLAC-PUB-5626 SCIPP 91/25 September 1991.

[4] Gianluigi Cibinetto, *Something about the prototype*, SuperB Workshop and Kick Off Meeting, Elba, May 31 2011

[5] Gianluigi Cibinetto, *Beam Test: data for analysis*, I SuperB meeting, London, Sep 15 2011

[6] Valentina Santoro, *IFR Background Report*, III SuperB meeting, LNF-Frascati, Mar 21 2012

[7] Pierre Jarron, CERN 1211 Geneva 23 Switzerland, *Radiation tolerant electronics for the LHC experiments*, Proceedings of the 4th Workshop on Electronics for LHC Experiments, Rome, Sept 1998, p. 7

[8] Federico Faccio, CERN 1211 Geneva 23 Switzerland, *Radiation effects in devices and technologies*, IN2P3 school, May 2005

[9] *ATLAS Policy on Radiation Tolerant Electronics: ATLAS Radiation Tolerance Criteria*, http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/WWW/RAD/RadWebPage/ATLASPolicy/Appendix_1.pdf

[10] W. Dabrowski (AGH University of Science and Technology, Krakow, Poland), *Challenges and benefits of designing readout ASICs in advanced technologies*, Nuclear Instruments and Methods in Physics Research A 579 (2007) pp. 821-827

[11] M.Angelone, M.Pillon, R.Faccini, D.Pinci, W.Baldini, R.Calabrese, G.Cibinetto, A.Cotta Ramusino, R.Malaguti, M.Pozzati, *Silicon photo-multiplier radiation hardness tests with a beam controlled neutron source*, Nuclear Instruments and Methods in Physics Research A 623 (2010) pp. 921-926

[12] Flavio Dal Corso (INFN Padova), *Studies of SiPM @ Padova: Neutrons irradiation at LNL 9-13 Oct 2009*, XI SuperB General Meeting , LNF, Frascati, Dec. 1 2009

[13] Enrico Feltresi (INFN Padova), *Neutron Damage on SiPMs studies at LNL*, XV SuperB General Meeting Caltech, Pasadena CA, USA, Dec. 14 2010

[14] Flavio Dal Corso (INFN Padova), *Status of SiPM; studies @ Padova*, XVI SuperB General Meeting , LNF, Frascati, Apr. 4 2011

[15] A. Cotta Ramusino (INFN Ferrara), *SuperB IFR electronics: update*, 2nd SuperB General Meeting , LNF, Frascati, Dec. 15 2011

[16] Orsay MicroElectronics Group Associated (OMEGA) (LAL, Orsay, France), *EASIROC DATASHEET Version: 5*, April 2011

[17] Orsay MicroElectronics Group Associated (OMEGA) (LAL, Orsay, France), *EASIROC SOFTWARE & TEST BOARD USER GUIDE Version: 11*, April 2011

[18] James W. Meadows, Engineering Physics Division, Argonne National Laboratory, Argonne, Illinois, USA, *The $^{9}Be(d, n)$ thick-target neutron spectra for deuteron energies between 2.6 and 7.0 MeV*, Nuclear Instruments and Methods in Physics Research A 324 (1993) pp. 239-246

[19] A. Cotta Ramusino (INFN Ferrara), *SuperB IFR electronics: update on prototype electronics and IFR_DAQ*, XII SuperB Workshop - LAPP Annecy, Mar. 17 2010

[20] E. Grauges et al. [SuperB collaboration], *SuperB progress report – Detector*, arXiv:1007.4241,2010

[21] A. Cotta Ramusino (INFN Ferrara), *SuperB IFR electronics: update*, 3rd SuperB meeting, LNF, Frascati, Mar. 13 2012

[22] R. Mos, J. Barszcz, M. Jastrzb, W. Kucewicz, J. Młynarczyk, E. Raus, M. Sapor, *Front-End electronics for Silicon Photomultiplier detectors*, Electrical Review 11a (2010) pp. 79-83

[23] A.Baschirotto, G.Cocciolo, M.De Matteis, A.Giachero, C.Gotti, M.Maino, G.Pessina, *A FAST AND LOW NOISE CHARGE SENSITIVE PREAMPLIFIER IN 90 nm CMOS TECHNOLOGY*, Journal of Instrumentation, Jinst, V 7 C01003 pp 1-8 2012.

[24] G. Mazza et al. (Dipartimento di Fisica - INFN Torino), *A CMOS 0.13um Silicon Pixel Detector Readout ASIC for the PANDA experiment*, 2012 JINST 7 C02015 doi:10.1088/1748-0221/7/02/C02015

[25] G. Dellacasa et al. (Dipartimento di Fisica - INFN Torino), *A 130 nm ASIC prototype for the NA62 Gigatracker readout*, Proc. of the Int. Workshop on Semiconductor Pixel Detector for Particles and Imaging (Pixel 2010), Nucl. Instr. and Meth. in Physics Research, A 650 (2011) pp. 115-119

[26] A. La Rosa et al., *Ionizing radiation effects on a 64-channel charge measurement ASIC designed in CMOS 0.35 um technology*, Nucl. Instr. and Meth. in Physics Research A 593 (2008) pp. 619-623

[27] PICMG, AdvancedTCA PCI Express PICMG 3.4 Specification, May 2003

[28] M. Baszczyk, P. Dorosz, S. Głb, W. Kucewicz, M. Sapor, *Four channels data acquisition system for silicon photomultipliers*, Elektronika 12 (2011) pp. 28-31

[29] Paolo Carniti, Andrea Giachero, Claudio Gotti, Matteo Maino, Gianluigi Pessina, *An introduction to CLARO: A fast Front-End ASIC for Photomultipliers*, 2nd SuperB Collaboration Meeting, LNF Frascati, Dec 15 2011

[30] C. Arnaboldi, A. Bau, A. Giachero, C. Gotti, M. Maino, A. Passerini, and G.Pessina, *A Very Low Noise AC/DC Power Supply System For Large Arrays Of Cryogenic Detectors*, 2011 IEEE Nuclear Science Symposium Conference Record, pp. 791-793, February 2012.

[31] G. Pessina Rev. Sci. Instr. **70**, 3473, 1999.

[32] S. Michelis, B. Allongue, G. Blanchot, F. Faccio, C. Fuentes, S. Orlandi, S. Saggini, S. Cengarle, F. Ongaro, J. of Instrumentation, JINST, 7, C01072, 2012.

[33] F. Faccio, P. Moreira, A. Marchioro, S. Velitchko, *A radiation-tolerant LDO voltage regulator for HEP applications* , Conference proceeding of the TWEPP-2005, Valencia (Spain).