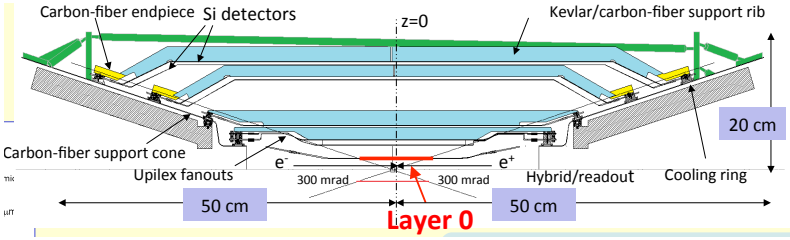
SVT - Update (I)

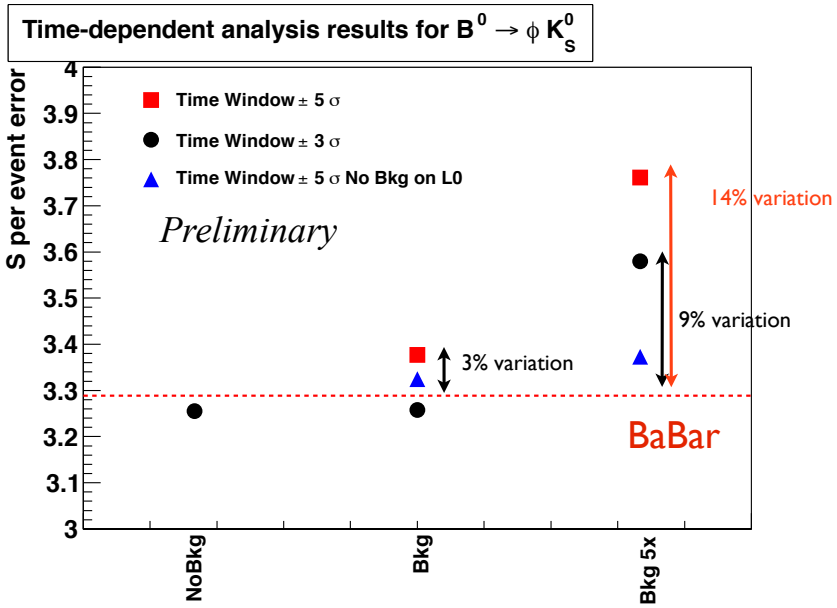


- Effects of background (nominal and x5) on detector performance being evaluated:
  - Back. From March official production used. New shielding configuration give only ~10% reduction in SVT layers.
- Efficiency reduction due to analog dead time evaluated for electronics: < 90 % in some layers with x5 safety
  - Small improvements reducing shaping time w.r.t nominal

Efficiency

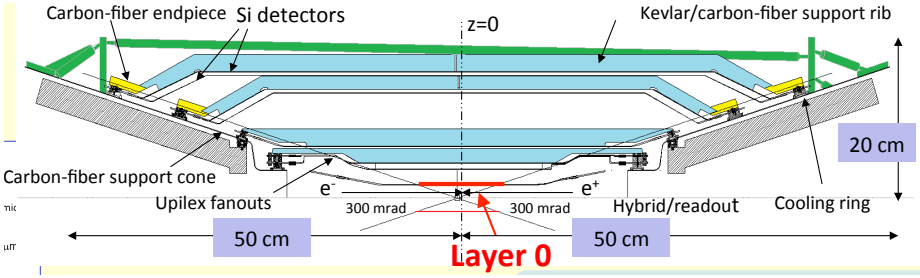
Layer	Peaking time (ns)	Bkg (%) (r-ϕ/z)	Bkg x5 (%) (r-ϕ/z)
L0	25	99/99	96/96
L1	100	98/98	88/89
L2	100	98/98	89/89
L3	200	95/95	77/86
L4	500	98/98	89/93
L5	1000	98/98	86/91

- Impact of background on performance due to resolution & efficiency deterioration evaluated with Fastsim: performance with striplets in Layer0 seems to be still reasonably good in presence of 5x bkg.
  - sizable effect on S per event error: 14% worsening with x5 bkg. Small change with nominal bkg (3%).



- Need to add the performance evaluated with Layer0 based on pixel (thin MAPS or "thin" hybrid pixel):
  - Pixel material budget higher → worse performance with no back. but deterioration wit back. expected to be marginal since pixel occupancy ~1/100 of striplets occupancy

SVT - Update (II)



- Effect of high occupancy on reconstruction still need to be evaluated: Fastim cannot be used, no time/manpower to do a real study for TDR.
  - In SuperB 3-15% strip offline occupancy and 2-5% cluster offline occupancy (x10 w.r.t. BaBar)
  - In BaBar 0.2-1% strip offline occupancy and 0.1-0.5% cluster offline occupancy.

Preliminary

Layer	View	Shaping time	S/N at the start of data taking	S/N in 75 ab-1	S/N in 75 ab-1 x5 bkg
1	phi	100	31	27	20
1	z	100	39	30	19
2	phi	100	29	27	21
2	z	100	37	31	21
3	phi	200	29	23	15
3	z	200	36	25	14
4	phi	500	22	19	13
4	z	500	27	22	14
5	phi	1000	23	20	15
5	z	1000	29	25	17

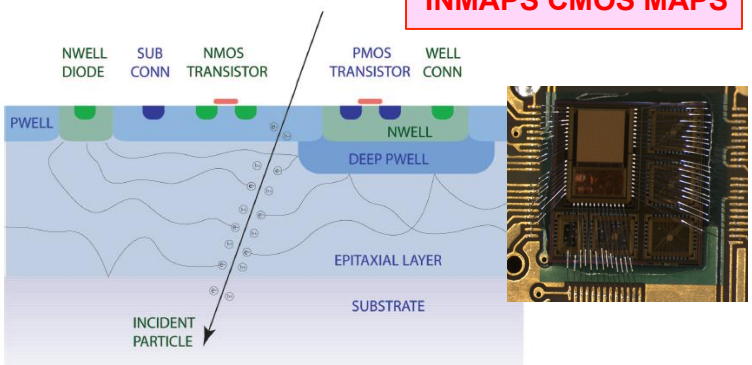
- Effect of radiation damage on sensor (increase on leakage current) and S/N degradation with the full life of the experiment (75ab-1 and x5) evaluated.
  - S/N a bit marginal with x5 safety
  - Could improve a bit selecting shorter shaping time after some accumulated damage
  - Start also to explore extra cooling to lower SVT sensor temperature & leakage current contribution

SVT - Pixel R&D

R&D on pixel: first results on new MAPS with INMAPS process: very promising option for thin pixel upgrade for Layer0.

- Noise and gain measured in good agreement with simulation:
  - ENC = 30 e- (~20% dispersion)
  - Gain=920 mV/fC (~10% dispersion)
- Standard functionality of new readout architecture verified in the two operation modes available on chip: data push & triggered.

INMAPS CMOS MAPS



- INMAPS CMOS process with quadruple well & high resistivity substrate to improve charge collection efficiency and radiation resistance

- Chips with 12 um high resistivity epitaxial layer (more rad hard) ready in June.
- Start the irradiation with neutrons during the summer and beam test in November.

SVT - TDR Status

- Good progress in the writing:
  - Almost all the sections in the svn repository (not final version!): ~35/70 pages
  - Writing on peripheral electronics and mechanics less advanced (starting this week)
  - Hope to have a complete document in 2 weeks for the internal editing

1. Vertex Detector Overview (10) – G. Rizzo still some text to be written
2. Backgrounds (4) – R. Cenci outline
3. Detector Performance Studies (6) – N. Neri almost completed
4. Silicon Sensors (6) – L. Bosisio still some text to be written
5. Fanout Circuits (6) – L.Vitale almost completed. working on text for L0
6. Electronics Readout (20)
   1. Readout Chips (8) –V. Re almost completed
   2. Hybrid Design (5) – M. Citterio working on text
   3. Data Transmission (5)– M. Citterio working on text
   4. Power Supplies (2) –M. Citterio working on text

   SVT DAQ (M.Villa) will be in the ETD section
7. Mechanical Support & Assembly (10) – S. Bettarini/F. Bosi outline/working on text
8. Layer0 pixel upgrade options (10) – L. Ratti almost completed
9. Services, Utilities (1)

SVT TDR in SVN

~ 35 pages