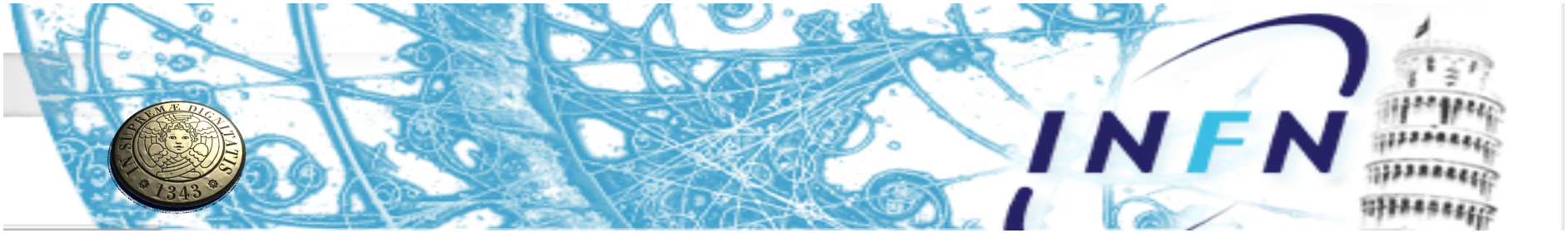
SVT Status Report

highlights from the SVT parallel sessions

S.Bettarini - Universita' di Pisa & INFN

On Behalf of the SuperB SVT Group



IV SuperB Coll. Meeting - Elba, Plenary session – 3 June 2012

SVT parallel sessions

16:00->*17:30* Parallel 1: SVT (Convener: Giuliana Rizzo (*PI*)) (Sala Maria Luisa) EVO meeting URL; EVO meeting information

16:00	Introduction & TDR status (15') (Slides)	Giuliana Rizzo (*PI*)
16:15	Update on activities in Strasbourg & tracking in high occupancy (20') (Slides)	Isabelle Ripp-Baudot (*IPHC, CNRS/IN2P3, Strasbourg*)
16:35	Update on background simulation (20') (Slides) → In MDI talk	Riccardo Cenci (*University of maryland*)
16:55	Fastsim performance studies (20') (Slides)	Nicola Neri (*MI*)

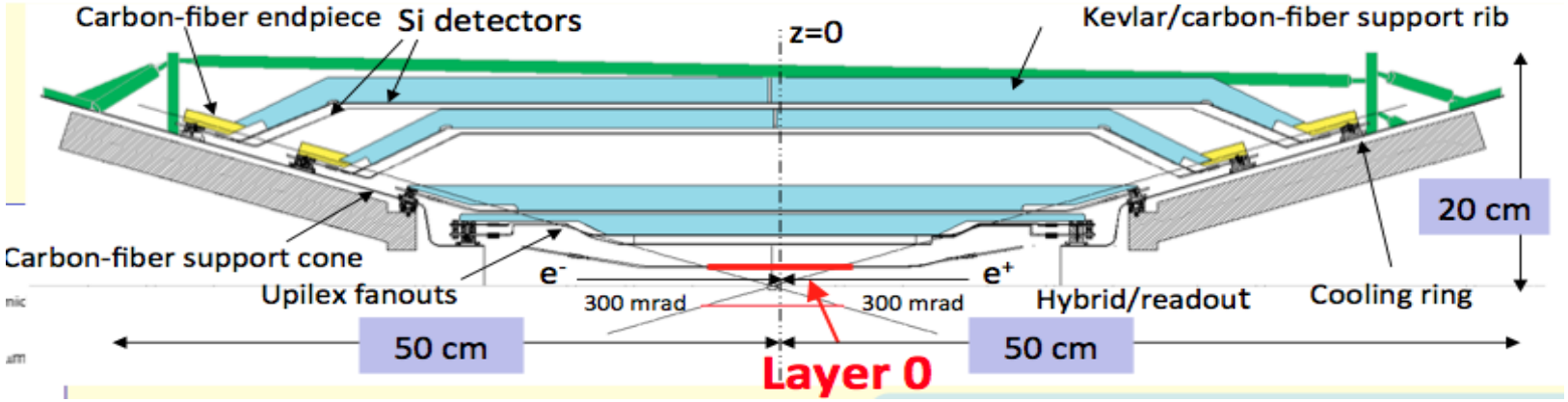
18:00->*19:40* Parallel 2: SVT (Convener: Giuliana Rizzo (*PI*)) (Sala Maria Luisa) EVO meeting URL; EVO meeting information

18:00	INMAPS chip results (20') (Slides)	Stefano Bettarini (*PI*)
18:20	INMAPS characterization in Pavia (15') (Slides)	Lodovico Ratti (*PV*) , Stefano Zucca (*PV*)
18:35	Update on FE chip performance inner layers (15') (Slides)	Massimo Manghisoni (*PV*)
18:50	Update on FE chip performance outer layers (15') (Slides)	Luca Bombelli (*MI*)
19:05	Update on sensor and fanout design in Trieste/Como (20') (Slides)	Luciano Bosisio (*TS*)

08:30->*10:30* Parallel 3: SVT (Convener: Giuliana Rizzo (*PI*)) (Sala Maria Luisa) EVO meeting URL; EVO meeting information

08:30	Update on HDI design and peripheral electronics (20') (Slides)	Mauro Citterio (*MI*)
08:50	Update on activities in Bologna (20') (Slides)	Mauro Villa (*BO*)
09:10	SVT Mechanics (20') (Slides)	Filippo Bosi (*PI*)
09:30	Update on SVT Mechanics in Milano (20') (Slides)	Simone Coelli (*MI*)
09:50	Update on activities in UK (20') (Slides)	Fergus Wilson Wilson (*RAL*)

SVT



SVT contributions here presented according to this schema:

- Baseline design:
1. Detectors
2. Fanouts
3. FEE
4. Read-out chain
5. Mechanics

- Performance studies:
1. Tracking in high occupancy(fastsim)
2. Extrapolation from Babar

- R&D on MAPS
1. Rad. Hardness studies
2. 4-well CMOS MAPS prototype characterization
3. Strasbourg:mimosa
4. UK:cherwell

Update on Sensor and Fanout Design

L.Bosisio (Ts)

- Parameter tables have been updated:
  - Series resistance of sensors reduced assuming 2.5 μm Al thickness (feasible).
  - Noise contribution of series resistance reevaluated (a factor √3 lower)
  - z-side options considered in the tables:
    - both pairing and ganging for Layers 1 to 3 (pairing will be adopted)
    - ganging only for Layers 4 & 5; the plan is to mix both pairing and ganging
  - Expected radiation fluences for 7.5 years of operation, with/wo 5x safety factor
  - Two Layer 3 readout options considered: *p*-type *or* *n*-type strips on *Φ*-side

For Example: Φ-SIDE - No 5x safety factor - Φ-SIDE READ OUT BY SENSOR P-SIDE

Layer	Sensor side	Read out pitch	Total module strip length	Sensor *C/L*	Sensor *Rs/L*	Poly-silicon *R_bias*	n-equiv. fluence (1 year) *Φ*	Max Fanout *C*	Max Fanout *Rs*	Total *C*	Total *Rs*	Total *R_bias*	Total leakage current	Voltage drop on *R_bias*	Shaping time	ENC from *Rs*	ENC from *R_bias*	ENC from *I_leak*	ENC from Rs + Rbias + I_leak
		(μm)	(cm)	(pF/cm)	(ohm/cm)	(Mohm)	(cm^-2)	(pF)	(ohm)	(pF)	(ohm)	(Mohm)	(nA)	(mV)	(ns)	(e)	(e)	(e)	(e)
0-u	p	50	1.97	2.50	13	1	3.4E+12	10	18	14.9	44	1.0	142	142	25	274	121	202	361
0-v	n	50	1.97	2.50	21	1	3.4E+12	10	18	14.9	59	1.0	142	142	25	320	121	202	397
1	n	50	11.03	2.50	8.6	1	6.8E+11	5.8	12	33.4	107	1.0	238	238	100	481	241	524	751
2	n	55	13.00	2.50	6.7	1	4.1E+11	4.7	7	37.2	94	0.5	187	94	100	503	341	465	765
3	p	100	19.00	1.70	4	2	2.2E+11	3.4	7.5	35.7	84	1.0	267	267	200	321	341	785	914
4a	p	100	29.30	1.70	4	8	5.0E+10	2.1	4.5	51.9	122	2.7	98	262	500	357	330	752	896
4b	p	100	30.34	1.70	4	8	5.0E+10	1.5	3.2	53.1	125	2.7	102	271	500	369	330	765	912
5a	p	100	36.90	1.70	4	20	1.5E+10	2.2	4.7	64.9	152	3.6	42	154	1000	353	400	698	878
5b	p	100	38.04	1.70	4	20	1.5E+10	1.5	3.2	66.2	155	3.6	44	158	1000	363	400	709	891

COMMENTS ON S/N and Lorentz Angle

Signal/Noise

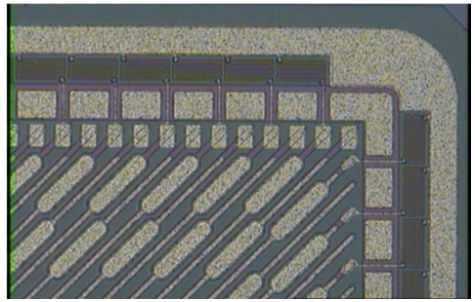
- On z-side, pairing gives better S/N than ganging (as expected).
- Radiation-induced leakage current gives a major contribution to noise (by far dominant with 5x safety factor). This suggests to investigate the possibility of cooling the sensors ($\Delta T = -8°C \Rightarrow$ 2x lower current).
- Polysilicon bias resistor values has been increased to ~20 MΩ in Ly5, and reduced in Ly1-3, keeping into account both the noise and the voltage drop with the high leakage currents after irradiation.

Lorentz Angle

- The **B** field along *z* will displace the carrier drift direction spreading the collected charge (it affects mainly Φ clusters, more for electrons than holes).
- In order to minimize the effect, it would be desirable to read the $r\Phi$ coordinate with the hole-collecting p-type strips (our choice Layers 4 and 5).
- However, Lys 1-2 will collect electrons on Φ-side, with a large Lorentz angle, and the inner layers (1 to 3) are arranged in a pinwheel geometry with faces tilted by 5.4 degrees. It is desirable to orient the faces so that the tilt angle will partially offset the Lorentz angle on Lys 1-2 and probably also in Layer 3.

INFN Trieste

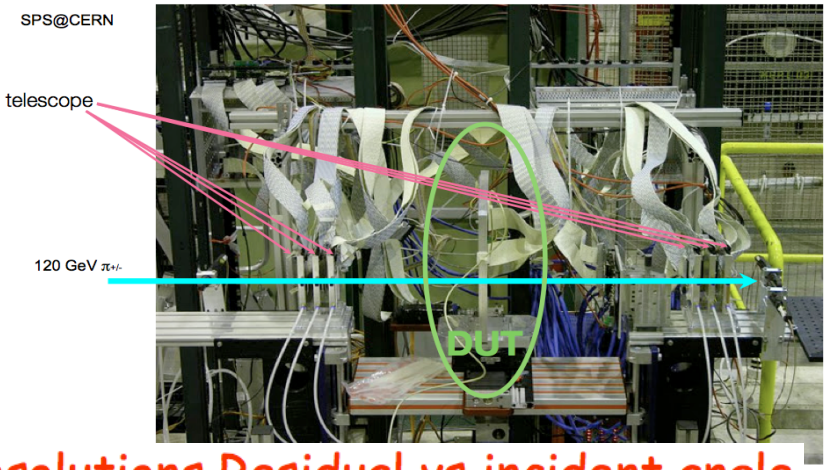
STRIPLETS DETECTOR: TEST-BEAM RESULTS



Efficiency: percentage of events in the DUT active region within **112 μm/cosθ** to the reconstructed track

(θ = angle of incidence)

θ	ε_U Low thr.	ε_U High thr.	ε_V Low thr.	ε_V High thr.
0	99.6	99.6	99.6	99.4
15	99.6	99.6	99.7	99.5
30	99.7	99.6	99.7	99.5
45	99.7	99.8	99.7	99.4
60	99.7	99.8	99.7	99.2
70	99.9	99.9	99.9	99.7



Resolutions Residual vs incident angle Sigma CORE (Frac CORE)

Incident angle	Resi_U Low thr. σ(μm) Frac %	Reso_U High thr. σ(μm) Frac%	Reso_V Low thr. σ(μm) Frac%	Reso_V High thr. σ(μm) Frac%
0	12.0 99.5	12.8 99.7	12.8 99.7	13.4 99.9
15	8.6 97.9	10.6 99.4	10.9 99.4	12.4 99.6
30	10.2 97.2	9.4 96.6	10.3 94.8	11.0 95.1
45	13.7 97.0	12.8 93.4	16.8 94.2	16.4 77.0
60	16.5 90.9	17.3 67.8	21.0 50.4	20.3 30.8
70	23.8 83.1	32.6 42.0	34.9 30.2	37.0 0

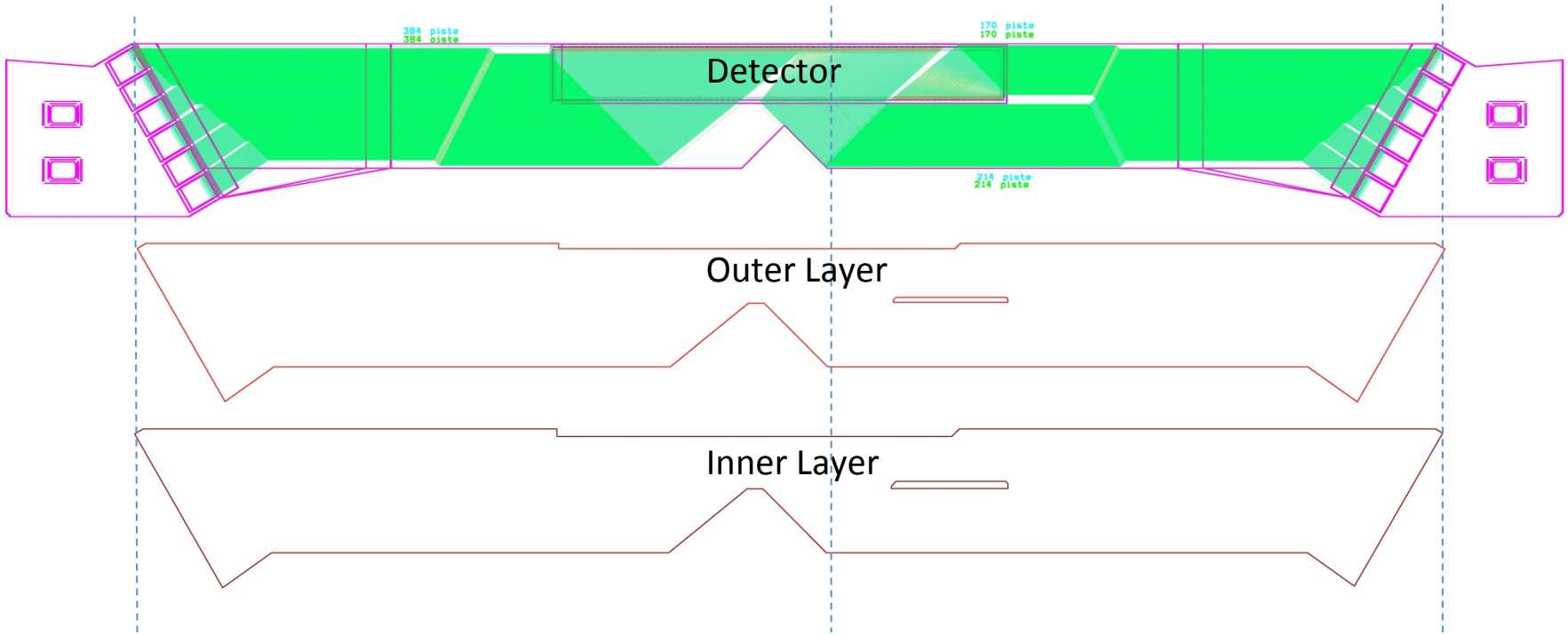
M.Villa (Bo)

Fanout (layer 0)

M.Citterio(Mi)

A layout has been completed based on two layers:

- → Trace pitch is 68 um, "soft corners" used
- → The traces are staggered plane to plane



Cu based fanout

Sensor	rad length cm	thickness cm	rad length %	density g/cm3
Si sensor	9.37	0.02	0.213447172	2.329
Fanout	rad length cm	thickness cm	rad length %	density g/cm3
Cu lines	1.436	0.00045	0.031337047	8.96
Glue	35.5	0.0025	0.007042254	1.2
Kapton	28.6	0.004	0.013986014	1.42
			0.052365315	
Support CF	rad length cm	thickness cm	rad length %	density g/cm3
	25.5	0.022	0.08627451	1.7
Total Material			0.404452311	

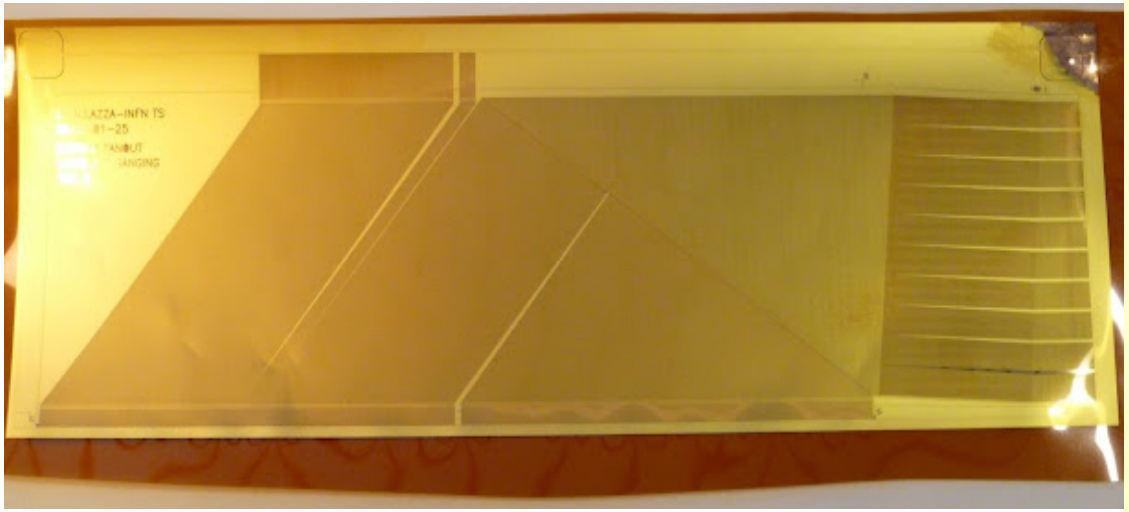
Al based fanout

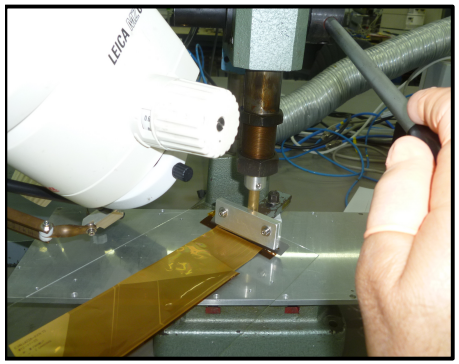
Sensor	rad length cm	thickness cm	rad length %	density g/cm3
Si sensor	9.37	0.02	0.213447172	2.329
Fanout	rad length cm	thickness cm	rad length %	density g/cm3
Al lines	8.9	0.001	0.011235955	2.7
Glue	35.5	0.0025	0.007042254	1.2
Kapton	28.6	0.004	0.013986014	1.42
			0.032264223	
Support CF	rad length cm	thickness cm	rad length %	density g/cm3
	25.5	0.022	0.08627451	1.7
Total Material			0.364250127	

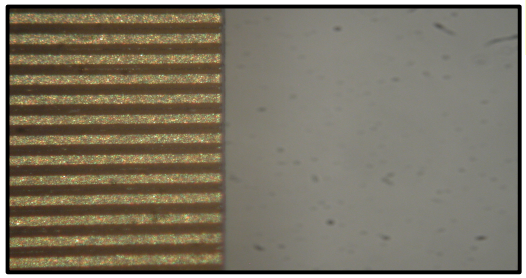
Fanouts L1-5 Design and production status (Como/Ts)

What we have designd up to now

- layer 1 – phi
- layer 3 - z with ganging and pairing
- layer 5b - z







What CERN has produced up to now

- layer 1 – phi (1x)
- layer 3 - z with ganging (3x)
- layer 3 with pairing (1x)

The layout conversion problems (causing the deposit of Cu and Au between the strips) were solved → a new production has started last month and the fanouts will be ready in a couple of weeks

Expected production yield

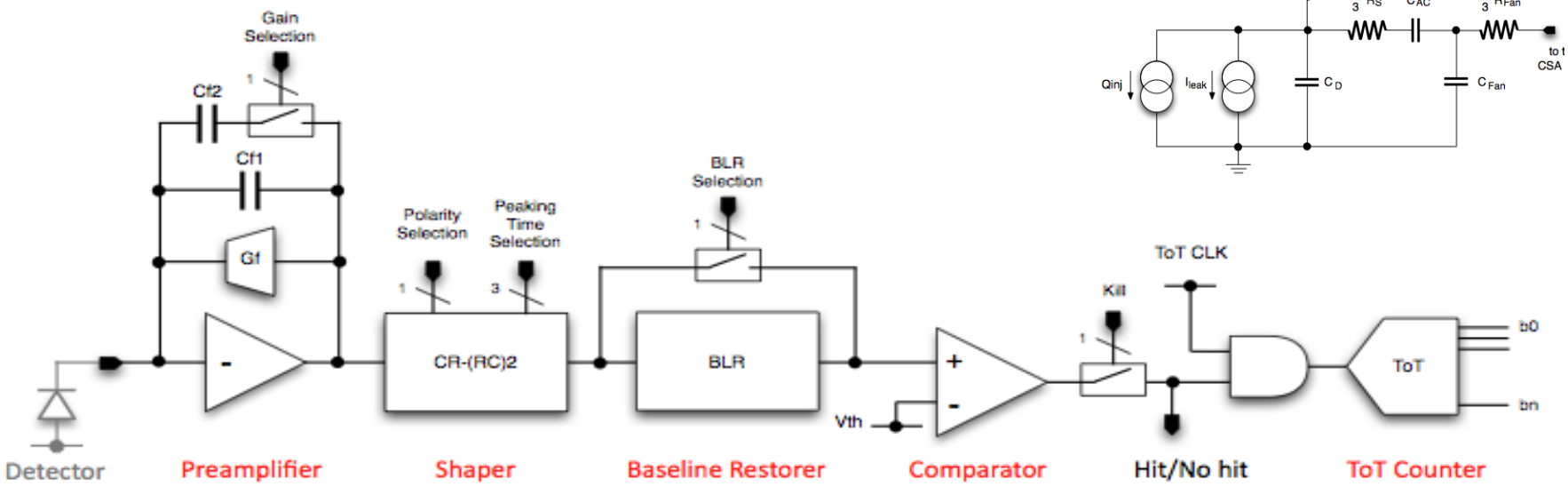
→ 20% perfect
→ 30 % with 1 short/open
→ 30% with 2 shorts/opens
→ more than 3 shorts/opens

ALL the produced fanouts have been cut @ Mipot and tested for bondability of the surface

Analog section of the FE chip for layers 0,1,2,3

M.Manghisoni(Pv)

Analog channel block diagram



Detector model used for the ENC evaluation

- Charge-sensitive preamplifier with gain selection (1 bit)
- Unipolar semi-Gaussian shaper with polarity (1 bit) and peaking time (3 bit) selection options
- Symmetric baseline restorer to achieve baseline shift suppression, may be included or not (1 bit)
- Hit discriminator (comparator)
- 3-4 bit analog-to-digital conversion will be performed by a Time-Over-Threshold (TOT) detection

Equivalent Noise Charge and S/N

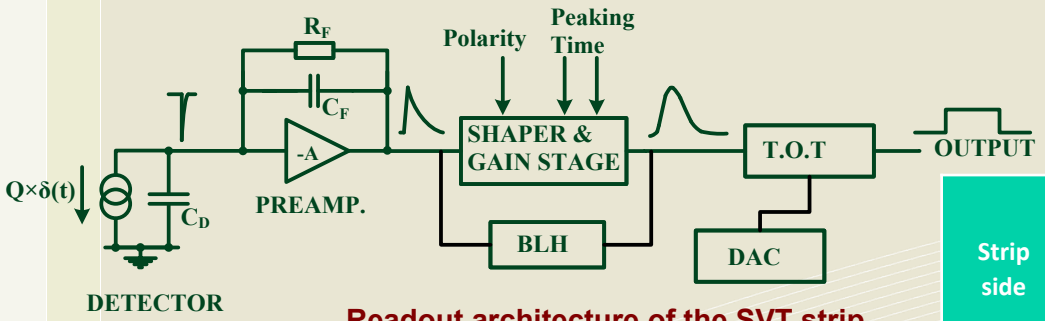
Layer	t_p [ns] Selected	Total ENC [e rms]	Total ENC [e rms] after 7.5 years	Total ENC [e rms] after 7.5 years with ×5 safety factor	S/N	S/N after 7.5 years	S/N after 7.5 years with ×5 safety factor
0 u	25	892	905	958	18	18	17
0 v	25	893	907	959	18	18	17
1 phi	75	1106	1160	1352	22	21	18
1 z	75	697	812	1165	34	30	21
2 phi	100	1070	1127	1332	22	21	18
2 z	100	660	778	1132	36	31	21
3 phi	150	864	1040	1470	28	23	16
3 z	150	669	836	1254	36	29	19

- Layer 0: S/N is always < 20
- Layer 1, 2 (phi): S/N close to 20 before and after 7.5 years of operation
- Layer 3 (phi): S/N close to 20 after 7.5 years of operation
- Layer 1, 2 and 3: S/N < 20 after 7.5 years of operation with the safety factor of 5 (with except for L1 and L2 z-side)

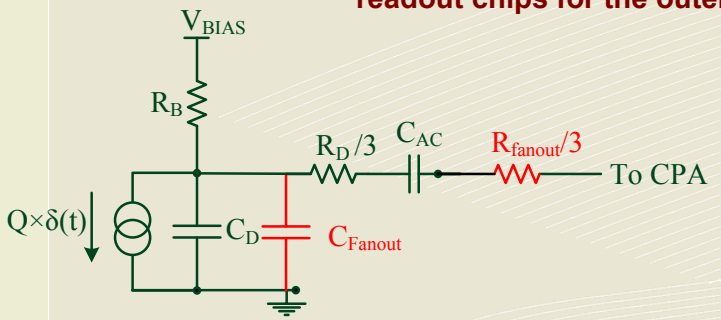
The shaping time flexibility [25;200]ns will allow a signal/noise optimization in the actual background conditions.

Front End Electronic Design for outer Layers of SVT

L. Bombelli



Readout architecture of the SVT strip readout chips for the outer layer.



Noise Estimation

Strip side	Layer	Peaking time (ns)	S/N At startup	S/N after 7.5 years Nomonal background	S/N after 7.5 years 5x Background
Phi	4	250	20	18	15
		375	21	19	14
		500	22	19	13
		750	23	19	12
Z	4	250	24	22	17
		375	28	23	15
		500	29	23	14
		750	31	22	13
Phi	5	375	19	18	16
		500	20	19	16
		750	22	20	16
		1000	22	20	15
Z	5	375	26	25	21
		500	28	26	20
		750	30	26	19
		1000	30	26	18

Better detector model including:

- Fan-out parasitic
- Radiation damage

Better performance achieved with shorter peaking time. (Added 250ns for L4, 1u will be eliminated!)

S/N still low with 5x safety on BKG.

Front End Electronic Design for outer Layers of SVT

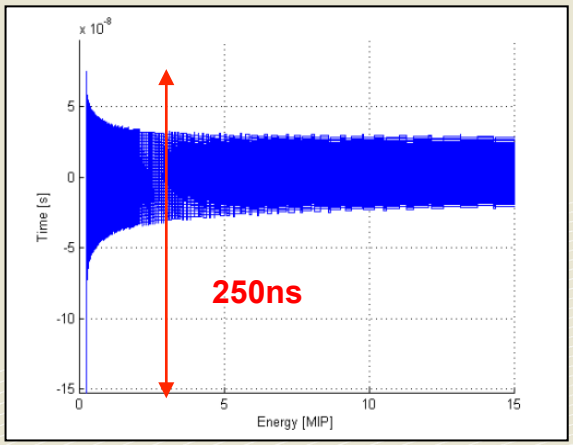
L. Bombelli

Residual error of time-stamp and time-walk correction

Time error due to:

1. Time stamp clock (33MHz)
2. Time walk, corrected with TOT amplitude
3. Effect of TOT error (TOT clock)

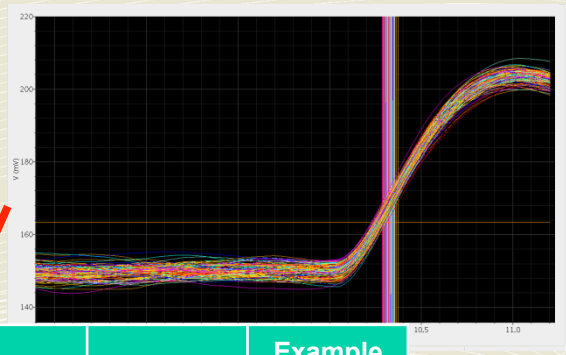
now also included.



Time jitter:

Depends on:

1. S/N ratio
2. Peaking time
3. Signal amplitude (worst case 0.3 MIP)



Expected Timing Resolution

Both contributions important for the outer layer

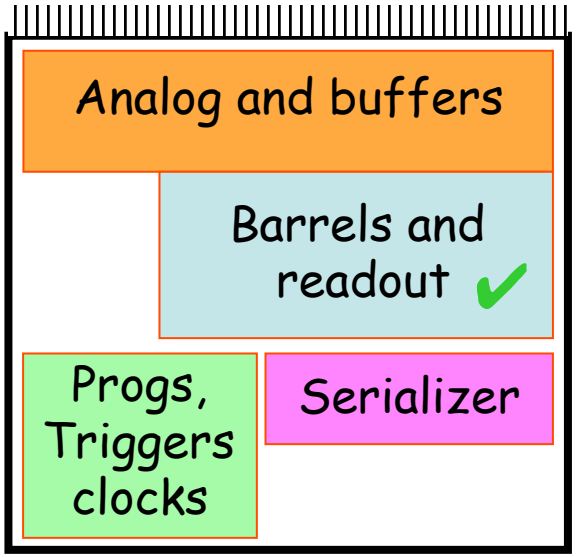
Better performance achieved with 6-bit TOT.

Prefer short peaking time when possible (same S/N)!

Peaking time (ns)	TOT bit	TOT clock (Mhz)	TS and Time walk error rms (ns)	Jitter for 0.3 MIP (ns)	Time resolution (ns)	Example Offline window (ns)
375	4	11.3	33	35	**48**	**290**
	6	47.5	15		**38**	**230**
500	4	8.5	41	43	**59**	**360**
	6	35.7	17		**46**	**280**
750	4	5.66	56	60	**82**	**500**
	6	23.8	21		**64**	**380**
1000	4	4.25	72	78	**106**	**640**
	6	17.8	25		**82**	**500**

PRELIMINARY

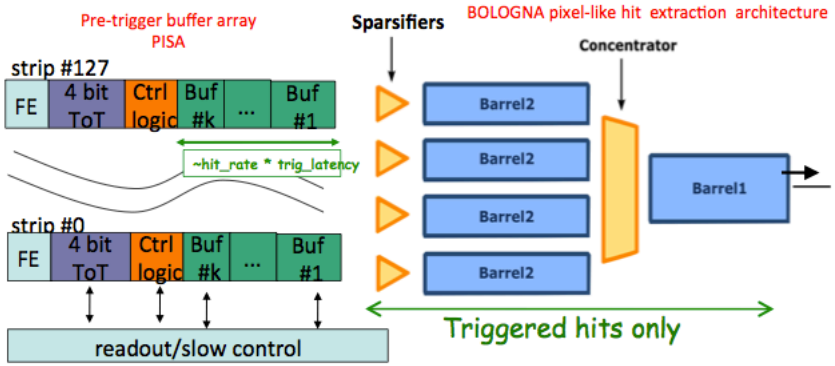
Digital periferical logic blocks



- Progs, Triggers, clocks:
  - Embedded in the readout architecture and actually part of it. It allows the trigger latency control, clock handling, channel masking, running

- Serializer Interface:
  - Sends out data (16 bits wide) on a programmable number of lines (1, 2, 4, 6)
  - Protocol (8b/10b?) and implementation to be defined.

Strip readout architecture under development



M.Villa (Bo)

Strip readout chip simulations

Strip FE architecture defined, modeled and simulated.
Digital readout efficiency measured value (simulations)
~100% with buffer depth = 32

2 MHz/strip : Layer 0

buffer size	16	32	64
buffered hits	3.8 M	12.9 M	12.9 M
of which triggered	23363	76850	23363
output triggered hits	14679	76849	23363
triggered hit lost	8684	1	0
Efficiency (%)	**62.8**	**99.9987**	**100**

Buffer Depth Scan

760 kHz/strip : Layer 1

buffer size	8	16	32
buffered hits	1.4 M	7 M	7 M
of which triggered	8748	28829	28829
output triggered hits	6788	28825	28829
triggered hit lost	1960	4	0
Efficiency (%)	**77.6**	**99.986**	**100**

SVT data load updates

Chip features

- Triggered, 128 channels, 60 MHz clock, 60/120/180 MHz output clock, serialized output.

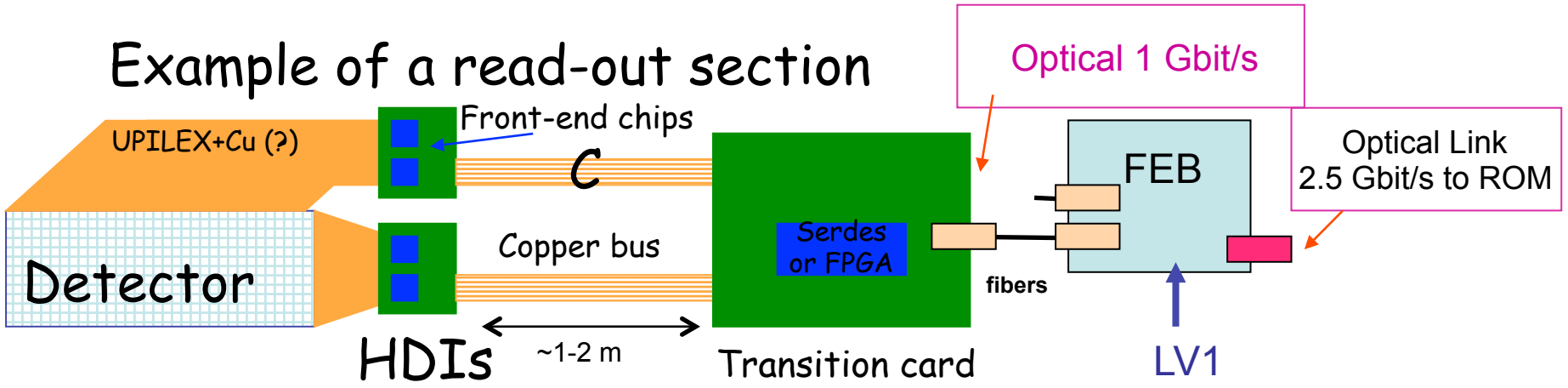
2 Data word: Time-stamp-like and hit

Hit: 7 bits Channel ID, 4 bits ToT, 1 bit word type,
4 bits to be defined, for a total of **16 bits**
Timestamp: 10 bits Timestamp, 1 bit word type,
5 bits to be defined, for a total of **16 bits**

Updated background simulation from R. Cenci (apr 2012)

Renormalization for pairs, rad bhabha and geometry→
-18%, -15% on average rates for inner layers
Inclusion of beam gas → **+35%** in outer layers

DAQ Activities

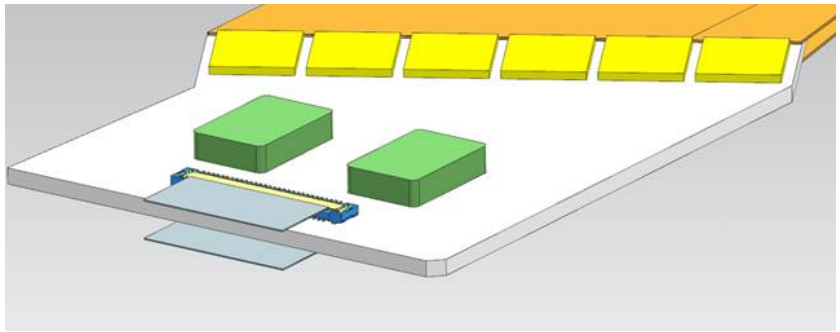


- Studies ongoing for fixed-latency data transmission over optical fibers.
- Latencies have to be **measurable** for: Clock, Timestamp and Trigger
- Test beds for optical links and latencies measurements in place: using xilinx FPGA SerDes
- Front-End board: component selection phase

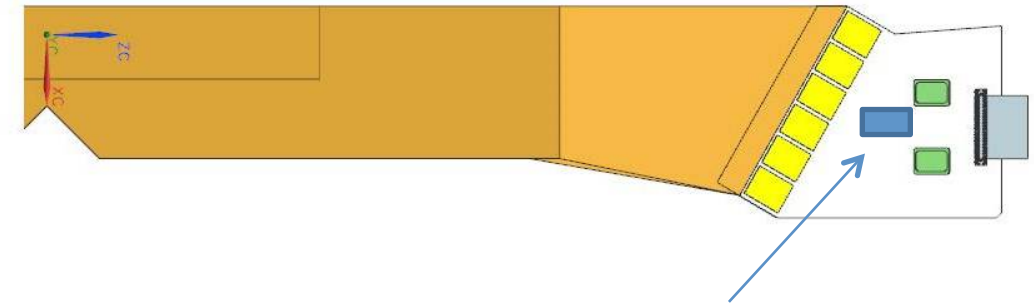
Copper Output Bus Update

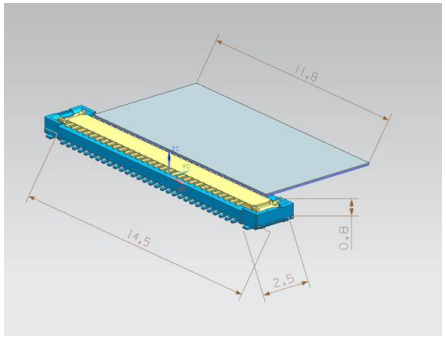
Proposal: a 3 layer Copper/Kapton tape to carry all LVDS lines from and to the front-end ICs.

Aspect ratio: ~ 10 mm x 400-500 mm
At the connector the tape is ~ 17 mm wide.



Update: Separate LV and HV cables !!!!
→ More LVDS data lines
→ Connector not really rated for the current needed by our frontend ICs (overheating)



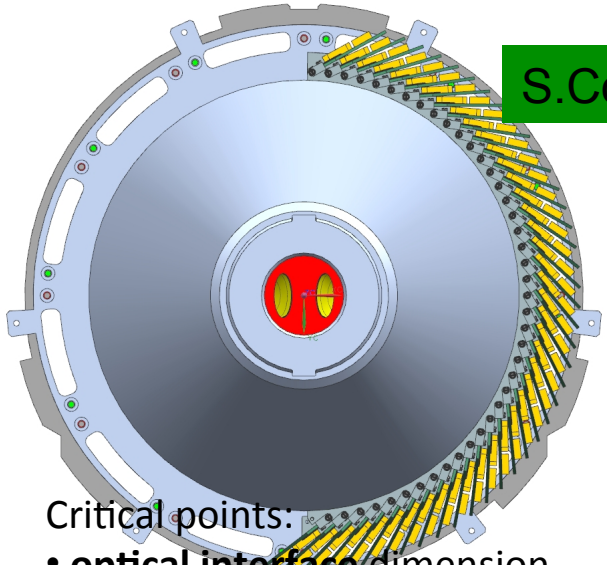


Serializer on the HDI still a possibility, however the baseline is shifting more and more towards multiple LVDS lines (~ 180 MHz) up to 14 +7 lines

Output connector has 0,4 mm pitch.
Goal is to use 70 contacts connector.
It could be increased to 80 contacts.
It will carry all LVDS lines

MECHANICS ACTIVITIES in MILANO AND WORK IN PROGRESS

- SVT transition cards
- Geometrical disposition and relative mechanics
- Thermal cooling analysis and test prototyping
- Routing of the flat-cables from the HDI to the transition cards
- Design of the connections for Layer Lo and L1-L5
- Routing from the transition cards to the detector outside
- Integration and installation sequence for mechanics and cables
- Quick-demounting constraints on the layout
- HDI cooling analysis



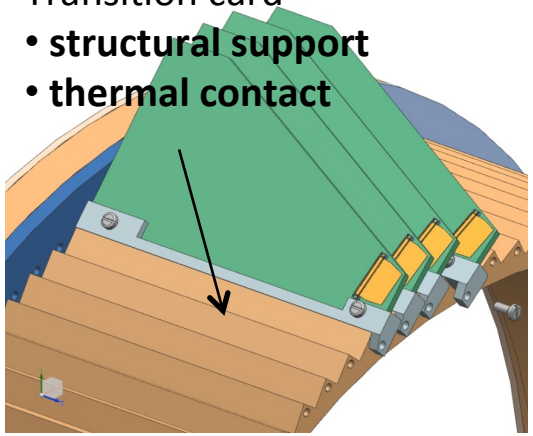
S.Coelli (Mi)

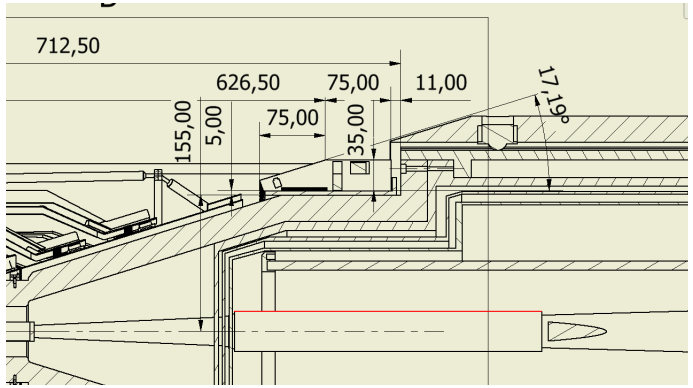
Critical points:

- **optical interface** dimension
- cables **bended routing** to pass through the openings in the W-shielding

Transition card

- **structural support**
- **thermal contact**



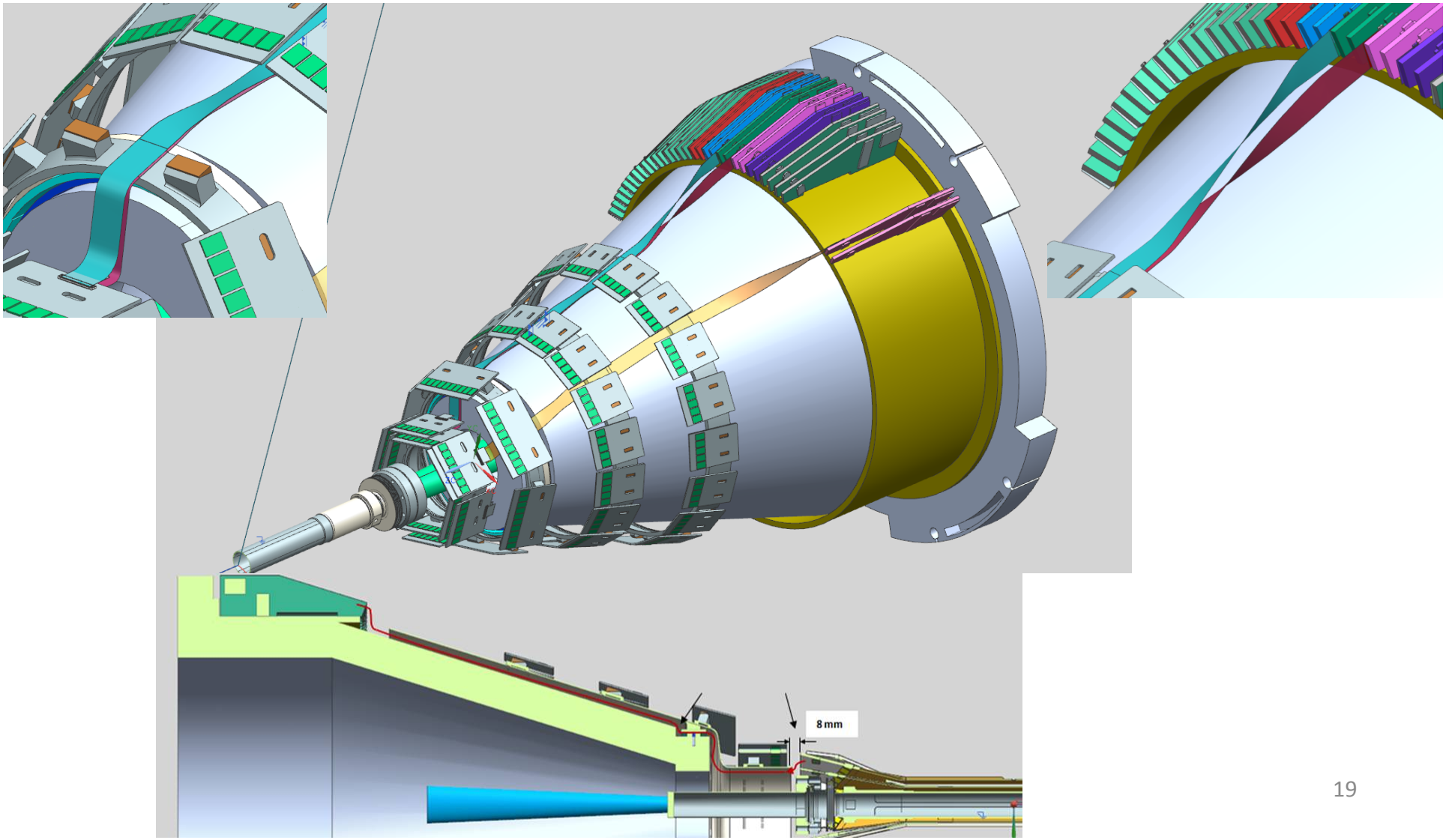


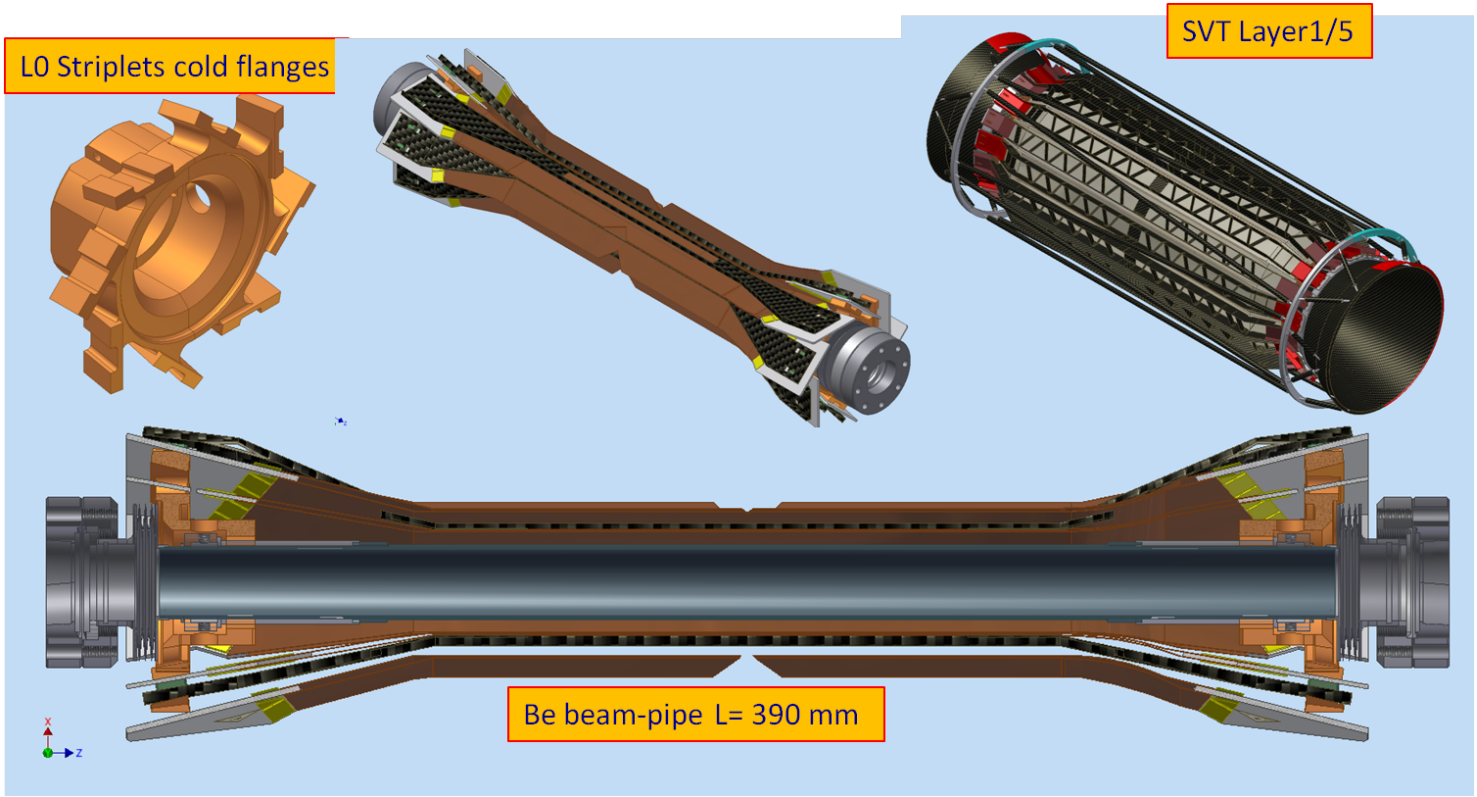
- **inclined card "turbine-like" disposition**
- **CRYOSTAT and W-SHIELDING MOVED BACK 30 mm**
- **both Layers L4 and L5 need less cards => actual total number 86 transition cards (from 120)**
- **Cooling ring**

- Half flange detailed mechanical design
- cooling ring details
- Connections with fittings
- Thermal FEA to verify the cooling
- Study of the conductivity of the materials
- Dummy card and sector production to test a cooled prototype with dissipating components or heaters

Path of the flat cables

Path of the flat cables from the **L1-L5** HDI to the transition cards **External** to the carbon cone support. Note: exagonal geometry
From the **L0** HDI to the transition card **between** the carbon cone support and the Tungsten conical shield. Note: octagonal geometry





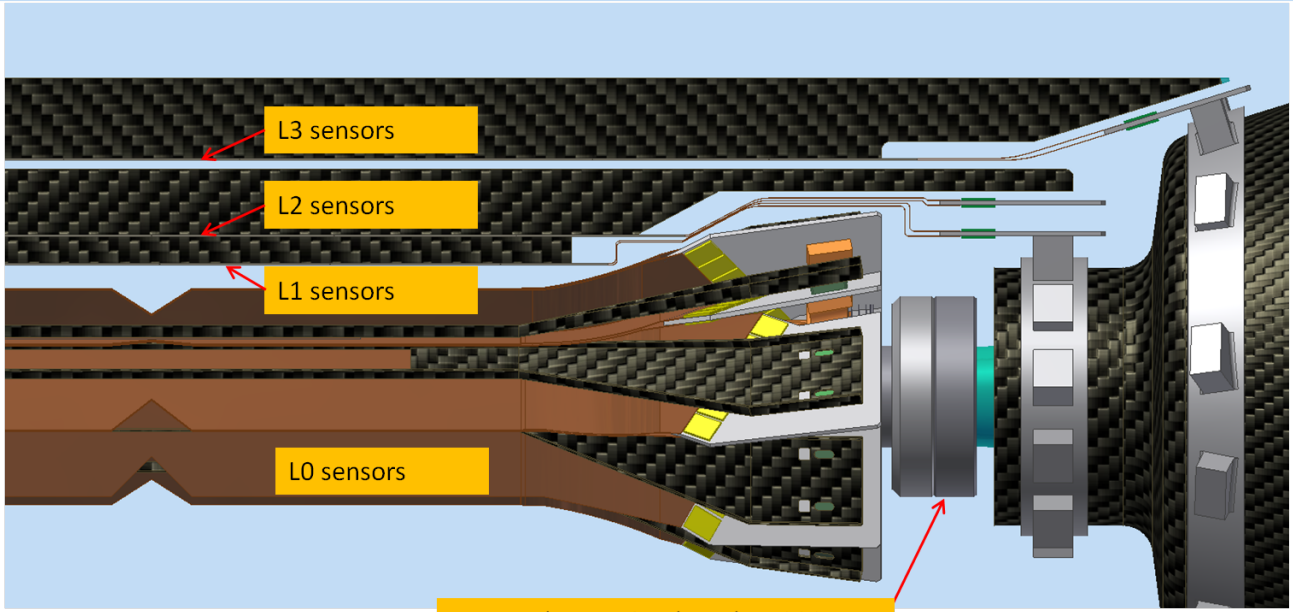
F.Bosi (Pi)

-New Be beam-pipe design (L=390 mm)

-L0 striplets update

-New cold flange L0 striplets design

-SVT L1/5 modules fitted on space frame structure



Cooling ring L1/2 forw/back moved outside from I.P

Reduction of the C.F. semicone nose length

Change for the fanout dimensions

Several effects of high background on det performance

- Efficiency reduction due to analog dead time evaluated for electronics: < 90 % in some layers with x5 safety
  - some improvements possible reducing the shaping time w.r.t nominal values

Efficiency

Layer	Peaking time (ns)	Bkg (%) (r-ϕ/z)	Bkg x5 (%) (r-ϕ/z)
L0	25	99/99	96/96
L1	100	98/98	88/89
L2	100	98/98	89/89
L3	200	95/95	77/86
L4	500	98/98	89/93
L5	1000	98/98	86/91

- Effect of high occupancy on reconstruction still need to be evaluated: Fastim cannot be used, no time/ manpower to do a real study for TDR.
  - In SuperB 3-15% strip offline occupancy and 2-5% cluster offline occupancy (x10 w.r.t. BaBar)
  - In BaBar 0.2-1% strip offline occupancy and 0.1-0.5% cluster offline occupancy.

Layer	View	Shaping time	S/N at the start of data taking	S/N in 75 ab-1	S/N in 75 ab-1 x5 bkg
1	phi	100	31	27	20
1	z	100	39	30	19
2	phi	100	29	27	21
2	z	100	37	31	21
3	phi	200	29	23	15
3	z	200	36	25	14
4	phi	500	22	19	13
4	z	500	27	22	14
5	phi	1000	23	20	15
5	z	1000	29	25	17

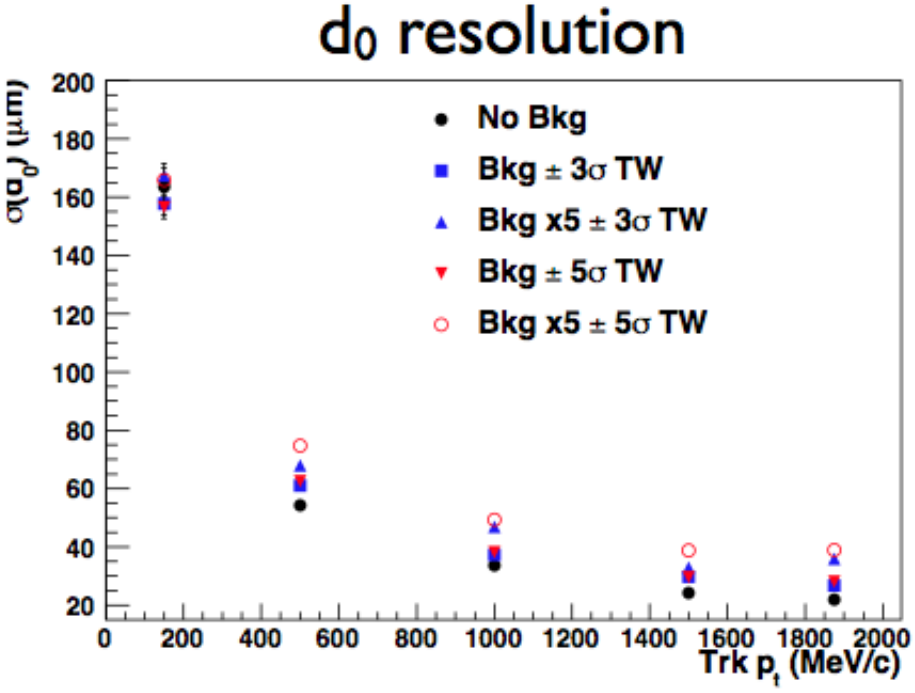
Preliminary

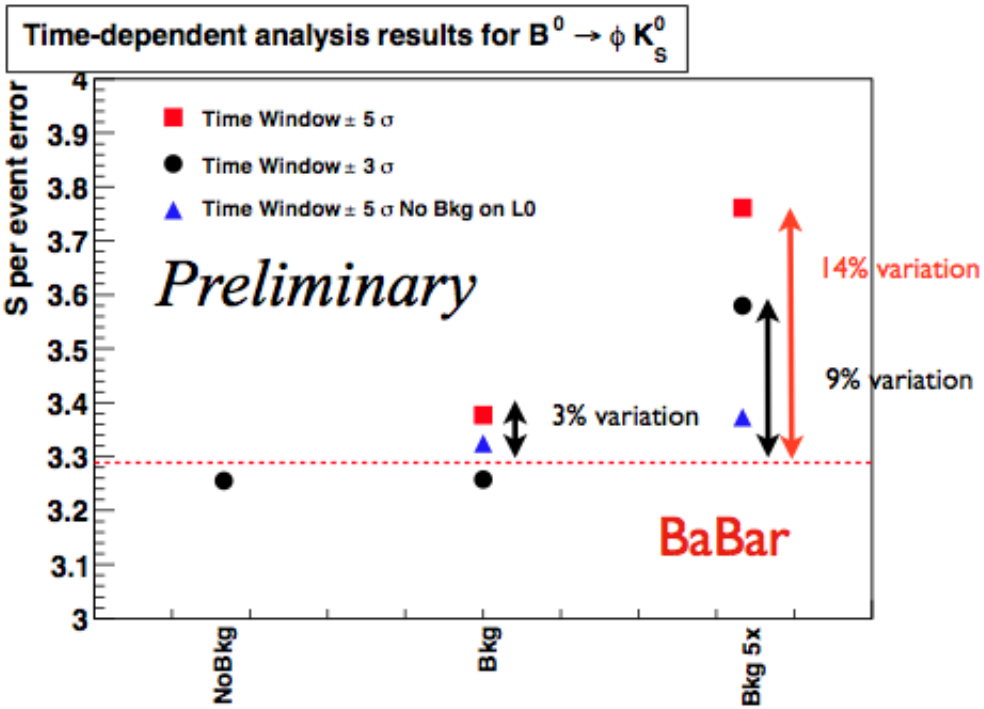
- Effect of radiation damage on sensor (increase on leakage current) and S/N degradation with the full life of the experiment (75ab-1 and x5) evaluated.
  - S/N a bit marginal with x5 safety
  - Could improve a bit selecting shorter shaping time after some accumulated damage
  - Start also to explore extra cooling to lower SVT sensor temperature & leakage current contribution

G.Rizzo (Pi)

BKG effects on SVT performance (fastsim)

N.Neri (Mi)





- Main results
  - sizable worsening in d0 and z0 resolution at x5 bkg rates.
  - sizable effect on S per event error: 9% (14%) worsening with x5 bkg and ±3σ (±5σ) time window cut. Small change with nominal bkg (3%).
- SVT performance seems to be very good in presence of bkg and reasonably good in presence of 5x bkg.

study of the SVT tracking performances

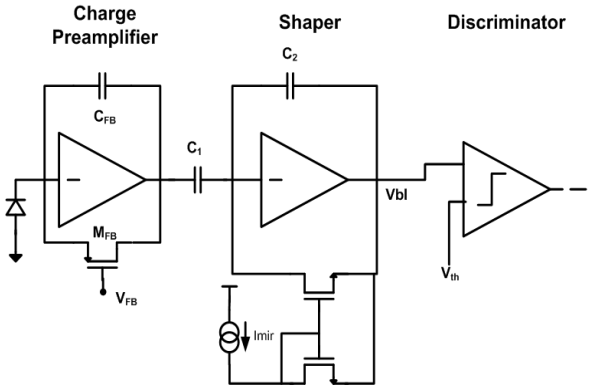
- BaBar AD 707: Final Report of the SVT Long Term Task Force (2004):
Study with BaBar dimuon data taken between Jan. and June 2003 (instantaneous luminosity increasing), of hit efficiency as a function of chip on-line occupancy.
  - ➛ translation of this BaBar study to SuperB.
- Next steps:
  - comparisons to FastSim results,
  - study SVT stand-alone tracking performances,
  - complete the TDR corresponding section.

	a	b	c = a x b
Layer	hit detection efficiency (x5 included)	hit-to-track matching efficiency	total hit efficiency
0 φ	0.96	0.96	0.92
0 z	0.96		0.92
1 φ	0.88	0.96	0.84
1 z	0.89		0.85
2 φ	0.89	0.97	0.86
2 z	0.89		0.86
3 φ	0.77	0.88	0.68
3 z	0.86		0.76
4 φ	0.89	0.96	0.85
4 z	0.93		0.89
5 φ	0.86	0.93	0.80
5 z	0.91		0.85

I. Ripp-Baudot
IPHC Strasbourg
CNRS/IN2P3 and Université de Strasbourg

INMAPS developments for the Layer0

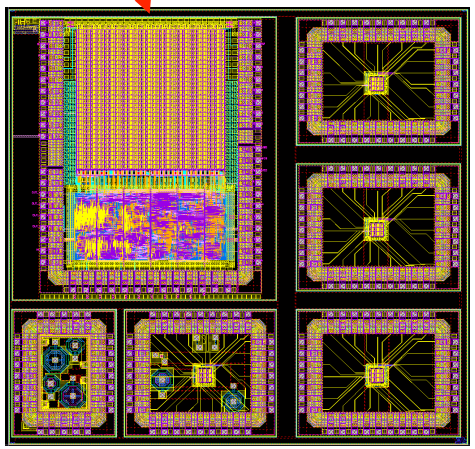
- Small N-well collecting diodes with small input capacitance and low power consumption.
- The forth-well prevents charge stealing by the parasitic N-wells (→ efficiency benefit).
- Implemented the digital architecture as in the latest APSEL chips, to cope with the high bkg rates.



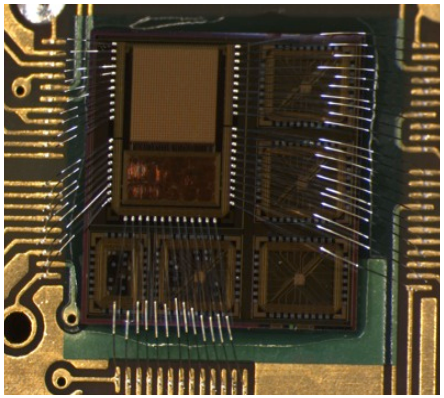
Apsel4well - Post Layout Simulation	
Charge sensitivity	930 mV/fC
t_p @ 800 injected electrons	240 ns
ENC (C_D = 30 fF)	26 e-
Threshold dispersion	23 e-
NLI (@ 2000e-)	1%
Analog Power consumption	18 μW/pixel
Pixel pitch	50 μm

32x32 matrix with sparsified digital readout architecture

3x3 analog matrices with different diodes configurations

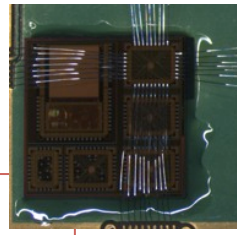


INMAPS Chip (5x5 mm^2)



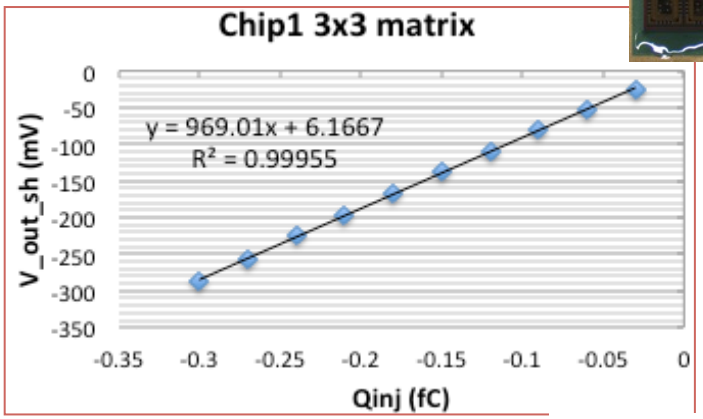
Bonded chips under test

INMAPS RESULTS: 3x3 analog matrix

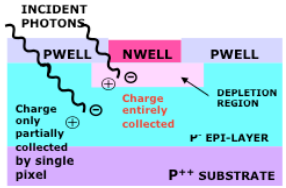


Noise and gain measured in 3x3 analog matrix in good agreement with PLS:

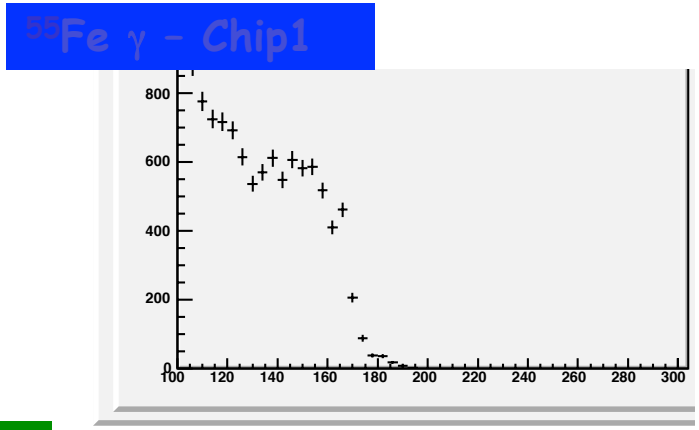
- ENC = 30 e- (~20% dispersion)
- Gain=920 mV/fC (~10% dispersion)



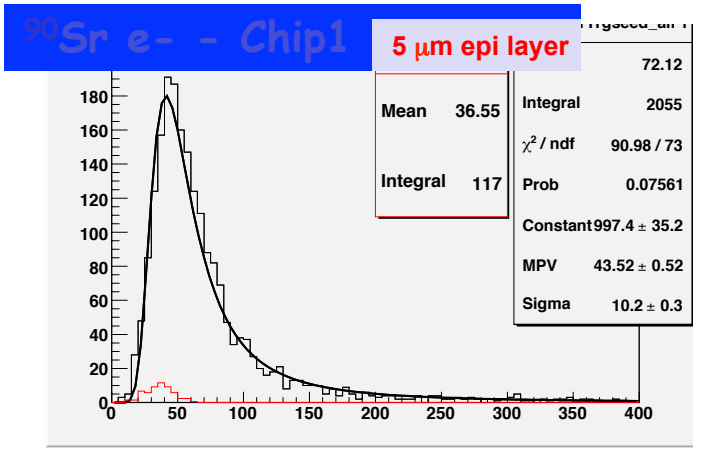
- Response to radioactive source
  - ^{55}Fe γ: 5.9keV foto peak hardly visible due to very small diode area.
    - Charge totally collected for γ interaction in the depleted volume below the diode. Partial collection elsewhere. End point (5.9 keV + 3 σ noise) used for gain evaluation (agreement within 10% with Cinj)



  - ^{90}Sr e- signal cluster: MPV ~ 350 e-, compatible with 5 um epi layer of first chips
    → chips with 12 um epi layer (standard & high resistivity) available in June.



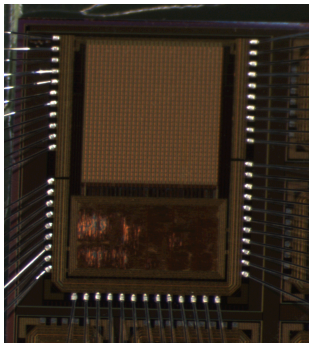
Pixel signal (mV)



Cluster signal (mV)

S.B.(Pi)

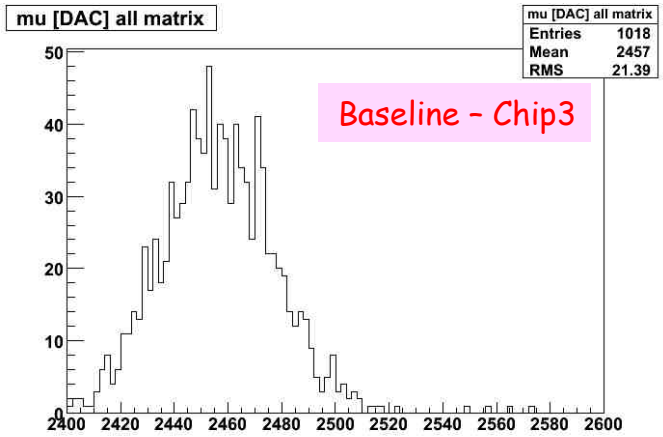
INMAPS 32x32 digital matrix



Noise and gain measured in pixels with Cinj and analog output

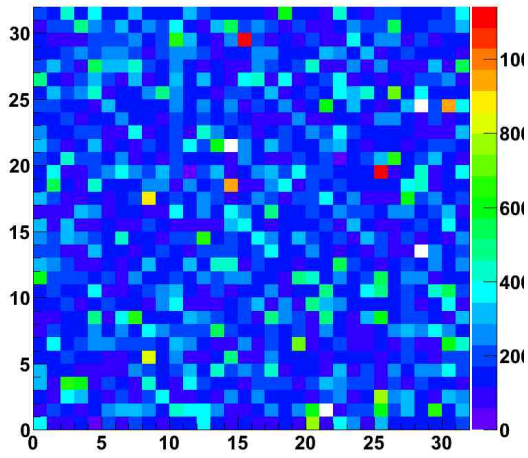
- ENC = 30 e- gain=680 mV/fC

- Threshold and noise dispersion inside matrix measured with noise scans (occupancy vs discriminator threshold)
  - Threshold dispersion = 7mV (~ 2 x σ_noise)
  - Noise (+gain) dispersion ~ 35-40%
  - Further tests to evaluate gain dispersion with Fe55 end point ongoing.

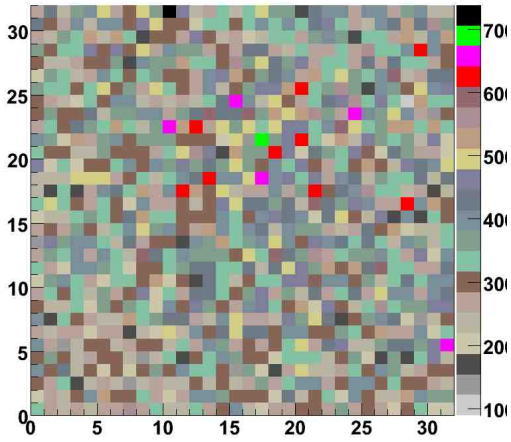


- Few dead pixels: ~ 0.3% (on 3 chips 32x32)

Noise hits – Chip3

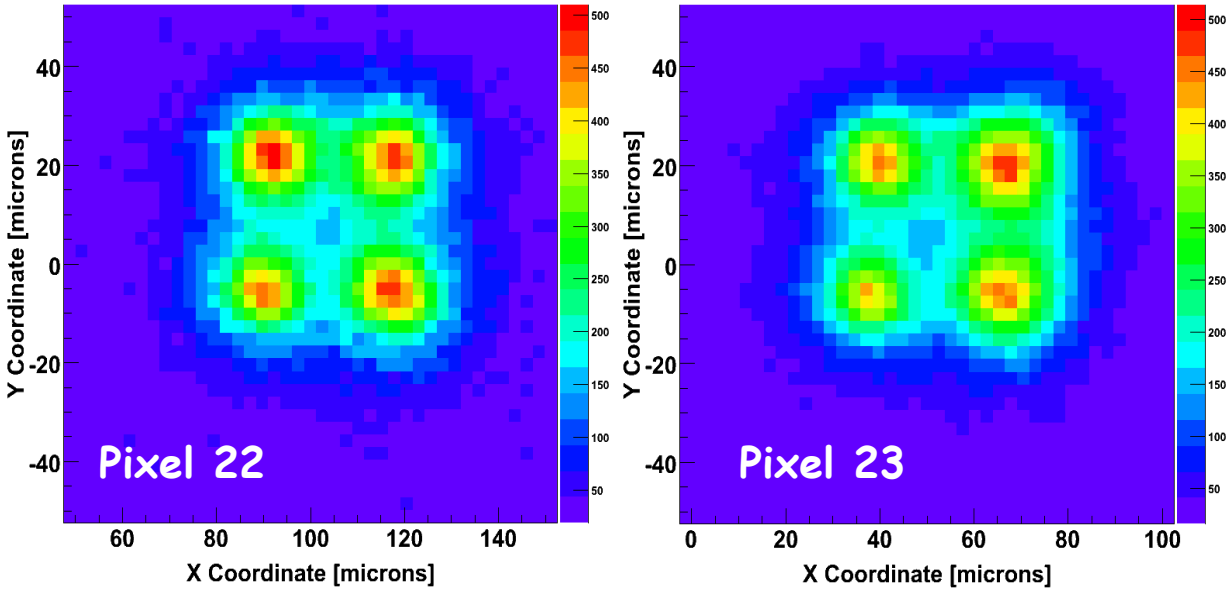


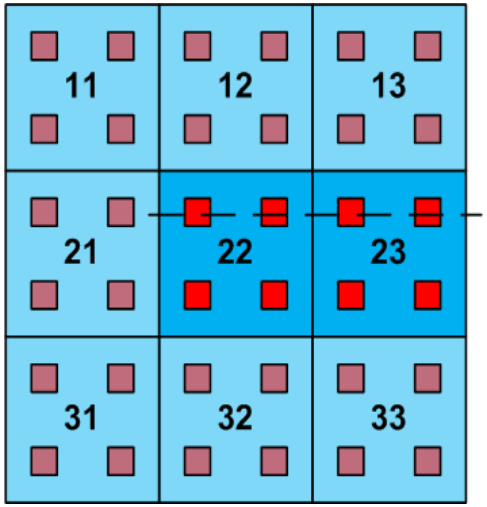
Sr90 hits – Chip1

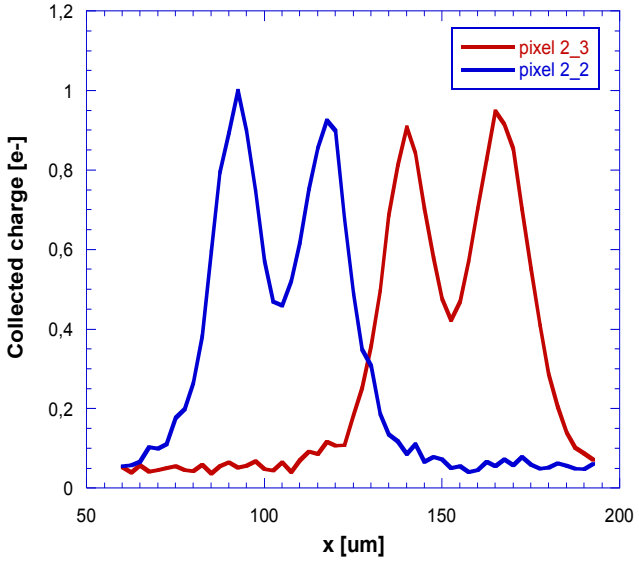


Charge collection performance

S.Zucca (Pv)







Measurement setup for precision scanning with IR laser featuring λ=1064 nm.

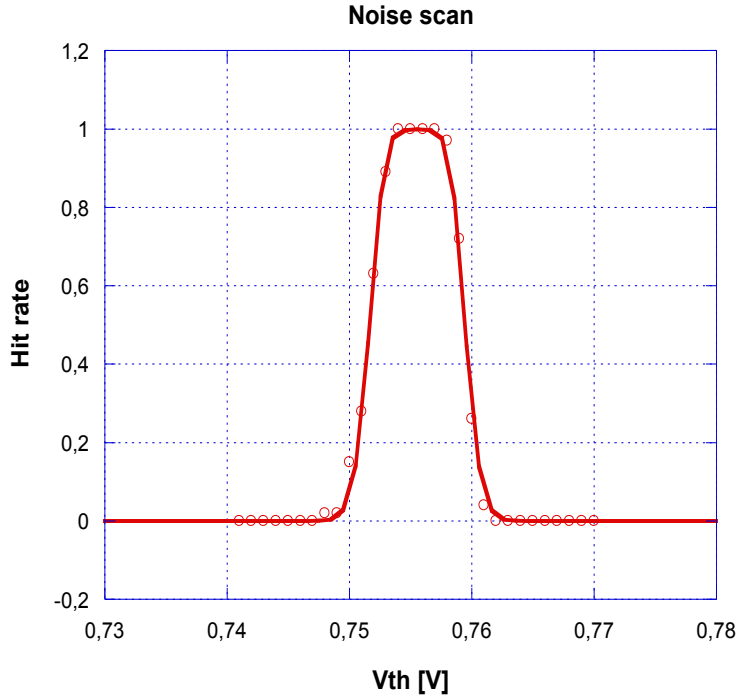
Scan of 2 adjacent pixels (3x3 matrix) designed on **standard resistivity epitaxial layer 5 µm thick**.

(waiting for chips fabricated with a 12 µm thick epitaxial layer)

Some issues with the comparator design

- During first tests noise and injection scans looks strange for small signals: after a deep investigation, we discovered that for small injected signal (and seen at the analog output) no hit were registered.

- This behavior was confirmed by transient noise simulations of the in-pixel readout:



Noise at the shaper output = 3.1 mV

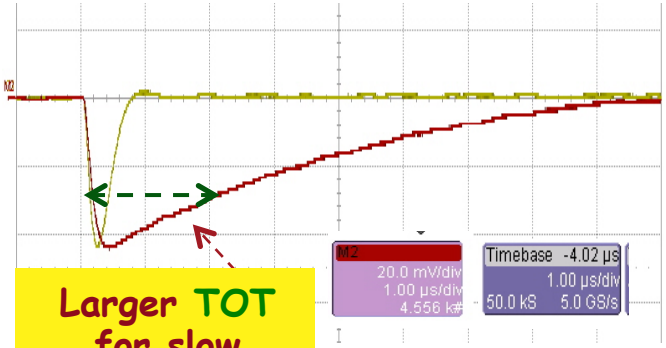
Extracted noise = 1.8 mV

Slightly asymmetrical behavior

- The problem was tracked with a "slow" turn on of the discriminator that prevent signals to be seen if the Time over Threshold (TOT) is too small

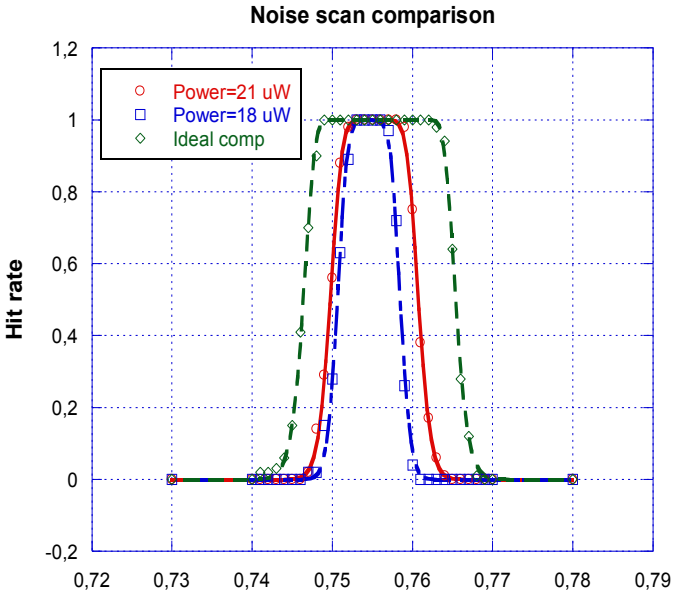
Possible fixes

- Discharge time (T_2) increase of the analog signal from the shaper to increase the TOT and to allow the "slow" comparator to fire (just for measurements, not suitable for fast operation conditions)



Larger TOT for slow discharging signal

- Need for new design solutions, in order to speed up the differential pair operation. First investigated solution:

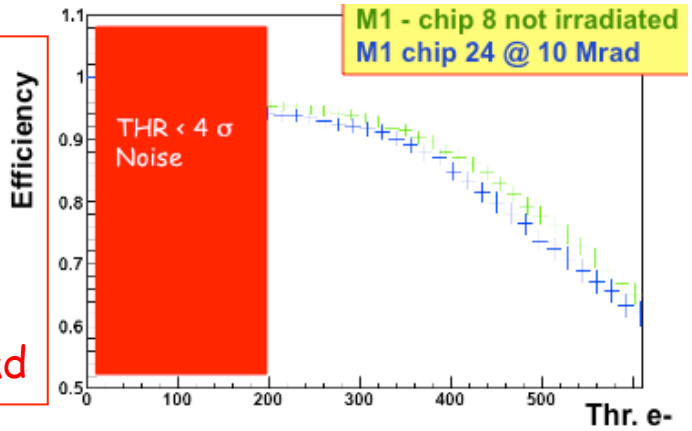


- Differential pair tail current increase for a faster charge/discharge of C
- An increase of about 15% of the power consumption leads to a slight improvement (still far from the behavior of an ideal comparator)
- Investigation on new fast comparator architectures might be necessary.

Apsel3T1 MAPS Radiation hardness

Irradiations with γ from ^{60}Co up to 10 Mrad

- beam test results for MAPS (3x3 matrix) with analog output (pre/post irrad)
  - Qcluster ~1040 e- for M1 (930 e- for M2)
  - S/N~15-20 depending on the electrode geometry
- modest reduction in collected charge and efficiency
  ENC increased by ~35% in chip irradiated up to 10 Mrad



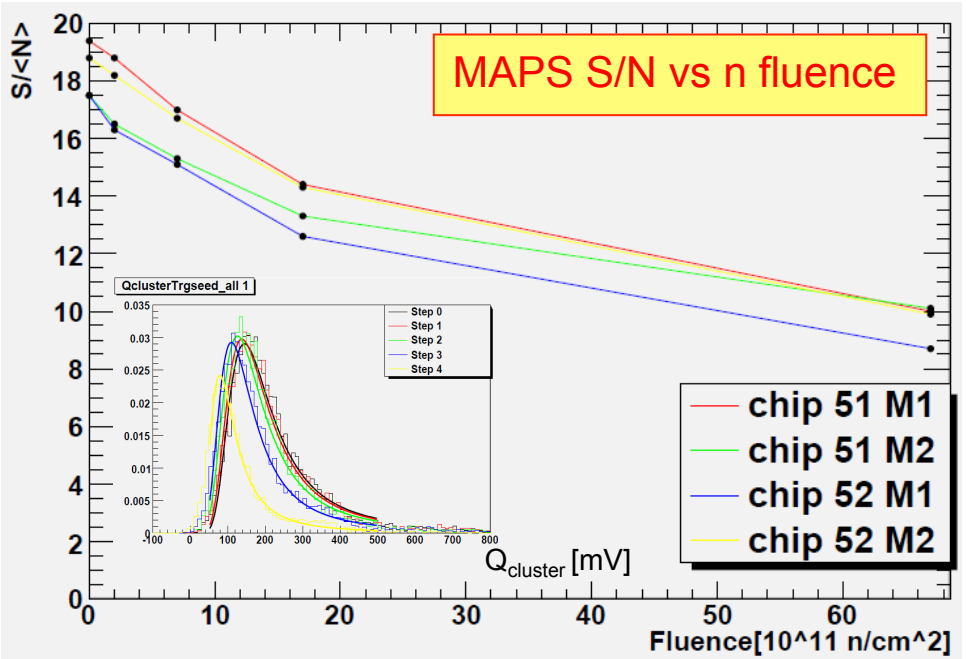
Irradiation with neutron up to ~ 7x10^{12}n/cm^2

- Expected fluence in Layer0 ~ 5x10^{12}n/cm^2/yr (no safety included)

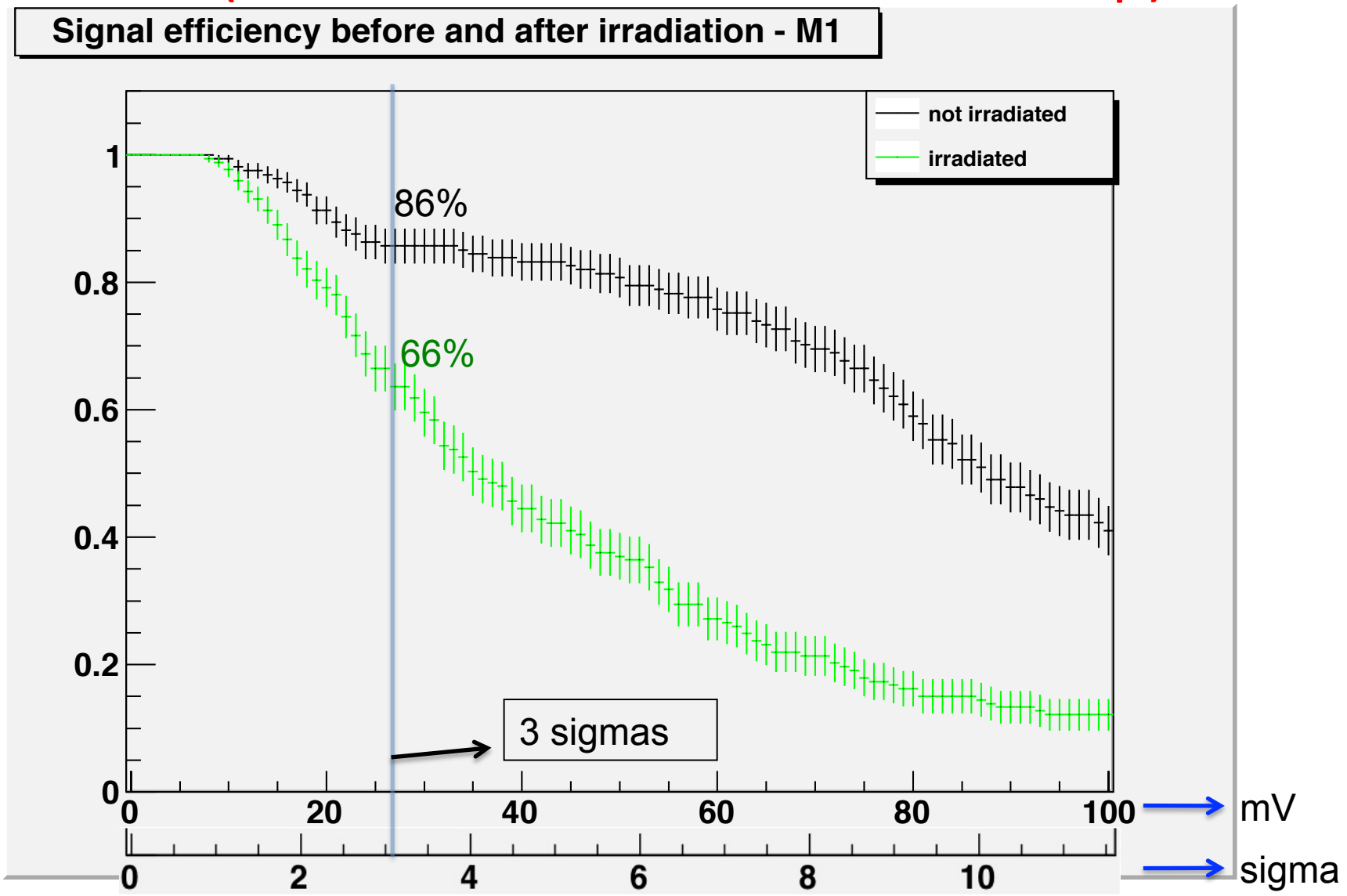
Lab. Results (with a β source):

- Noise and gain not affected by neutron
- Signal degradation studied with β Sr^{90} source at each step:
- S/N → 10 in last step → limitation for application in Layer0
- Expect higher resistance with MAPS on high resistivity epitaxial layer

Chip 52 put on beam

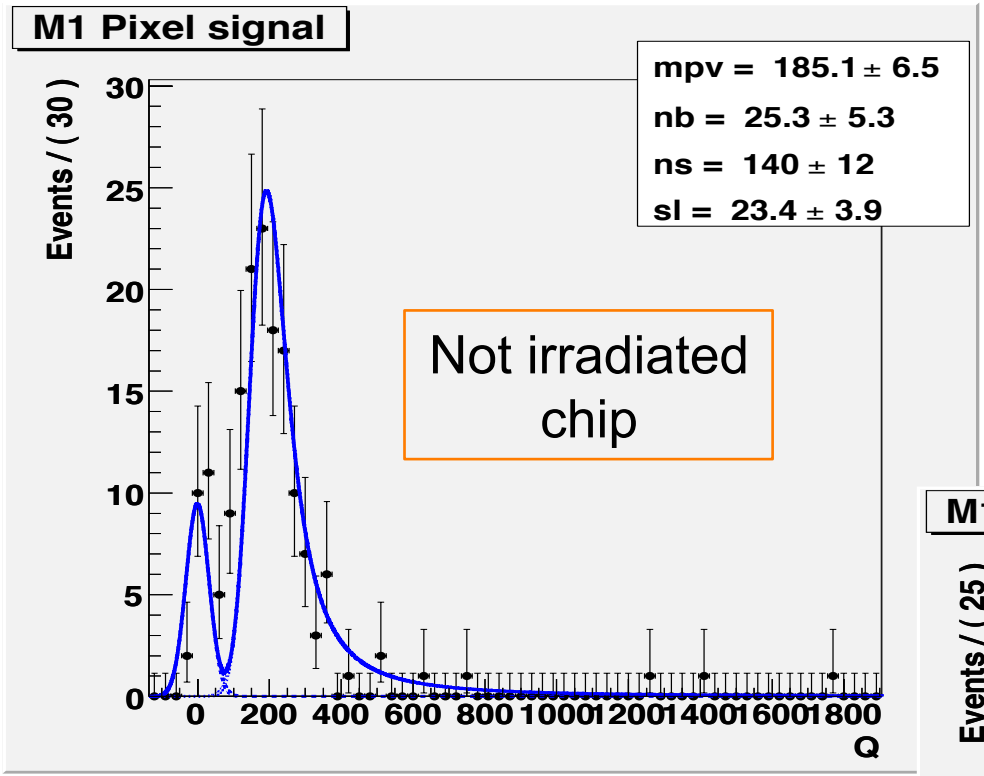


Test-beam results: Efficiency
(not-irradiated and irradiated chip)



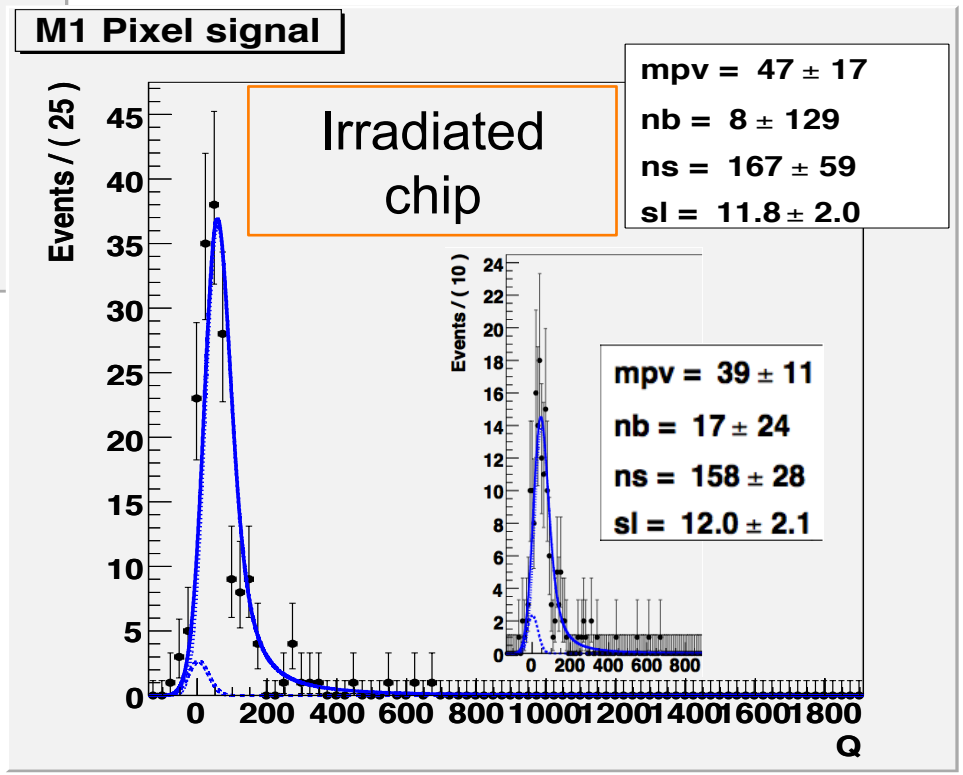
S.B.(Pi)

Test-beam results: Landau



Pdf = nb * Gauss +
ns * Landau(mpv,sl) x Gauss

Fit parameters:
nb # of bkg events
ns # of sgn events
mpv Landau
sl sigma (=Γ/4) of the Landau curve

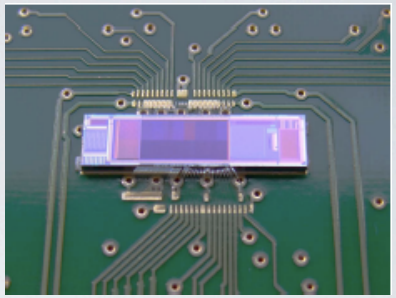


Low statistics and small signal charge:
In the irradiated chip the fit is not able to distinguish the sgn from noise.
With smaller bin: see the inset.

0.18 µm CMOS technology validation in Strasbourg

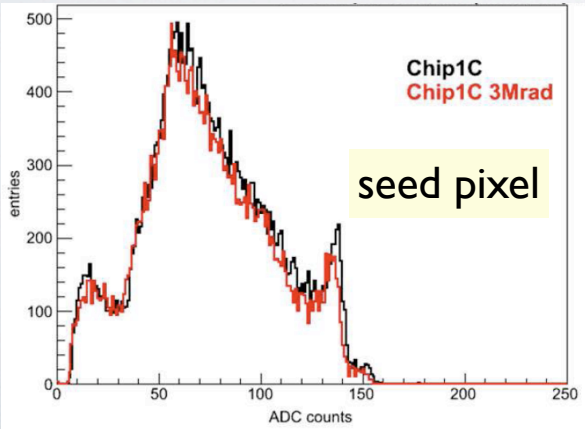
- Mimosa-32 sensor:
  - epitaxial layer: 18 µm thick, High-Resistivity 1-5 kΩ.cm,
  - quadruple well, 4 to 6 Metal Layers.
  - total surface ~ 43 mm^2.

➢ Submitted in Oct. 2011, delivered in January 2012, lab. tests since April 2012.



- Prototype sub-divided in several blocks to explore different pixel sizes (20x20 → 20x80µm^2, explore different charge amplification / collection systems (diode sizes ~9-15 µm^2, N-MOS and P-MOS transistor based amplifiers) and explore in-pixel discrimination.

- First results:
  - Charge collection: seed pixel (20x20 µm^2): 40-50 % of total charge ➢ S/N ~ 30.
  - Noise: ~15-20 e^- at room T°.
  - Ionising radiations: 3 MRad ➢ no impact at room T° (tests on going with 6 - 8 MRad).
  - Non ionising radiations: $3x10^{12}$ - 10^{13} - $3x10^{13}$ n_{eq}/cm^2 ➢ results next week.



➢ more results to come.

- Several beam tests scheduled during this Summer.
- Several submissions already scheduled in 2012,

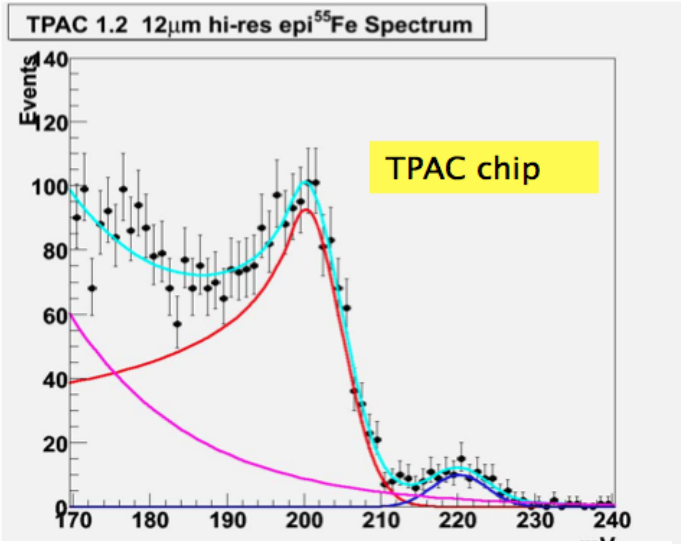
towards a sensor with:
- a read-out time ~ 1.5 µs,
- radiations tolerance,
- low power consumption.

Arachnid Project

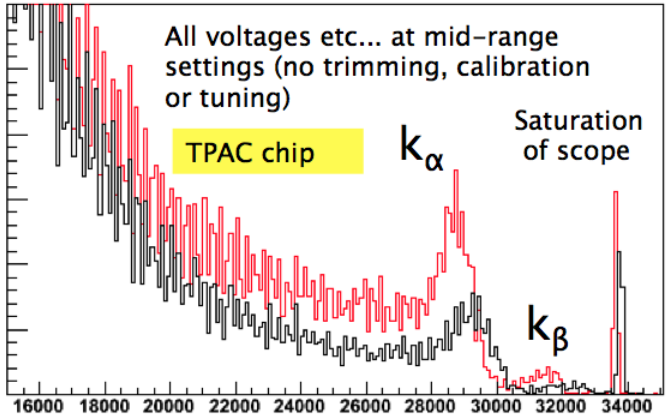
4th SuperB Collaboration meeting, Elba, 2nd June 2012

F. Wilson on behalf of Arachnid members:

Birmingham, Bristol, QMUL, STFC - RAL, STFC - Daresbury



First results with Fe^{55} at QMUL 16th May 2012



CHERWELL Chip Reminder

- CMOS MAPS
- Low power, low noise, small inactive area
- Rolling Shutter, Correlated Double Sampling (CDS) and 4T architecture
- Control and readout electronics distributed in active area
- Power pulsing (CLIC/ILC)
- Binary and digital readout
- On-board 10-bit ADCs

Current Plans

- We are designing a next generation chip.
- It will take on-board the needs of SuperB but ...the chip is targeted at ALICE Inner Tracker upgrade due to:
  - Upgrade and CDR/TDR schedules
  - UK funding
  - UK Nuclear Physics priorities and size of group
- There is good overlap between ALICE and SuperB needs
- Main goals are:
  - Prove radiation hardness
  - Identify power requirements
- Possible Schedule:
  - Hope to design, produce and begin first testing by Spring 2013
- Continue to support SuperB access to CMOS foundry.

SVT - TDR Status

- Good progress in the writing:
  - Almost all the sections in the svn repository (not final version!): ~35/70 pages
  - Writing on peripheral electronics and mechanics less advanced (starting this week)
  - Hope to have a complete document in a few weeks for the internal editing

1. Vertex Detector Overview (10) – G. Rizzo still some text to be written
2. Backgrounds (4) – R. Cenci outline
3. Detector Performance Studies (6) – N. Neri almost completed
4. Silicon Sensors (6) – L. Bosisio still some text to be written
5. Fanout Circuits (6) – L.Vitale almost completed. working on text for L0
6. Electronics Readout (20)
   1. Readout Chips (8) – V. Re almost completed
   2. Hybrid Design (5) – M. Citterio working on text
   3. Data Transmission (5)– M. Citterio working on text
   4. Power Supplies (2) –M. Citterio working on text

   SVT DAQ (M.Villa) will be in the ETD section
7. Mechanical Support & Assembly (10) – S. Bettarini/F. Bosi outline/working on text
8. Layer0 pixel upgrade options (10) – L. Ratti almost completed
9. Services, Utilities (1)

G.Rizzo(Pi)