SVT-Status

SVT Parallel Sessions – Frascati, March 21- 2012
3rd SuperB Collaboration Meeting

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SVT Parallel sessions

Wednesday Mar 21, 9-11	
Introduction	G. Rizzo (PI)
Analog FE for inner layer strips and next pixel submission in Pavia	L. Ratti (PV)
Analog FE for outer layer strips in Milano	L. Bombelli (MI)
FE chip simulation and next pixel submission in Bologna	F. Giorgi (BO)

Wednesday Mar 21, 11:30-13:30	
Next pixel submission activities in Pisa	F. Morsani (PI)
First INMAPS lab tests and beamtest results for analog maps	S. Bettarini (PI)
Update on sensor and fanout design in Trieste	I. Rashevskaya (TS)
Update on activities in UK	A.Bevan (QMUL)

Wednesday Mar 21, 15:00-16:30	
Activities in Valencia	A. Oyanguren (IFIC)
Update on activities in Strasbourg	I.Ripp-Baudot (IN2P3)
Fastsim performance studies	N. Neri (MI)
Discussions on performance studies and SVT SW development	All

Wednesday Mar 21, 17:00-18:30	
Update on background simulation	R. Cenci (Maryland)
SVT Mechanics	F. Bosi (PI)
Update on HDI design and peripheral electronics	M. Citterio (MI)
Discussion on TDR writing	All

SVT – Background Update

- Many tests done to understand the high SVT rates from Dec. 2011 production
- Total rates (several sources included) were too high for SVT (not only in Layer0)
  - Pairs increased a lot w.r.t May 2011: in L0-1-2 +40-20% x2.5-x4 in L3-4-5!!!!
  - Some reasons understood and fixed, but pairs rates still higher than before +20% in inner layers +80% in outer layers (different material in the I.R. is important for external layers)
  - Touscheck is as high as pair in L1-5. Rad Bhabha not negligible in L3-L5
- Some sources still to be included and new shielding configuration need to be studied

x5 safety included

Layers	lato	readout pitch	Strip rate kHz	Ratio pairs / total	Ratio rad bhabha / total	Ratio touscheck LER/ total	Ratio touscheck HER/ total
0	1	50	1.21E+03	0.90	0.03	0.06	0.02
0	2	50	1.21E+03	0.82	0.04	0.11	0.04
1	phi	50	7.24E+02	0.58	0.04	0.30	0.07
1	z	100	4.73E+02	0.39	0.04	0.45	0.12
2	phi	55	5.25E+02	0.48	0.05	0.38	0.08
2	z	100	4.54E+02	0.31	0.05	0.52	0.12
3	phi	100	4.19E+02	0.33	0.11	0.47	0.08
3	z	110	2.70E+02	0.23	0.10	0.56	0.11
4	phi	100	9.00E+01	0.35	0.23	0.34	0.08
4	z	210	4.70E+01	0.36	0.20	0.35	0.09
5	phi	100	5.44E+01	0.39	0.21	0.32	0.08
5	z	210	3.08E+01	0.37	0.19	0.35	0.09

Joint Background Workshop with BelleII in Feb. very useful:

- Discrepancy with BelleII pairs estimate has been solved and our result is still valid.
  - The factor 15 was due to some "problems" in the initial BelleII value and to some misinterpretation of our results by Belle colleagues. The hit rates expected in Layer0 for both experiments is consistent. SuperB estimate also agrees with measurement performed with SVD Belle data.

Impact of high background on performance

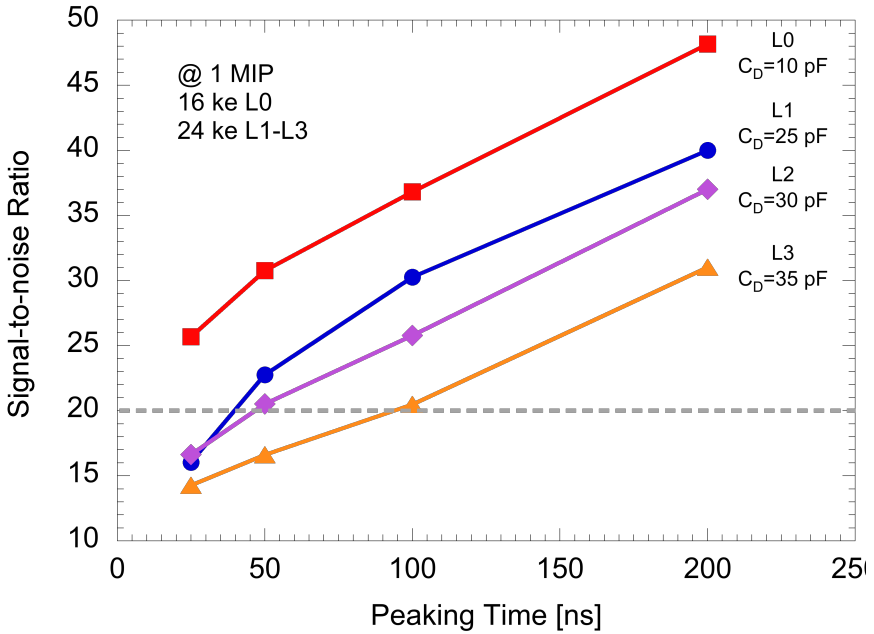
- Low efficiency due to analog dead time
  - Detailed simulation of the analog efficiency performed using info on energy deposited per strip (from Bruno) → ~ 90 % in some layers
  - Impact of inefficiency on performance can be evaluated with fastsim
- High occupancy
  - Detailed simulation of hit time resolution performed, with present FE chip configuration, to evaluate minimal time window cut for reconstruction → minimal offline occupancy achievable:
  - ~4-6% in L0-L3 and ~2.5% in L4-5 (x5-x10 w.r.t. BaBar!)
  - Impact of occupancy on resolution can be evaluated with fastsim
  - High occupancy can also affect reconstruction: in BaBar tests done with occupancy x5 showed reconstruction code started to suffer.
  - Fastsim as it is cannot be used to evaluate this effect but we need to face the issue of reconsctruction in high occupancy at some point.
    - Need more manpower on SW! Would like to start the discussion today.
- Many tests done to check initial discrepancy in background estimates using fullsim vs. fastsim.
  - Partly solved, difference anyway expected for the different details implemented.
- Fastim tools to study SVT performance in high occupancy almost ready

x5 safety included

SVT-Detector Design and TDR status (I)

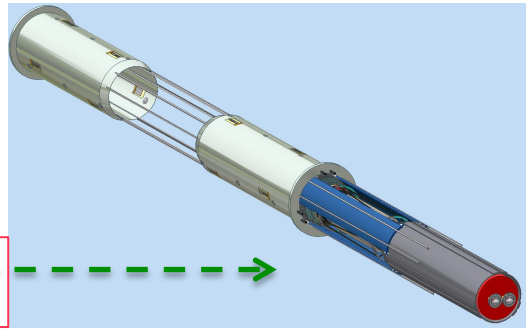
Activities almost completed in all areas

- Silicon Sensors: geometry defined and detailed parameters provided for better noise evaluation.
- Fanouts: Layer1-5 - prototypes in production at CERN : Layer0 - some details still to be defined.
- FE chip development:
  - Readout architecture simulated (VHDL): 100% digital efficiency achievable even for high Layer0 rates (2 MHz/strip).
  - Analog channel simulated; shaping time reduction for some layers under evaluation to mitigate background impact:
  - Shorter shaping time gives
  - → lower inefficiency due to analog dead time
  - → better hit time resolution and lower occupancy
- FE chip work completed for TDR
- Next step: prepare first FE chip submission with IBM 130 nm - Nov. 2012



SVT-Detector Design and TDR status (II)

- Peripheral Electronics: some progress on definition of HDI components, connectors, copper bus & transition cards.
  - Some work still needed in this area but my feeling is that we can tune the level of details we want to give in the TDR!
- DAQ & FEboard: Electronics load reevaluated with new inputs (new geometry and background rates)
- Performance studies: some work still needed, these results crucial for TDR
  - Performance with nominal & x5 background with striplets & pixel (?)
- Pixel R&D is continuing: INMAPS chip under test now
- Mechanics:
- Detailed procedure for quick demounting defined (presentation at the Integration session).



•Insert a temporary cage to make SVT/Be pipe more rigid then slide criostats, W conical shields, cage + SVT+Be pipe w.r.t W cilindrical shields

- Complete the TDR work in ~1-2 months, needed only in some areas.
- Tech Board decided for a complete draft of the TDR written by Elba: it needs to be published by Sept. 2012, then reviewed to get significant funding for construction starting in 2014! We need to start now:
  - concentrate on TDR writing: SVT first complete draft by April 13th (SVT-Meeting)
  - review carefully cost estimate and construction schedule (should go in TDR!)

SVT TDR Writing

~ 20 pages in svn

backup

Cylindrical Shielding 1300 Kg

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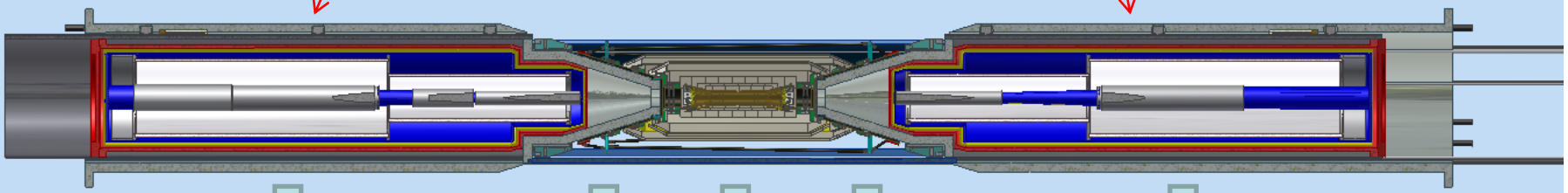


250 Kg + 150 Kg + 50 Kg Criostate + External tube + Cables

200 Kg Conical Shielding

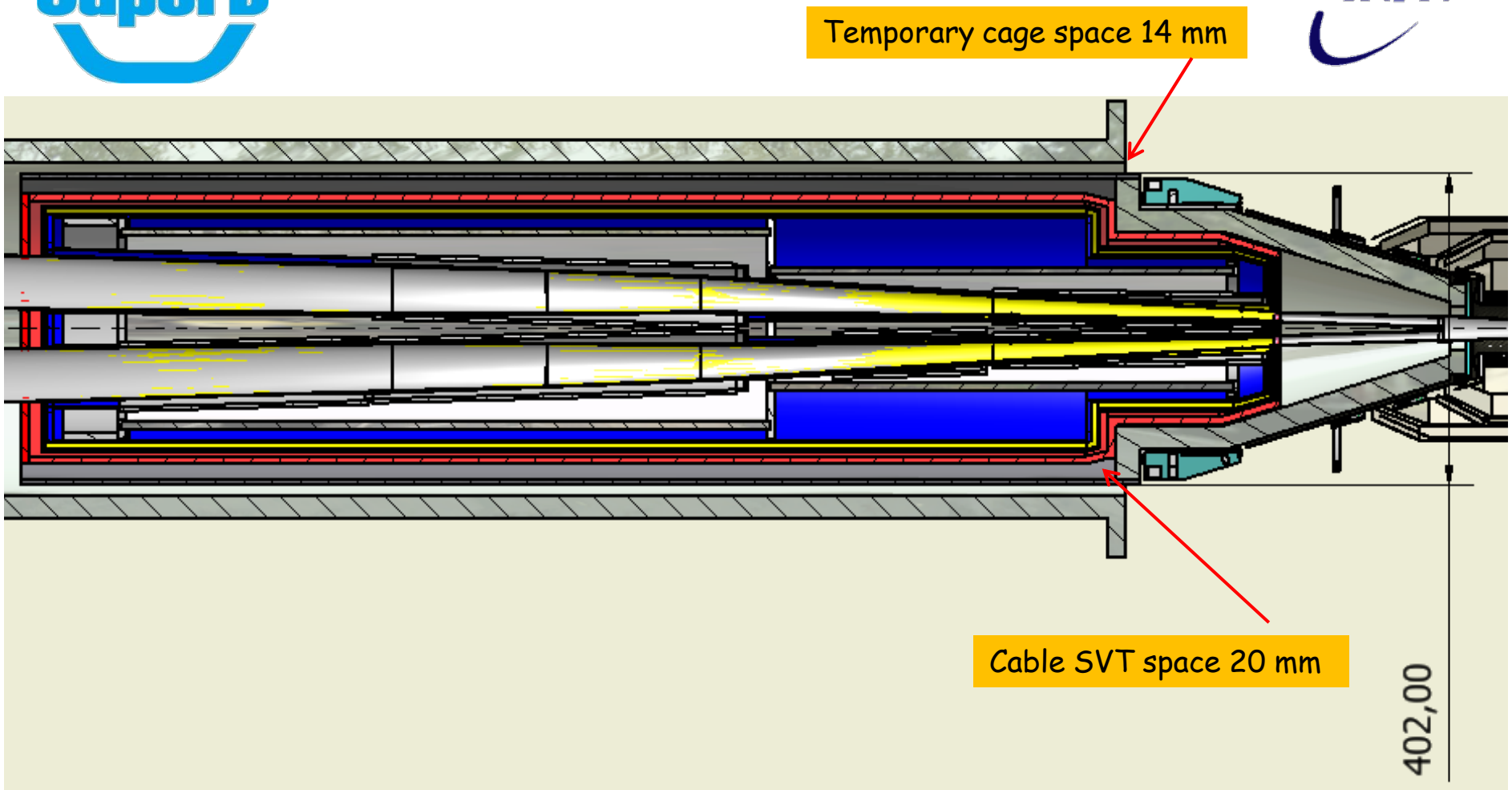
50 Kg + 50 Kg SVT + Temporary Cage

200 Kg Conical Shielding

250 Kg + 125 Kg + 50 Kg Criostate + External tube + Cables

Total weight to move for quick demounting ≈ 1400 Kg

Quick demounting



Quick demounting