First measurements on INMAPS prototypes & Analog MAPS: preliminary test-beam results

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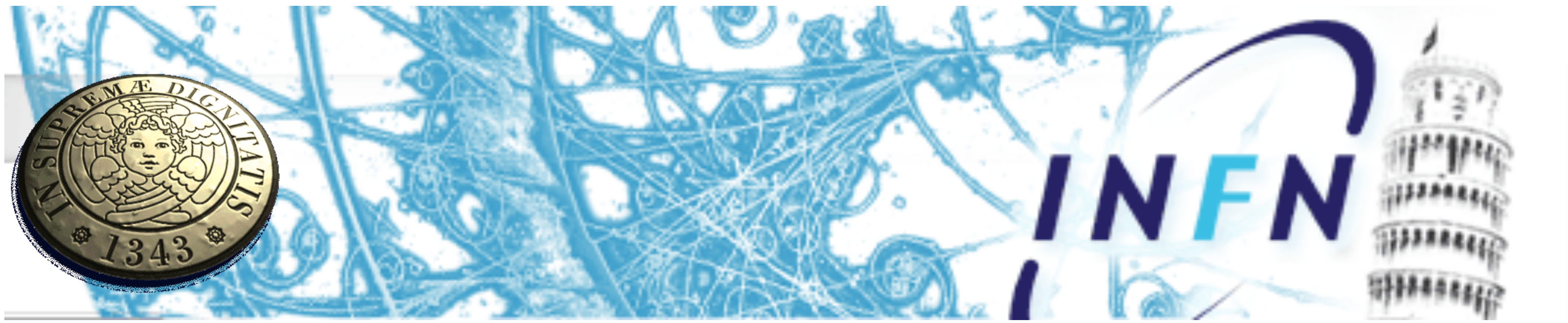
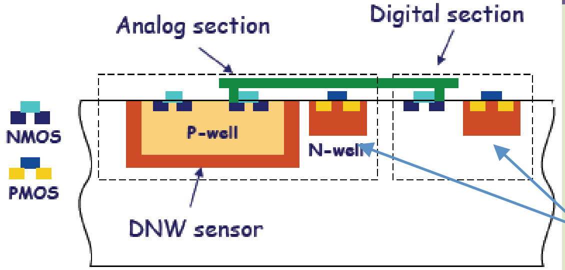


III SuperB Coll. Meeting - LNF, SVT Parallel session - 21 March 2012

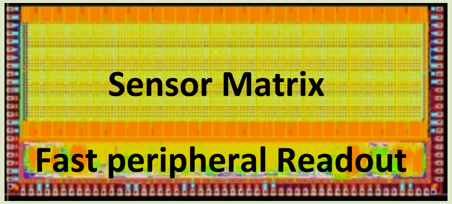
Outline

- INMAPS 32x32 prototype:
  - 1st chip on test
  - Analog response
  - Digital tests
- A5ttc (2D VI tier): analog 3x3 matrices maps on beam:
  - Set-up
  - Lab. Characterization
  - Test-beam results (MPV-Landau, efficiency)
- Conclusions

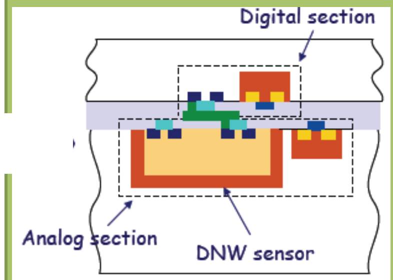
Pixel technologies under study



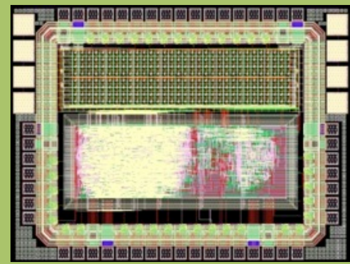
Deep N-well MAPS,
- **In-pixel** front-end electronics (pre, shap, discr).
- **competitive N-well** issue



APSEL4D chip
ST 0.13 um
Beam test **CERN 2008**.
90% efficiency compatible with deep N-well fill factor

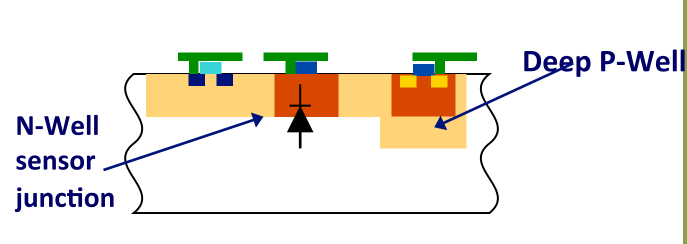


3D MAPS
- **Digital tier: dense pixel digital logic** and peripheral readout
- **In-pixel** analog FE
- **Less competitive N-well issue**

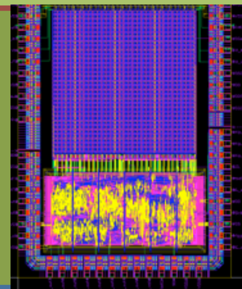


APSEL3D
Tezzaron
Chartered
32x8 matrix

Ongoing tests

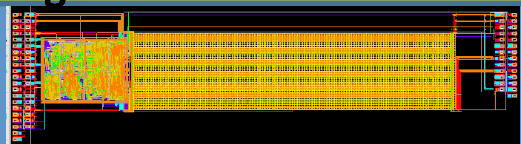


INMAPS technology
- **Deep P-well preventing charge-stealing** by competitive N-wells.
- **High resistivity substrate → more robust against radiation.**

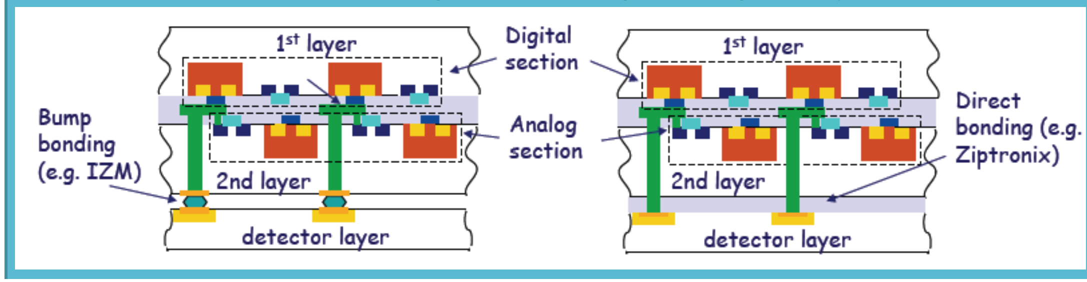


INMAPS 0.18 um
32x32 matrix
submitted July 2011

Hybrid Pixels 50x50 um pitch
- High resistivity, **fully depleted sensor**
- **Fast readout** (analog FE and digital logic at pixel level)



SuperPix0 chip
- **Beam Test** Sept. 2011.
- **Preliminary results presented**



FUTURE… 3D front-end chip
- Dedicated **digital tier**
- **analog tier:** FE electronics.
- **Fully depleted detector** Bump Bonded / Directly Bonded

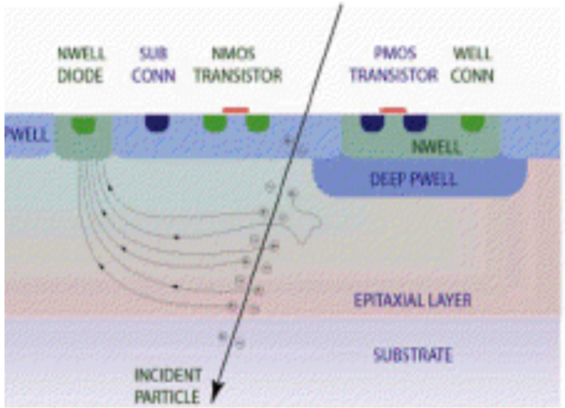
Why INMAPS

Standard MAPS: Tolerance to displacement damage could be a showstopper.

Avoid charge collection in parasitic N-wells by means of a buried P-type layer (deep P-well)

Improved charge collection by means of high resistivity epitaxial layer (~1 kOhm cm)

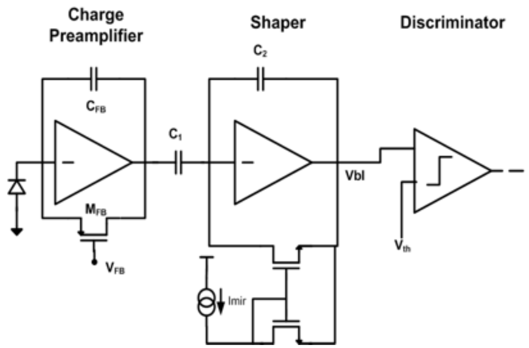
A high-resistivity, fully depleted sensing layer with analog CMOS front-end might be the solution.



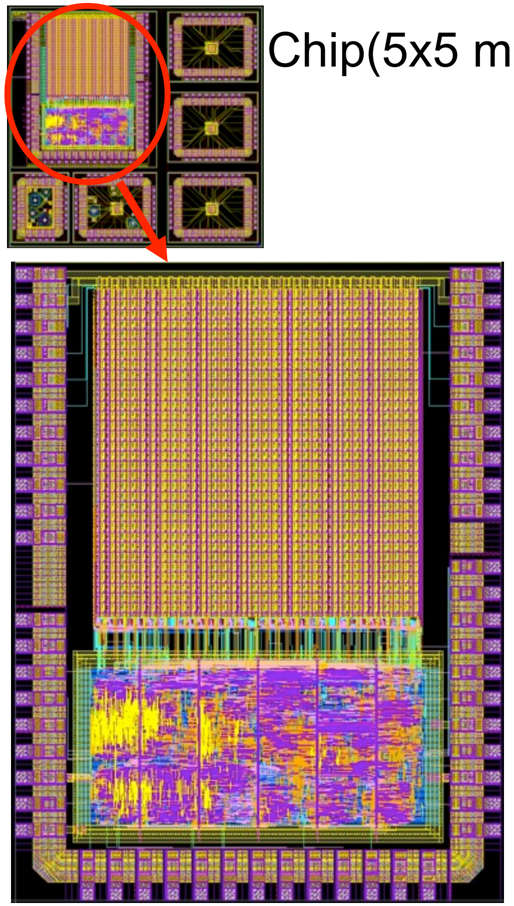
CMOS sensor in the 180nm INMAPS process with high-Ω epilayer

INMAPS developments for SuperB Layer0

- Small N-well collecting diodes with small input capacitance and low power consumption.
- The forth-well prevents charge stealing by the parasitic N-wells (→efficiency benefit).
- Same analog and digital architecture as APSEL chips, to fit at best the high background rate of Layer0.



Charge sensitivity	930 mV/fC
Peaking time @ 800 injected electrons	240 ns
ENC (estimated C_D = 40 fF)	30 e rms
Threshold dispersion before/ after correction	22 e rms
Analog power consumption	18 μW/pixel
Detector capacitance	40 fF
Matrix size	32x32 pixels
Pixel pitch	50 μm



Chip(5x5 mm^2)

Matrix 32x32

Submitted: 4th July

Received: Dec. 2011)

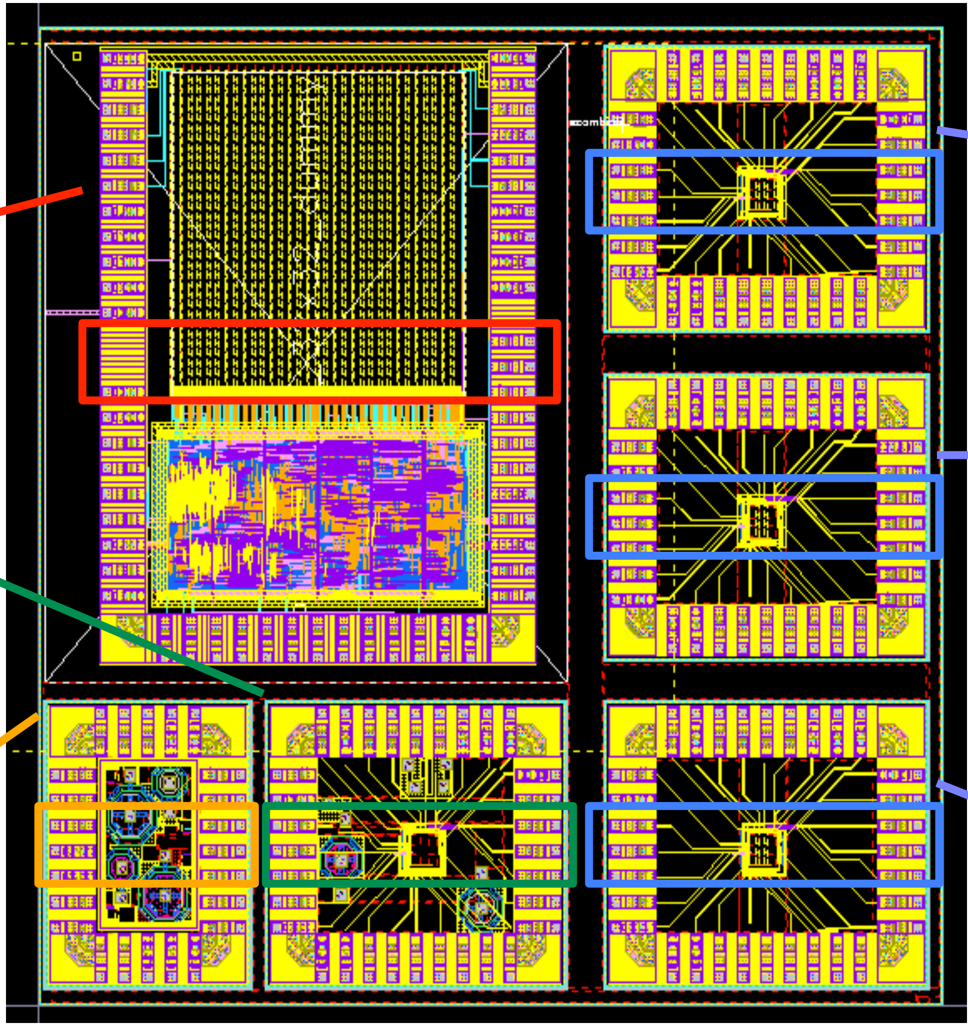
INMAPS CHIP

In 3x3 matrices all the analog outputs are available and an injection capacitor is connected to the central pixel

32x32 matrix (4-diode pixels) with sparsified digital readout architecture

3x3 matrix, 4-diode, no DPW, preampli input device with EL structure, Nw/Pepi diodes and accumulator capacitors

Nw/Pepi diodes, single channels

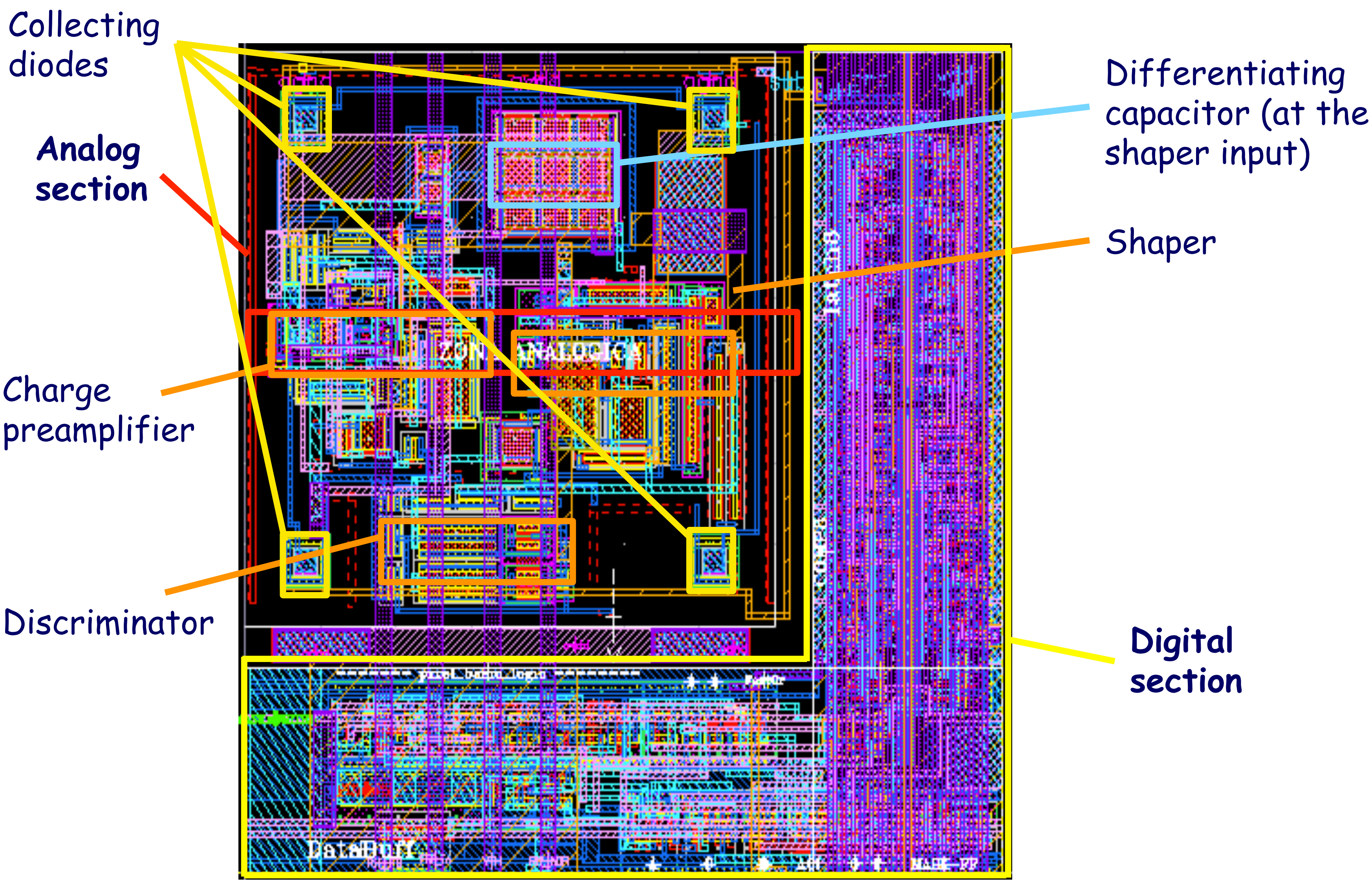


3x3 matrix, 4-diode pixels, DPW, preampli input device with EL structure

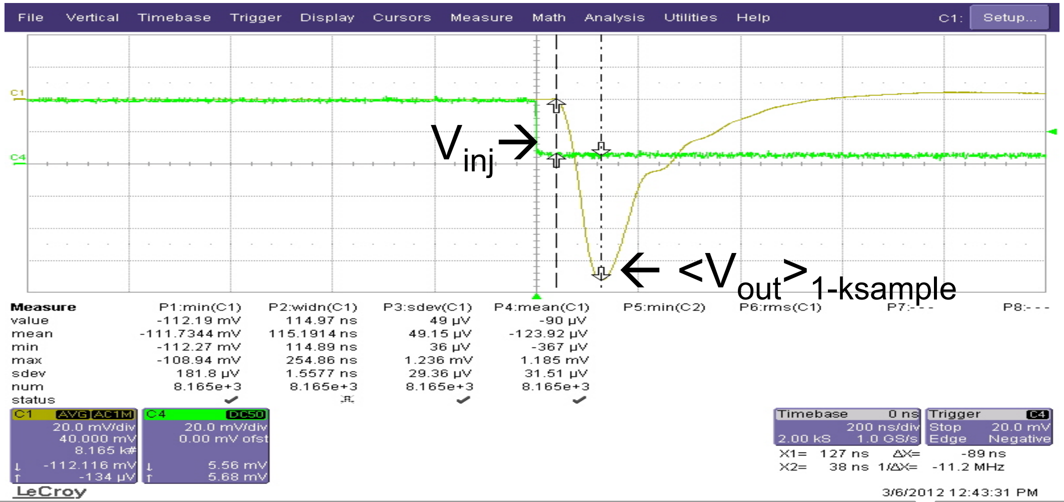
3x3 matrix 4-diode pixels, DPW, preampli input device with open structure

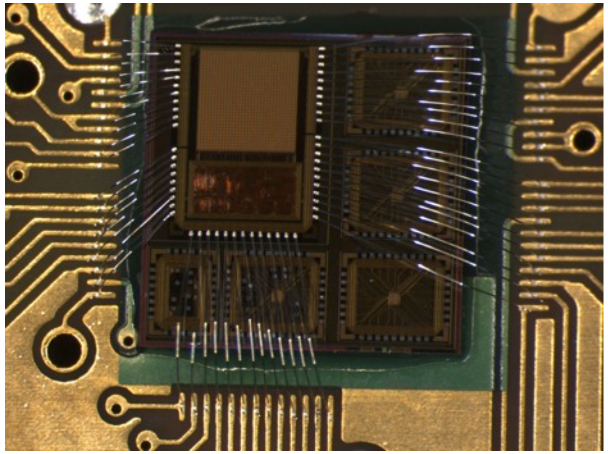
3x3 matrix 2-diode pixels, DPW, preampli input device with EL structure

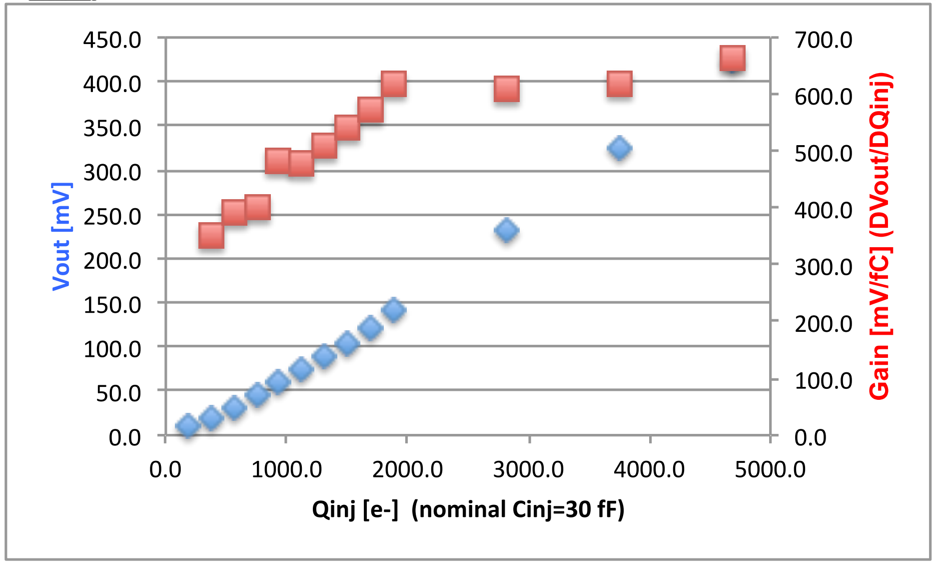
INMAPS CELL

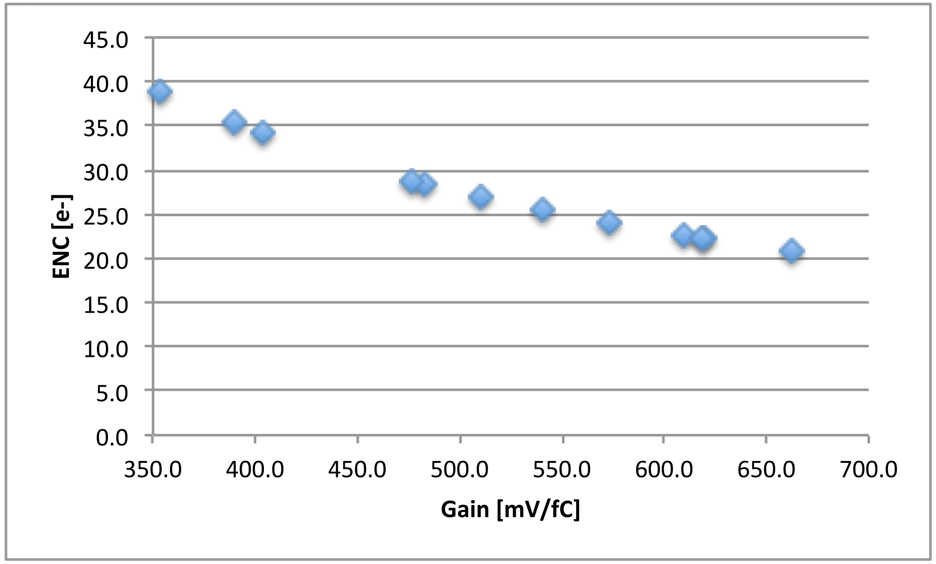

Collecting diodes
Analog section
Charge preamplifier
Discriminator
Differentiating capacitor (at the shaper input)
Shaper
Digital section

Gain Calibration on pixel(31,31) by C_{inj}



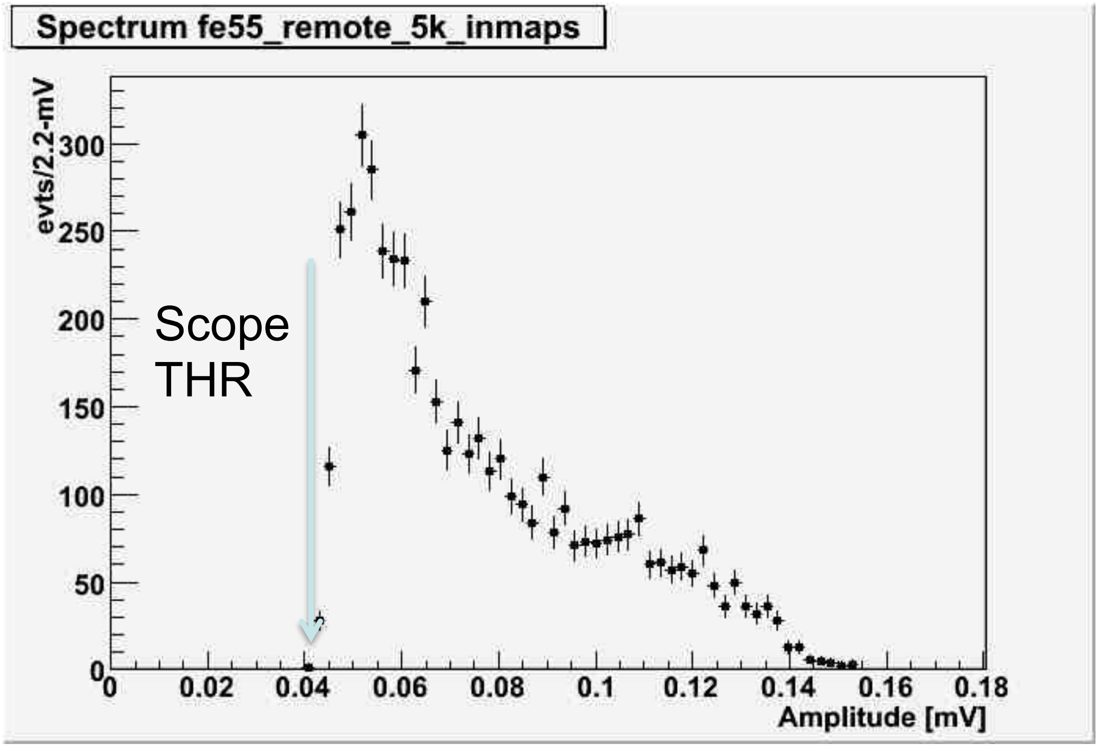






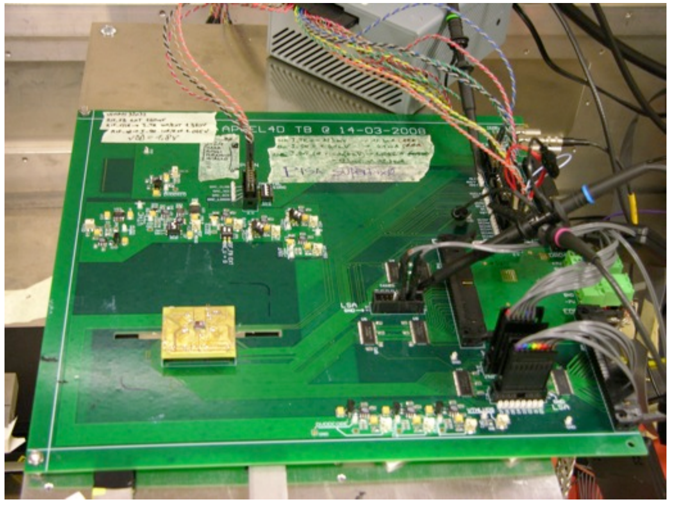
The pixel having analog output used to verify the correct working point (Rif_FB, Rif_Mir, Rif_IN): Vout has a RMS_{noise}~2.4 mV.

Gain calibration pixel(31,31): Fe^{55} source



With 1.5-h statistic, apparently no peak is present (RMS_{noise}~2.4 mV).
Note: The #evts in the photo-peak (1640 e-) is proportional to the depleted volume (small electrodes→much less in inmaps than in DEEP-N-well MAPS)
Considering the spectrum “endpoint” @ 130 mV → Gain~500 mV/fC
To be done for chips on High-Ω epilayer (still waiting for the info from the foundry to indentify the wafers).

Noise scan calibration



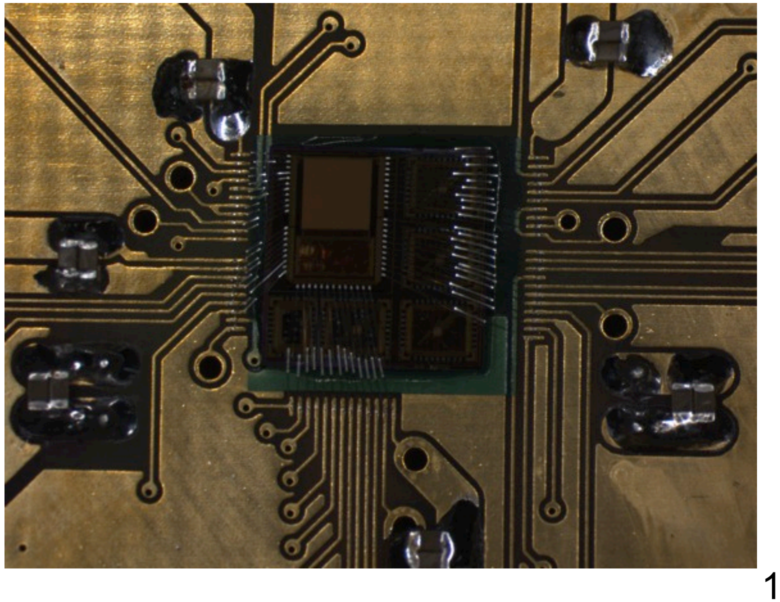
INMAPS chip on carrier mounted on the modified apsel4D board with TLA and scope probes

Set-up for INMAPS 32x32:

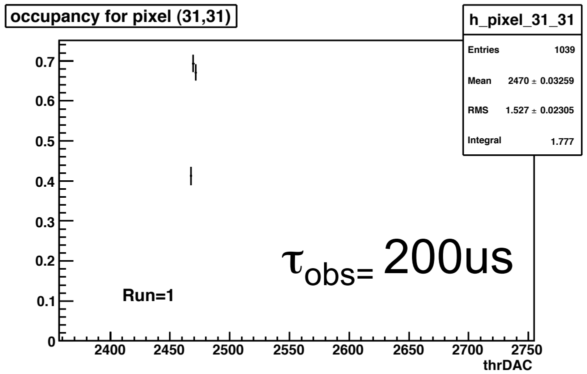
- Modified sequences (directives and operands) for chip initialization according to “user-guide”
- Implemented the noise-scan

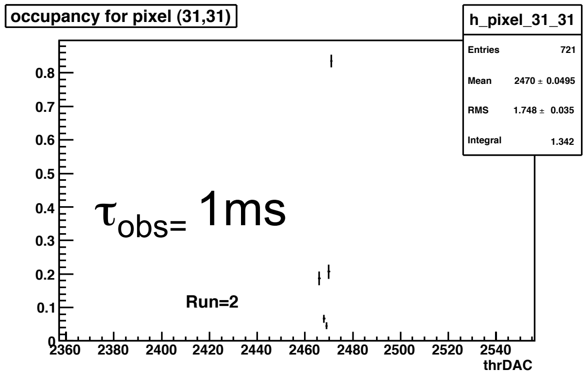
- found the (expected) limit on the buffer preventing data output from the 2nd submatrix (problem only during calibration, well dimensioned for data rate > 100 Mhz/cm^2)

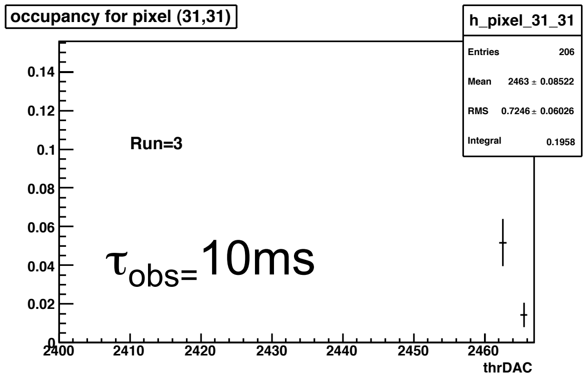
- Calibrations: ¼ chip at a time
- Noise (on the scope): 2.4 mV
- τ_{obs}= 200us → 1ms in different scan configurations

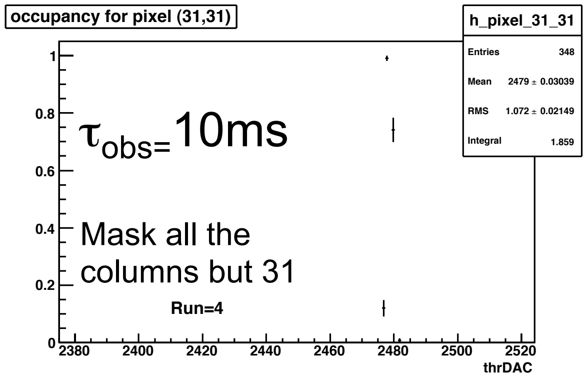


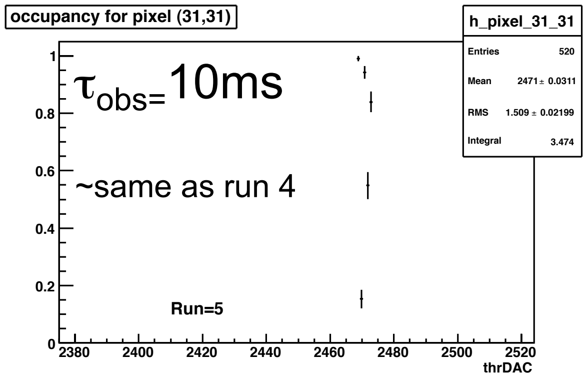
Noise scan calibrations: pixel (31,31)

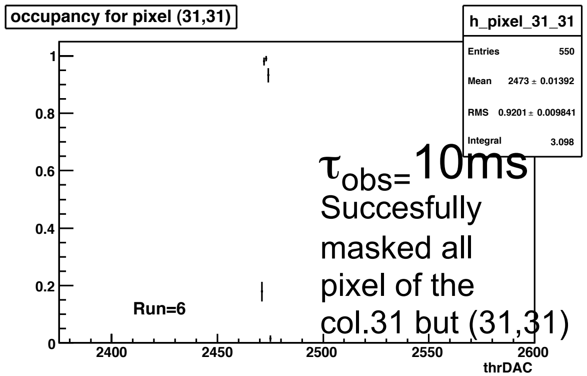








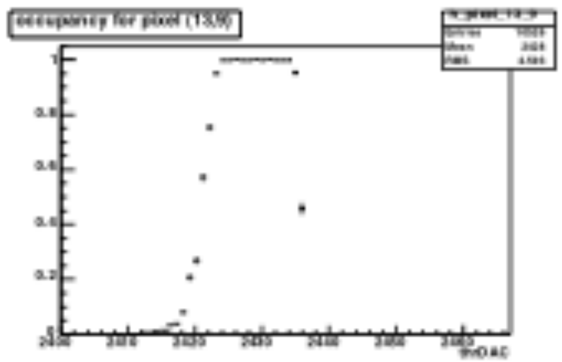




We expected that the S-curves rise/fall in some σ_{noise} (σ_{noise} =2.4 mV /0.3 ~ 7 DAC).

Instead this sharp edge is a hint of something that is causing the pixels suddenly fire, un-correlated with noise. No-change by varing τ_{obs} .

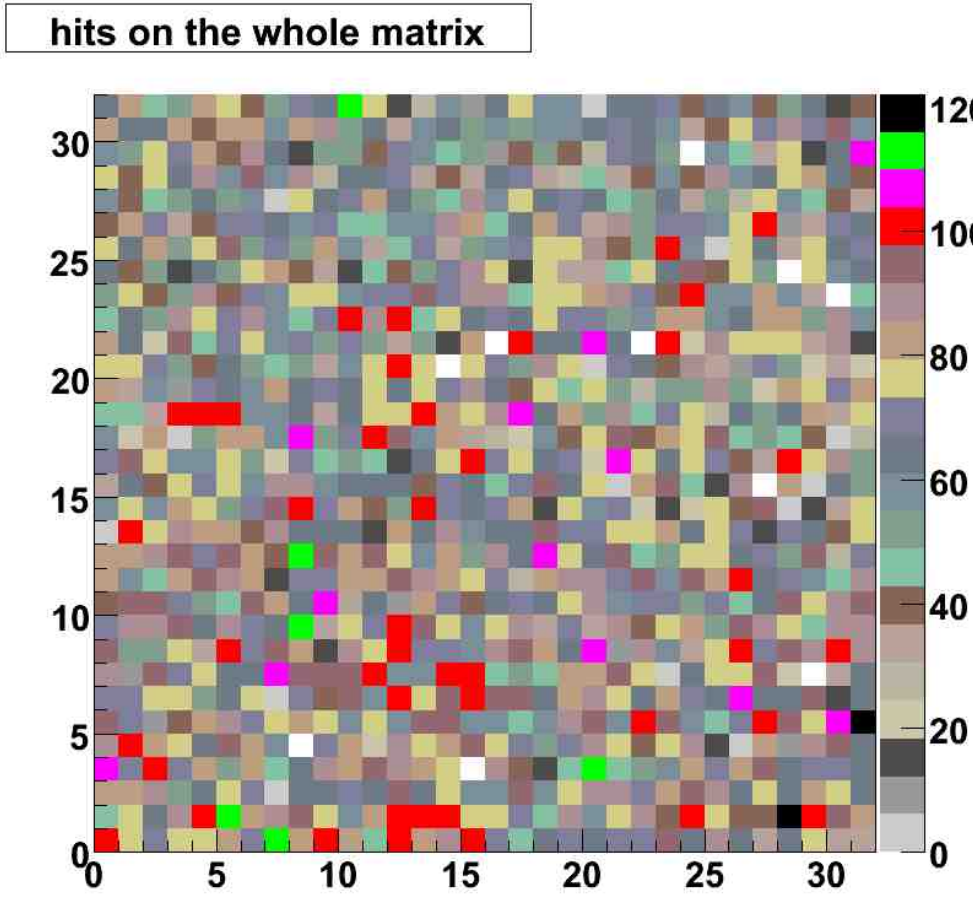
Only few pixels (out of 32x32) respond “as expected”:



HINTS of INDUCTION ?

Response to a Fe^{55} source

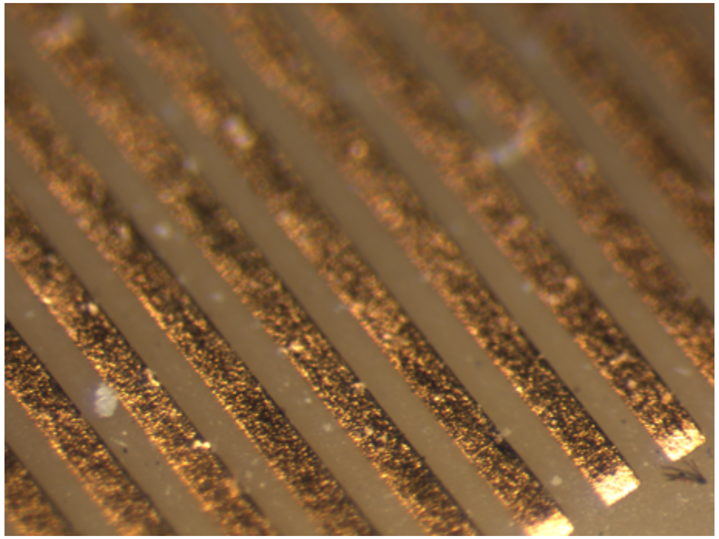
Matrix acquired at THR = 2250 DAC (→ 60 mV)
Some pixels are not responding and dis-umiformity (Gain spread?) in the matrix.

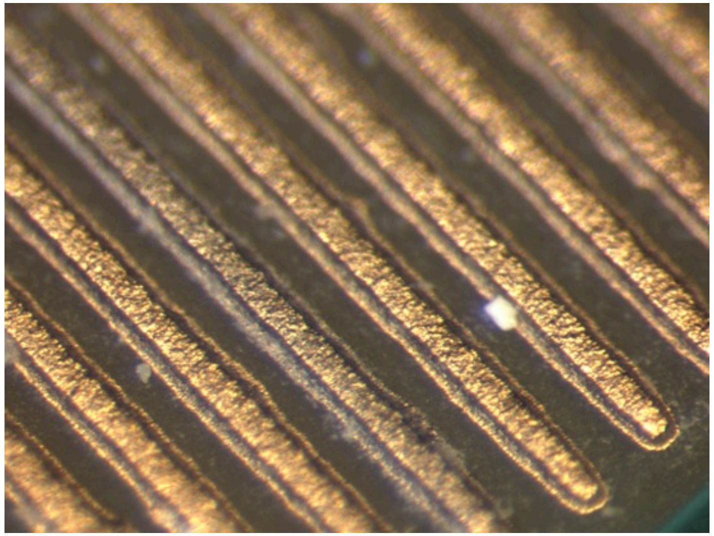


120 counts → ~1 Hz rate

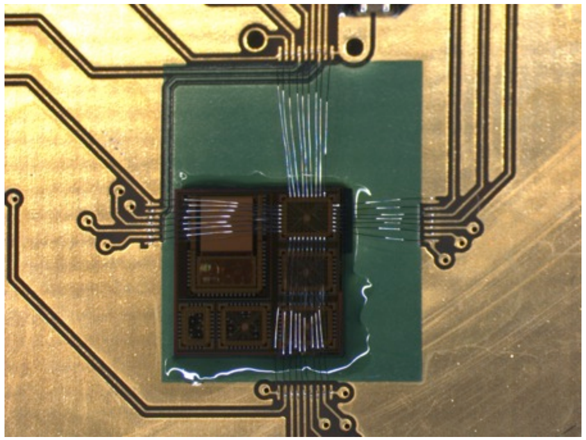
List of empty pixels
(all but one "alive" in noise scan)
x=8 y=4
x=14 y=20
x=15 y=5
x=16 y=21
x=22 y=21
x=24 y=29
x=27 y=15
x=28 y=24
x=29 y=7 Dead
x=30 y=23

Problems on INMAPS Carriers





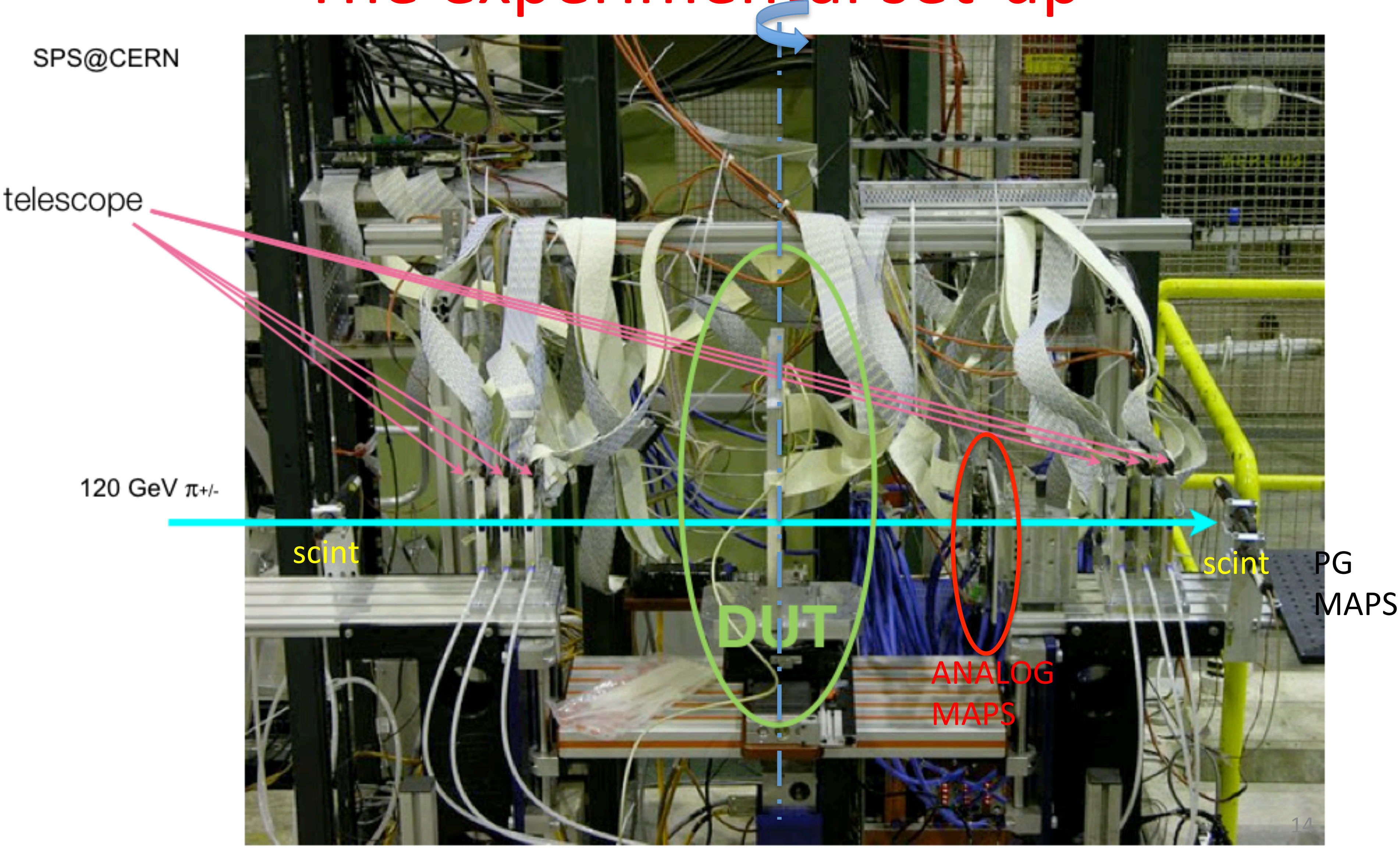
Our usual company (who made in the past dozens of carriers) is experiencing problems in the production process: the quality of the gold traces is really BAD.
F.Morsani is following the problem… This caused a long delay in the test!
We decided to proceed: with some tricks, our technician successfully bonded 2 chips on the 2^{nd} version of the carriers, even if the yield/reliability of the bonding is not ensured.



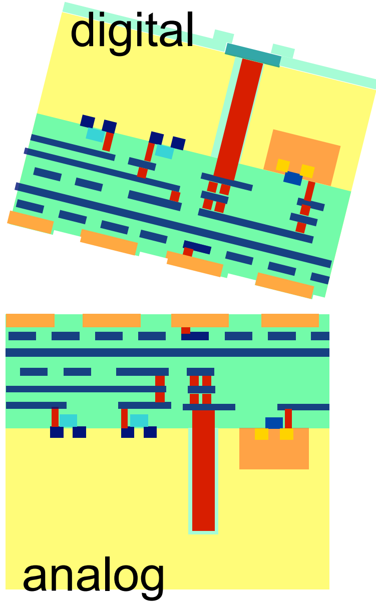
←INMAPS 3x3 analog: ready to be tested

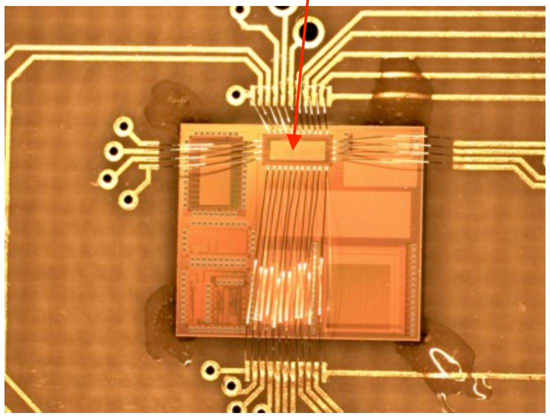
Test-beam 2011

The experimental set-up



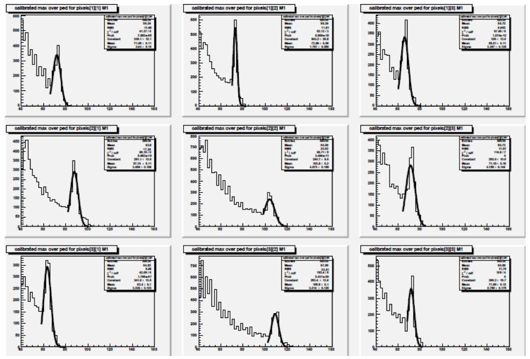
Tests of the layer with sensing electrode and analog front-end in APSEL chips from the first run of the 3D-IC consortium





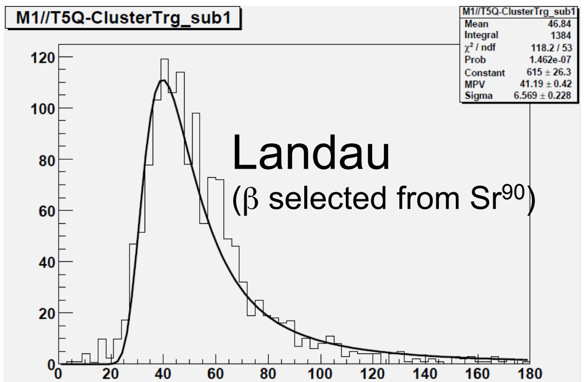
Pitch = 40 um

Fe^{55} γ (5.9 keV) on test (3x3) matrices



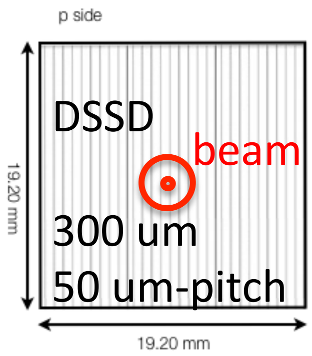
M	<μ> [mV]	<σ> [mV]	G [mV/fC]	ΔG/G [%]	<enc> [e-]
1	80	3.4	304	21	44
2	72	2.9	276	20	40

→ ENC~45e-
Gain([mV/fC] ~ 300

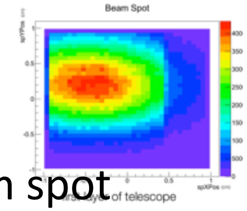


→ First estimate of MIP-signal ~ 800e-

analog signal from a pixel

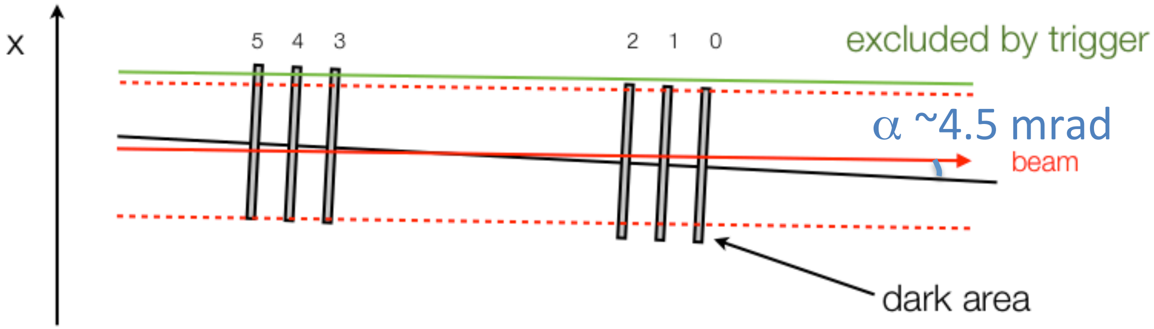


Telescope

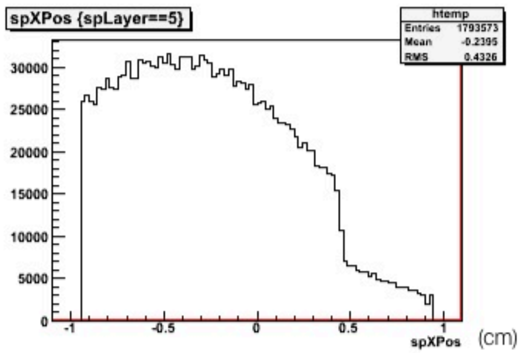


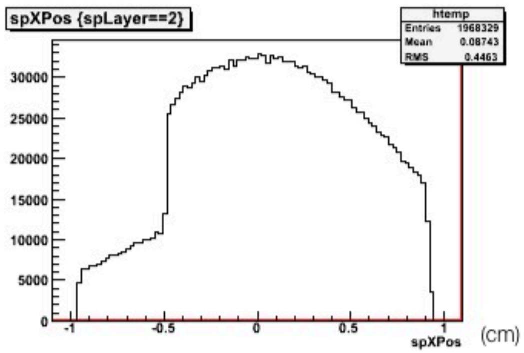
MISALIGNMENT OF TELESCOPE wrt BEAM AXIS

trigger: 1-8-8 => beam hit at least 4 layer (0,2,3,5)

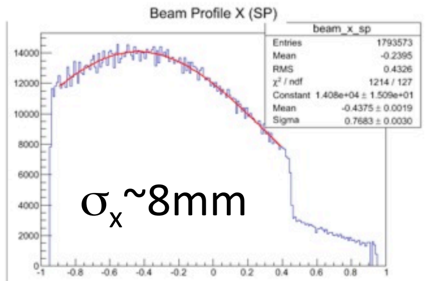


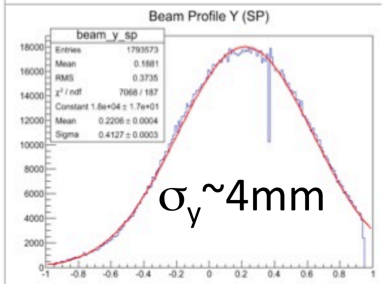
the dark area is in the positive x region for the first three layers and in the negative region for the latter.

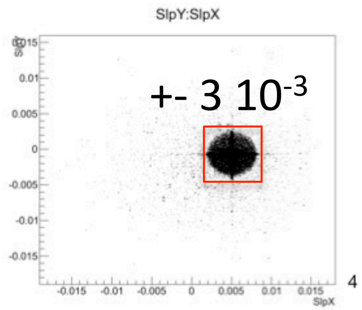




run 2277







SLOPE

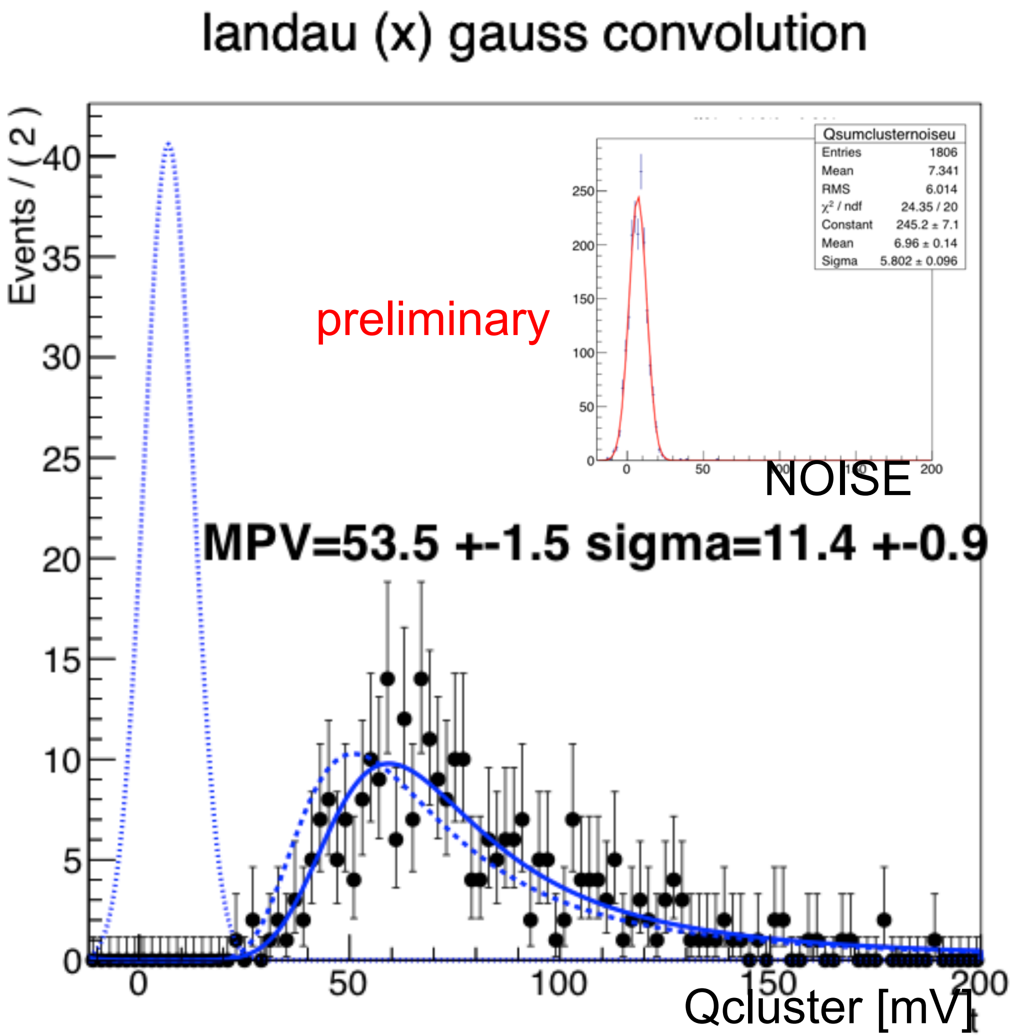
Analog MAPS on beam

- So far, analyzed only 1 matrix in one chips VI
- Alignment check: the runs must be reconstructed with the correct align. constant, otherwise a fake inefficiency may arise
- By cutting on the PH of pixels→defined the center of the matrix area with tracks extrapolated at the MAPS plane.

  Then we select a window of +- 1pitch around the center.
- Analisys to be done :
  - for the other v.i. matrix and the second chip
  - for the 2 matrices of apsel3T1 n-irradiated/not-irr
  - Apsel65 nm
- Important info:
  - Landau MPV on MIP →charge collection
  - Efficiency (parasitic n-well at work)

Chip1 m2: Landau

(#run~50, #evt-fin=301 in window +-1 pitch)



Noise events==off time window (w.r.t. scintillator)

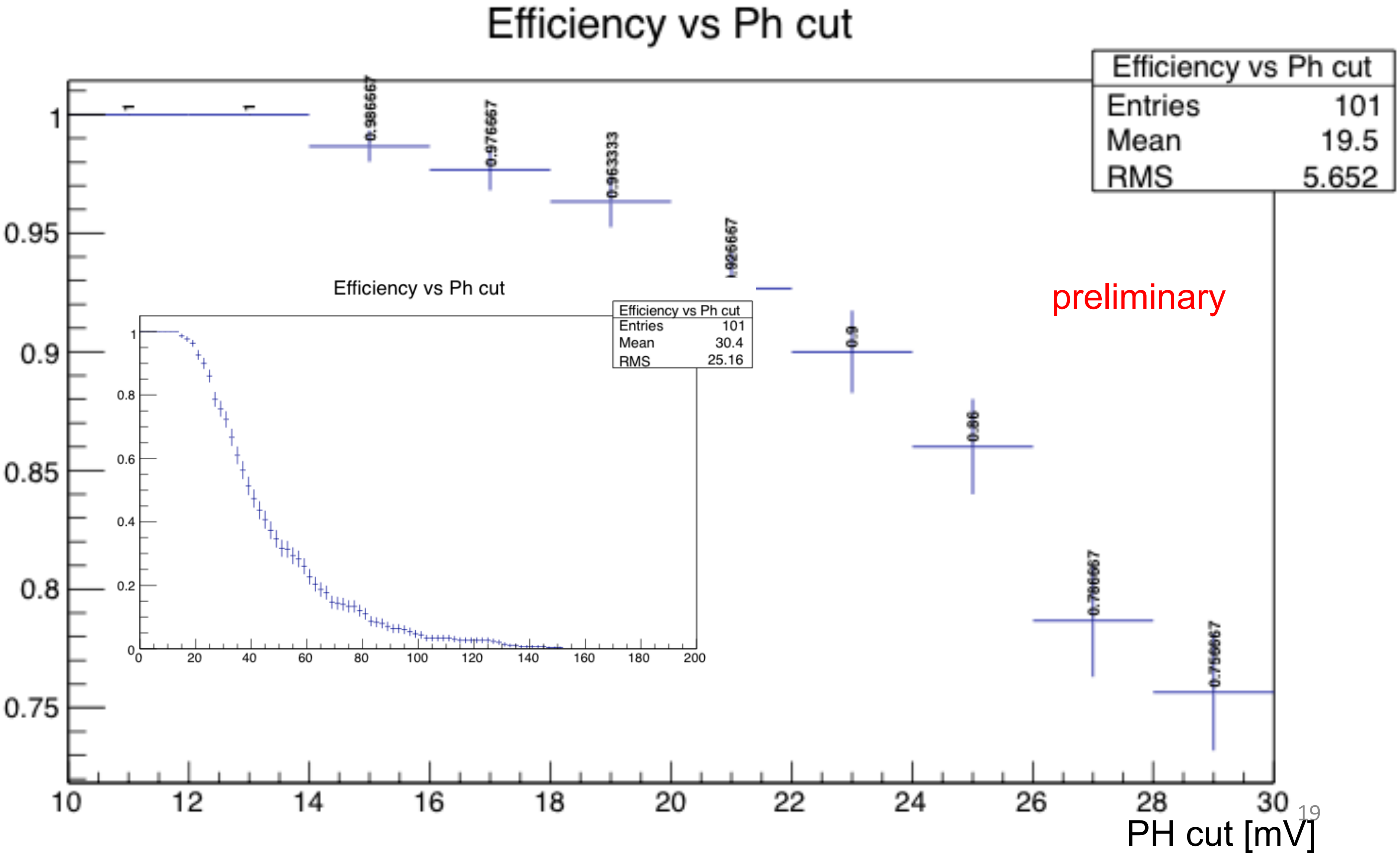
From Fe55 :G=320 mV/fC

MPV = 53.5/G/1.6e-4=1044 e-

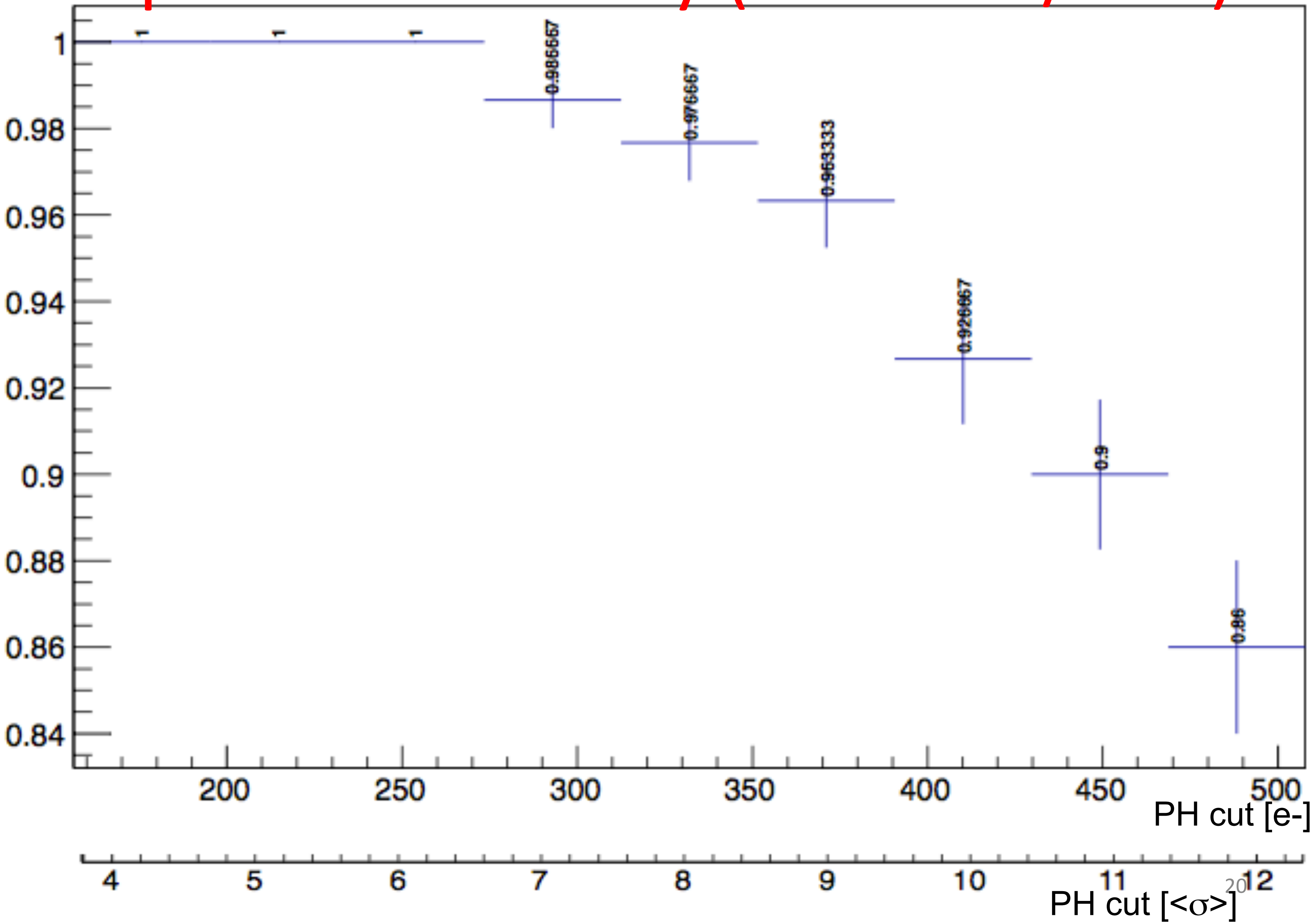
After syncing the DAQ telescope and the DAQ maps, the info is merged.
Find the max ph in a 1us after the scint. pulse.
Sum the ph@time-max of other 8 pixels to give the Qcluster

Note: there is a (+) bias is due to the max. search.
To be taken into account the gain spread (20%)

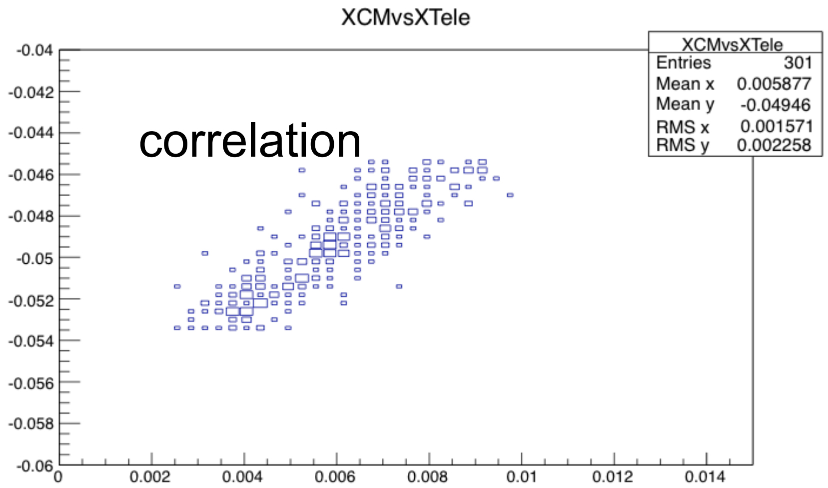
Chip1 m2: efficiency
Count the events with Phmax>Phcut
(+- 1 pitch window from the center of the extrapolated shadow)

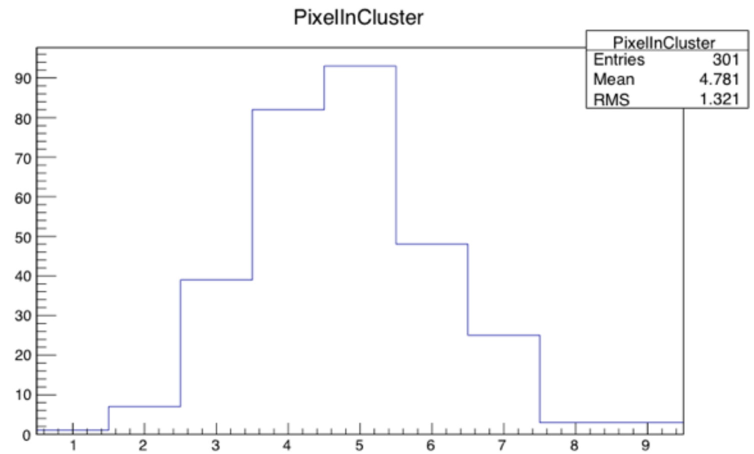


Chip1 m2: efficiency (in e- or S/<N>)

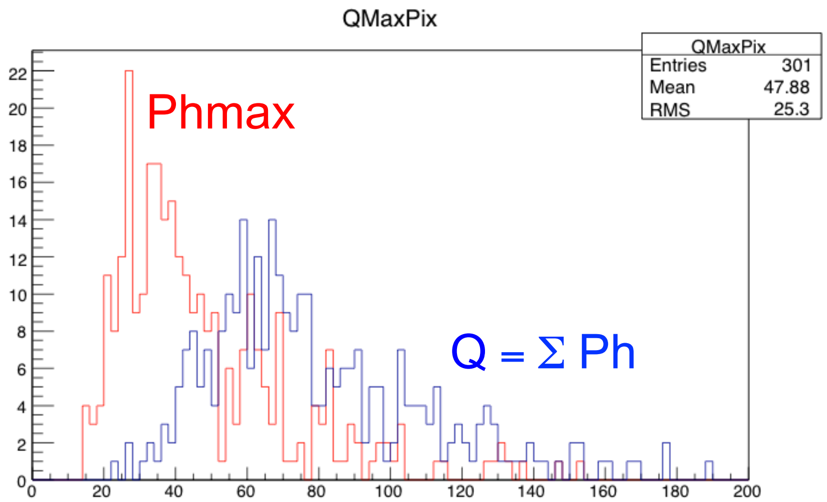


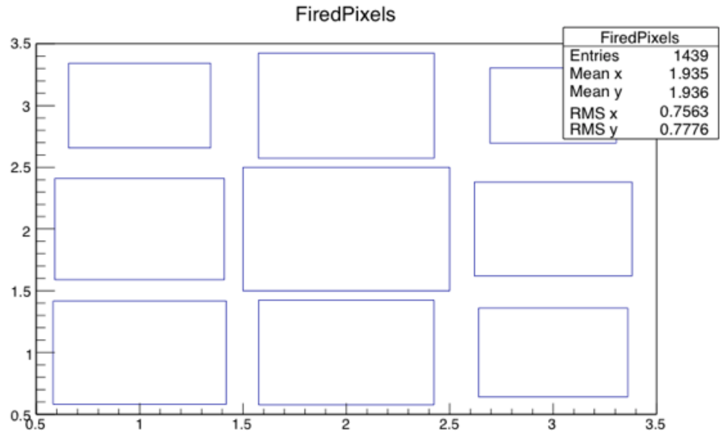
Chip1 m2



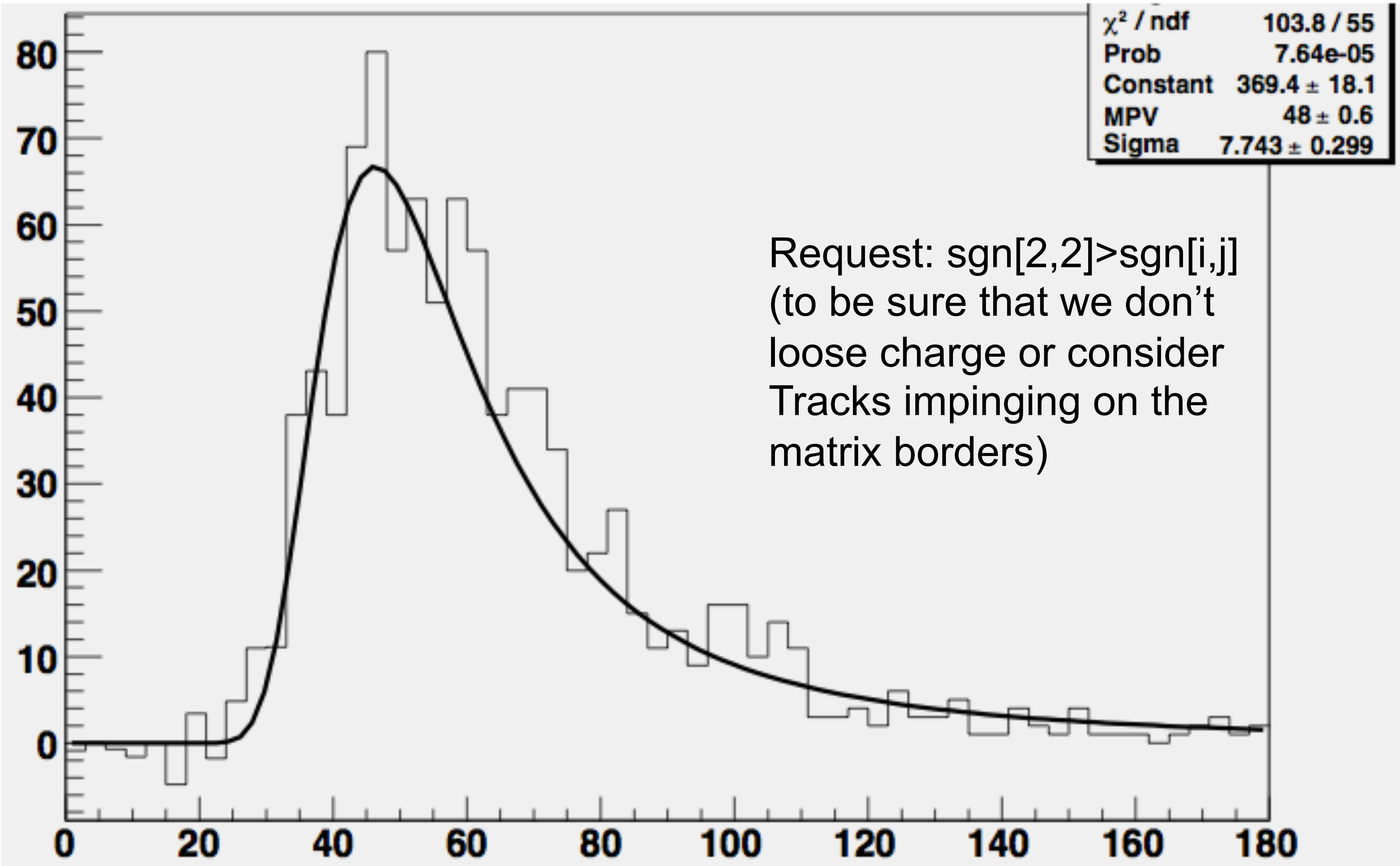


Request:
Phmax>5σ and 3σ on the others partecipating to the cluster





Lab. Test with Sr^{90} source



Request: sgn[2,2]>sgn[i,j]
(to be sure that we don't
loose charge or consider
Tracks impinging on the
matrix borders)

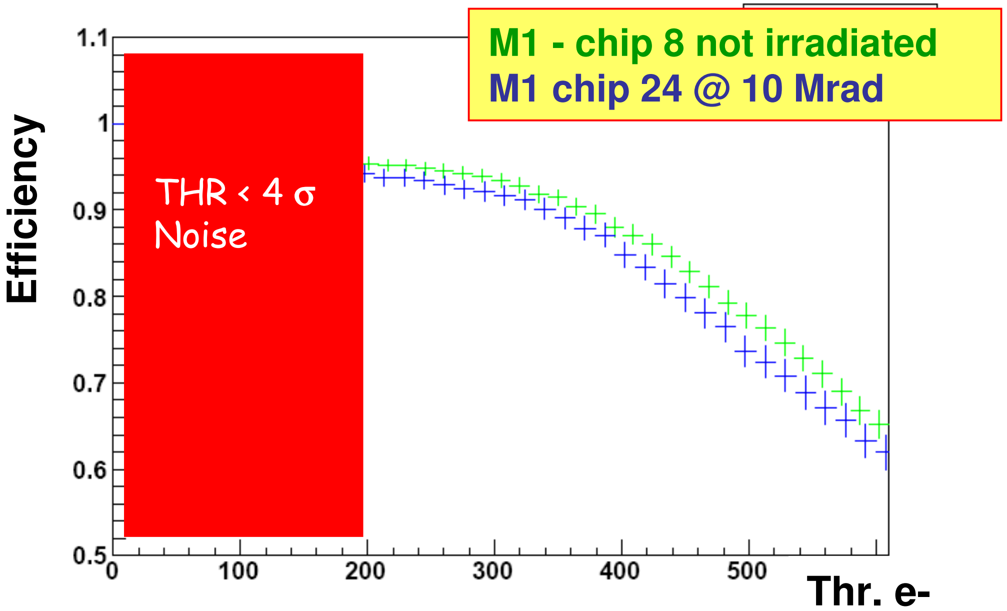
mV

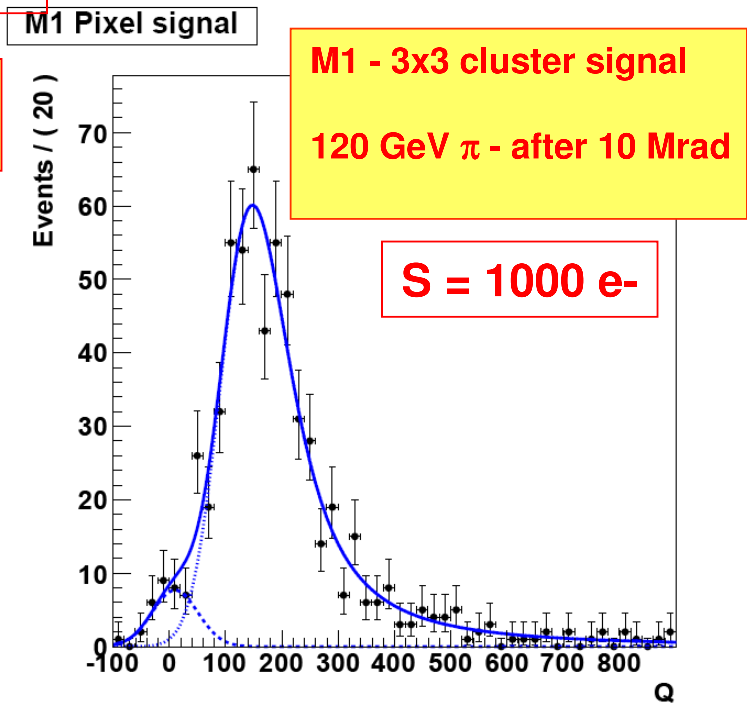
Comparison vs apsel3T1 (TB 2009)

Tesbeam with γ irradiated MAPS - 2009

Results for MAPS (3x3 matrix) with analog output (pre/post irrad. 10 Mrad ^{60}Co γ)

- Qcluster ~1000 e- for M1 (930 e- for M2)
- S/N~15-20 depending on the electrode geometry
- Efficiency~90% for both M1,2 in agreement with the measurements on digital MAPS
- Modest reduction in collected charge and efficiency in chip irradiated up to 10 Mrad
  - ENC increased by ~35% (after annealing)





Conclusions

- Preliminary tests of the latest days on the INMAPS 32x32 matrix have shown that the analog section is working (ENC~30 e-) and the basic digital functionalities are insured.
- We observed a too fast turn on/off curve: to be further investigated with more chips and systematic tests (hints of induction?).

- Promising test beam preliminary results on VI 3x3 matrix:
  - Efficiency greater than 98% for THR < 8 x <RMS(noise)>
  - Collected Q cluster ~ 1000 e-
- Analisys to be completed with the other analog structures