ETD/Online Summary
SuperB Collaboration Meeting
LNF, March 2012

S. Luitz, D. Breton, U. Marconi

For the ETD/Online Team

3 Parallel Sessions

1. Common Items
   1. Schroff xTCA for Physics presentation
   2. Raffaele – Radiation tests of FPGAs (for links)
   3. Umberto – ROM R&D
   4. Gianluigi - Power Supplies
2. Front-End Electronics / Sub-Detectors
3. Trigger, Event Data Chain and TDR discussion
   1. Paolo - Update on trigger tests
   2. Steffen / all – TDR planning & discussion

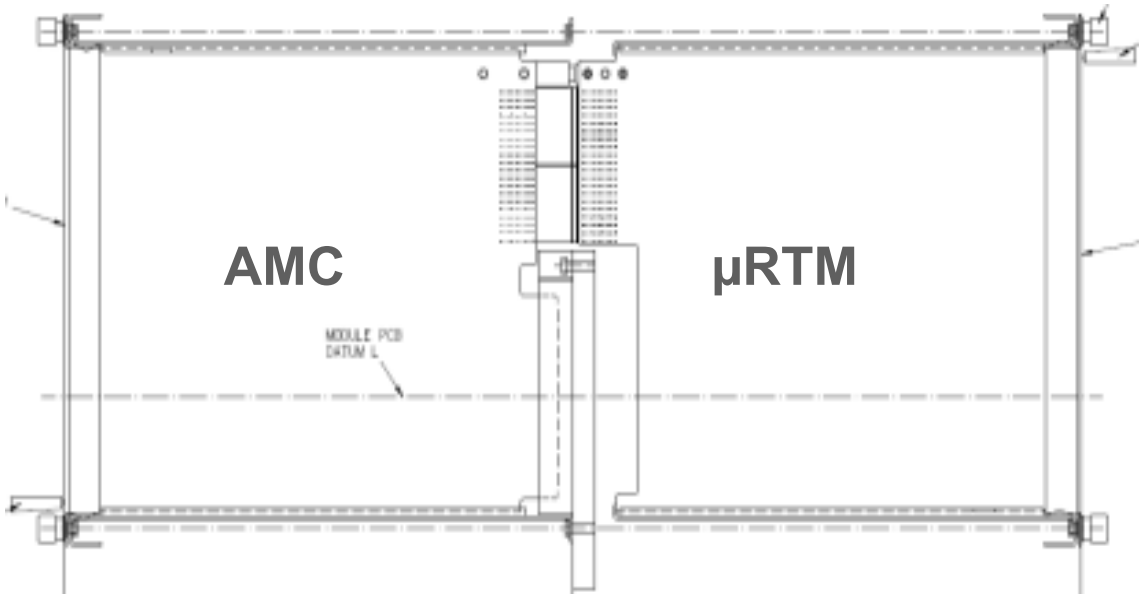
MicroTCA.4 (xTCA for physics)

Schroff

- **Why are enhancements needed to the existing MicroTCA specification?**
  - **No Rear Transition Module (RTM) for MicroTCA defined**
    - Physics applications typically require a large number of I/O cables.

    It makes sense to connect them to the rear of the chassis.
  - **Special clock and trigger topology**
    - MicroTCA.0 specifies 3 Clocks and AMC.0 R2.0 specifies 4 Telecom and 1 Fabric Clock on the AMC Module. Physics / measurement applications typically need additional Clocks and Triggers

6-slot crate



12-slot crate

Results From Serial Links Beam Testing

- Tests with 62-MeV protons at LNS, measured Virtex-5 and Virtex-6 (Xilinx FPGAs) configuration memory cross-section/bit and link design SEU-tolerance
- Virtex-5
  - New encouraging results, improvement thank to synergy of TMR + scrubbing + 'hardening by placement'
- Virtex-6
  - configuration cross-section/bit a factor 2 better than V5 family
  - however design performed worse than V5 version, reasons need to be investigated (probably failure not due to configuration errors)

- For a dose rate of 5 kGy/year (Si), 62-MeV proton equivalent

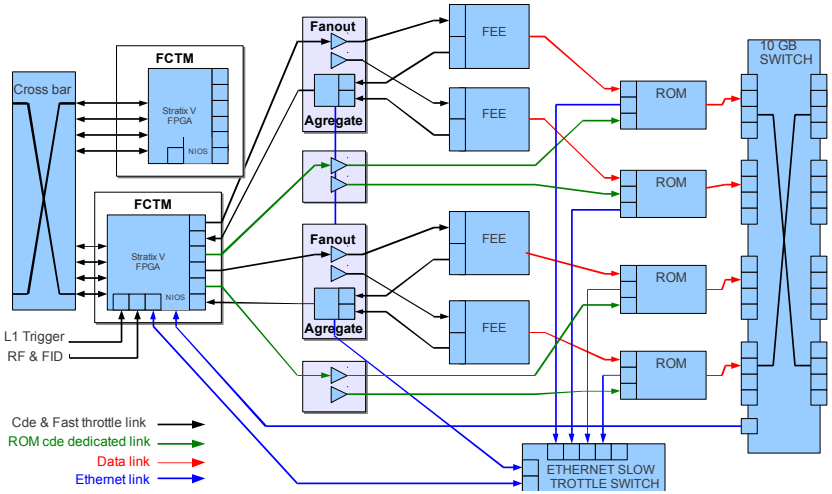
Device	Failures/ year	MTBF (days)	Notes
FPGA V5 – TMR	133	3	Current variation, removed by scrubbing
FPGA V5 – No TMR	407	1	Current variation, removed by scrubbing
FPGA V6	Too many	Too low	
TLK2711-A	33	11	TID effects, unrecoverable failure at 250-430 Gy
DS92LV18 tx	9	41	TID effects, current variation
DS92LV18 rx	0.4	1023	TID effects, current variation
DS92LV18 loss-of-lock	2.1	170	TID effects, current variation
DS92LV2421 (tx)	856	0,43	No current variations vs TID

- Test of the Texas DS92LV2421 Serializer
  - candidate for data links only, huge and variable latency
  - very sensitive to radiation (weaker than designs in V5 FPGAs)
- So far, DS92LV18 is (by far) the most reliable device tested
- Next test beam (@LNS, 62-MeV protons) scheduled for July 2012
  - Will focus on Xilinx Kintex-7 FPGA family and optoelectronics

Raffaele

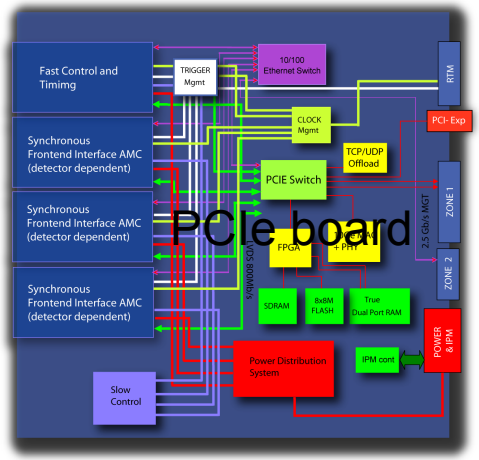
ROM Status

Umberto



ROM throughput ~ 10 Gb/s
150 kHz × 500 kByte: ~ 60 ROMs

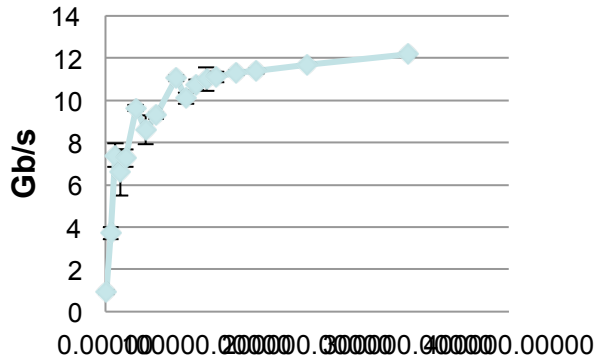
PCIe board DMA PC memory load
10 Gb/s achievable with buffer size ~500 kB



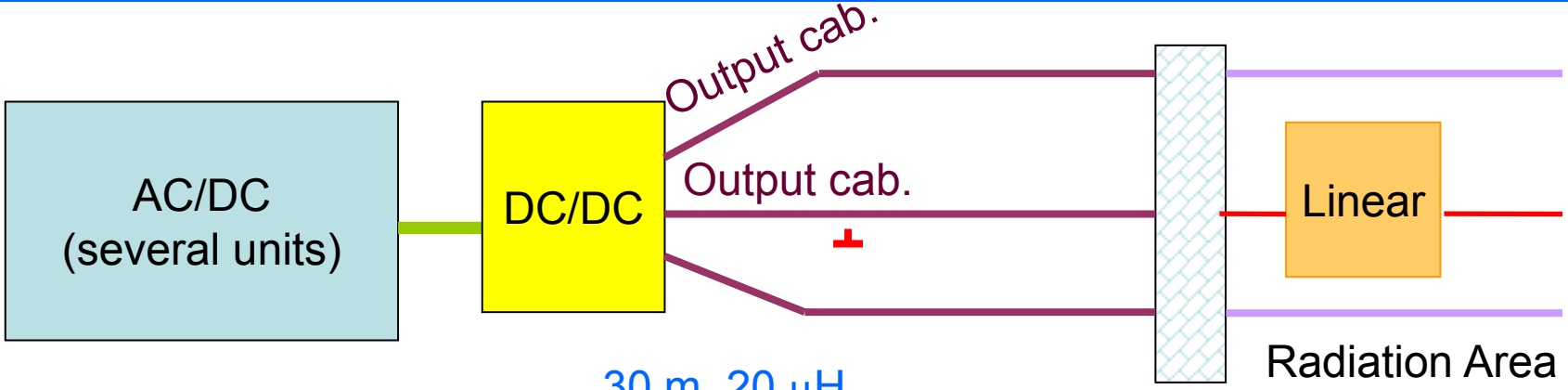
PCIe board emulator

~ 10 Gb/

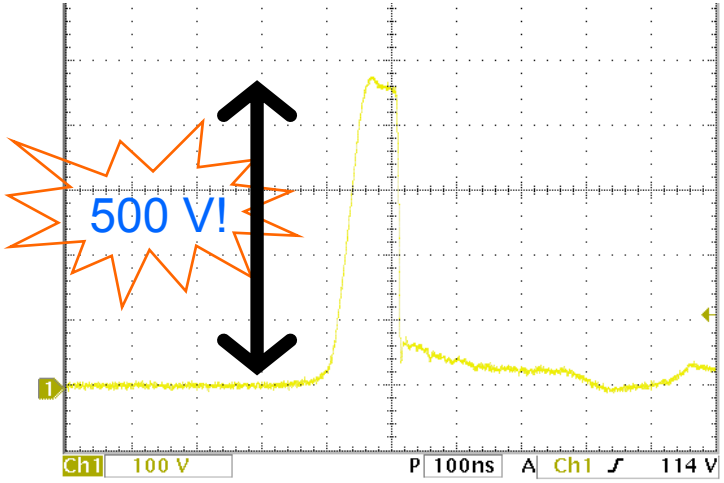
Host PC



Voltage supply system strategy (INFN Milano-Bicocca)



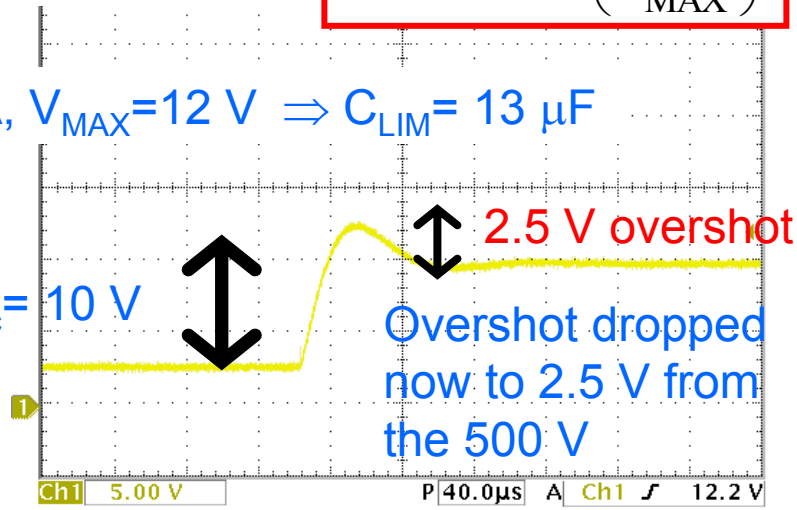
Voltage overshoot, after a short c. at the load with C_{LIM}0F



Overshoot after C_{LIM} satisfies:

$$C_{LIM} \geq L_{cable}\left(\frac{I_{short}}{V_{MAX}}\right)^2$$

I_{SHORT}=10 A, V_{MAX}=12 V $\Rightarrow$ C_{LIM}= 13 μF



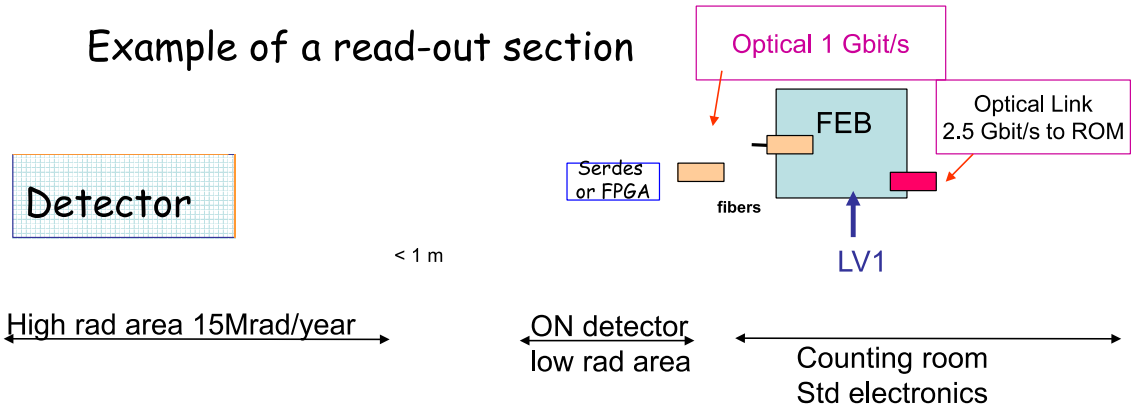
Gianluigi

Need to understand rad-hardness requirements first …

Update on HDI design and peripheral electronics

M. Citterio(MI)

Example of a read-out section

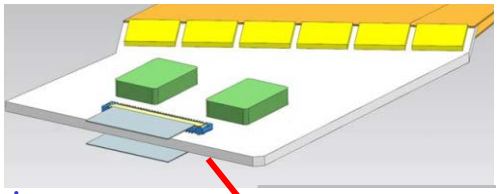


Mauro

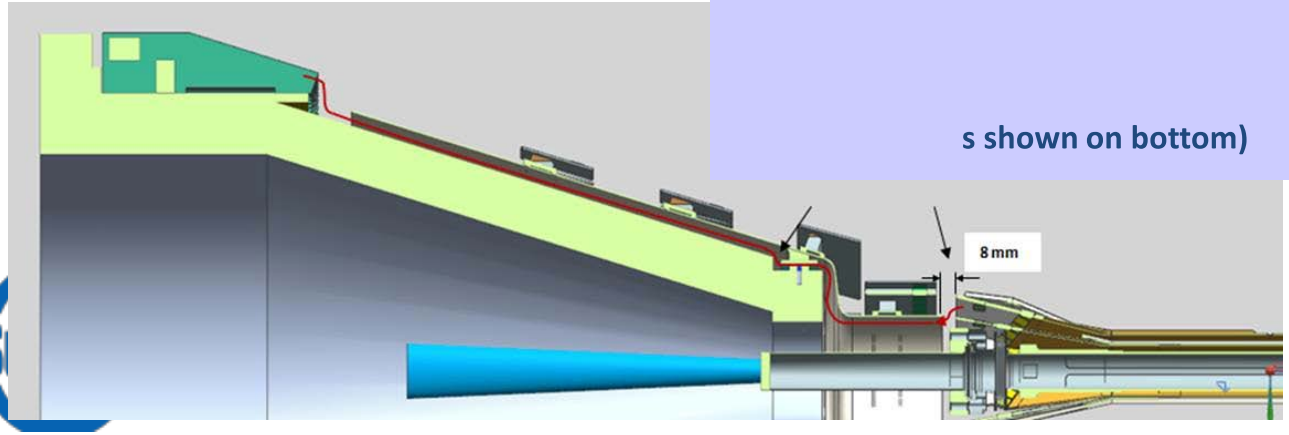
Progress on the definition of the on detector reading chain, still some options open and not all the details defined.

Choices are a compromise among:

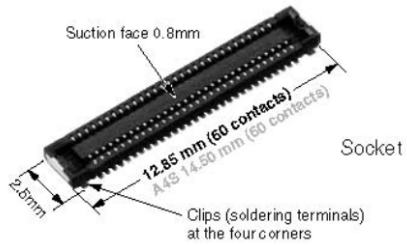
- data rates, number of lines & where to put serialization
- space is critical for HDI, connectors, copper bus, transition cards



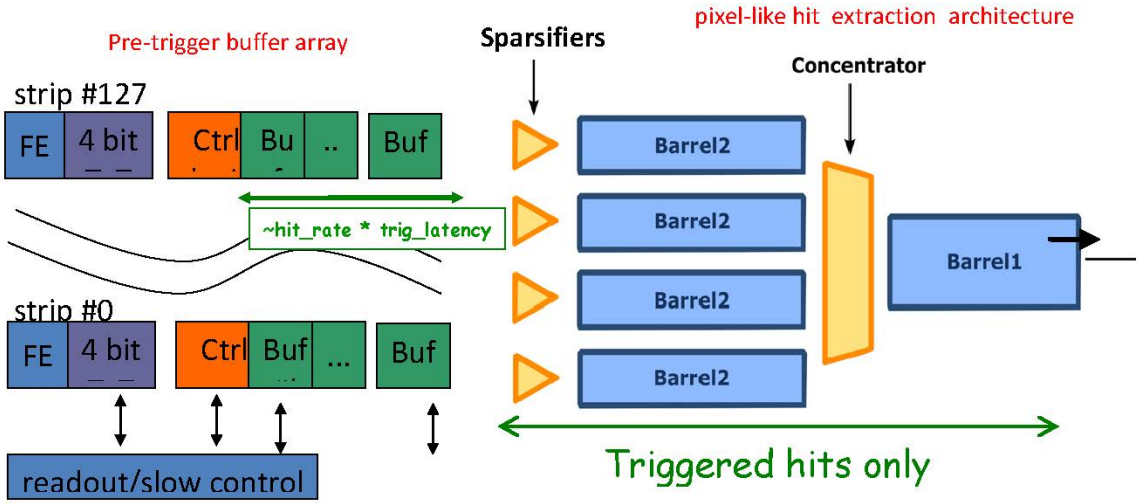
1. The world's smallest size* (width: 2.5 mm, Terminal pitch: 0.35 mm and Mated height: 0.8 mm)
The footprint when mated is down approx. 10% from our existing A4S model (60 contacts), contributing to the functionality enhancement and size reduction of target equipment.



s shown on bottom)



Strip readout architecture under development



Asynchronous logic assumed:

Triggered event size not known a-priori

(thus readout time as well)

Simulation results (L0/L1)

ASIC

2 MHz/strip : Layer 0

buffer size	16	32	64
buffered hits	3.8 M	12.9 M	12.9 M
of which triggered	23363	76850	23363
output triggered hits	14679	76849	23363
triggered hit lost	8684	1	0
Efficiency (%)	**62.8**	**99.9987**	**100**

How many buffers?

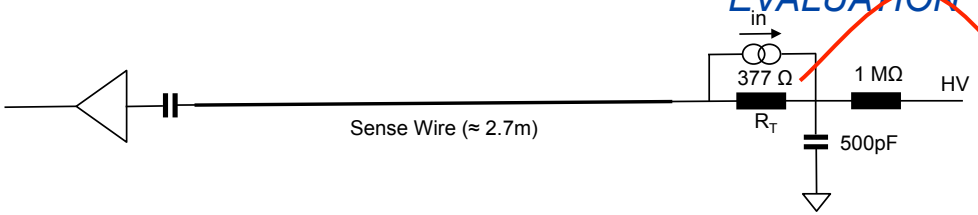
How many barrels?

760 kHz/strip : Layer 1

buffer size	8	16	32
buffered hits	1.4 M	7 M	7 M
of which triggered	8748	28829	28829
output triggered hits	6788	28825	28829
triggered hit lost	1960	4	0
Efficiency (%)	**77.6**	**99.986**	**100**

Giulietto

CLUSTER COUNTING FE CHAIN NOISE EVALUATION



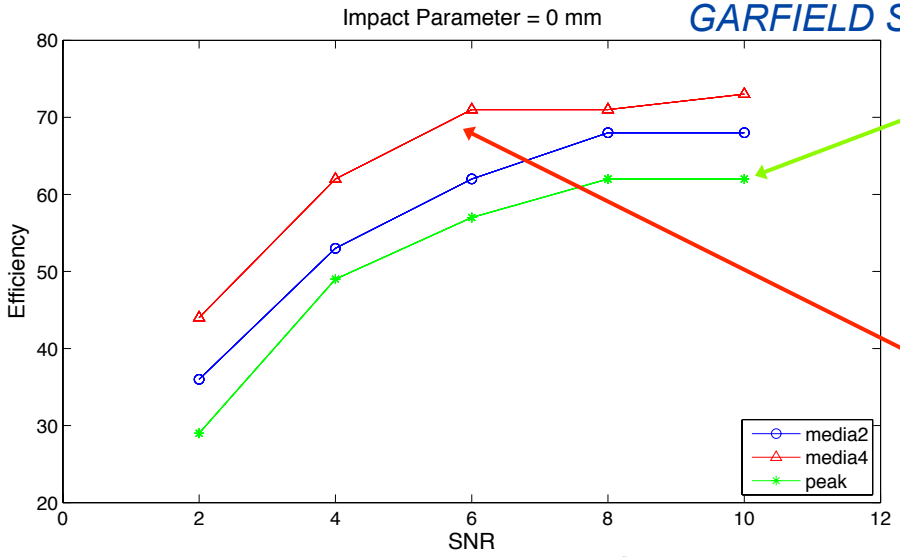
$$ENC = e \cdot \sqrt{\frac{kT}{R_T}\frac{1}{2}} \cdot \tau \simeq 0.35\ fC \simeq 2200\ erms$$

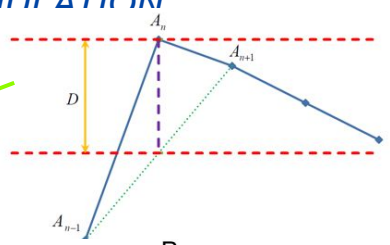
Adding preamplifier noise (≈ 2100 erms) ➡ *ENC = 3100 erms ≈ 0.5 fC*

Single electron cluster charge collected on the wire @ nominal gas gain = 10^5 ➡ *1 fC (worst case)*

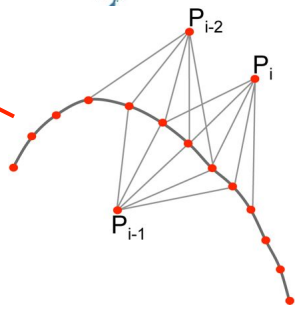
SNR = 2

CLUSTER COUNTING ALGORITHMS EFFICIENCY STUDY BASED ON GARFIELD SIMULATION





$$D = A_n - \left(\frac{A_{n-1} + A_{n+1}}{2}\right) \geq 3\sigma_d$$



$$P_i = A_i - \frac{\sum_{n=1}^{4} A_{i-n}}{4}$$

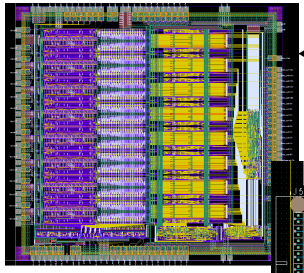
$$C_1 = P_i - P_{i-1} \qquad C_2 = P_{i-1} - P_{i-2} \qquad C_3 = P_i - P_{i-2}$$

$$(C_1 < -Thr)\ AND\ (C_2 < -Thr)\ AND\ (C_3 < -3\,Thr)$$

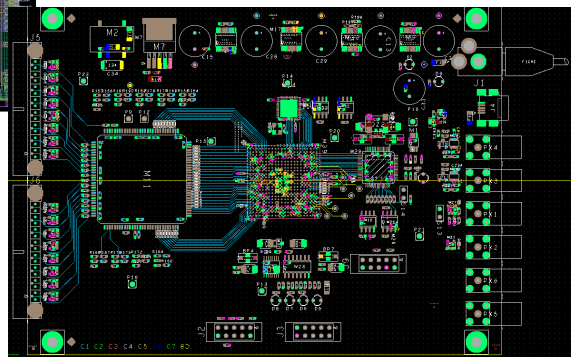
PID Electronics

Christophe

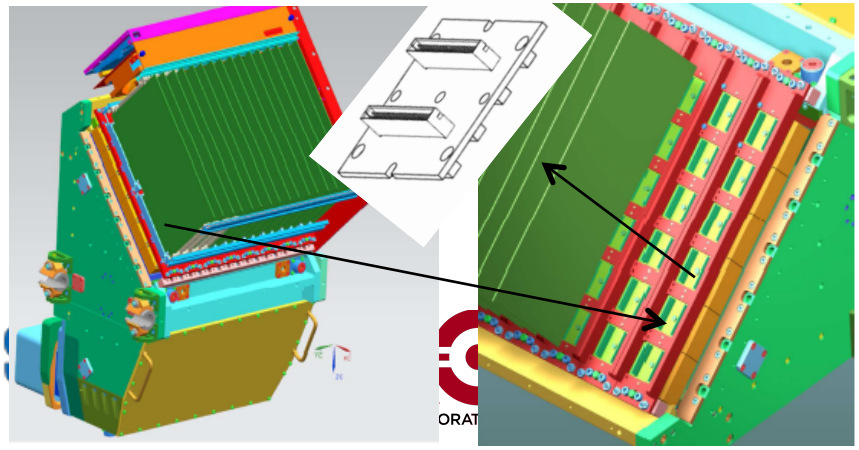
- There were 5 presentations dedicated to electronics and integration. Two on PM tests with many very interesting results on cross talk, timing performances, resolution, including results from our colleague of LHCb Rich
- FTOF : A 16-channel board based on 3.2GHz-1k analog memory is under test. First results show better than 10 ps resolution. A ps-resolution TDC called SAMPIC is under design and will be submited next month.



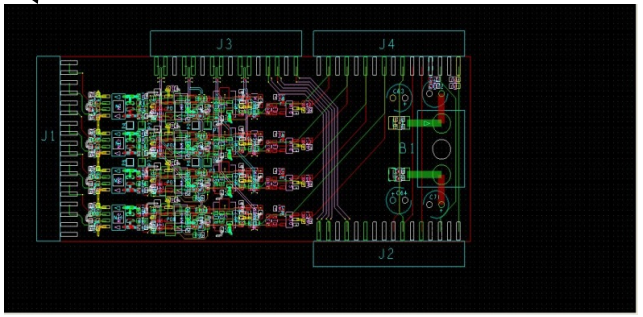
SCATS
~25 mm2 and test board



- Barrel : SCATS TDC delivered. Test board nearly finished. Software & Firmware are developed both @ LAL Bari and Padova
- Good progress on integration and design of the electronics on the FBLOCK



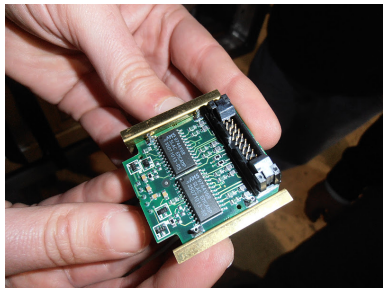
Analog board with low walk discri, to be coupled with SCATS is under test @LPNHE. The design of the Analog chip PIF started with simulations of some parts.

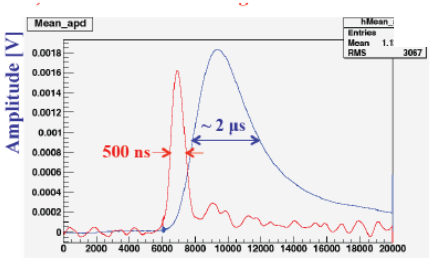


EMC

Barrel

Barrel Front End Replacemet

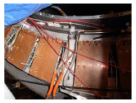


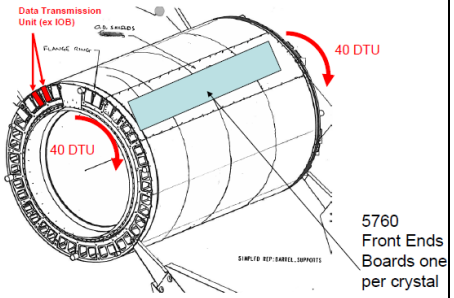


From Paolo Gauzzi

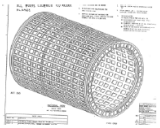
Meeting with Texas Instruments Field Application Engineer to find components candidate for a new Front Ends design with shorter integration time (hundreds of ns instead of microseconds) and shorter shaping time.
- LDO(TPS7A49) to filter and regulate voltage
- Input FET (BF862)
 CSP OPAMP (LMH6624 100mW alone under decision)
 Shaper OPAMP (OPA836)
 Differential driver (THS4521)

Location of the Front End electronics in the EMC barrel

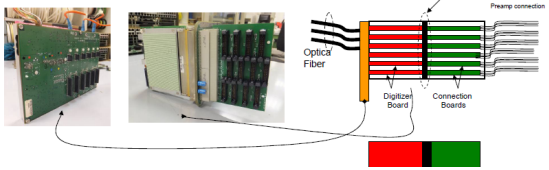


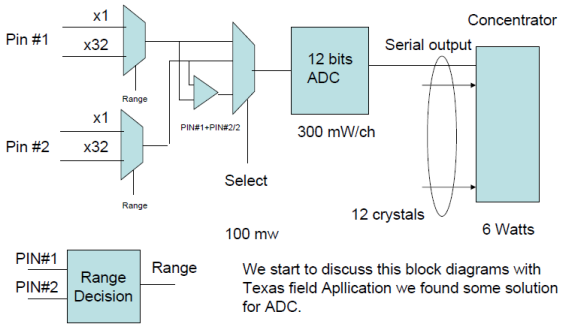


5760 Front Ends Boards one per crystal



Mini Crate structure





We start to discuss this block diagrams with Texas field Apllication we found some solution for ADC.

Forward

Valerio

Forward Crystals Tests

BGO:

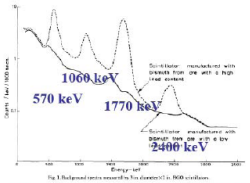
Electronic noise

- BTF test with LYSO crystal ⇒ electronic noise was ~ 250 keV
- Lab test of BGO ⇒ 1.5 – 2 MeV

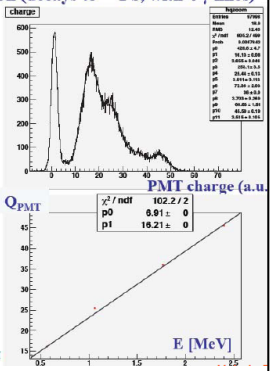
$$\frac{Noise(BGO)}{Noise(BTF)} = \frac{LY_{LYSO}}{LY_{BGO}} \frac{G_{APD}(BGO)}{G_{APD}(BTF)} \frac{1}{Atten_{BTF}} =$$

$$= \frac{75}{9} \frac{1}{4} \frac{1}{0.175} \simeq 10$$

- BGO activity due to ^{207}Bi contamination (decays to ^{207}Pb, with 4 γ lines)



[from Lewis, NIMA264(1988)534]



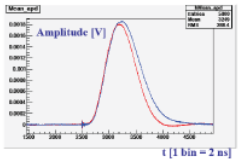
P.Gauzzi

3rd SuperB CM

BGO - APD signal

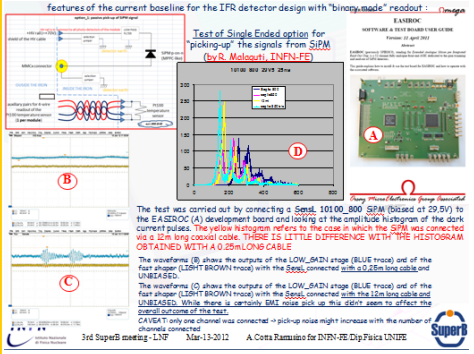
Bin by bin average over 50000 waveforms

- CSP Hamamatsu i.t.= 1 μs
  s.t. = 500 ns
  FWHM =1.2 μs
- CSP Cremat i.t. = 140 μs
  s.t. = 500 ns
  FWHM = 1.4 μs

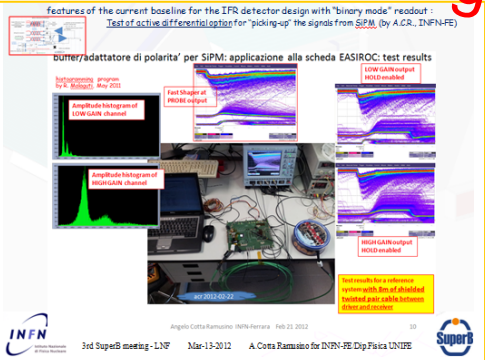


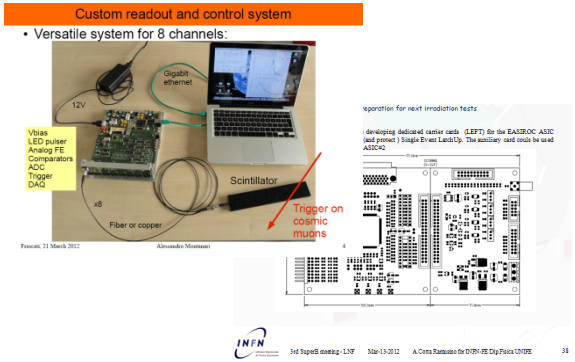
SuperB IFR electronics update: summary slide

Angelo



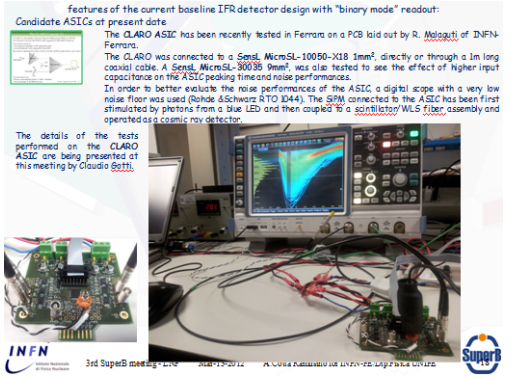
❑ two options for coupling the SiPM signals to the EASIROC ASIC have been tested. Both allowed the SiPM to be located at least 8m away from the ASIC. Acknowledgment to the LAL Omega Group for providing the EASIROC test board



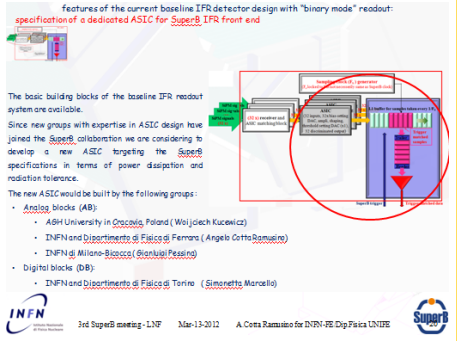


❑ more irradiation tests are being planned to study cumulative effects on SiPM (also with a new readout system by INFN-Bologna) and to evaluate TID effect and SEL rates for present candidate ASICs (EASIROC, RAPSODI ASIC#2 and CLARO)

❑ the new "CLARO" ASIC, developed at INFN-Milano Bicocca by Gianluigi Pessina's group, has been successfully tested with signals from a 1mm^2 SiPM. "CLARO" is also a condidate ASIC for the baseline design of the IFR readout



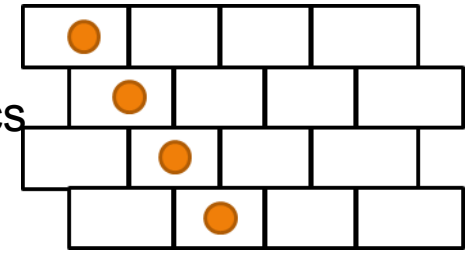
❑ the development of a new ASIC for SiPM readout complying with the IFR constraints is being planned. It would result from a joint effort of teams from AGH University, INFN Milano Bicocca, Dip.to di Fisica and INFN Torino, Dip.to di Fisica and INFN Ferrara

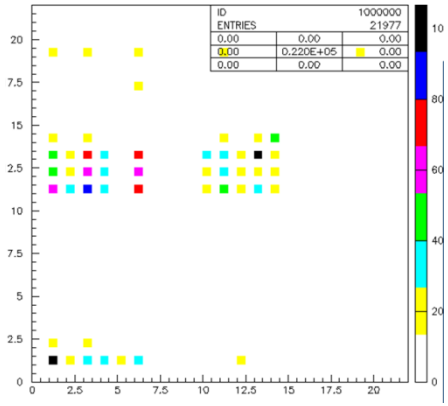


Trigger system integration with DC

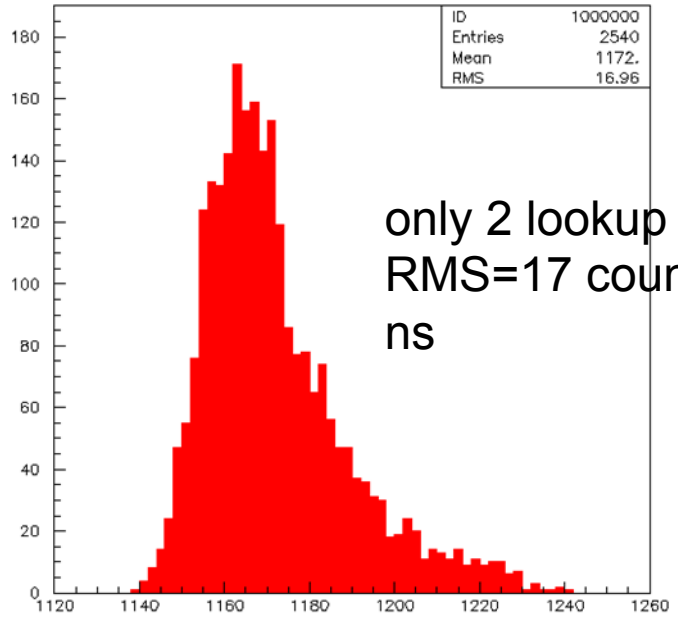
Paolo

Trigger clocked disc have arrived
They have been tested and found working. Integration with DC electronics already occurred.





First measurements with chamber prototype at LNF



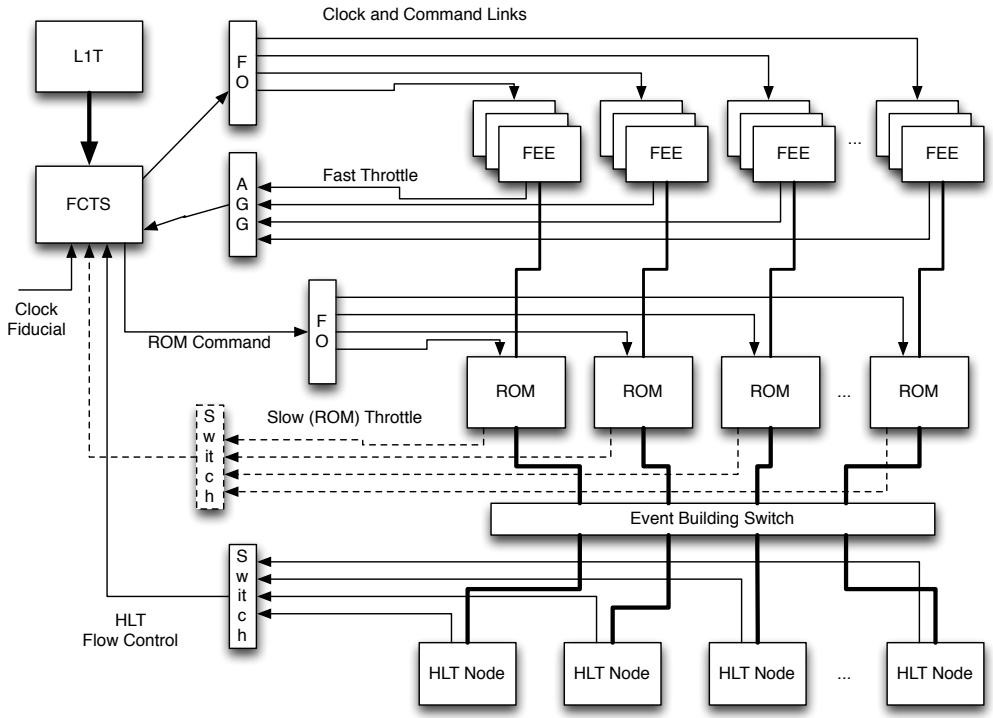
only 2 lookup tables fired
RMS=17 counts i.e. 27 ns

Trigger: Situation in the CsI (tl doped)

We have received and tested all the Sipm electronics we have developped 32 channels
We have now a setup LYSO based (1 crystal)
We need now a test matrix to play with ask Bill about it.
Unfortunately a MOU is needed.

Event Data Chain Implementation

- Proposed implementation:
  - Push architecture
    - Minimum demands on ROM "intelligence"
  - FCTS determines flow control and event routing
  - Timestamp / MDI
- Discussion of error detection, handling and recovery
- Question about total event size
  - Don't want it to grow beyond 200kB! At least for permanent logging



Steffen

TDR Planning

Steffen / All

- ETD/Online Outline (official name: ETD/ONLINE)
  - ETD/Online introductory paragraph in the main introduction chapter.
  - Then 2 dedicated chapters:
    - ETD/Online (with 3 major sections)
      - Requirements and design philosophy
      - Event data chain: Trigger, DAQ, Event Builder, HLT and data logging
      - Support services (ECS, DCS, monitoring, run control, etc.)
    - Electronics
      - description of the hardware implementation of electronics.
- Draft by Elba meeting
- Review names and assignments
  - Who is on board and who is not?
- Conveners will send out "instructions"
- Hope to have first draft (collection of contributions in ~ 1 month from now)

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