SVT-Status

3rd SuperB Collaboration Meeting
Frascati, March 21- 2012

> ➤ Summary from SVT parallel sessions
>
> ➤ TDR status

Giuliana Rizzo
Universita' & INFN Pisa

SVT Parallel sessions

Wednesday Mar 21, 9-11	
Introduction	G. Rizzo (PI)
Analog FE for inner layer strips and next pixel submission in Pavia	L. Ratti (PV)
Analog FE for outer layer strips in Milano	L. Bombelli (MI)
FE chip simulation and next pixel submission in Bologna	F. Giorgi (BO)

Wednesday Mar 21, 11:30-13:30	
Next pixel submission activities in Pisa	F. Morsani (PI)
First INMAPS lab tests and beamtest results for analog maps	S. Bettarini (PI)
Update on sensor and fanout design in Trieste	I. Rashevskaya (TS)
Update on activities in UK	A. Bevan (QMUL)

Wednesday Mar 21, 15:00-16:30	
Activities in Valencia	A. Oyanguren (IFIC)
Update on activities in Strasbourg	I. Ripp-Baudot (IN2P3)
Fastsim performance studies	N. Neri (MI)
Discussions on performance studies and SVT SW development	All

Wednesday Mar 21, 17:00-18:30	
Update on background simulation	R. Cenci (Maryland)
SVT Mechanics	F. Bosi (PI)
Update on HDI design and peripheral electronics	M. Citterio (MI)
Discussion on TDR writing	All

SVT – Background Update

R. Cenci - Maryland

- Many tests done to understand the high SVT rates from Dec. 2011 production

- Total rates (several sources included) were too high for SVT (not only in Layer0)
  - Pairs increased a lot w.r.t May 2011: in L0-1-2 +40-20% x2.5-x4 in L3-4-5!!!!
  - Some reasons understood and fixed, but pairs rates still higher than before +20% in inner layers +80% in outer layers (different material in the I.R. is important for external layers)
  - Touscheck is as high as pair in L1-5. Rad Bhabha not negligible in L3-L5

- Some sources still to be included (beam gas almost ready) and new shielding configuration need to be studied

x5 safety included

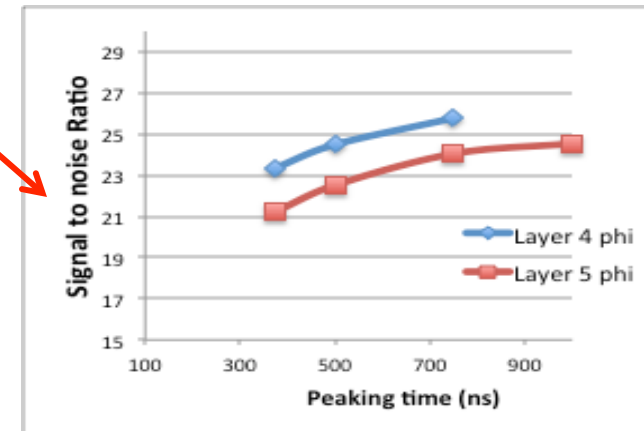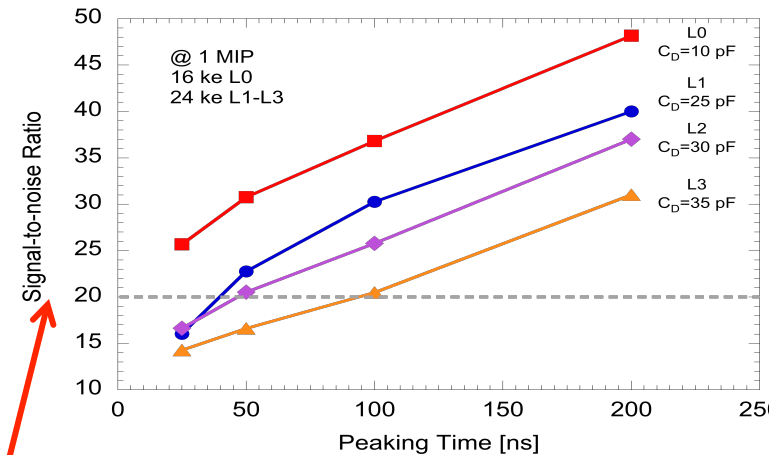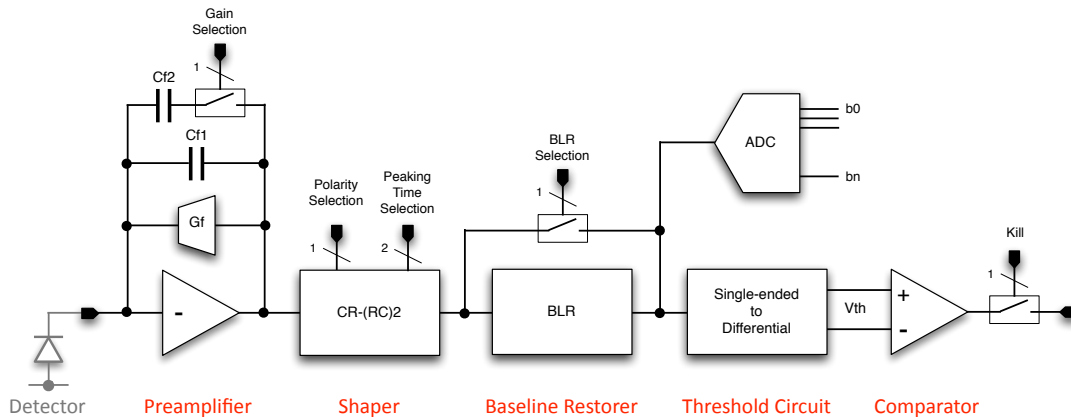| Layers	lato	readout pitch	Strip rate kHz	Ratio pairs / total	Ratio rad bhabha / total	Ratio touscheck LER/ total	Ratio touscheck HER/ total
0	1	50	1.21E+03	0.90	0.03	0.06	0.02
0	2	50	1.21E+03	0.82	0.04	0.11	0.04
1	phi	50	7.24E+02	0.58	0.04	0.30	0.07
1	z	100	4.73E+02	0.39	0.04	0.45	0.12
2	phi	55	5.25E+02	0.48	0.05	0.38	0.08
2	z	100	4.54E+02	0.31	0.05	0.52	0.12
3	phi	100	4.19E+02	0.33	0.11	0.47	0.08
3	z	110	2.70E+02	0.23	0.10	0.56	0.11
4	phi	100	9.00E+01	0.35	0.23	0.34	0.08
4	z	210	4.70E+01	0.36	0.20	0.35	0.09
5	phi	100	5.44E+01	0.39	0.21	0.32	0.08
5	z	210	3.08E+01	0.37	0.19	0.35	0.09

Joint Background Workshop with BelleII in Feb. very useful:

- Discrepancy with BelleII pairs estimate has been solved and our result is still valid.
  - The factor 15 was due to some "problems" in the initial BelleII value and to some misinterpretation of our results by Belle colleagues. The hit rates expected in Layer0 for both experiments is consistent. SuperB estimate also agrees with measurement performed with SVD Belle data.

Strip FE chip development (I)

➤ Need to develop 2 new chips since existent chips do not match all the requirements : analog info, high rates in inner Layers (2 MHz/strip in L0) & short shaping time (25-100ns), long shaping time (0.5-1 us) in Layers 4-5

Block diagram: Detector — Preamplifier (Cf2, Cf1, Gf, Gain Selection) — Shaper (CR-(RC)2, Polarity Selection, Peaking Time Selection) — Baseline Restorer (BLR, BLR Selection) — Threshold Circuit (Single-ended to Differential, ADC b0...bn) — Comparator (Vth, +/-, Kill)

@ 1 MIP
16 ke L0
24 ke L1-L3

L0 C_D=10 pF
L1 C_D=25 pF
L2 C_D=30 pF
L3 C_D=35 pF

Signal-to-noise Ratio vs Peaking Time [ns]

Signal to noise Ratio vs Peaking time (ns) — Layer 4 phi, Layer 5 phi

➤ Performance for analog FE channel simulated (PV/BG fast channels for Layer0-3 & MI slower channels for Layers4-5)

➤ Shaping time reduction under evaluation to mitigate background impact. Shorter shaping time gives:
  → lower inefficiency due to analog dead time
  → better hit time resolution and lower occupancy

→ Selectable shaping time will be implemented

Strip FE chip development (II)

- Readout architecture simulated VHDL (BO/PI) :
  - Evolution of our readout architecture for pixels
  - Hits stored with their timestamp (TS) and pulse height (TOT) inside in-strip buffers. Only triggered TS hits are readout by peripheral logic and sent to output bus.
- 100% digital efficiency even for high Layer0 striplet rates (2 MHz/strip)

F. Giorgi (BO)

2 MHz/strip : Layer 0			
buffer size	16	32	64
buffered hits	3.8 M	12.9 M	12.9 M
of which triggered	23363	76850	23363
output triggered hits	14679	76849	23363
triggered hit lost	8684	1	0
Efficiency (%)	62.8	99.9987	100
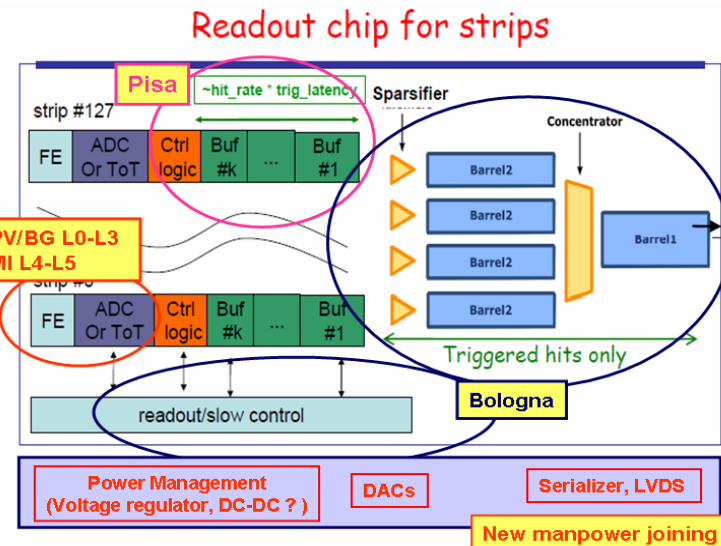
- FE chip work completed for TDR
- Next step: prepare first FE chip submission with IBM 130 nm - Nov. 2012

I. Rashevskaya (TS)

- Sensor and fanout geometry defined.
- First detailed table with sensors & fanouts parameters supplied by TS to FE chip designers for noise evaluation. Will be udpated after some measurements.

| Layer	Sens ors ide	Rea dout pitch	# of barrel sensor s in rea	# of sens or s in	Barrel sensor length	Barrel module strip length	Total modul e strip length	Total strip volume	C/L	Rs/L	Poly-silicon R_bias	n-equiv. fluence Φ	Radiation induced current / volume	Max Fanout C	Max Fano ut Rs	Total C	Total Rs	Total R_bias	Total leakage current	Voltage drop on R_bias	Shaping time	ENC from Rs	ENC from R_bias	ENC from I_leak	ENC from Rs + Rbias + I_leak
		(µm)			(cm)	(cm)	(cm)	(cm^3)	(pF/cm)	(ohm/c)	(Mohm)	(cm^2)	(nA/cm^3)	(pF)	(ohm)	(pF)	(ohm)	(Moh)	(nA)	(mV)	(ns)	(e)	(e)	(e)	(e)
1	n	50	1	1	11.17	11.03	11.03	1.65E-03	2.50	8.6	4	1.0E+11	2.0E+04	4.5	13	23.3	107.9	4.0	35.3	141	100	589	122	202	635
2	n	55	2	2	6.64	13.00	13.00	2.15E-03	2.50	6.7	8	4.5E+10	9.0E+03	3.5	11	25.6	98.1	4.0	21.9	88	100	619	122	159	651
3	p	100	2	2	9.64	19.00	19.00	5.70E-03	1.70	4	8	9.0E+09	1.8E+03	2.5	7.5	34.8	83.5	4.0	14.1	56	200	549	173	180	603
4a	p	100	2	3	11.46	22.64	29.30	8.79E-03	1.70	4	8	7.5E+08	1.5E+02	1.1	3.2	50.9	120.4	2.7	7.2	19	500	610	334	203	724
4b	p	100	2	3	11.98	23.68	30.34	9.10E-03	1.70	4	8	7.5E+08	1.5E+02	1.1	3.2	52.7	124.5	2.7	7.4	20	500	642	334	207	753
5a	p	100	3	4	10.22	30.24	36.90	1.11E-02	1.70	4	10	3.5E+08	7.0E+01	1.1	3.2	63.8	150.8	2.5	8.2	20	800	676	437	274	851
5b	p	100	3	4	10.60	31.38	38.04	1.14E-02	1.70	4	10	3.5E+08	7.0E+01	1.1	3.2	65.8	155.3	2.5	8.4	21	800	707	437	278	877
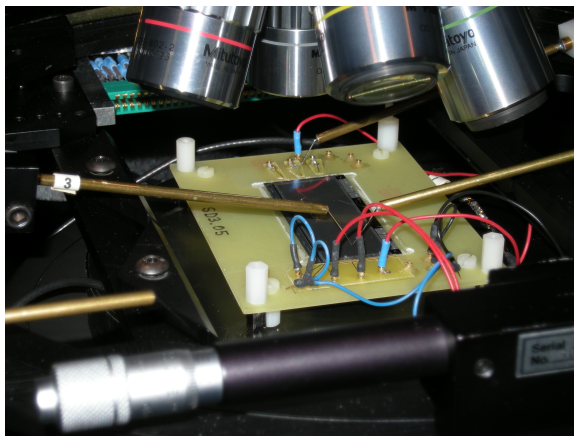
- Very detailed work to assemble and measure sensors capacitance in different bonding configuration (ganging vs pairing). Measurements on fanout prototypes (now in production at CERN) also foreseen.

STRIP PAIRING		NO	X2		X3		X4	
C _First	pF/cm	0.99	1.40	41%	1.51	52%	1.58	59%
neighbouring strips	pF/cm		1.48	5.4%	1.60	6.0%	1.66	5.2%
C _ P side	pF/cm	1.28	1.59	24%	1.67	30%	1.76	37%
	pF/cm		1.66	4.1%	1.78	6.3%	1.84	4.8%
C Total P+N side	pF/cm	1.62	2.25	39%	2.70	66%	3.11	92%
	pF/cm		2.36	4.9%	2.84	5.3%	3.24	4.1%

Hit time resolution and analog efficiency study

L. Ratti (PV) - L. Bombelli (MI)

➢ Detailed MC simulation, with present FE chip configuration, to evaluate:
1. analog efficiency using info on energy deposited per strip (from Bruno)
2. hit time resolution → time window cut for reconstruction → minimal offline occupancy
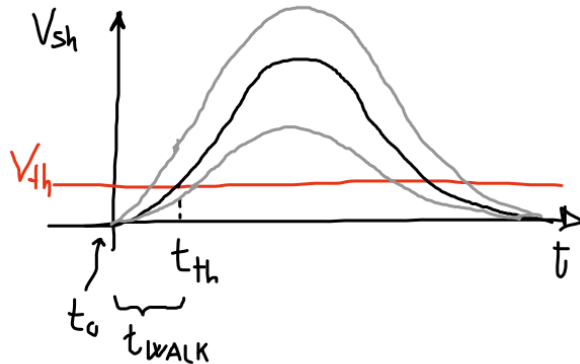
2. The time of arrival of a particle t_0 estimated from the hit crossing time t_{th} and the time walk. t_{walk}
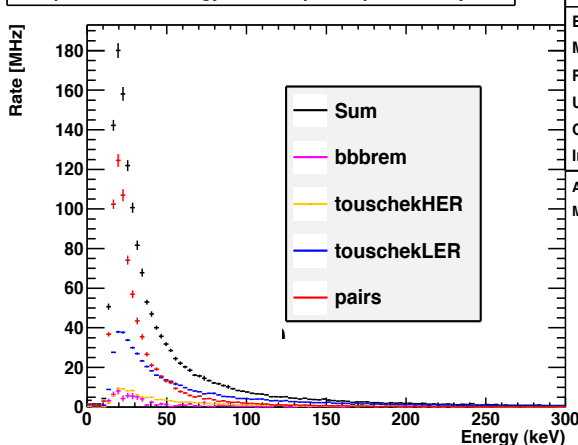
$$\sigma_0 = \sigma_{th} \oplus \sigma_{walk}$$

depends on time stamping

can be estimated with amplitude measurement

1. Hits arriving when the channel is already above threshold are not seen; this analog dead time depends on pulse height and affect the efficiency (x5 safety on back. rates included)

Strip Phi rate vs energy released per strip on Svt Layer 1

Layer	side	Analog Efficiency (x5 bkg, nominal shaping time
0	1	0.95
0	2	0.95
1	phi	0.89
1	z	0.90
2	phi	0.92
2	z	0.90
3	phi	0.78
3	z	0.89
4	phi	0.92
4	z	0.90
5	phi	0.94
5	z	0.93

Layer	t_p [ns]	$t_p / T_{CK,TOT}$	$f_{CK,TS}$ [MHz]	σ_{walk} [ns]	σ_{t0} [ns]
0	25	3	30	2.1	9.8
1	100	3	30	8.3	12.7
2	100	3	30	8.3	12.7
3	200	3	30	16.7	19.2
4	500	3	30	41.7	42.8
5	1000	3	30	83.3	83.9

Important inputs for performance studies

2012

Update on Fastsim performance studies

N. Neri (MI)

Fastim used to evaluate some effects of high background on SVT performance:

➢ low hit efficiency due to analog dead time ~ 90 % in some layers

▸ resolution worsening due to high offline occupancy

  ▸ hit merging and pat rec confusion algorithms add bkg hits to the track

  ▸ offline occupancy achievable with tight cut on hit time

  ▸ ~4-6% in L0-L3 and ~2.5% in L4-5 (x5-x10 w.r.t. BaBar!)

▸ Many tests done to check initial discrepancy in background estimates using fullsim vs. fastsim (thanks to M.Rama and A. Perez fro their help)

  ▸ Partly solved, difference anyway expected for the different details implemented.

▸ Several validation tests performed by Nicola to use fastsim tools for SVT studies.

▸ Effects on track parameters and vertex resolution studied

▸ Machinery now in place and first exercise done BUT need to plug in "final" background numbers to evaluate the effect on performance.

▸ Performance with striplets and pixels will be evaluated

▸ High occupancy can also affect reconstruction but fastsim cannot be used to evaluate this effect.

▸ Discussion started but need more manpower on SW to face this issue!

Preliminary results – background need to be updated !

Time-dependent analysis results for $B^0 \to \phi K_S^0$

- ■ hit efficiency corrected: 97% (PairBkg), 95% (Pair Bkg 5x)
- ● hit efficiency 99%
- ▲ hit efficiency 99% and no bkg on L0

Preliminary

S per event error

2% variation

5% variation

BaBar

NoBkg   PairBkg   PairBkg 5x

R&D on pixel for Layer0 in Italy (PV/BG/BO/PI)

WB/BB pad

TSV

Inter-tier bond pads

2nd wafer

1st wafer
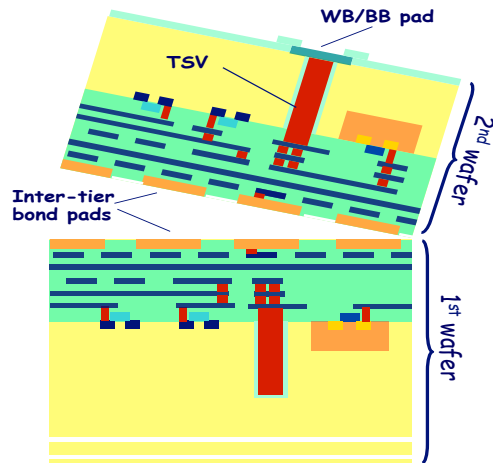
Next submission with Vertical Integation technology (2 CMOS layers interconnected):
- APSEL_VI: DNW MAPS matrix 128x96
- Superpix1: FE chip for hybrid pixel 32x128

Latest readout architecture implemented
- Sparsification in-pixel, Fast timestamp 100 ns
- Data push & triggered
- Target Layer0 with 100 MHz/cm2 hit rate

Layout in the final stage…

Design activity carried out by Luigi Gaioni, Gianluca Traversi (Bergamo) Filippo Giorgi, Alessandro Gabrielli (Bologna), Alessia Manazza (Pavia) and Fabio Morsani (Pisa)

Pixel cell layout

top   Inter-tier bond pad   top

dx   dx

sx   sx

AVDD ITBP   AGND ITBP   PIXEL HIT ITBP
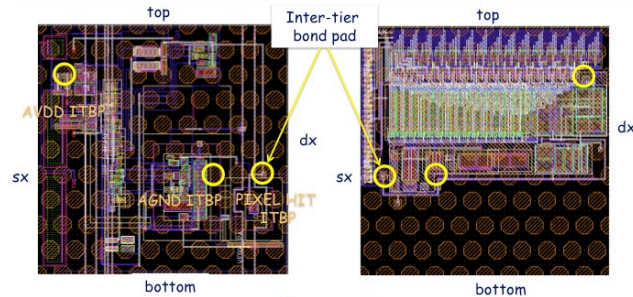
bottom   bottom

ANALOG LAYER   DIGITAL LAY

L. Ratti, "Update on microstrip front-end and Layer0 pixel upgrade", III SuperB Collaboration Meeting

Matrix bottom-left corner, analog part not shown

Signals routing to readout: DEAD AREA

DRIVERS   DELAYS

21/03/2012   Fabio Morsani - INFN Pisa   16
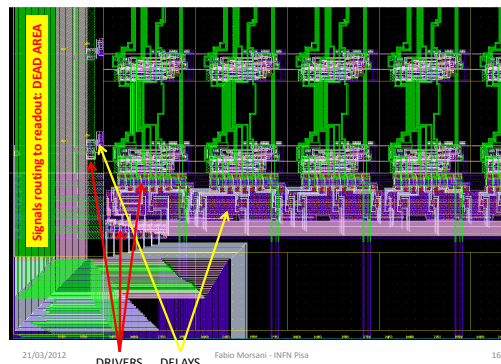
3D–IC submissions - *Layout*

- Readout circuits placed and routed
- Post layout circuit (clock-trees, pads) simulated (some problems with std-cell timing library)
- Static Timing analysis converging (Encounter)
- PADS disposition almost defined.
- Definitive routing when all custom blocks are closed.

APSEL_VI

matrix
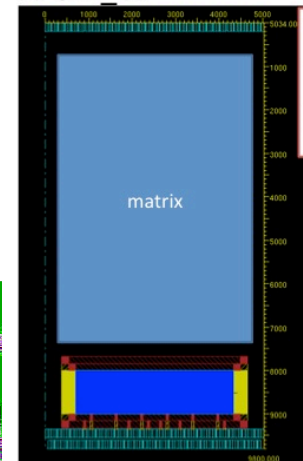
5034 um x **9800** um die area

70 k Std-Cell readout

Readout power estimate
min 100 mW (1.08 V, +125C) →slow
max 200 mW (1.65, -40C) →fast

2 rows of staggered pads
← 146 um pitch
130 um pitch →

SuperPix1

3255 um x **9421** um die area

40k Std-Cell readout

Readout power estimate
min 70 mW (1.08 V, +125C) → slow
max 140 mW (1.65, -40C) →fast

G. Rizzo   - 2012   9
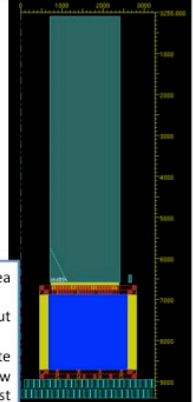
…but they haven't lost their sense of humor!

Pixel, you provoked me …

From behavioral (mental) model to the smallest and fastest cmos in-pixel circuit

Design activity carried out by Luigi Gaioni, Gianluca Traversi (Bergamo) Filippo Giorgi, Alessandro Gabrielli (Bologna), Alessia Manazza (Pavia) and Fabio Morsani (Pisa)

No crosstalk!
Scalability!
Faster! Smaller!
Less power!
Yield!
Less metals for routing!
Minimal dead area!

"Pasta, you provoked me and I'll destroy you now, pasta! I'm going to eat you, ahmm!"

Submission in July?

SuperB

First INMAPS lab tests & beamtest results for 3D analog maps

S. Bettarini - PI

INMAPS 32x32 matrix
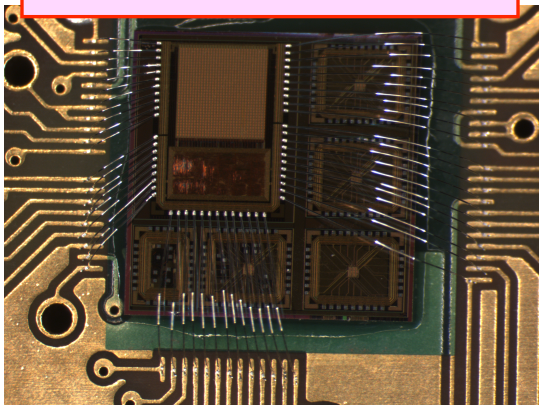
- INMAPS CMOS process with quadruple well & high resistivity substrate to improve charge collection efficiency and radiation resistance

- Latest readout architecture implemented (specs for Layer0)

- ENC ~ 30 e-.

- Readout is working.

- Need to investigate detailed features and possible source of

Gain calibration: Fe^{55} source
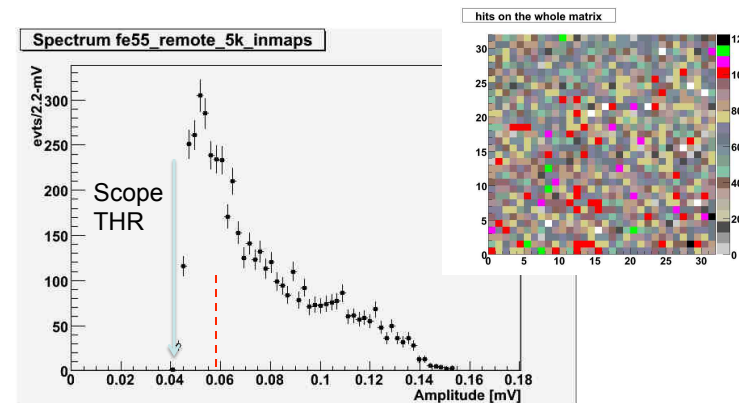
3D MAPS, sensor+analog layer test structures

- Promising test beam preliminary results on VI 3x3 matrix:
  - Efficiency greater than 98% for THR < 8 σ
  - Q cluster collected ~ 1000 e-

digital

Digital layer

Analog layer
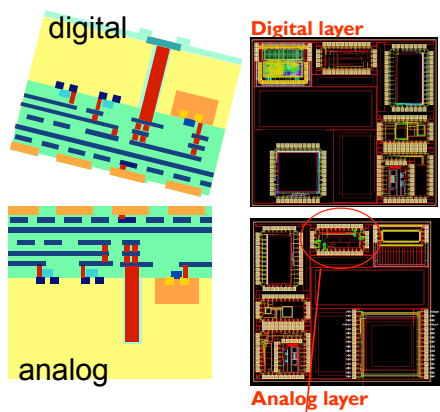
g

Rizzo

Chip1 m1: results (in e- or S/<N>)

landau (x) gauss convolution

NOISE

MPV=53.5 +-1.5 sigma=11.4 +-0.9

Qcluster [mV]
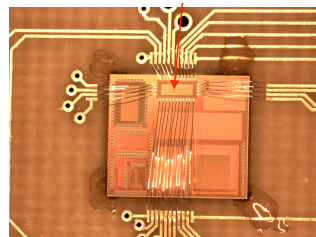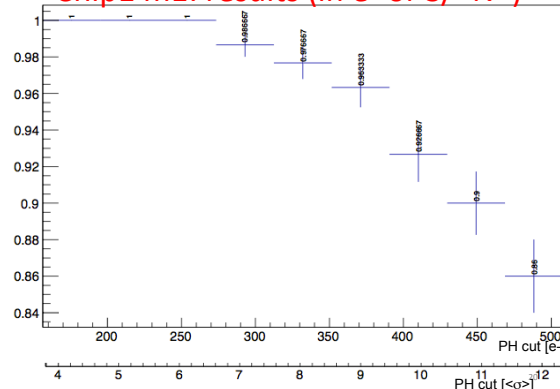
Frascati, March 22 - 2012
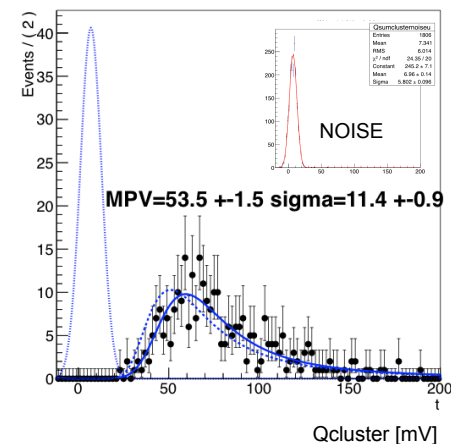
Update on MAPS activities in UK

A. Bevan (QMUL)

Queen Mary
University of London
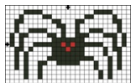
Arachnid Collaboration

- CMOS MAPS R&D programme
  - Continuation of the SPiDeR programme
  - Birmingham, Bristol, Daresbury, DESY, QMUL, RAL
  - Targeting SuperB and ALICE projects as well as generic MAPS development.

- Characterization of several MAPS chips (produced with INAMPS process for other applications) will give important information on the technology.

- The design of a MAPS chip with SuperB specs can be done during this R&D project.

- The team now fully in place

Queen Mary
University of London

SuperB
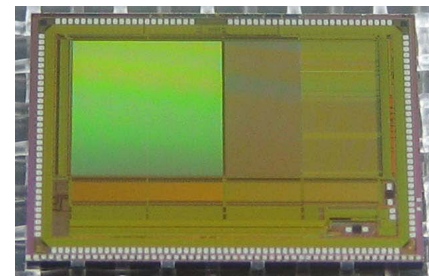
Beam Tests

- Planned proton (CERN) and photon (RAL) irradiation programmes during 2012, will start as soon as we have full functionality to test chips in firmware.
  - 3 splits for the Cherwell chips, on standard and hi-res substrates.

- Also plan to perform TPAC irradiation to compare 3T vs. 4T radiation hardness.

- Later in 2012: include electron test beam (DESY) in the programme.
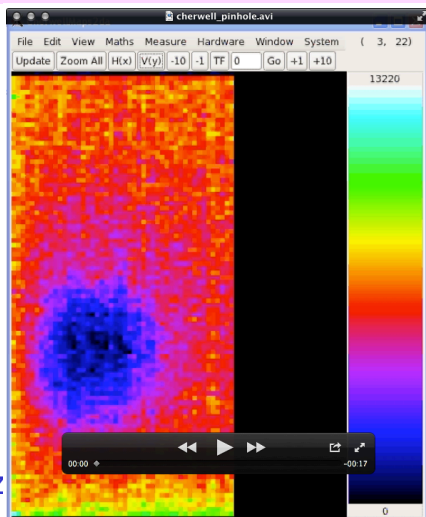
I. Ripp–Baudot
(IPHC Strasbourg)

Strasbourg shown a detailed & interesting plan of CMOS MAPS submissions to reach specs for ALICE pixel upgrade with good synergy with SuperB Layer0 specs.

Starting point:

- MIMOSA-28 chip: 0. 35 um process, rolling shutter design →100 us timestamp, Power ~ 200 mW/cm2.

Final goal:

- AROM chip (Accelerated ROlling-Shutter Mimosa chip) 0.18 um process, in-pixel discriminator + optimized rolling shutter

    → 1.5 us timestamp, Power ~ 1W /cm2.

Update on HDI design and peripheral electronics

M. Citterio(MI)

Example of a read-out section

UPILEX+Cu (?)

Front-end chips

Optical 1 Gbit/s

Optical Link
2.5 Gbit/s to ROM

C

FEB

Detector

Copper bus

Serdes
or FPGA

fibers

HDIs   < 1 m

Transition card

LV1

High rad area 15Mrad/year

ON detector
low rad area

Counting room
Std electronics
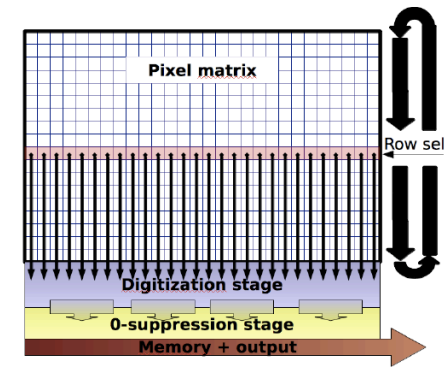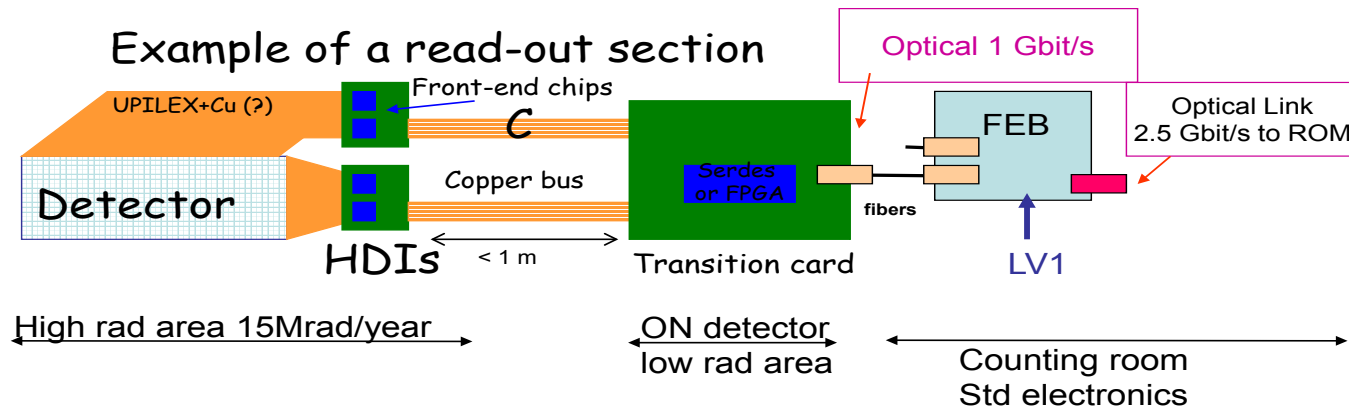
Progress on the definition of the ON detector ing chain

Still some options open and not all the details defined.

Choices are a compromize among:

- data rates, number of lines & where to put seriali
- critical for HDI, connectors, copper bus, ards
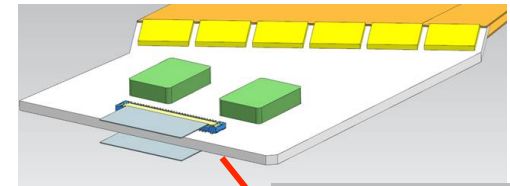
1. The world's smallest size* (width: 2.5 mm, Terminal pitch: 0.35 mm and Mated height: 0.8 mm) The footprint when mated is down approx. 10% from our existing A4S model (60 contacts), contributing to the functionality enhancement and size reduction of target equipment.

Suction face 0.8mm

Socket

Width of Output Bus is determined by geometrical reasons:
- **Dimension of Transition Card**
- **Routing of Bus through available openings (an example is shown on bottom)**

1. The world's smallest size* (width: 2.5 mm, Terminal pitch: 0.35 mm and Mated height: 0.8 mm) The footprint when mated is down approx. 10% from our existing A4S model (60 contacts), contributing to the functionality enhancement and size reduction of target equipment.

8 mm

Suction face 0.8mm

12.85 min (60 contacts)
A4S 14.50 mm (60 contacts)

2.5mm

Socket

Clips (soldering terminals) at the four corners

SVT Mechanics

F. Bosi (PI)

- All the details of the SVT modules in the 3D model of the I.R. (ribs, fanouts ..)

- Good collaboration with QMUL and Milano eng. to complete the design for TDR.

- Progress shown on pixel module support with microchannel cooling.

Space-frame with safe clearance respect to the ribs envelope

Modelling ribs -fanouts for L1-2-3

Long L1-2 end-piece
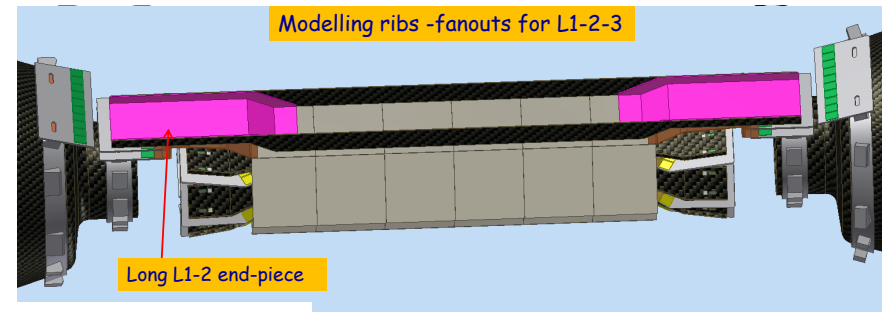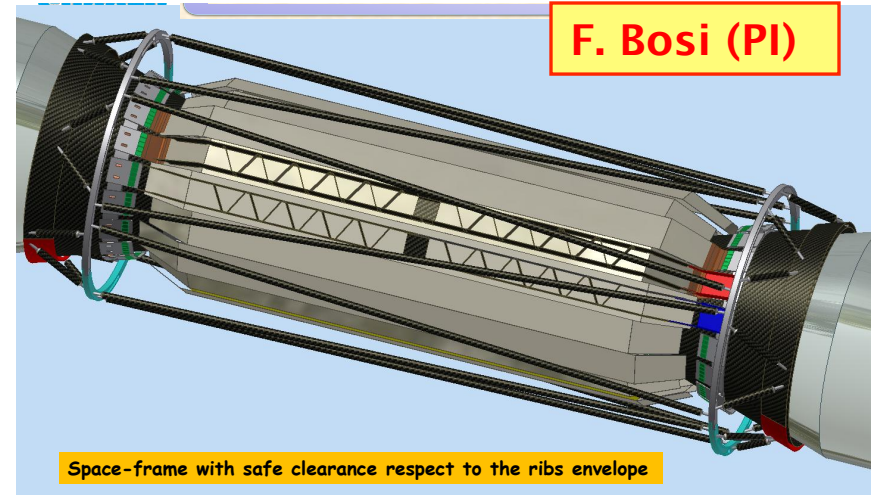
➢ Detailed procedure for quick demounting defined

•Insert a temporary cage to make SVT/Be pipe more rigid then slide criostats, W conical shields, cage + SVT+Be pipe w.r.t W cilindrical shields
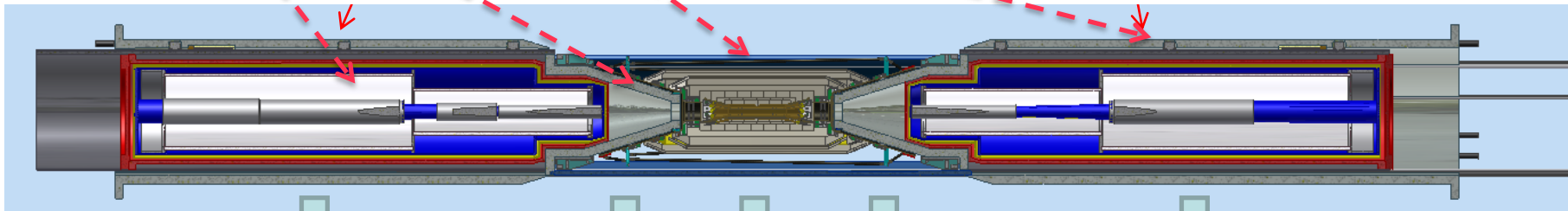
➢ Many details can be refined but now concentrate on TDR writing.

Activities in Valencia

A. Oyanguren (*IFIC - Valencia*)

The IFIC's lab.

80m^2 clean room *class 10000* (ISO7) with 25m^2 *class 1000* (ISO6), 1°C controlled temperature and ±5% humidity:

Two wafer probe stations: 1 manual, the other automatic/programable
Wire-bonders: one fully automatic, one manual and one test bonder
Laser interferometer system, glue dispenser, sensor test cage

→ detector characterization, module assembly, bonding, metrology and electrical QA test

[ATLAS-SCT endcap module testing, assembly and QC]

People (Valencia + U. Barcelona)

Valencia:	U. Barcelona associates:
-Seniors:	
Fernando Martínez-Vidal **(IP)** [Prof.]	Lluís Garrido [Full Prof.]
Arantza Oyanguren [Ten. Track]	Eugeni Graugés [Prof.]
Victoria Castillo [Full Prof.]	
Emilio Higón [Full Prof.]	
Oscar Vives [Prof., theorist co-convener τ group]	
-Engineers:	
José Mazorra de Cos	David Gascón
	Albert Comerma
-PhD students:	
Pablo Ruiz Valls	

➢ Group is proposing to contribute to:
   ➢ FEE Electronics design and simulation
   ➢ Silicon sensor testing

SVT-TDR Status

Activities almost completed in all areas to have a consistent design

- <u>Silicon Sensors</u>: geometry defined and detailed measurements of parameters under way for better noise evaluation.

- <u>Fanouts</u>: Layer1-5 - prototypes in production at CERN :<u> </u>Layer0 - some details still to be defined.

- <u>FE chip development</u>: simulation activities for TDR completed
  - Next step: prepare first FE chip submission with IBM 130 nm - Nov. 2012

- <u>Peripheral Electronics:</u> progress in the design
  - Some work still needed but we can tune the level of details we want to give in the TDR!

- <u>DAQ & FEboard:</u> Electronics load reevaluated with new inputs (new geometry and background rates)

- <u>Performance studies</u>: many progress in the setup of the machinery with fastsim (ready)
  - SVT Performance with nominal & x5 background with striplets & pixel will be evaluated

- <u>Pixel R&D is continuing</u>

- <u>SVT Mechanics:</u> all the components in the 3D model and quick demounting procedure defined. Need to start the TDR writing even if some details need to be refined.

- Complete the TDR work in ~1-2 months and concentrate in TDR writing to have a complete draft by the Elba Meeting.

backup

SVT TDR Writing

~ 20 pages in svn

Cylindrical Shielding 1300 Kg

Cylindrical Shielding 1300 Kg

250 Kg + 150 Kg + 50 Kg
Criostate + External tube + Cables

200 Kg Conical Shielding

50 Kg + 50 Kg SVT + Temporary Cage

200 Kg Conical Shielding

250 Kg + 125 Kg + 50 Kg Criostate + External tube + Cables

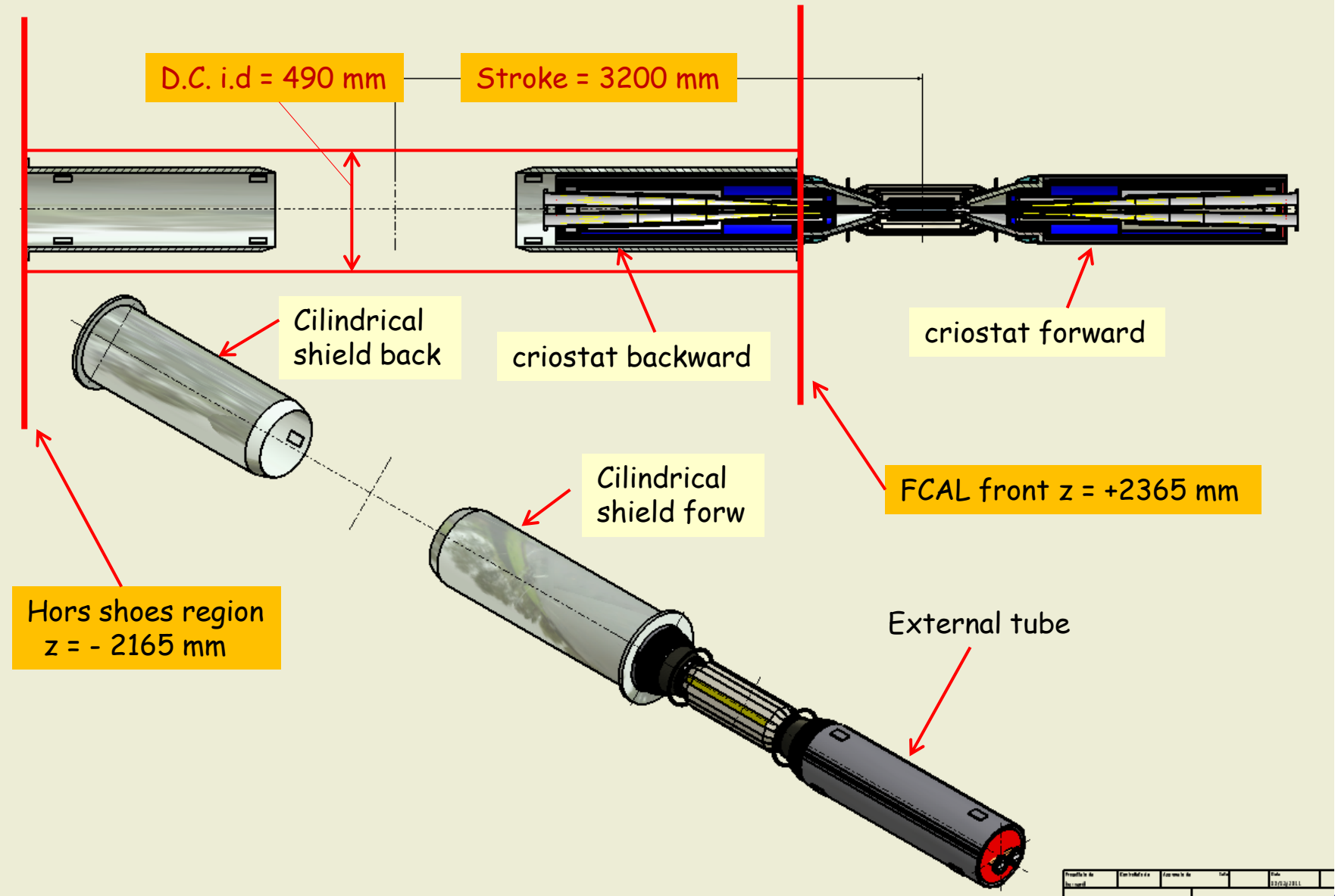Total weight to move for quick demounting ≈ 1400 Kg

Quick demounting
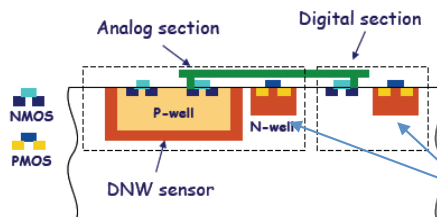

Temporary cage space 14 mm

Cable SVT space 20 mm

402,00

Quick demounting

D.C. i.d = 490 mm

Stroke = 3200 mm

Cilindrical shield back

criostat backward

criostat forward

FCAL front z = +2365 mm

Cilindrical shield forw

Hors shoes region z = - 2165 mm

External tube

Pixel technologies under study

Deep N-well MAPS,
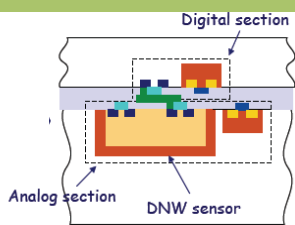- **In-pixel** front-end electronics (pre, shap, discr).
- **competitive N-well** issue

Sensor Matrix
Fast peripheral Readout
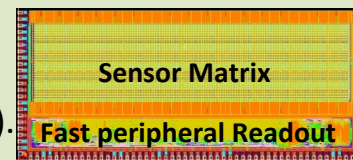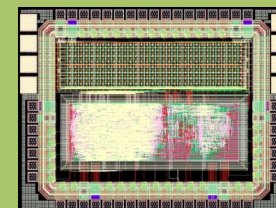
APSEL4D chip ST 0.13 um
Beam test **CERN 2008**.
90% efficiency compatible with deep N-well fill factor

3D MAPS
- **Digital tier: dense pixel digital logic** and peripheral readout
- **In-pixel** analog FE
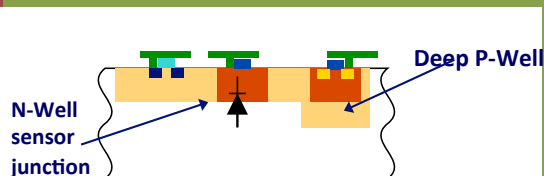- **Less competitive N-well issue**
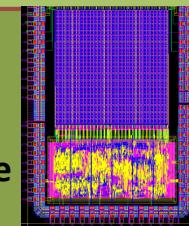
APSEL3D Tezzaron Chartered 32x8 matrix

Ongoing tests

INMAPS technology
- **Deep P-well preventing charge-stealing** by competitive N-wells.
- **High resistivity substrate → more robust against radiation.**
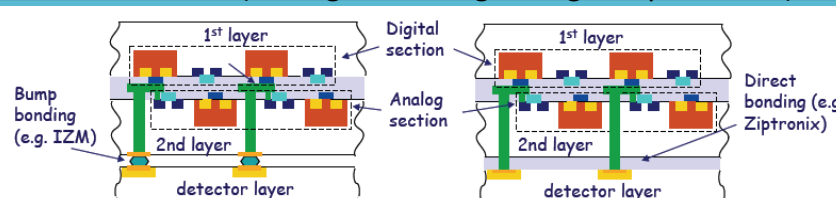
INMAPS 0.18 um 32x32 matrix submitted June 2011

Hybrid Pixels 50x50 um pitch
- High resistivity, **fully depleted sensor**
- **Fast readout** (analog FE and digital logic at pixel level)

SuperPix0 chip
- **Beam Test** Sept. 2011.
- **Preliminary results presented**

FUTURE... 3D front-end chip
- Dedicated **digital tier**
- **analog tier:** FE electronics.
- **Fully depleted detector** Bump Bonded / Directly Bonded