PID Summary

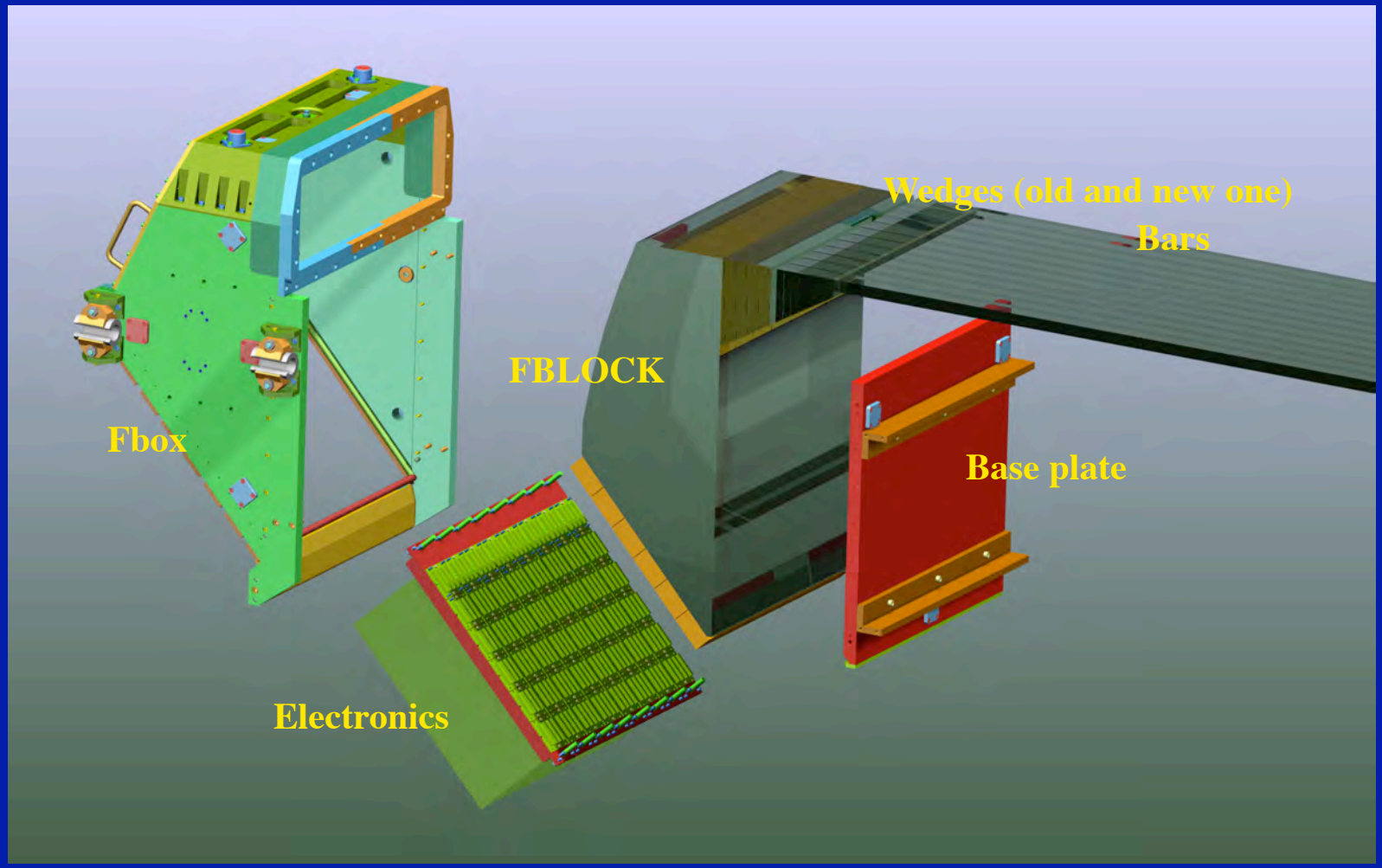
J. Va'vra

SuperB collaboration meeting in Frascatti, March 2012

FDIRC prototype

Photon camera: Definitions of names

(A new beautiful drawing from Massimo)



FBLOCK optics

J. Va'vra

QC of FBLOCK:

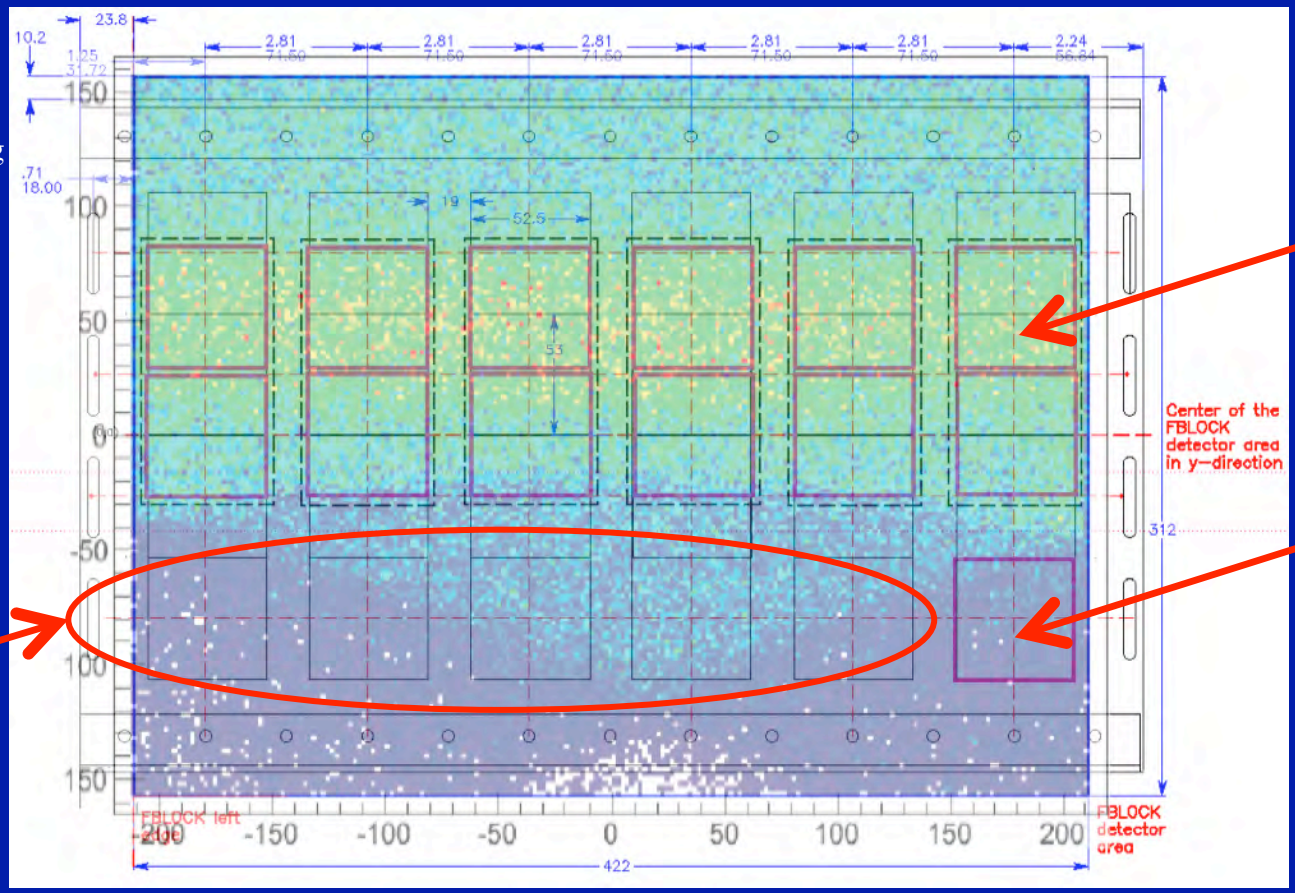
Assembly into Fbox:

- **We found the alignment within tolerances on all critical numbers.**
- **Many issues are not trivial, but we now tend to think that this kind of optics is doable.**

Detector layout with IRS2 digitizer

J.Va'vra with input from D. Roberts & M. Andrew & G. Varner

Overlay a G-10 detector holder drawing with Doug's MC display drawing



SLAC amplifier + IRS2 double-package handles two H-8500 tubes

H-8500 tube for analog monitoring

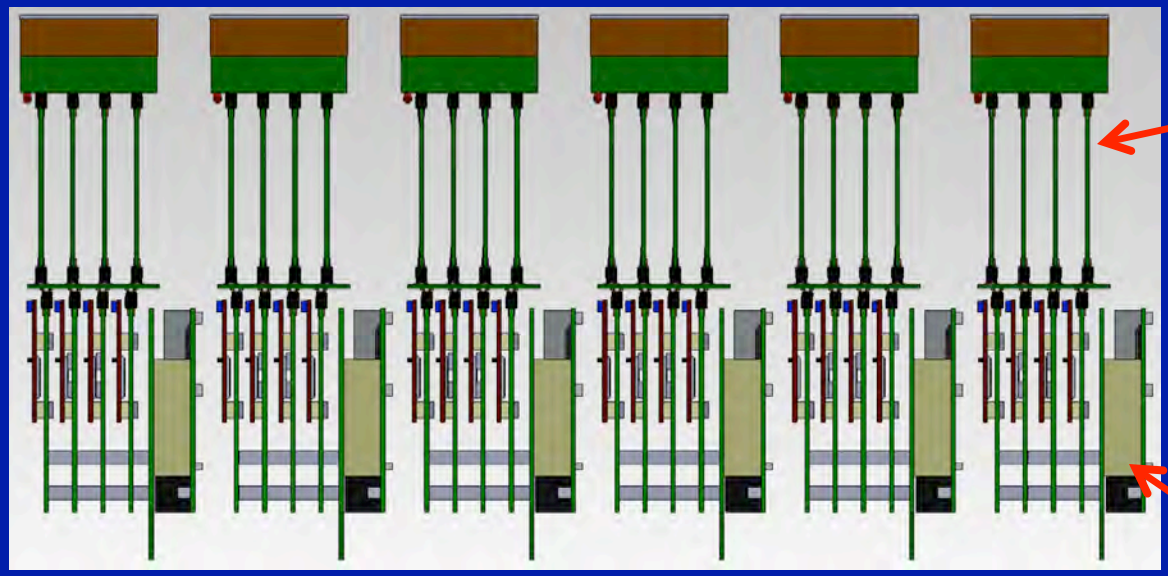
Available for tests of final electronics or other tubes

- **12 H-8500 tubes will be read out by SLAC + Hawaii electronics.**
- **One tube is allocated for analog monitoring.**
- **5 slots available for tests of final electronics or other tubes.**

SLAC amplifier + Hawaii IRS2 digitizer

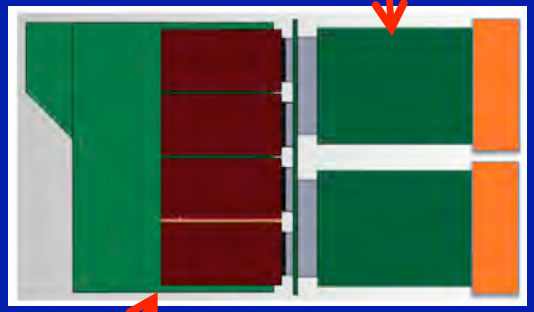
M. Andrew, J. Va'vra

Top view:



SLAC amplifier

Side view:



H-8500

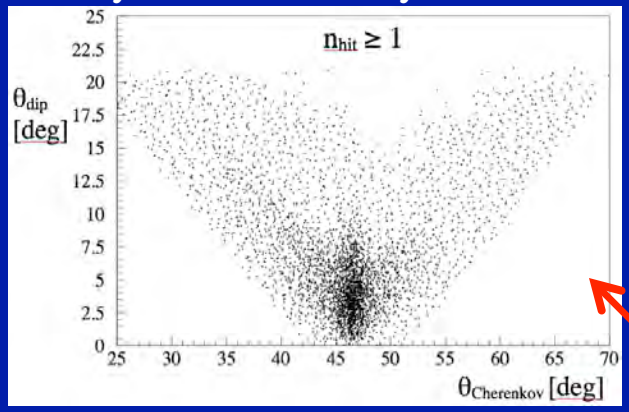
IRS2 electronics

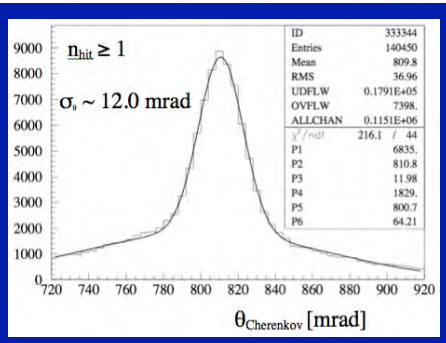
- **12 H-8500 tubes.**
- **Benefit of this electronics: will have time & pulse height on every pixel.**

Analysis of the 1st FDIRC prototype

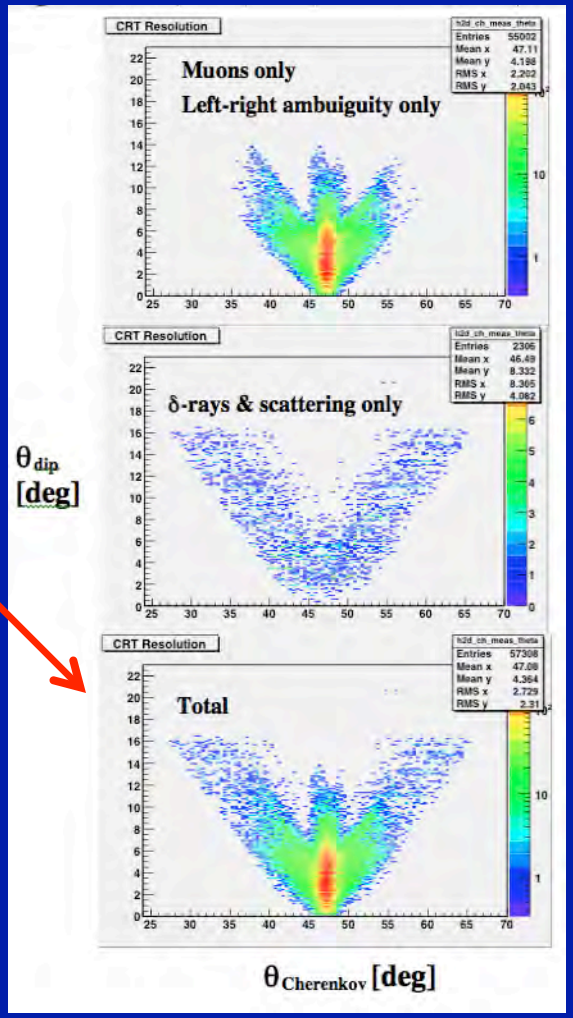
B. Bay, D. Shtol, J. Va'vra

Jerry: CRT data analysis





B. Day: CRT MC simulation

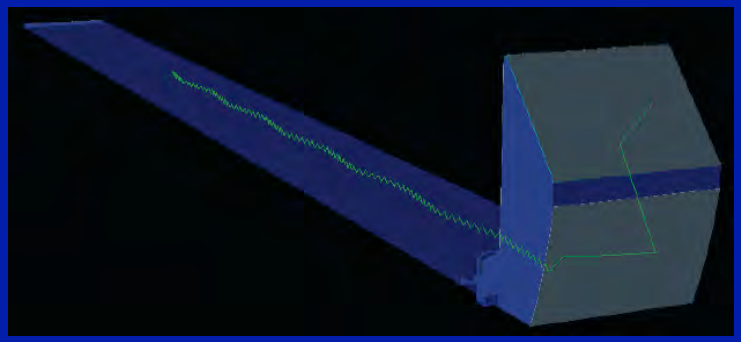


- **The Cherenkov angle distribution has tails.**
- **In the 1st FDIRC prototype we have only two ambiguities (there is no wedge), and that at is enough to create tails.**
- **The final FDIRC will have many more ambiguities, so we should study this topic carefully !!**

FDIRC reconstruction for FDIRC prototype

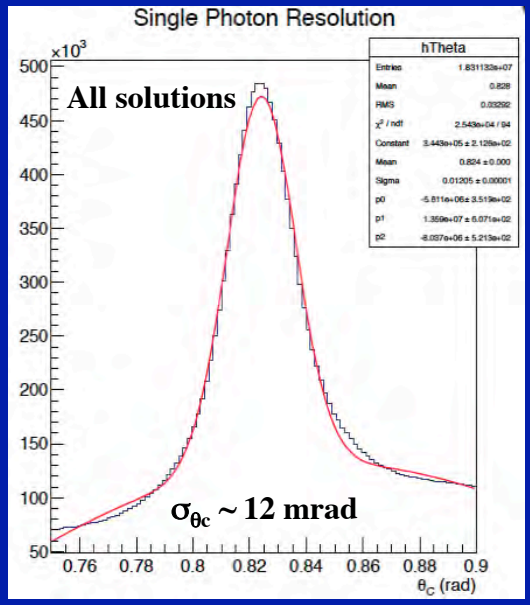
Doug Roberts

FDIRC prototype model:



(Multiple paths to a given pixel -> leading to different solutions)

Cherenkov angle resolution:



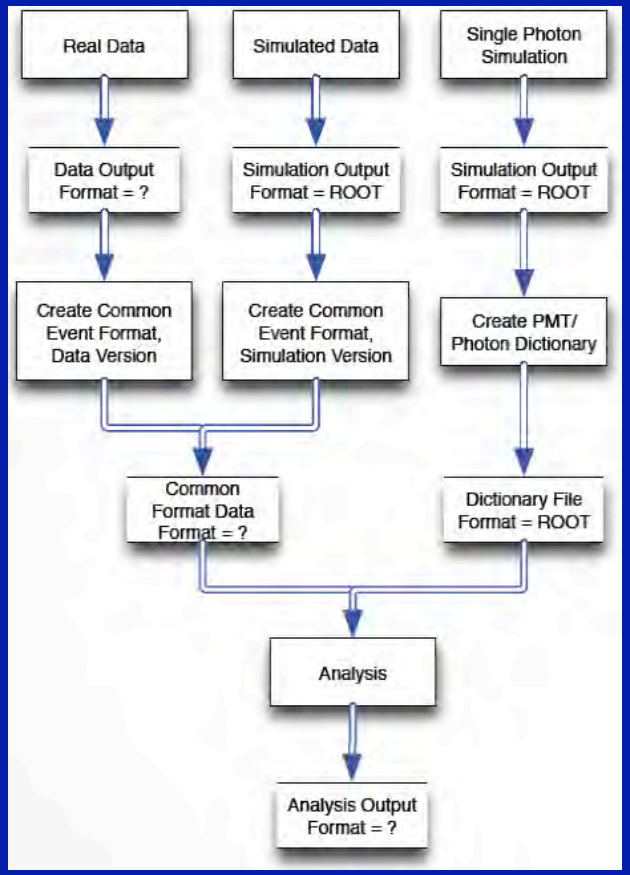
(~16 solutions/photon)

- **Detailed geometry of FDIRC prototype installed in MC simulation program.**
- **Generate photon k_x, k_y assignments for each pixel.**
- **More complicated than the 1-st prototype because of wedges and FBLOCK sides.**
- **Present methodology is considering all solutions with "equal" weight.**
- **Studying various methods how to (a) reduce number of solutions or (b) to weigh them.**

FDIRC analysis chain

Doug Roberts

FDIRC analysis chain:

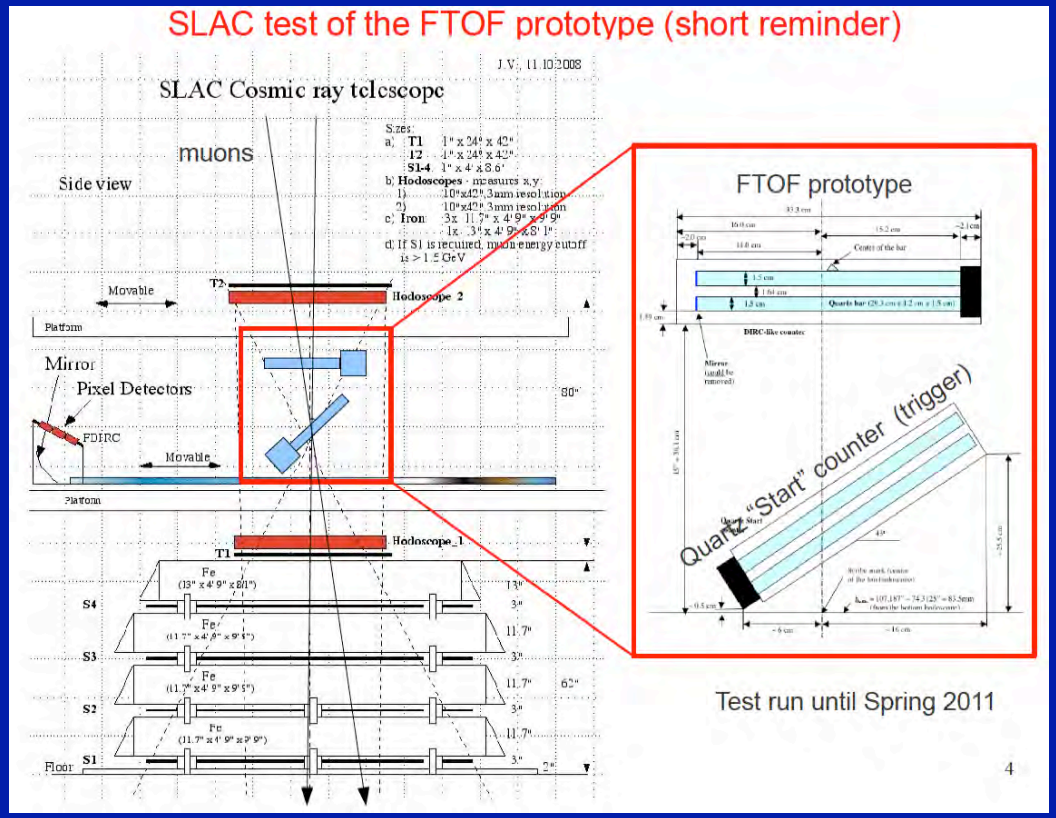


- **Until now we had separate programs for MC, data analysis, pixel assignments.**
- **Dough is trying to unify this effort so one can run the data stream and MC stream through the same analysis path.**

What FDIRC can use from FTOF CRT run ?

Leonid Burmistrov

FTOF test in CRT at SLAC:



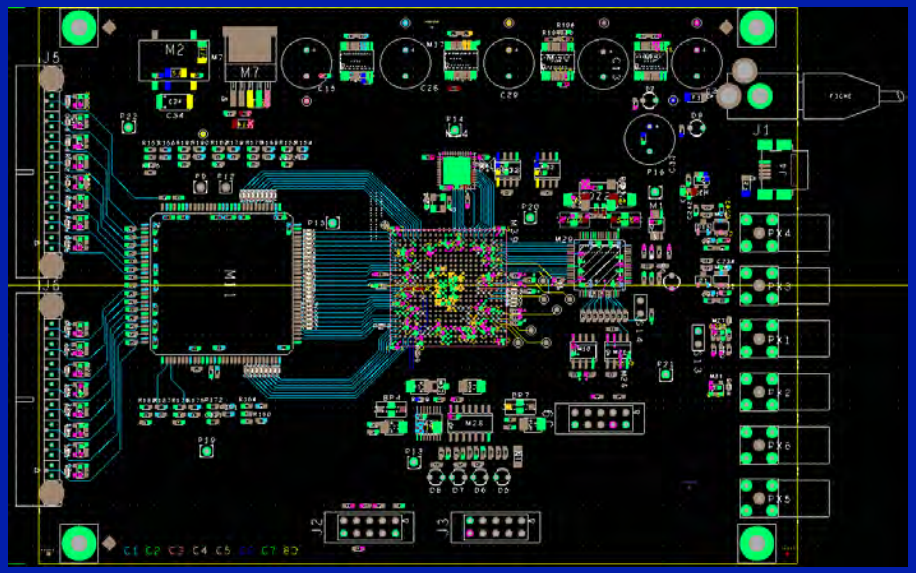
- **Many programs created, which could contribute to FDIRC analysis.**
- **One of the most useful program to be used in the next FDIRC run is automatic monitoring status every 1000 events, which was sent to several e-mail addresses to alert people for possible hardware problems.**

FDIRC at SuperB

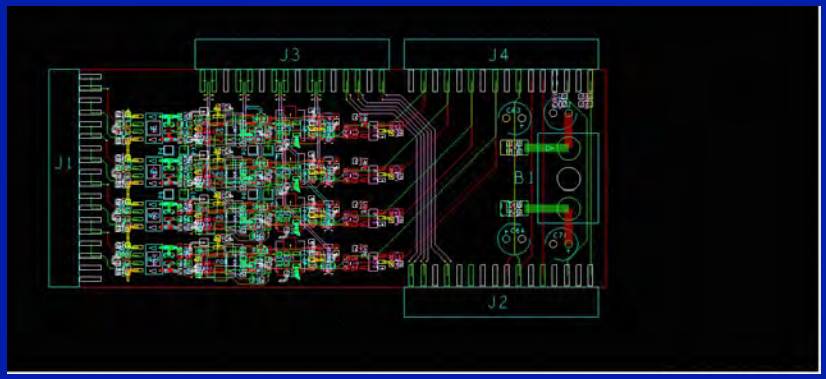
FDIRC electronics

Ch. Beigbeder

SCAT test board current status:



Analog board for testing front end:

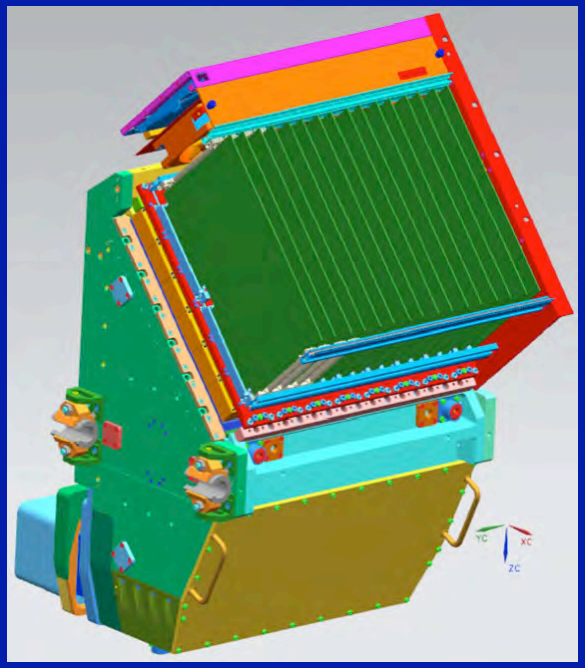


- **10 SCAT chips delivered. SCAT test board is being designed.**
- **Analog test board delivered. Tests of analog board in progress.**
- **The aim is to end up with 2 and half H-8500 tubes instrumented. Test them in the Bari's scanning setup first, and later on install them in FDIRC prototype in CRT.**

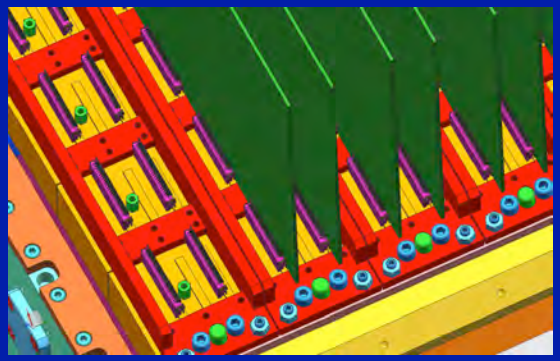
FDIRC motherboard

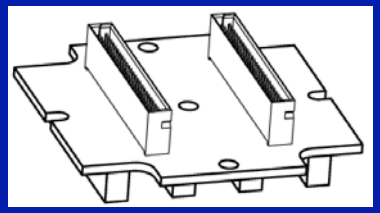
M. Benettoni

FDIRC final electronics:

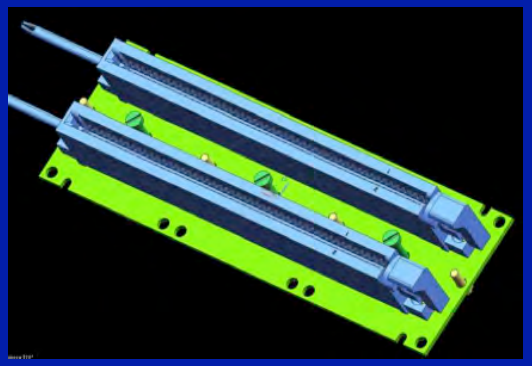


Press-fit connector:





ZIF connector alternative:

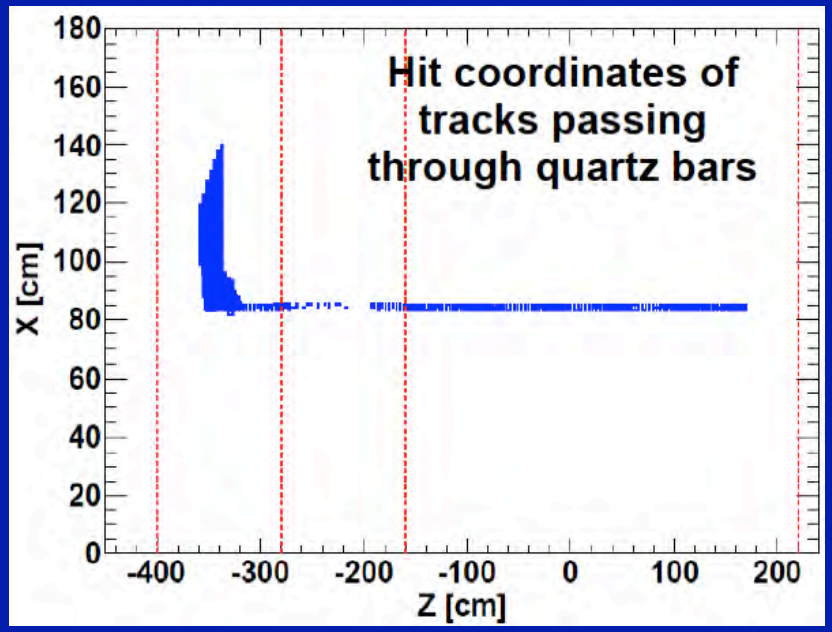


- **The concept of motherboard is being defined (mechanics only at the moment).**
- **Two possible connector alternatives:**
  - SMC-Q 64004 press fit connector, 50 contacts/pc, 100/PMT, Insertion force 26N each.
  - ZIF connector, Larger dimensions due to pitch of 2.54 mm, 50+50 contacts, length of connector body ≃150 mm, 200 contacts per group of 3 PMTs
- **HV & LV distribution is yet to be defined.**

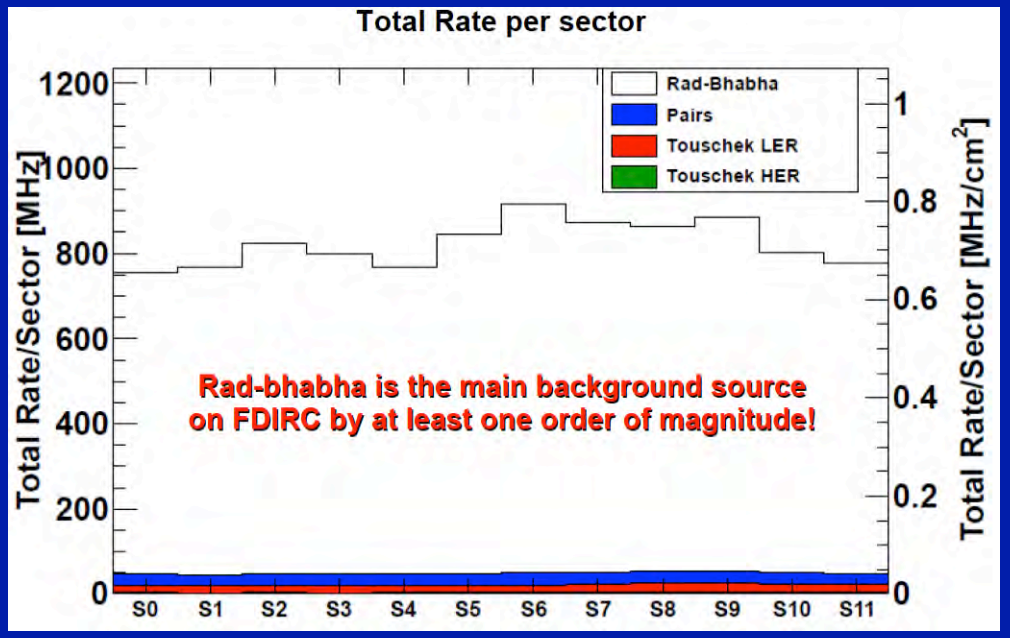
FDIRC background

Alejandro Perez

FDIRC camera must be shielded:



Total rate per sector:

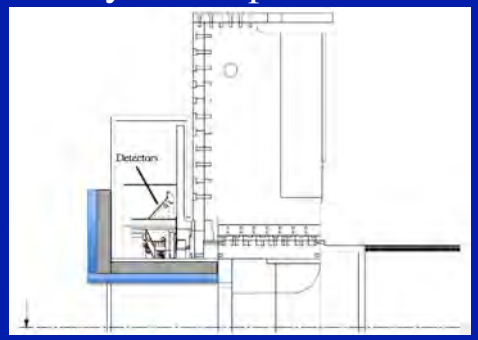


- **Clearly, FDIRC camera must be shielded.**
- **Radiative Bhabhas dominate.**
- **Rate per double pixel (before any shielding):**
  - 550 kHz/ double pixel contribution from FDIRC camera
  - 85 kHz/double pixel contribution from active volume.

FDIRC shielding

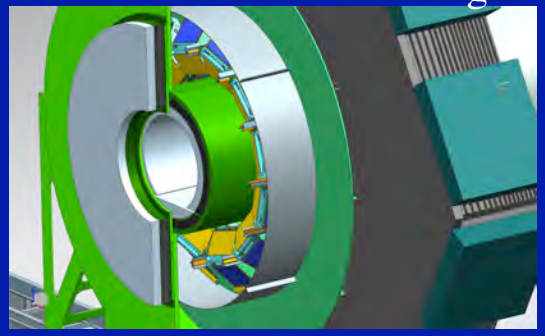
J. Va'vra

Jerry: concept

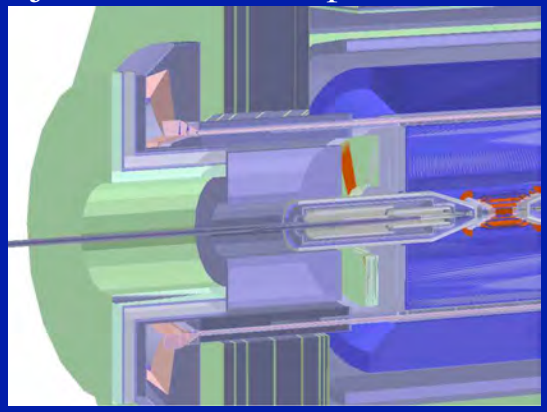


- 10 cm thick Boron-loaded polyethylene
- 10 cm lead in between two 2.5 cm-thick steel plates

Massimo: mechanical design



Alejandro: Bruno implementation



Requirement:

a) Reduce photoelectron rate from the FBLOCK.

b) Protect FPGA electronics from neutrons.

c) Need easy access to electronics.

Note:

To handle neutrons correctly one needs to cover much **larger area with neutron absorbers**.

The reason for Boron: It is actually a ^{10}B isotope, which is doing the job, and makes (n, **alpha**) reaction. There is also **~0.5 MeV Gamma** - much softer than other hard-Gamma n-capture reactions.

Detector studies

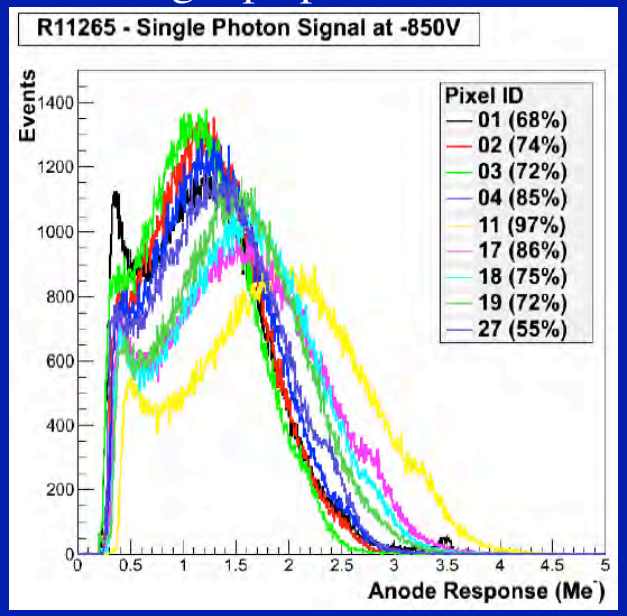
Comparison of several PMTs

Matteo Maino

A new Hamamatsu R11265 PMT:

R11265
185-650 nm
UV glass / 0.8 mm
26.2 x 26.2 mm^2
23 x 23 mm^2 (>85%)
64 / 2.9 x 2.9 mm^2
Super Bialkali
12
1100 V
1 x 10^6 at 1000V
0.4 nA
0.6 / 5.1 ns
1 : 3

Single pe pulses:

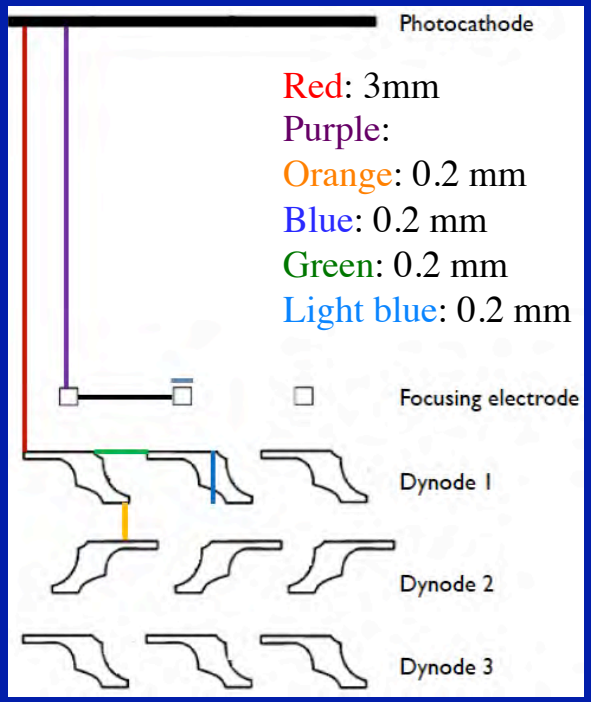


- **Many test results comparing H-9500, R7900 and R11265 tubes.**
- **A new R11265 has several attractive features:**
  - Smaller dead space around edges compared to older R7900 PMT (~15%).
  - Super Bialkali QE (~35% ?)
  - Allows smaller pixel size in the y-direction (2.9 mm) (FDIRC: combine 8 pixels to 23.2 mm width)?
- **At the moment, R11265 seems attractive solution for the LHCb experiment.**

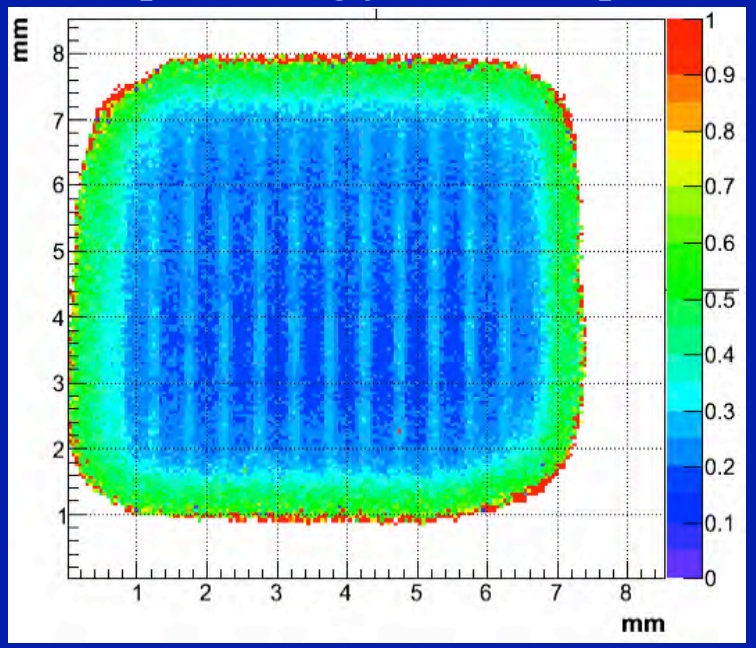
Detailed study of H-8500 timing response

Fabio Gargano

H-8500 electrode structure:



2D map of timing jitter in one pixel:



(presently done with multi-photon signal)

- **Detailed test of timing jitter across one pixel: see electrode structure.**
- **Resulting effective timing resolution will be worse than the best sweat spot.**
- **Do not know yet what will be a single pe timing resolution, but perhaps, at a level of 200-250ps.**
- J.V.'s note: that is what we were getting in the SLAC FDIRC test beam.

PID status

Barrel

- TDR: PID section is almost completed (~80%).
- Missing chapters:

Physics requirements
Reconstruction
MC Simulation
- Fast simulation
- Full simulation
Effect of Background on PID performance
Impact on other systems
Support services for electronics
Data flow
Earthquake analysis of FBLOCK & bar box structure
Experience with the final FDIRC prototype in CRT
Management structure
Institutional breakdown by task (needs to be completed)
Cost, Schedule and Funding (needs to be completed)
Schedule and Milestones
Critical path items

FTOF

2-3 pages of summary of this option

Summary

- **Clearly progress.**
- **Many tests going on.**
- **Should slowly drift towards testing of the final electronics.**
- **The target dates for FDIRC prototype:**
  - Fbox assembly: April
  - FDIRC assembly in CRT: May
  - SLAC/IRS2 electronics: June 15.
  - Start initial data taking: July.