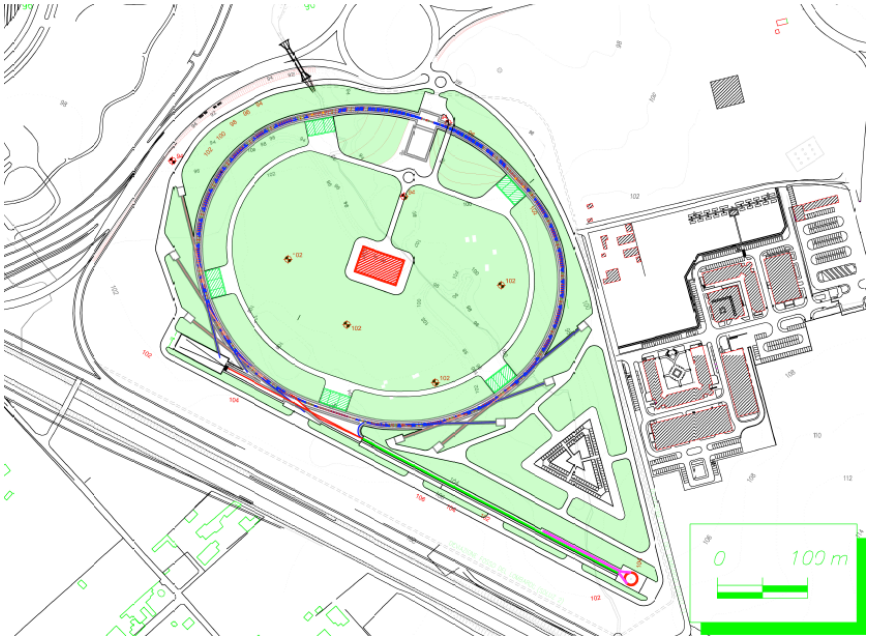


Detector Status

F.Forti, INFN and University, Pisa

Overview

- Detector design is fairly advanced
  - Progress report: arxiv.org/abs/1007.4241
- R&D continuing in several areas
- Most options are defined
- Proto-collaboration organization is in place and working well
- Transition to full collaboration well advanced

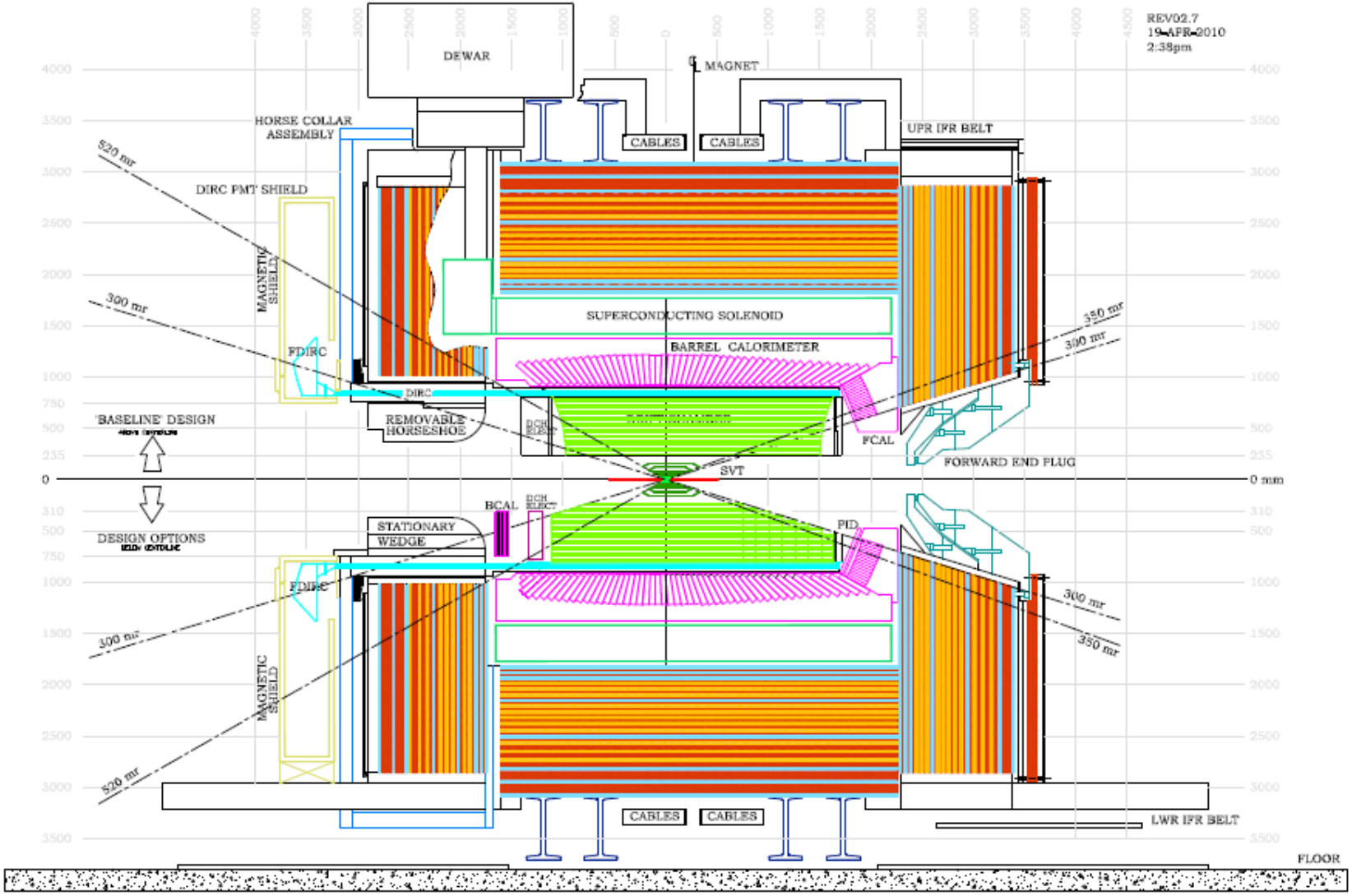
… but …

- Significantly more physicists and engineers are needed
- Need to define funding sources and committments
- Need to baseline design/schedule and move on to construction
- → Plan to produce TDR even if not everything is clear

Institutions

System	Institutions
SVT	Bologna, Milano, Pavia, Pisa, Rome3, Torino, Trieste, Trento, LBNL, Queen Mary, RAL, Strasbourg, Bari, Valencia
DCH	LNF, McGill, Montreal, TRIUMF, UBC, Victoria, Lecce
PID	SLAC, BINP, Cincinnati, Bari, Padova, Maryland, LAL, LPNHE, UC Riverside
EMC	Bergen, Caltech, Perugia, Rome1, Napoli
IFR	Ferrara, Padova, Krakow, Bologna, Mexico
ETD	SLAC, Caltech, Napoli, Bologna, LAL, Padova, Rome3
Computing	Padova, Ferrara, Torino, Bari, Bologna, Rome2, Pisa, Perugia, LNF, LBNL, Napoli, SLAC
Magnet/ Integration	SLAC, LNF, Pisa, Genova
Backgrounds/MDI	SLAC, Pisa, LNF, LNS, Roma2, Cagliari, Ohio State,
TBD	(Barcelona, Annecy, Tel Aviv, Liverpool, Kiev, ITEP, Kansas, Livermore, Louisville, Notre Dame,Ohio State, Princeton, Southern Methodist, South Carolina, Austin, Utah)

Detector Design (with *fewer* options)



Detector Design Issues

System	Baseline	Issues (technical OR manpower; R&D)
MDI	Initial IR designed	Magnetic elements and radiation masks. Design of tungsten shields. Cryostats radius Background simulations: global map, detector occupancy
SVT	6-layer silicon	Technology for Layer 0: striplets or pixels. Thin pixels R&D. Readout chip for strips. Mechanical design.
DCH	Stereo-axial He-based	Dimensions (inner radius, length). Mechanical structure. Cluster counting option.
EMC	Barrel: CsI(Tl) Forw: LYSO	Electronics and trigger. Mechanical structure Forward EMC technology: LYSO / LYSO+CsI(Tl); Pure CsI. Backward EMC: cost/benefit analysis
PID	DIRC w/ FBLOCK	FBLOCK design. Photon detection. Mechanical structure Forward PID: cost/benefit analysis. Prove TOF technology.
IFR	Scintillator+ fibers	8 vs 9 layers. SiPM radiation damage and location. Extra 10cm iron. Mechanical design and yoke reuse.
ETD	Synchronous const. latency	Fast link rad hardness. L1Trigger (jitter and rate). ROM design. Link to computing for HLT.

TDR process and timeline

- The Technical Design Report is an essential step to get funding and get the detector built.
- Conflicting requirements
  - Essential to enlarge the collaboration, define institutional responsibilites and find resources for designing and building the detector
  - Essential that collaboration members, institutions and countries take ownership of the design and fabrication
- Funding and schedule
  - The TDR must contain an initial definition of funding and resource availability
  - Open question about how to incorporate funding agencies intentions and committments into the TDR:
    - → Proposal to have a separate financial document to detail the agencies contributions

Timeline

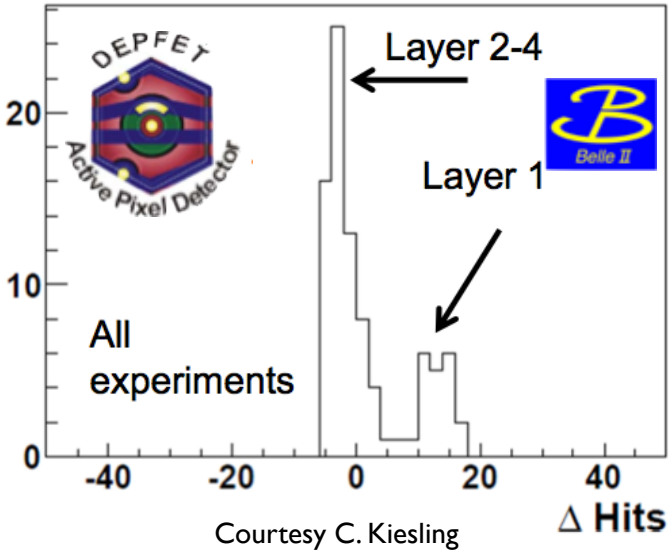
- June-July: setup SVN repository + initial outline
- September 2011
  - Detailed outline with page count + editorial responsibilities
  - Tentative institutional matrix of responsibilities and money allocation
- ~~December 2011~~ → March 2012
  - First (in)complete draft,
  - Decision about what is in and what is out
  - ~~Updated budget and schedule for construction~~
- ~~February 2012~~ → June 2012
  - Complete draft into final editing
  - Final readers identified
- July 2012
  - Updated budget and schedule for construction
- September 2012: Publish

MDI

Eugenio Paoloni

Background simulations

- The SuperB - Belle II joint meeting was very fruitful
  - Their rate measurements of pairs and our simulations are in fairly good agreement
  - Consensus reached that radiative Bhabha backgrounds are not negligible in **both** experiments
  - We learned from Belle-II the dangers of multi turn Radiative Bhabha losses: we plan to simulate it asap



Courtesy C. Kiesling

Full Monte-Carlo simulation: 3 x naive expectation: **curlers** !

These are not SuperB predictions !

SuperB predictions 10^{34} Hz/cm^2

Experiment	SVD layers	Hits	QED hits	KoralW	SuperB(BDK)
Belle	1	~ 100	13.3 ± 2.6	11.31	62.2 ..... 11.7
	2 - 4	~ 45	-2.9 ± 2.1	2.38	13.1
Belle II	Occupancy (1st PXD)			0.7%	4.0%

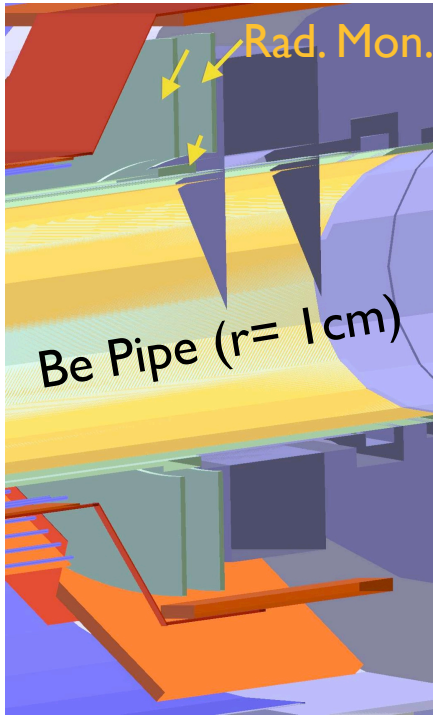
By Giuliana accurate rescaling

Table 6.1: Comparison between data and Monte Carlo

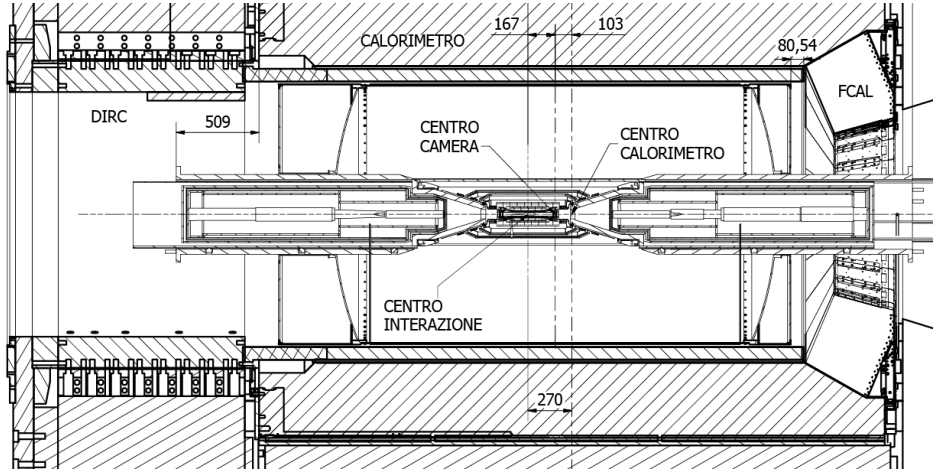
Courtesy C. Kiesling

MDI & Bkg. Simulation

- Progresses in the simulation:
  - minor bug fixes in the geometry and magnetic field configuration
  - Radiation Monitor put in the Bruno simulation
  - Cherenkov light simulation for the FTOF (final checks)
  - EMC energy deposits binned in time for a more accurate simulation of the system response
  - Beam gas sample provided by Manuela simulated with Bruno



- Progresses in the mechanical design:
  - Filippo progressed in the design of the quick mounting/demounting procedures (Parallel on Integration)
  - Fabrizio Raffaelli is going to study the mechanical fixture of the W shields



SVT

Giuliana Rizzo

SVT – Some highligths since Dec.

Background simulation: many tests to understand new numbers from Dec.

- Total rates from Dec. production (several sources included) too high for SVT!
- Pairs increased a lot; some reasons understood and fixed, but rates still higher
  - +20% in inner layers +80% in outer layers, where different material close to IP can count.
- Touscheck as high as pair in L1-5. Rad Bhabha not negligible.
- Some sources still to be included and new shielding configuration need to be studied

Joint Background Workshop with BelleII in Feb. very useful:

- Discrepancy with BelleII pairs estimate has been solved and our result is still valid.
  - The factor 15 was due to some "problems" in the initial BelleII value and to some misinterpretation of our results by Belle colleagues. The hit rates expected in Layer0 for both experiment is consistent. SuperB estimates also agrees with measurement performed with SVD Belle data.

Performance studies: high background deteriorates performance

- low efficiency due to analog dead time (< 90 % in some layers)
  - Impact will be evaluated with fastsim

x5 safety included,
some source still missing

- High offline occupancy: ~4-6% in L0-L3 and ~2.5% in L4-5 (x5-x10 w.r.t. BaBar)
  - Impact on resolution will be evaluated with fastsim
  - Can affect reconstruction (difficult to evaluate the impact but need to face issue)
- Many tests done to check discrepancy among fullsim and fastsim (for background studies); fastim tools to study SVT performance in high occupancy almost ready

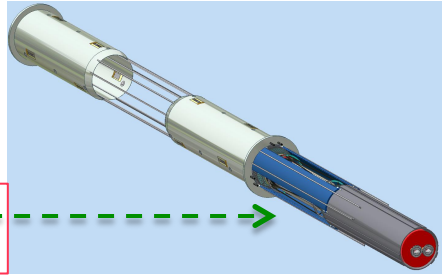
R&D on pixel: INMAPS chips received and under test now

SVT-Detector Design and TDR status

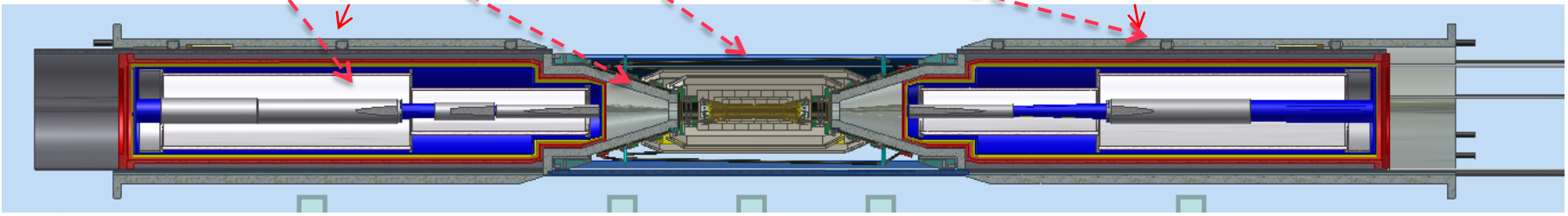
Activities almost completed in all areas

Complete the work in ~1-2 months then concentrate on TDR writing

- Silicon Sensors: geometry defined and detailed parameters provided noise evaluation.
- Fanouts: Layer0 - some details still to be defined. Layer1-5 - prototypes in production at CERN
- FE chip development: Readout architecture simulated (VHDL): 100% digital efficiency achievable even for high Layer0 rates (2 MHz/strip).
  - "Analog" inefficiency and hit time resolution simulated with present FE design.
  - Shaping time reduction for some layers under evaluation to mitigate background impact.
- Peripheral Electronics: progress on definition of HDI components, connectors, copper bus & transition cards. Some work still needed
- DAQ & FEboard: Electronics load reavaluated with new inputs (new geometry and back. rates)
- Performance studies: some work still needed
- Mechanics: Detailed procedure for quick demounting defined (presentation at the Integration session).



Insert a temporary cage to make SVT/Be pipe more rigid then slide criostats, W conical shields, cage + SVT+Be pipe w.r.t W cilindrical shields



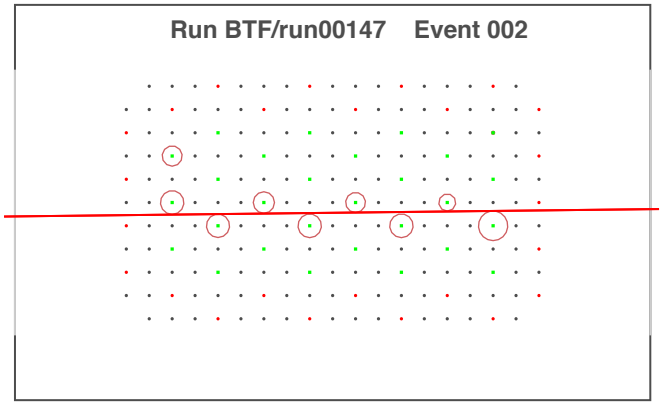
DCH

Giuseppe Finocchiaro and Mike Roney

Beam test of Prototype2 at BTF

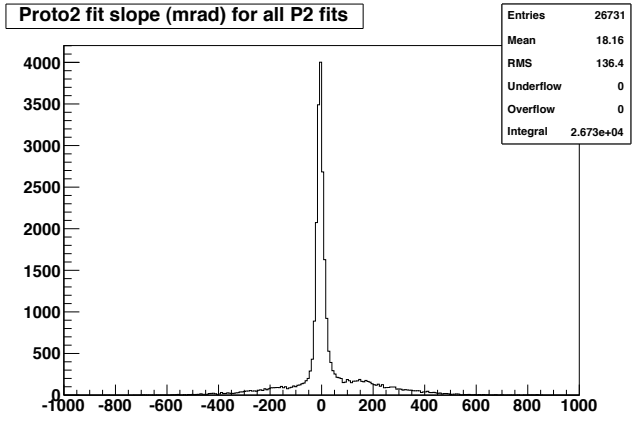
- *2.5m* long prototype with 28 sense wires arranged in 8 layers
  - Goal: study DCH response from single clusters in a realistic environment, and serve as a test bench for the final FEE and for test of DCH trigger implementation

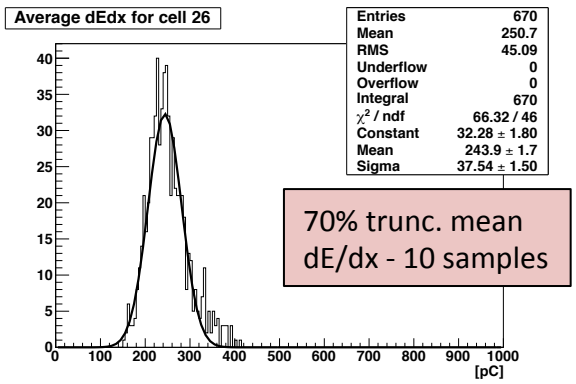
Analysis of Proto2 data



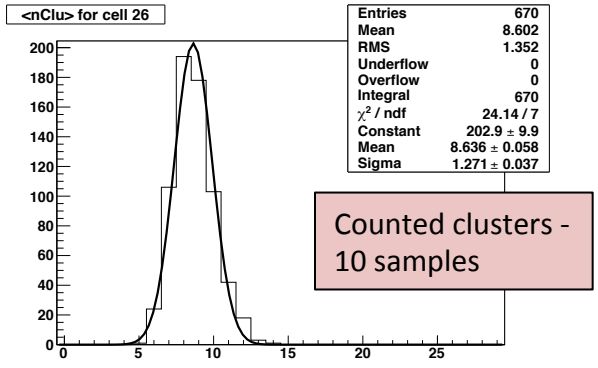
Analysis status will be reviewed during the meeting. Examples:

- Tracking
- comparison of cluster counting and dE/dx performances





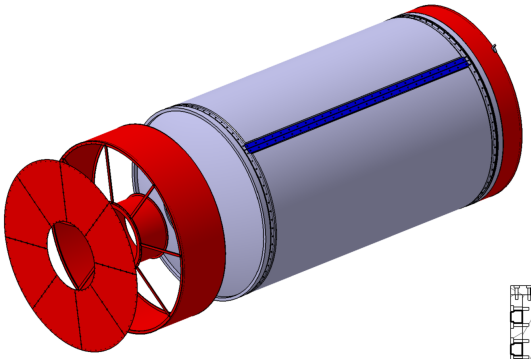
70% trunc. mean dE/dx - 10 samples



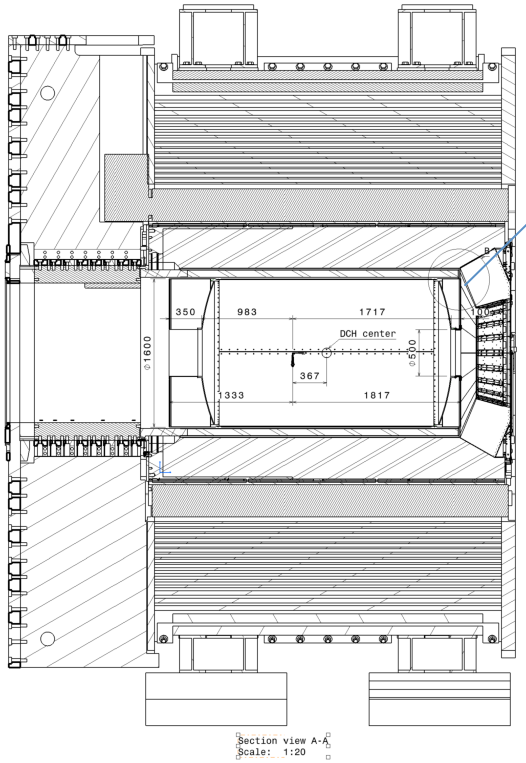
Counted clusters - 10 samples

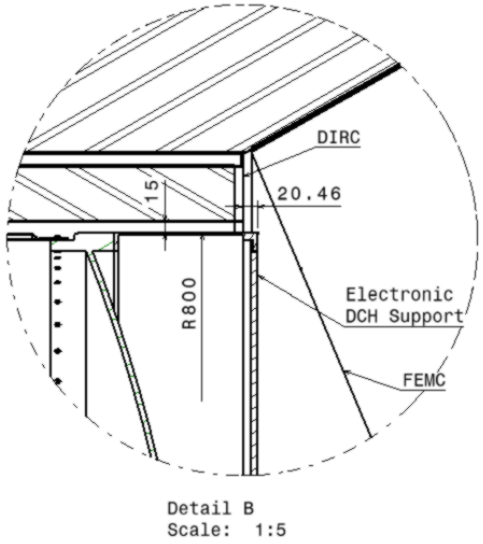
Mechanical Structure

- More Progress on the DCH technical design, including:
  - services (shielding, support for electronics)

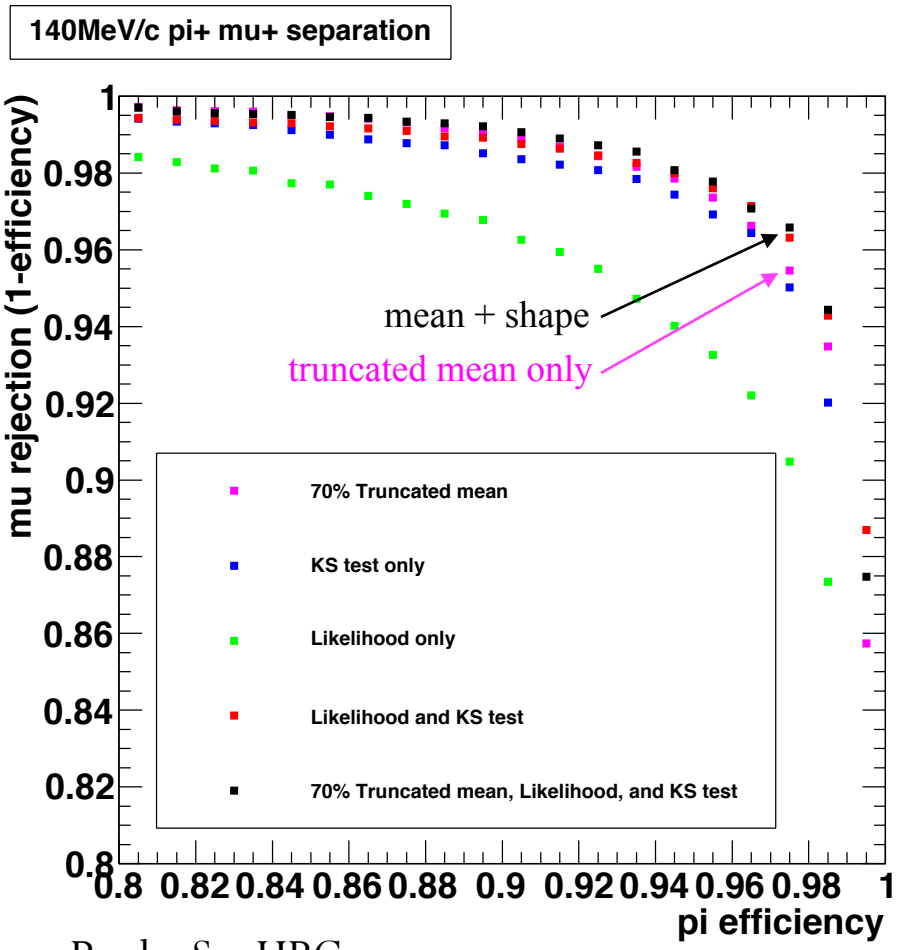


  - integration





TRIUMF DCH beam test dE/dx analysis

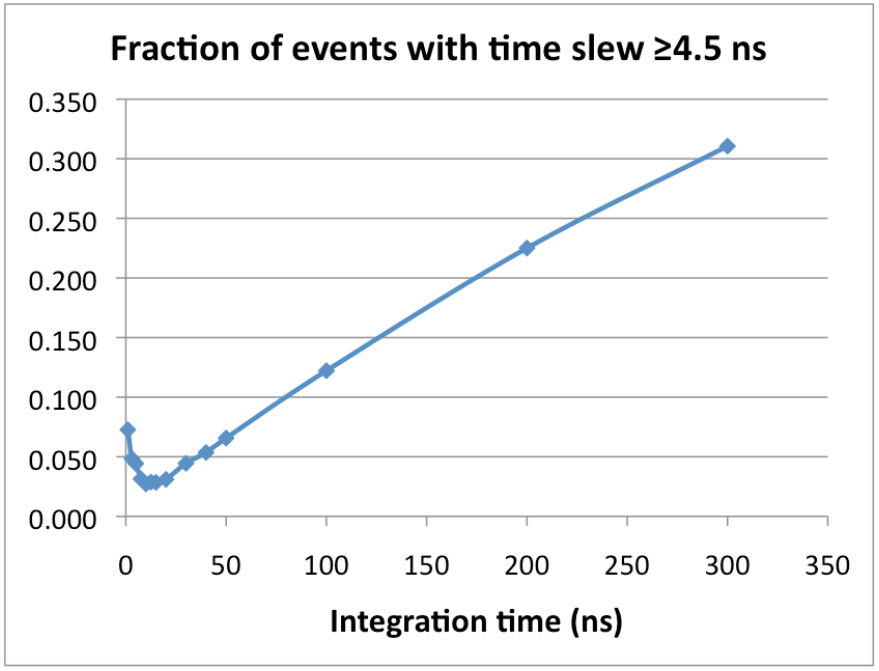


Rocky So, UBC

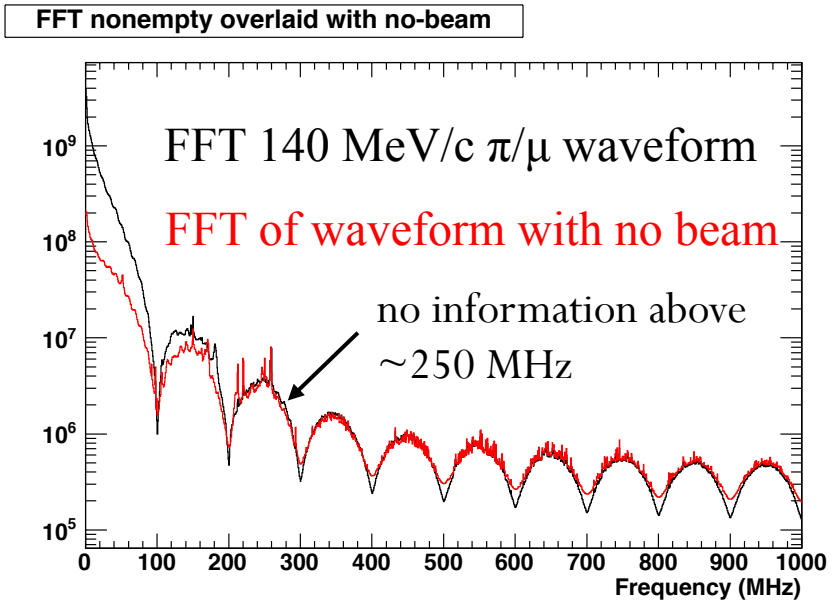
- Study PID performance using standard readout for comparison to cluster counting.
- Can perhaps do better than traditional truncated mean by looking at distribution of energies among the samples recorded by 40 layer DCH.
- dE/dx plus cluster counting should give best performance

Amplifier properties: noise and bandwidth

- Quantify impact of noise by slew: change in measured drift time for 1σ change in threshold.
  - no TDC; time extracted from waveform.
  - results are comparable to BaBar



- One goal was to check whether Montreal amplifier prototype had adequate bandwidth for cluster counting.
- Bandwidth limitation of readout limits usefulness of test. New data this summer.



PID

Nicolas Arnaud and Jerry Va’vra

PID status

a) FDIRC prototype

- FDIRC optics (SLAC):
  - QC of FBLOCK and Wedge completed.
  - Fbox is being assembled around FBLOCK – expect to finish in April.
  - Final assembly in CRT - expect to finish in May-June.

- FDIRC electronics:
  - Electronics for the FDIRC prototype is being built (SLAC & Hawaii).
  - Expect to have the prototype's electronics available in June

- Software development:
  - FDIRC prototype optics in MC simulation (Maryland)
  - Continuing work to understand data from the 1st FDIRC prototype (SLAC).

PID status

b) FDIRC at SuperB

- FDIRC electronics:
  - Final electronics motherboard for SuperB FDIRC designed (LAL & Padova)
  - Work on the final SuperB FDIRC electronics continues (LAL):
    (SCATS chips received, Test boards being finalized, Tests of the analog boards have started, new 16-channel Wavecatcher board is ready for tests)

- FDIRC shielding (SLAC, Padova):
  - The 1st version of the SuperB FDIRC shield design completed
  - It has been included in MC background simulation program (Alejandro).

- Continuing work on H-8500 tube tests (Maryland, Bari, Padova, SLAC).

- TDR: PID section is almost completed (~80%).

FDIRC optics was published in “SLAC Today”

https://news.slac.stanford.edu/features/slac-physicists-build-prototype-particle-identification-detector

FBLOCK optics:

- **There is a short article describing highlights.**

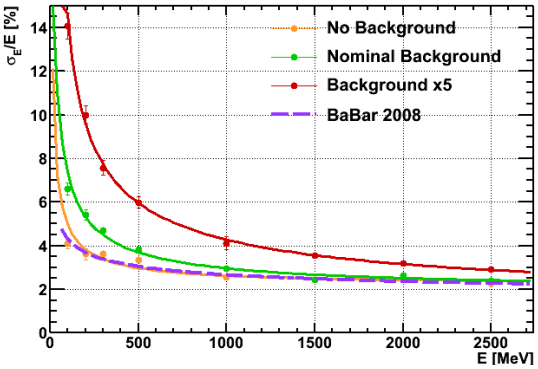
EMC

Claudia Cecchi and Frank Porter

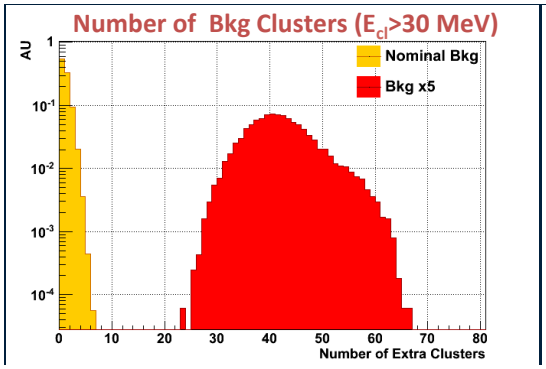
EMC - Barrel

- Babar Barrel will be reused replacing the preamps.
- Background in Barrel (Radiative Bhabhas).
  - Large effect of x5 safety factor with current shielding

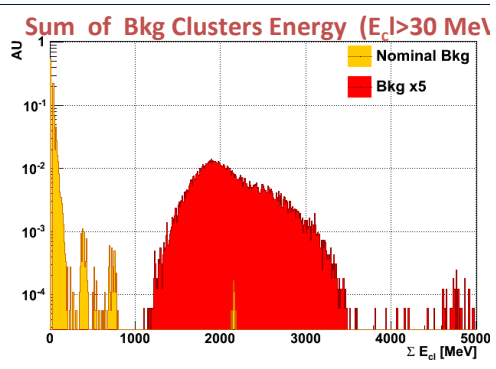
Resolution



Number of background clusters



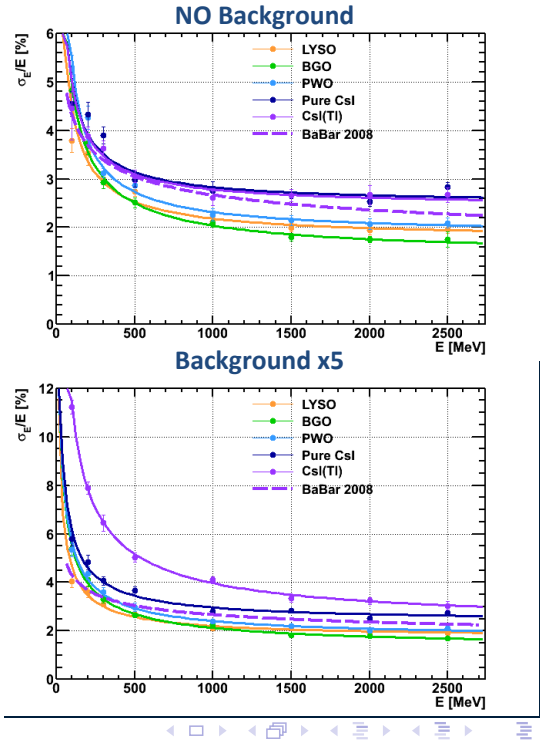
Background clusters energy



- Question: Do we disassemble barrel for move to Italy?
  - Barrel not designed for long trips; risk of damage to crystals
  - Disassembly and reassembly represents a substantial cost in schedule,labor, and facilities
  - Subject of discussion at this meeting

EMC – Forward technology

Forward alternatives – resolutio
Stefano Germani



LYSO in a thin structure is technically optimal for forward EMC.
If we can't mitigate backgrounds, the barrel performance is degraded, and a highly performant forward calorimeter is difficult to justify (i.e., pay for).
Alternative forward schemes under discussion:
To be updated and discussed this week

Option	Number of new crystals	New crystal volume (cc)	Crystal cost/cc ($)	Crystal cost (M$)	Photo-detectors (M$)	Laser/LED system (M$)	Mounting structure (M$)	Total cost (M$)
LYSO full (baseline)	4500	401622	25.00	10.04	0.57	-	2.27	12.88
LYSO old structure	3600	401622	25.00	10.04	0.57	-	0.25	10.86
Hybrid (CsI(Tl)+LYSO)								
3 CsI(Tl) + 6 LYSO	2160	244734	25.00	6.19	0.49	-	0.25	6.93
4 CsI(Tl) + 5 LYSO	1760	197911	25.00	4.95	0.40	-	0.25	5.60
5 CsI(Tl) + 4 LYSO	1360	153783	25.00	3.84	0.31	-	0.25	4.40
Pure CsI	900	692220	5.09	3.52	0.56	-	0.25	4.33
BGO	4500	392181	9.00	3.53	0.57	1.2-3.0	2.27	7.57-9.37
$PbWO_4$	4500	305714	5.00	1.53	0.57	1.2-3.0	2.27	5.57-7.37

David Hitlin

Advisory Committee on Forward Technology

Giuseppe Finocchiaro
Chris Hearty, chair
Eugenio Paoloni
Matteo Rama
Bill Wisniewski

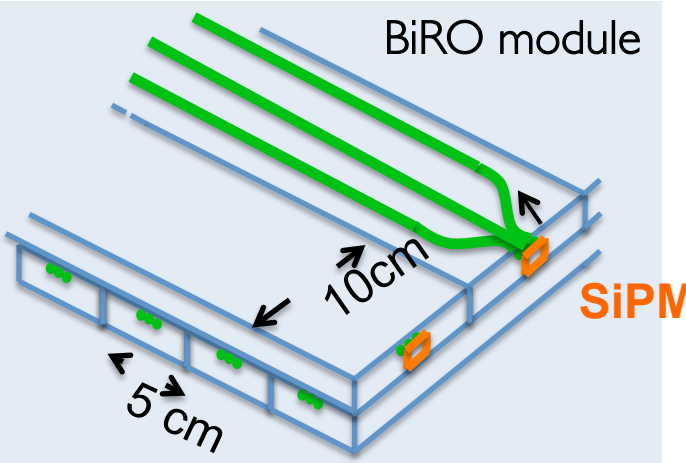
17:00 EMC session devoted to forward EMC baseline in TDR

IFR

Roberto Calabrese

IFR overall status

Critical issues for final detector design



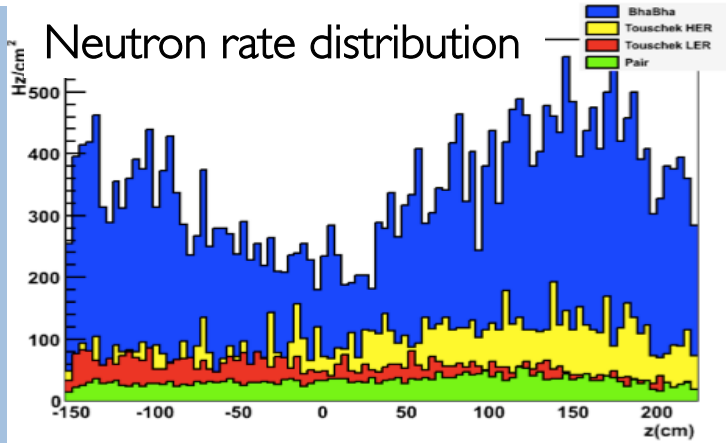
☑ Binary readout vs time readout for the barrel ➡ Binary readout is now our baseline

☐ Number of active layers: 8 vs 9 ➡ 9 active layers is the baseline for the TDR, but the 8-layer option is not discharged

☐ Amount of absorber and flux return configuration ➡ 92cm of iron is the current baseline for the TDR. Under investigation the possibility to use less absorber. The BaBar iron will be reused with no major modification.

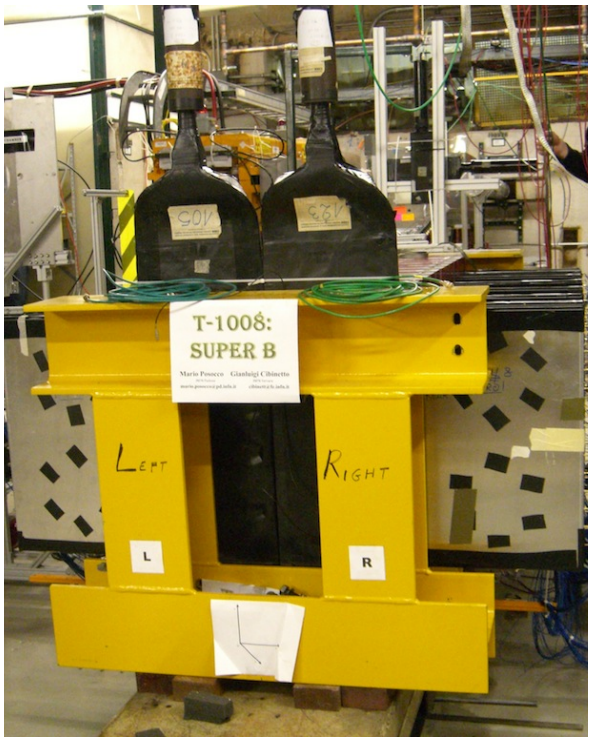
☑ Position of the photodetectors

SiPM will be placed at the end of the scintillators inside the gaps. Neutron rate is high (up to some 100Hz/cm^2) but with the binary readout it's possible to rise the thresholds to reduce the increasing of the noise.



Beam Test

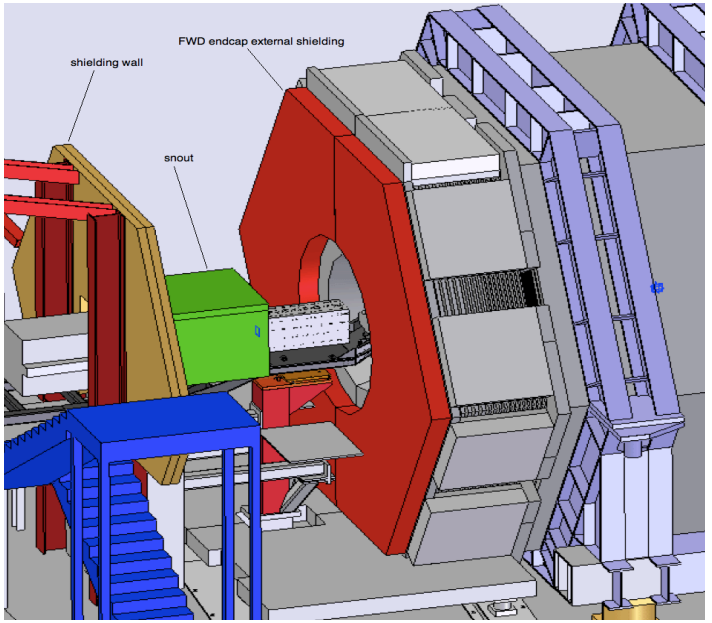
- Our last beam test at Fermilab with muon/pion beam just done (end March 14th)
- Main purpose: "calibration" run at high momenta (5-10 GeV) where the beam composition is well known and data are cleaner.
- Experimental setup and trigger system improved.

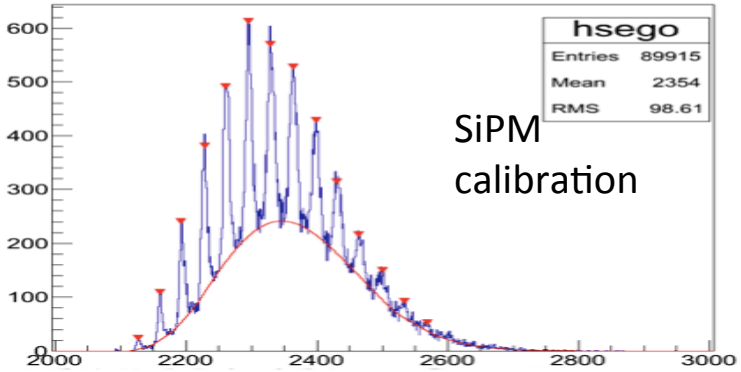


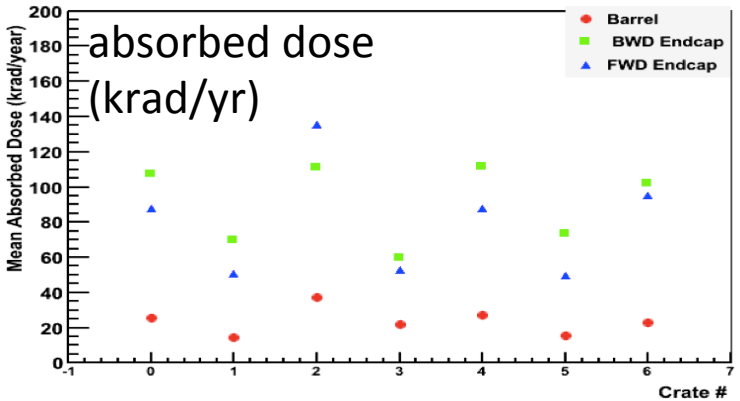
- New analysis strategy: tune Monte Carlo (Bruno) simulation based on high momenta test beam data.
- Great reliability, operational stability and performances of the IFR prototype during all the beam test runs

Other ongoing activities

- Background simulation: external mechanical structures and other shielding studies.
- Flux return and detection module mechanics.
- R&D activities in Bologna, Ferrara and Padova to optimize/finalize the module design.
- Preparation of the next irradiation tests for SiPM and electronics.
- TDR preparation ongoing.







ETD/Online

Dominique Breton, Umberto Marconi, Steffen Luitz

ETD - 1

- Since last meeting, progress on many different items
  - Clock and control links:
    - test beam at LNS of Virtex5 and Virtex6. Measurements of SEU cross-section with respect to memory configuration and link design (as a whole)
    - test beam at LNS of National off-the-shelf serializer (TX only), AVAGO VCSEL transceivers and again Virtex5 at different dose rate and with different SEU mitigation strategies.
  - Trigger:
    - 32 channels with clocked discriminators have been successfully integrated on DCH and readout with a TDC.
    - 2 different track elements have been implemented thanks to a look-up table.
    - Cosmic and test beam results will be shown.
    - Single LYSO crystal has been read out by PM on one side and SiPM on the other.
    - Contact has been taken with BW to get a matrix in order to test an analog sum.
  - ROM:
    - 10 GbE is in the hand of Bologna engineers team => should work in few months.
    - PCIe solution as far as electronics is concerned is fine in principle.
    - We have to design a low consumption mezzanine board, meant to be pluggable to a PC mother board to the PCIe bus.
    - Linux driver needs instead additional work to achieve better performances.

ETD - 2

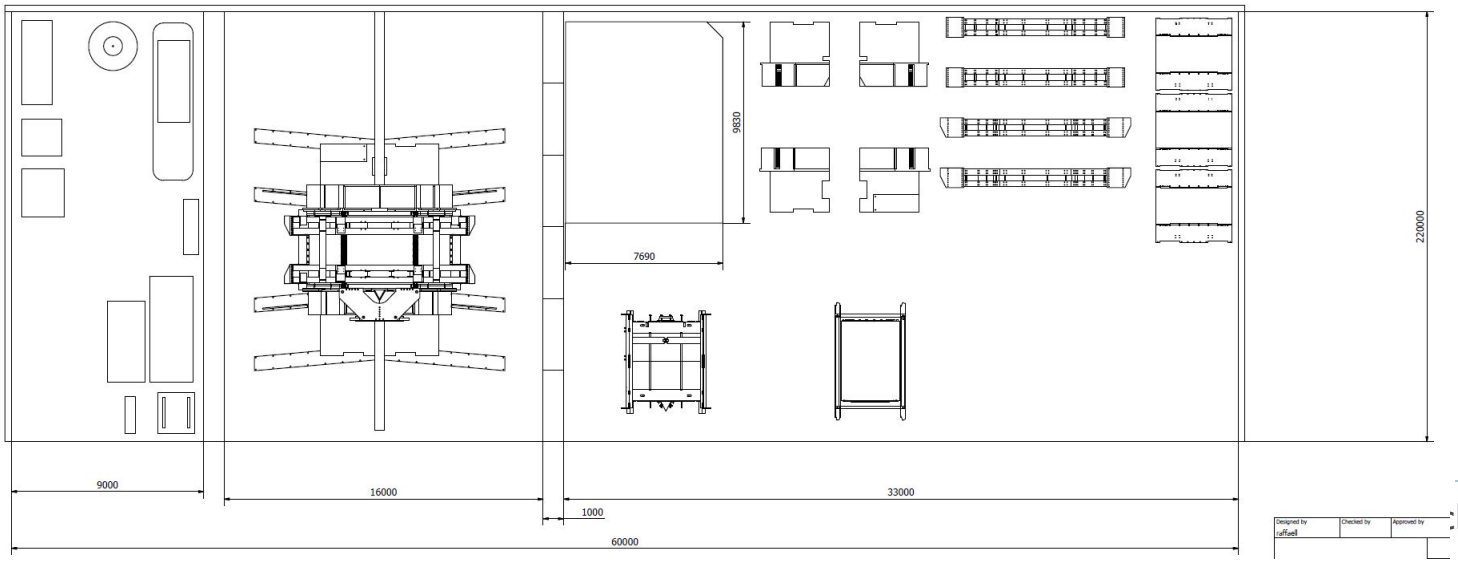
- Progress was also made on outline and writing of the ETD/Online TDR chapters:
  - ETD/Online introductory paragraph in the main introduction chapter.
  - Then 2 dedicated chapters:
    - ETD/Online (with 3 major sections)
      - Requirements and design philosophy
      - Event data chain: Trigger, DAQ, Event Builder, HLT and data logging
      - Support services (ECS, DCS, monitoring, run control, etc.)
    - Electronics
      - description of the hardware implementation of electronics.
- Have an event data chain design proposal. Will discuss during this meeting.
- We will have 3 sessions during this workshop:
  - one concerning common items => Wednesday 11:30
  - one concerning front-end electronics=> Thursday 9:00
  - one dedicated to hardware trigger => Thursday 11:30
- During all sessions, we will focus on the following items:
  - the writing of the TDR sections
  - the answers given to the integration and power supplies questionnaires

Integration

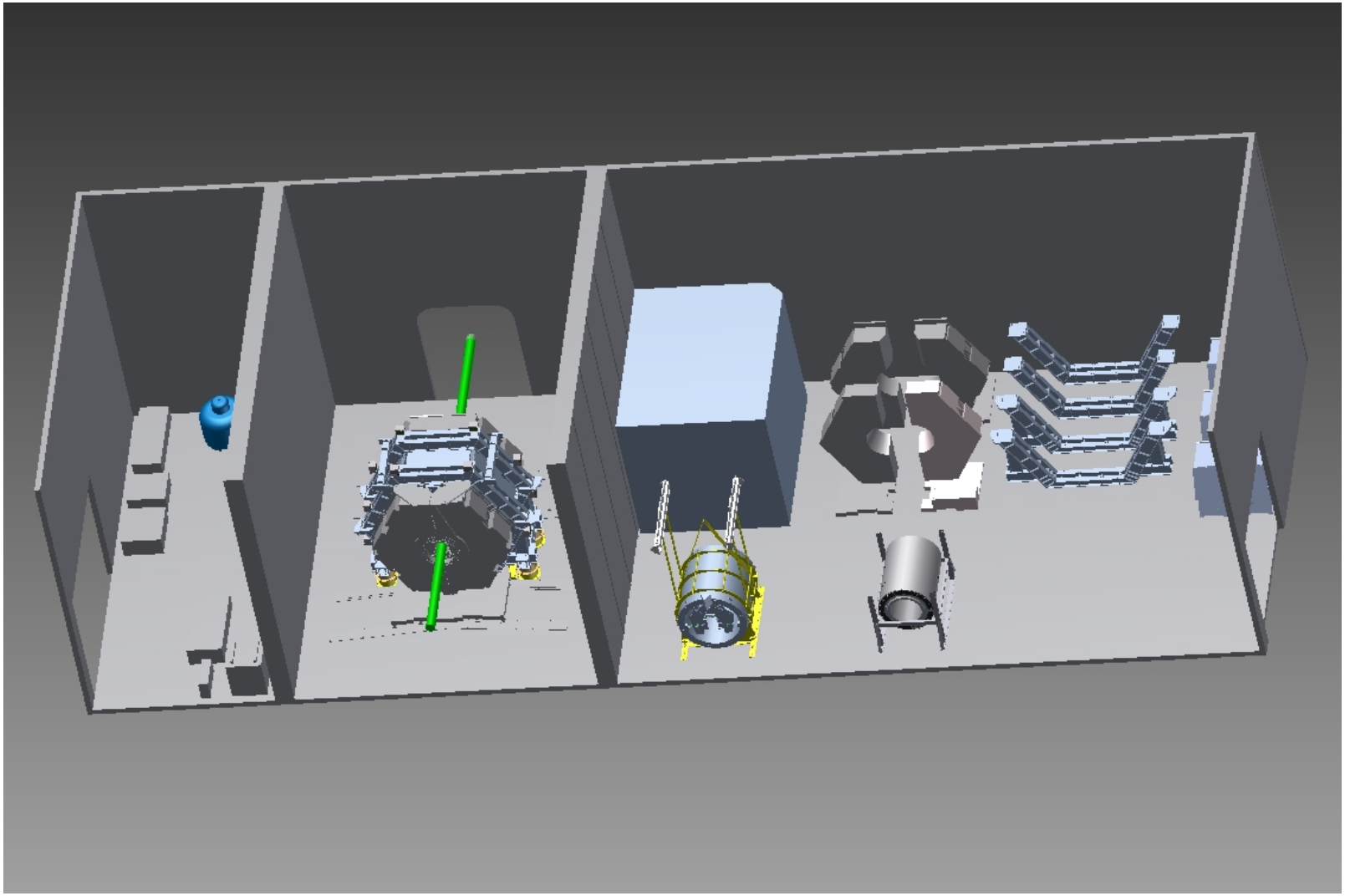
F.Raffaelli, W.Wisniewski

Integration issues

- Mechanical integration group operational
  - Integration and assembly of detector
  - Experimental hall structure
  - Transportation issue
  - Refurbishing strategies
- Gathering info from subsyst.
  - Cables, services etc.
  - Dimension and location of infrastructures
  - Power, cooling, etc.



IR Hall Scheme



Interaction with accelerator team

- Need to be boosted, with more regular technical contact
- Started to look at common project management tools
  - Session on Thursday morning
- Large questions need to be addressed soon
  - IR Hall: dimensions, layout, services, power, cooling, cryo, etc.
  - Envelopes in Machine-Detector Interface. Strategies for mechanical integration between detector and machine
  - Commissioning strategy: is the full 1.5T field needed for machine commissioning ? Big impact on detector assembly and commissioning strategy.
  - Overall schedule: need to start laying down the overall integrated schedule for accelerator and detector construction

Agenda

SuperB Collaboration Meeting
March 19 - 23, 2011
Laboratori Nazionali di Frascati

Agenda

All Plenary Sessions will be held in Aula Touschek

Meeting Registration Desk: aula T75

Social Dinner: Ristorante Cacciani

	Mon, Mar 19		Tue, Mar 20		Wed, Mar 21		Thu, Mar 22		Fri, Mar 23
9:00	PARALLEL	9:00	PLENARY	9:00	PARALLEL IV	9:00	PARALLEL VIII	9:00	PLENARY
DA	Accel	Tou 10 20 20 20 20 20	*Introduction and Status* Welcome Project status (M.Giorgi) Accelerator (M.Biagini) Physics (A.Bevan) Detector (F.Forti) Computing (F.Bianchi)	Tou A-1 Sem B-1 Conv DA	SVT DCH PID EMC IFR Accel	Tou Conv Sem DA	Accel+Det: Proj Mgmt COMP: Overflow PHYS Det: ETD II	Tou	SUMMARIES AND OUTLOOK I Computing Physics ETD Integration Det Outlook
		11:00	*Coffee Break*	11:00	*Coffee Break*	11:00	*Coffee Break*	11:00	*Coffee Break*
		11:30	PARALLEL I	11:30	PARALLEL V	11:30	PARALLEL IX	11:30	PLENARY
DA	Accel	Tou B-1 DA A-1	COMP: Distributed Comp. EMC Accel DCH	Tou A-1 Sem DA	Det: ETD I DCH SVT Accel	DA Conv Sem Tou	Det: ETD III COMP: Fullsim&Background PHYS Accel: Proj. Mgmt		SUMMARIES AND OUTLOOK II Accel Design MDI, IR & Backgrounds Cabibbo Lab (R.Petronzio)
		13:30	*Lunch*	13:30	*Lunch*	13:30	*Lunch*	13:30	*Lunch*
14:00	PARALLEL	15:00	PARALLEL II	15:00	PARALLEL VI	15:00	PARALLEL X	15:00	
ADir DA	Detector Technical Board Accel	Tou Sem DA	Det+Acc: MDI / Backgnd COMP: R&D Accel	Tou A-1 Sem B-1 Conv DA	SVT DCH PID EMC IFR Accel	Tou Sem DA	INTEGRATION COMP+PHYS: Production Plan Accel	ADir DA	Detector Technical Board Accelerator Board
16:30	*Coffee Break*	16:30	*Coffee Break*	16:30	*Coffee Break*	16:30	*Coffee Break*	16:30	*Coffee Break*
17:00	PARALLEL	17:00	PARALLEL III	17:00	PARALLEL VII	17:00	PARALLEL XI	17:00	
ADir DA	Detector Technical Board Accel	Tou Sem	Det+Acc: MDI / Backgnd COMP+PHYS: Physics Tools	Tou A-1 Sem B-1 Conv DA	SVT DCH PID EMC IFR Accel	Tou DA	Det Summaries Accel	ADir	Project Board
18:30		18:30		18:30		18:30		18:30	
				19:30	*Social Dinner*		*Council*		

DETECTOR TIMELINE CARTOON

Data Taking

Bkgnd/ Commissioning Detector

Detector Assembly

Start

Detector Procurement

Start

MDI IR Hall Services

Design

2017

2016

2015

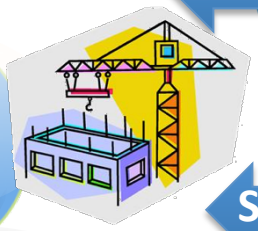
2014

2013

2012

Detector Commissioning

Transp. of Babar pieces



Detector TDR

Circulating Beams

IR Hall Available

Civil Construction

Start

CabibboLab

BACKUP

Proto-Detector Organization

Detector Coordinators – B.Ratcliff, F. Forti
Technical Coordinator – W.Wisnieswki

- SVT – G. Rizzo
- DCH – G. Finocchiaro, M.Roney
- PID – N.Arnaud, J.Va'vra
- EMC – F.Porter, C.Cecchi
- IFR – R.Calabrese
- Magnet – W.Wisniewski
- Electronics, Trigger, DAQ – D. Breton, U. Marconi
- Online/DAQ – S.Luitz
- Offline SW –
  - Simulation coordinator – D.Brown
  - Fast simulation – M. Rama
  - Full Simulation – F. Bianchi
- Background simulation – M.Boscolo, E.Paoloni
- Machine Detector Interface –
  - Rad monitor –
  - Lumi monitor –
  - Polarimeter –

Detector Geometry Working Group
Chairs M.Rama, A.Stocchi

Forward Task Force
Chair H.Jawahery

Backward Task Force
Chair W. Wisniewski

Mechanical integration team
F. Raffaelli

To be created:
Central electronics team

International Funding of Detector

- Italy
  - General agreement that will provide about 50% of funds needed for detector. Need to work on baseline and funding profile.
- France
  - Request will be presented in Fall 2011
- Canada
  - Request will be presented in Fall 2011
- UK
  - Ongoing negotiations. Desireable a larger participation of UK groups
- Poland
  - Request presented in 2011
- US
  - Request will be presented in late 2011 / early 2012
- Russia
  - Exchange contribution for IGNITOR to be understood. Bulk will be for accelerator work, but some could go to detector
- China
  - Ongoing negotiations.
- Spain, Germany, Norway, Israel, …
- For all it is essential to have a clear picture of the organization and schedule of infrastructure and accelerator