



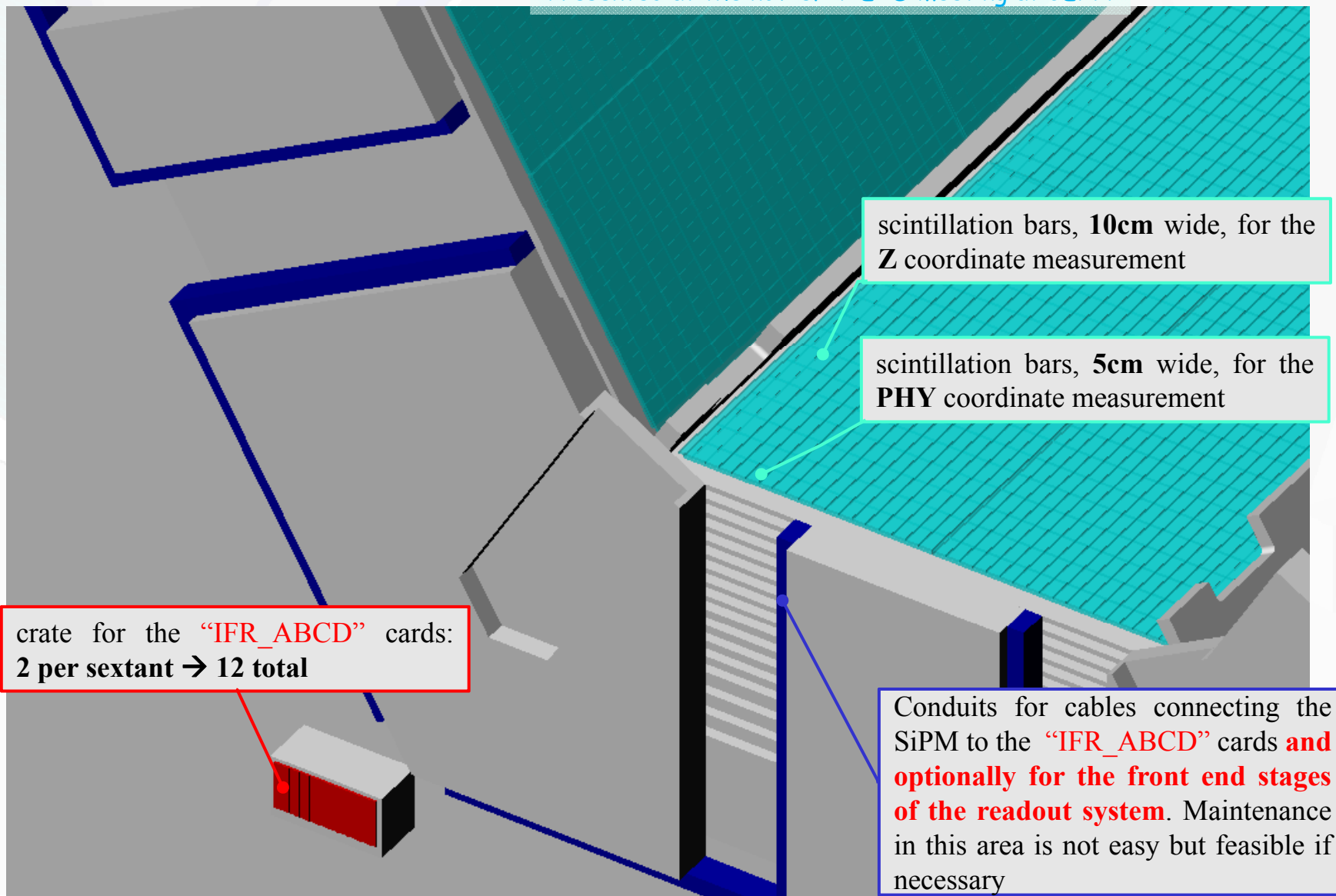
SuperB IFR electronics: update

SuperB IFR electronics: update

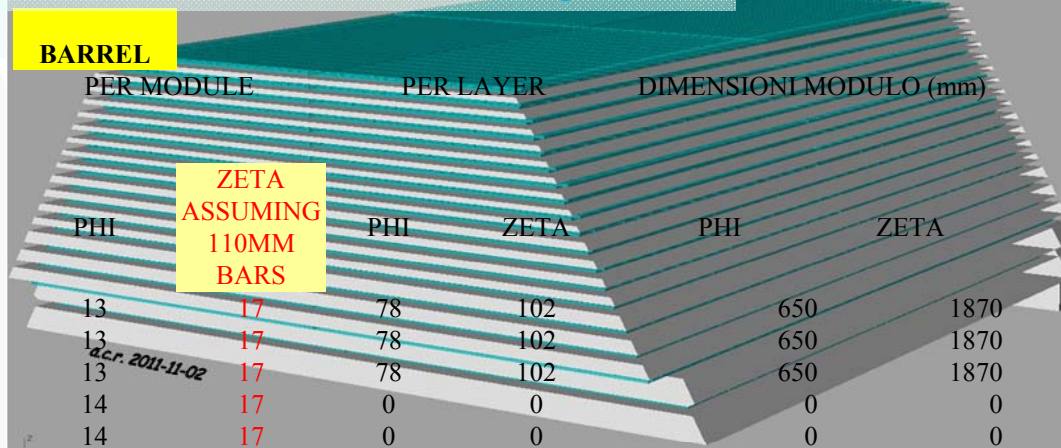
- features of the current baseline for the IFR detector design with "binary mode" readout
 - layout of the scintillator bars in the barrel
 - layout of the scintillator bars in the endcaps **updated**
 - channel number and data bandwidth estimation **updated**
 - test of passive Single Ended and active Differential options for "picking-up" the signals from SiPM **new**
 - block diagram of the "IFR_ABCD" front end card
 - test of "CLARO" chip for SiPM readout **new**
 - specification of a dedicated ASIC for SuperB IFR front end **new**
- addressing the radiation issues
 - background rates estimates at the location of IFR front end electronics **updated**
 - results of measurements at the INFN Laboratori Nazionali di Legnaro of neutron induced effects on some key elements of the current baseline IFR readout electronics
 - overview of the next irradiation tests being planned **new**

a.c.f. 2011-11-02

features of the current baseline IFR detector design with "binary mode" readout: barrel
Presented at the nov16/17 ETD meeting at CERN



channel number estimation: barrel
Presented at the nov16/17 ETD meeting at CERN



LAYER WIDTH	LAYER	No.Modules per layer	LAYER ENABLE
1963	1	6	1
1987	2	6	1
2050	3	6	1
2113	4	6	
2176	5	6	
2240	6	6	1
2304	7	6	
2367	8	6	
2431	9	6	
2494	10	8	1
2569	11	8	
2641	12	8	
2712	13	8	1
2784	14	8	
2879	15	8	1
2973	16	8	
3068	17	8	
3144	18	8	1
3296	19	8	1

PHI	ZETA ASSUMING 110MM BARS	PHI	ZETA	PHI	ZETA
13	17	78	102	650	1870
13	17	78	102	650	1870
13	17	78	102	650	1870
14	17	0	0	0	0
14	17	0	0	0	0
14	17	84	102	700	1870
15	17	0	0	0	0
15	17	0	0	0	0
16	17	0	0	0	0
12	17	96	136	600	1870
12	17	0	0	0	0
13	17	0	0	0	0
13	17	104	136	650	1870
13	17	0	0	0	0
14	17	112	136	700	1870
14	17	0	0	0	0
15	17	0	0	0	0
15	16	120	128	750	1870
16	16	128	128	800	1870

NUMBER OF MODULES per sextant:

64

TOTAL PER SEXTANT

1950

878

1072

TOTAL NUMBER OF MODULES

384

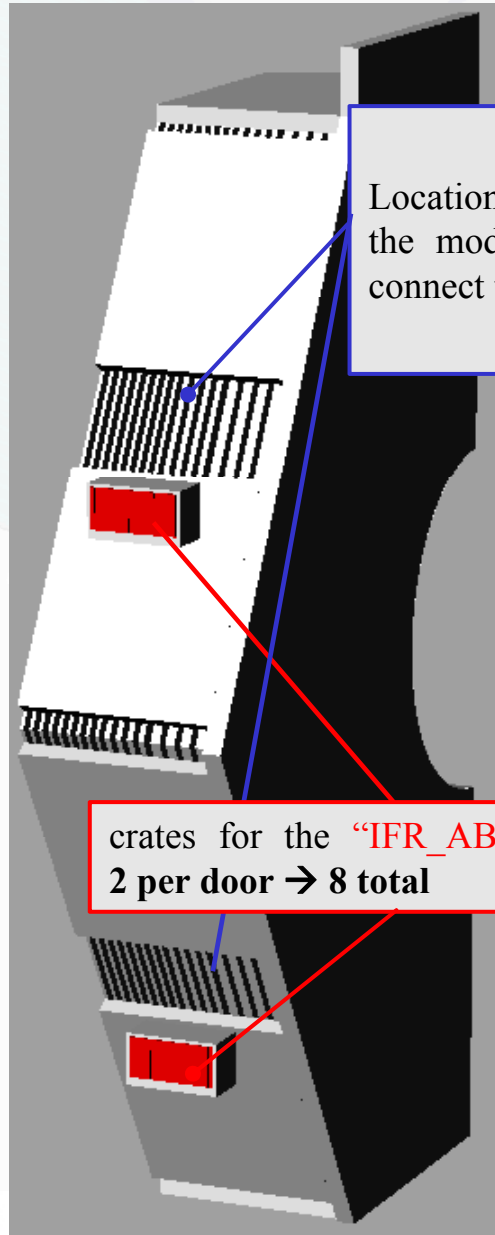
TOTAL CHANNELS PER BARREL

11700

5268

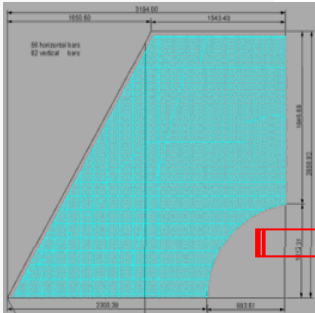
6432

features of the current baseline IFR detector design with "binary mode" readout: endcaps

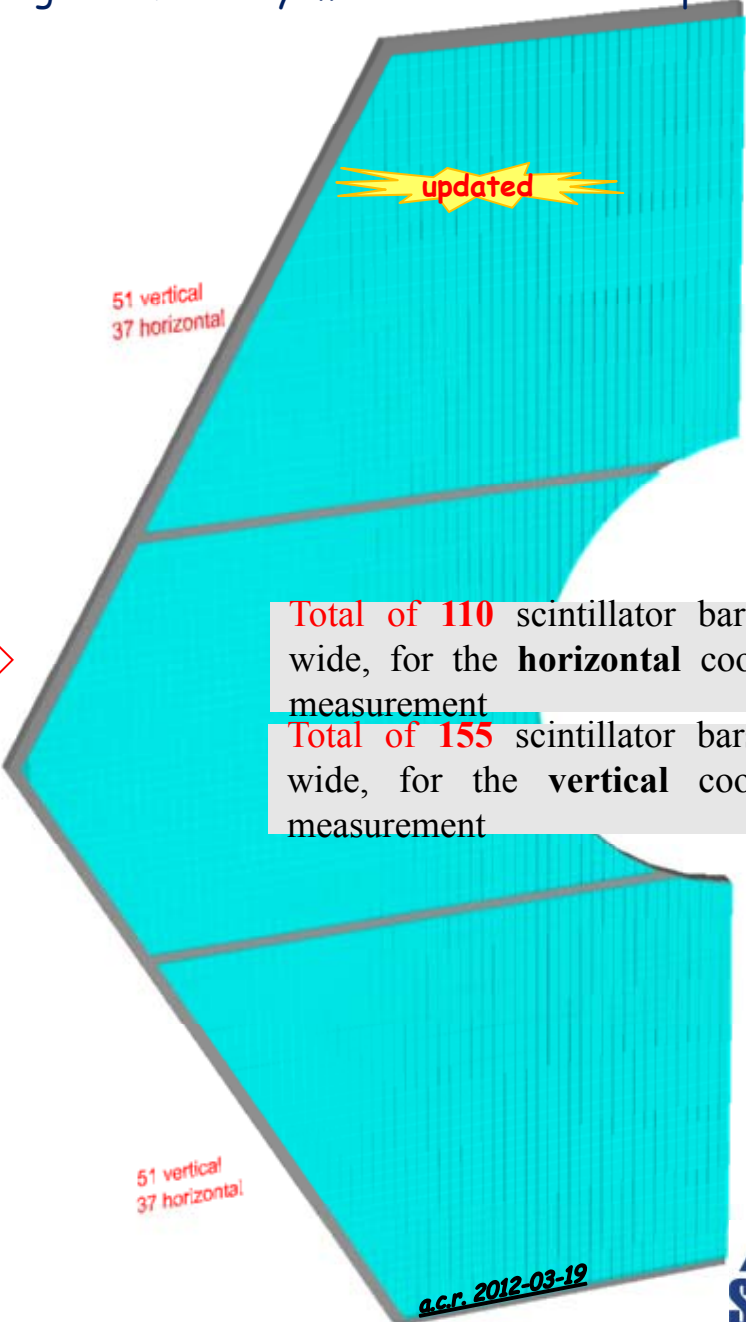


Locations at which the cables from the modules can exit the iron and connect to the "IFR_ABCD".

crates for the "IFR_ABCD" cards:
2 per door → 8 total



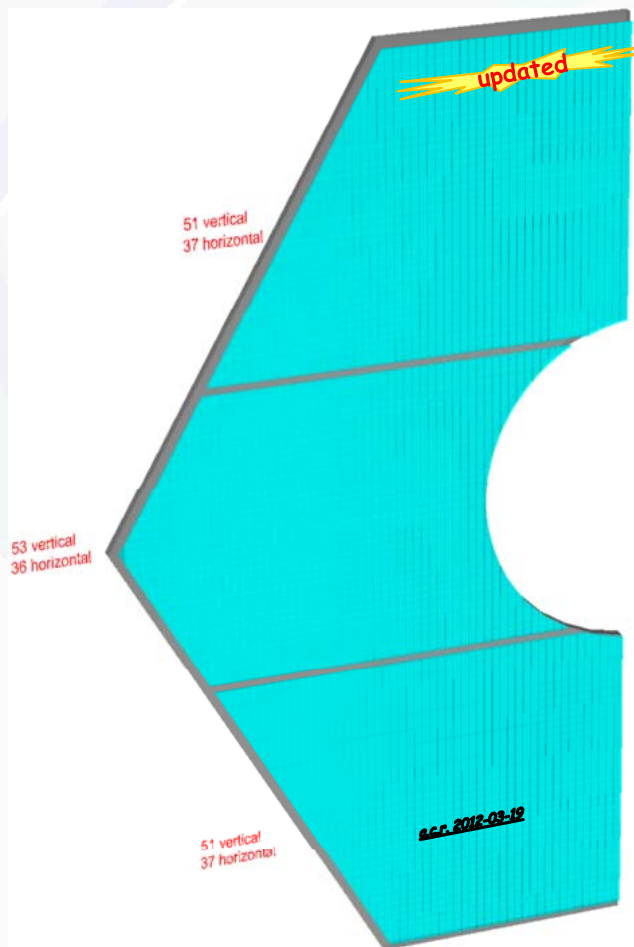
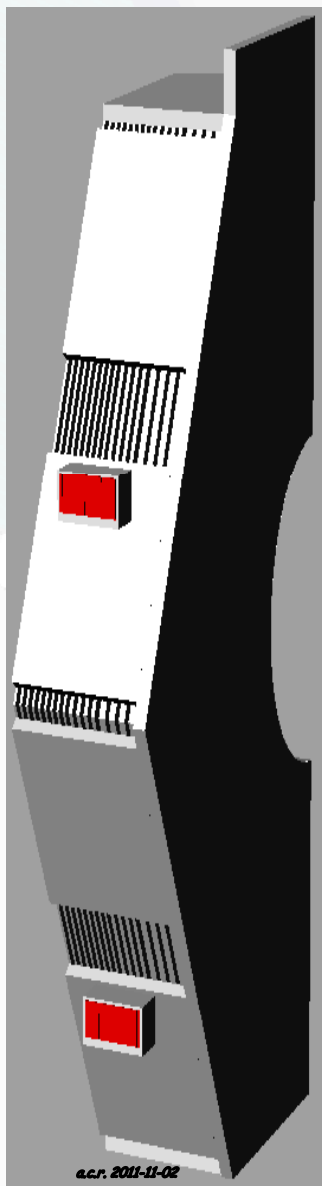
53 vertical
36 horizontal



Total of **110** scintillator bars, **5cm** wide, for the **horizontal** coordinate measurement
Total of **155** scintillator bars, **5cm** wide, for the **vertical** coordinate measurement

a.c.r. 2012-03-19

channel number estimation: endcaps



ENDCAP

top	horizontal bars per module:	37
section	vertical bars per module:	51
center	horizontal bars per module:	36
section	vertical bars per module:	53
bottom	horizontal bars per module:	37
section	vertical bars per module:	51
AVERAGE	channel count per module:	88,4
NO_OF_MOD_PER_LAYER_EC:		3
	horizontal bars per layer	110
	vertical bars per layer	155
	NUMBER OF LAYER PER DOOR	9
	NUMBER OF DOORS IN ENDCAPS	4
		+50%
TOTAL NUMBER OF MODULES IN ENDCAPS:		108
	horizontal bars per door:	990
	vertical bars per door:	1395
	TOTAL HORIZONTAL BARS:	3960
	TOTAL VERTICAL BARS:	5580
TOTAL CHANNELS IN ENDCAPS:		9540
		+12.3%

Increment relative to the numbers presented at the nov16/17 ETD meeting at CERN

data rate / data link count estimation: at nominal conditions (trigger rate 150KHz)

BARREL			
NUMBER OF CRATES PER SEXTANT	2	NUMBER OF CHANNELS PER CRATE	999
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNEL PER BOARD	83,25
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	2	NUMBER OF 32-CHANNEL PROCESSING UNITS	3
TRIGGER RATE (kHz)		150	
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)		150	
n: NUMBER OF SAMPLES PER TRIGGER		8	
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (MOD32)	10		
EVENT SIZE IN BYTES PER EACH MOD32 UNIT	40	TOTAL NUMBER OF MOD32 UNITS	432
		BARREL EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL MOD32 UNITS)	17280
TOTAL BARREL BANDWIDTH (MB/s)	2592	TOTAL BARREL BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	25,92
TOTAL NUMBER OF DATA LINK		bandwidth per link (Gbps)	
24		1,08	

ENDCAP			
NUMBER OF CRATES PER DOOR	2	NUMBER OF CHANNELS PER CRATE	1192,5
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNELS PER BOARD	99,375
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	2	NUMBER OF 32-CHANNEL PROCESSING UNITS (MOD32) PER BOARD	4
TRIGGER RATE (kHz)		150	
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)		150	
n: NUMBER OF SAMPLES PER TRIGGER		8	
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (MOD32)	10		
EVENT SIZE IN BYTES PER EACH MOD32 UNIT	40	TOTAL NUMBER OF MOD32 UNITS	384
		ENDCAP EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL MOD32 UNITS)	15360
TOTAL ENDCAP BANDWIDTH (MB/s)	2304	TOTAL ENDCAP BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	23,04
TOTAL NUMBER OF DATA LINK		bandwidth per link (Gbps)	
16		1,44	

updated

+33% due to modularity of data processing units

data rate / data link count estimation: at higher luminosity (trigger rate 500KHz)

BARREL			
NUMBER OF CRATES PER SEXTANT	2	NUMBER OF CHANNELS PER CRATE	999
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNEL PER BOARD	83,25
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	4	NUMBER OF 32-CHANNEL PROCESSING UNITS	3
TRIGGER RATE (kHz)		500	
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n: NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (MOD32)	10		
EVENT SIZE IN BYTES PER EACH MOD32 UNIT	40	TOTAL NUMBER OF MOD32 UNITS	432
		BARREL EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL MOD32 UNITS)	17280
TOTAL BARREL BANDWIDTH (MB/s)	8640	TOTAL BARREL BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	86,4
		TOTAL ENDCAP BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	76,8
TOTAL NUMBER OF DATA LINK	48	bandwidth per link (Gbps)	1,8

ENDCAP			
NUMBER OF CRATES PER DOOR	2	NUMBER OF CHANNELS PER CRATE	1192,5
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNELS PER BOARD	99,375
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	4	NUMBER OF 32-CHANNEL PROCESSING UNITS (MOD32) PER BOARD	4
TRIGGER RATE (kHz)		500	
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n: NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (MOD32)	10		
EVENT SIZE IN BYTES PER EACH MOD32 UNIT	40	TOTAL NUMBER OF MOD32 UNITS	384
		ENDCAP EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL MOD32 UNITS)	15360
TOTAL ENDCAP BANDWIDTH (MB/s)	7680	TOTAL ENDCAP BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	76,8
		TOTAL ENDCAP BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	76,8
TOTAL NUMBER OF DATA LINK	32	bandwidth per link (Gbps)	2,4

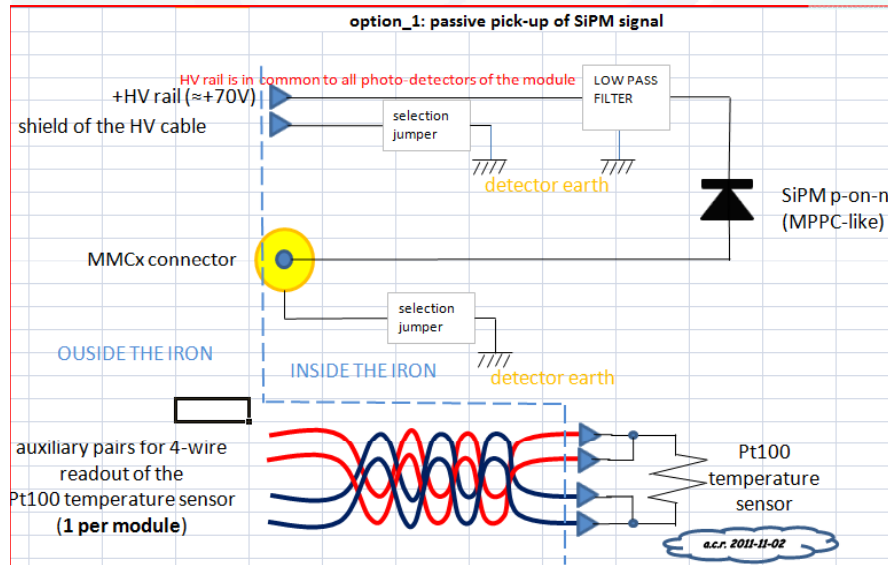
updated

+33% due to modularity of data processing units

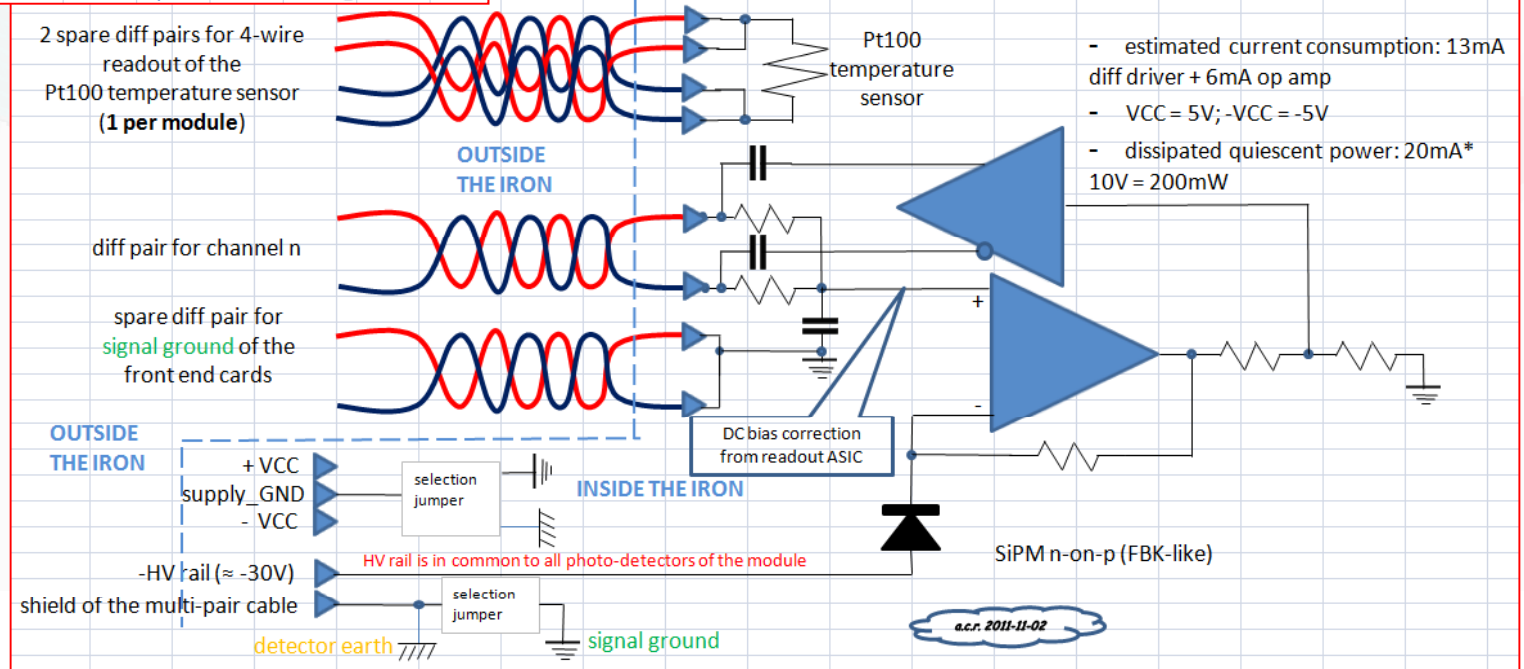
features of the current baseline for the IFR detector design with "binary mode" readout :

Presented at the nov16/17 ETD meeting at CERN

Single Ended vs active Differential options for "picking-up" the signals from SiPM

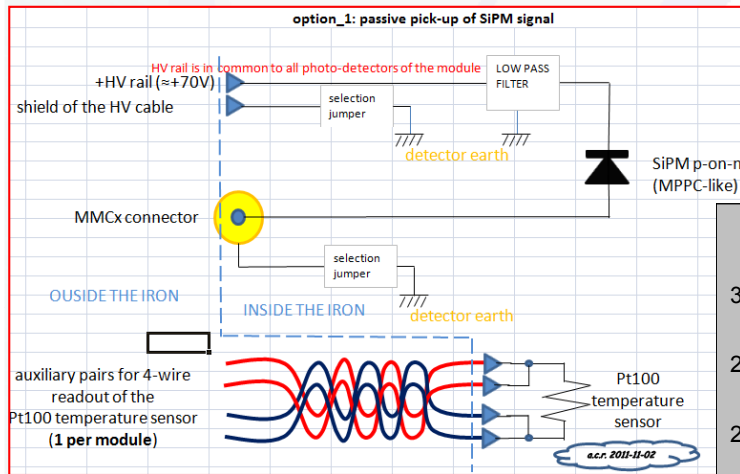


on_2: active pick-up of SiPM signal

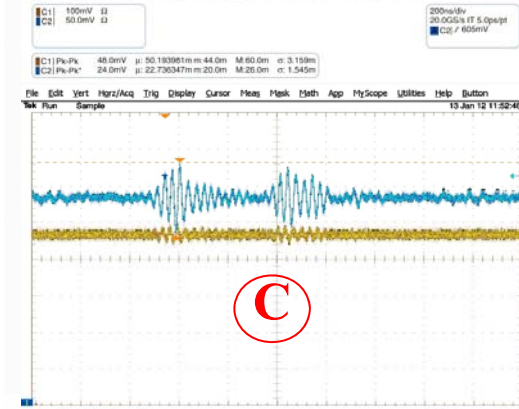
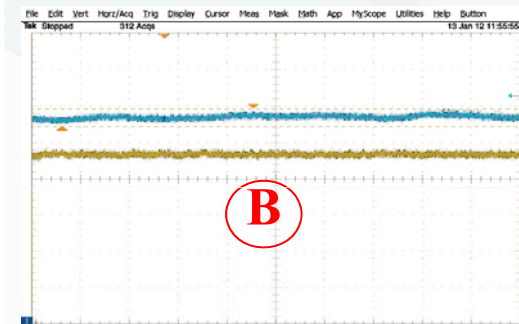
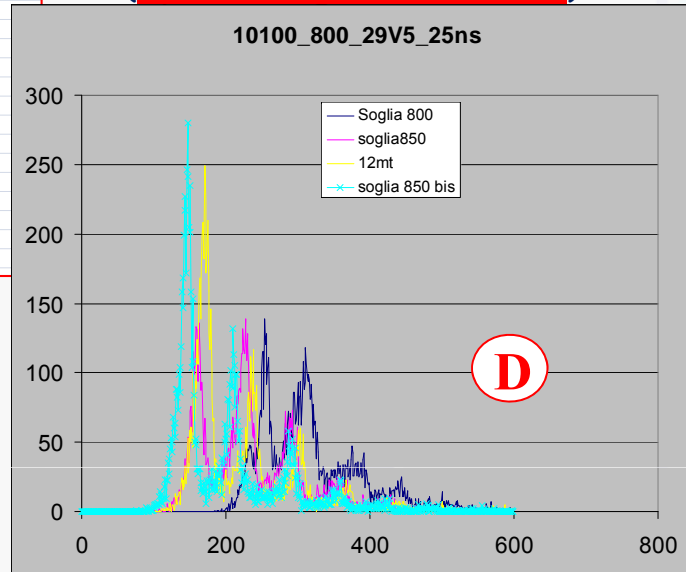


features of the current baseline for the IFR detector design with "binary mode" readout :

USPR GUIDE



Test of Single Ended option for "picking-up" the signals from SiPM (by R. Malaquti, INFN-FE)



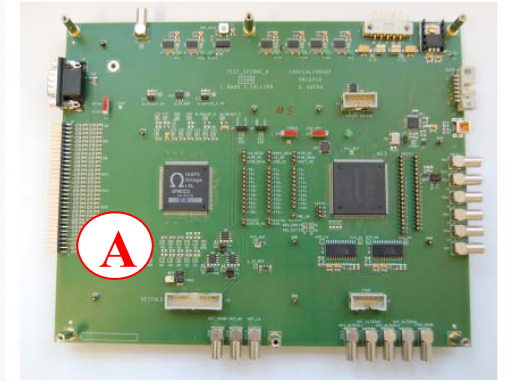
EASIROC SOFTWARE & TEST BOARD USER GUIDE

Version: 11 April 2011

Abstract

EASIROC (previously SPIROCO), standing for *Extended Analogue Silicon pm Integrated Read Out Chip*, is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors.

This guide explains how to install & use the test board for EASIROC and how to operate with the associated software.



Orsay MicroElectronics Group Associated

The test was carried out by connecting a SensL 10100_800 SiPM (biased at 29,5V) to the EASIROC (A) development board and looking at the amplitude histogram of the dark current pulses. The yellow histogram refers to the case in which the SiPM was connected via a 12m long coaxial cable. THERE IS LITTLE DIFFERENCE WITH THE HISTOGRAM OBTAINED WITH A 0.25m LONG CABLE

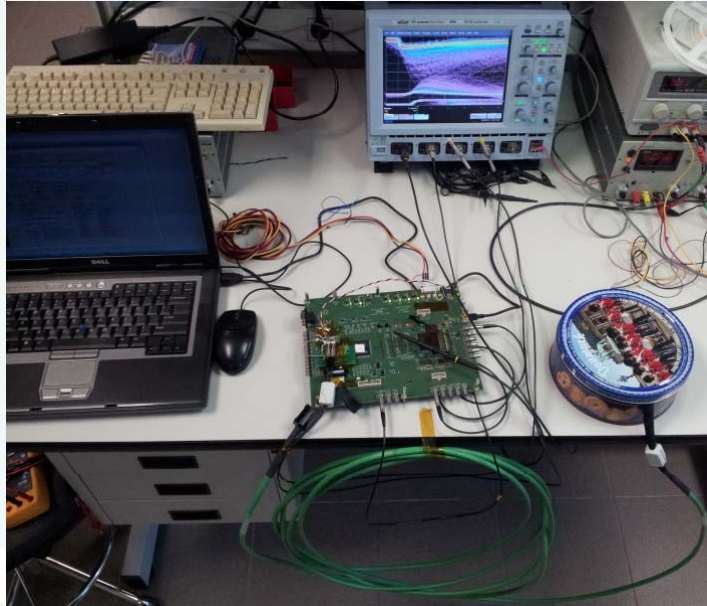
The waveforms (B) shows the outputs of the LOW_GAIN stage (BLUE trace) and of the fast shaper (LIGHT BROWN trace) with the SensL connected with a 0,25m long cable and UNBIASED.

The waveforms (C) shows the outputs of the LOW_GAIN stage (BLUE trace) and of the fast shaper (LIGHT BROWN trace) with the SensL connected with the 12m long cable and UNBIASED. While there is certainly EMI noise pick up this didn't seem to affect the overall outcome of the test.

CAVEAT: only one channel was connected -> pick-up noise might increase with the number of channels connected

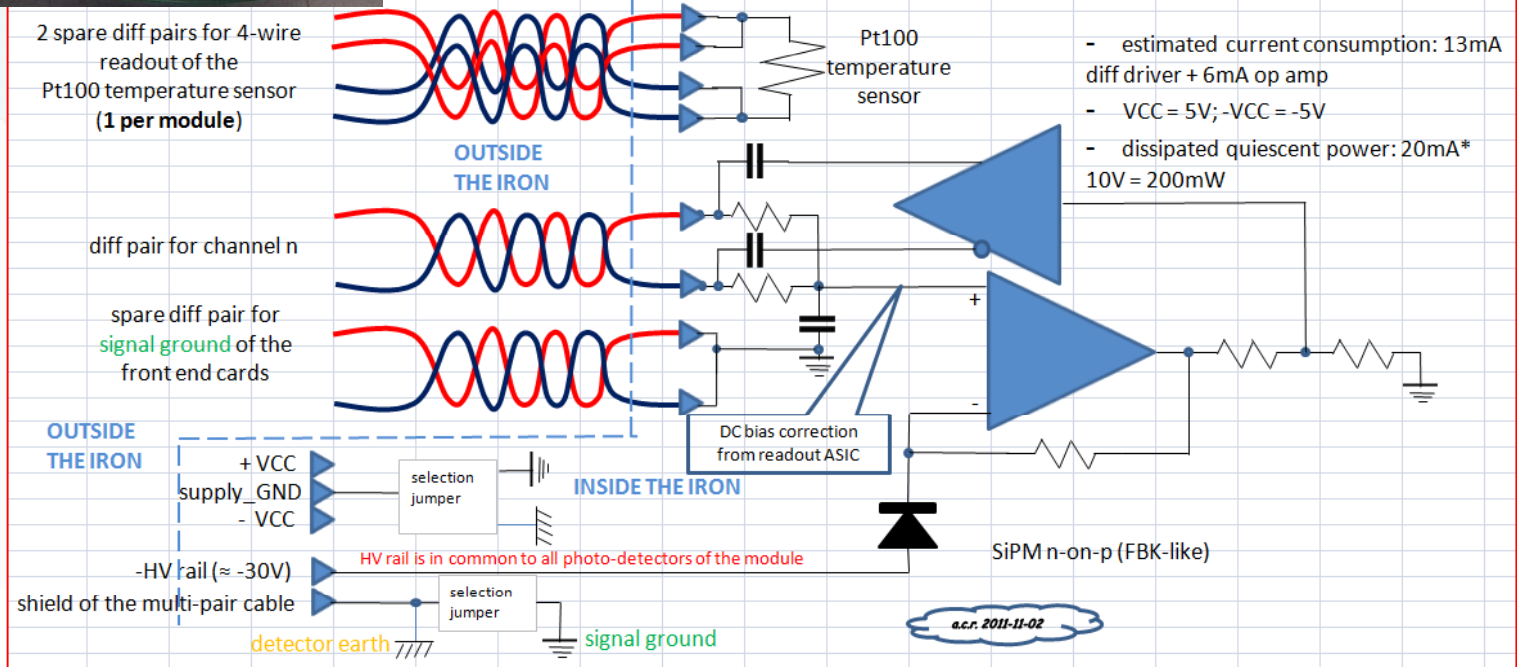


features of the current baseline for the IFR detector design with "binary mode" readout :



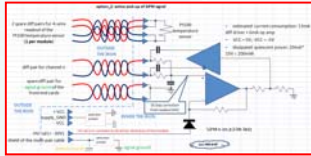
Test of active differential option for "picking-up" the signals from SiPM
(by A.C.R., INFN-FE)

option_2: active pick-up of SiPM signal

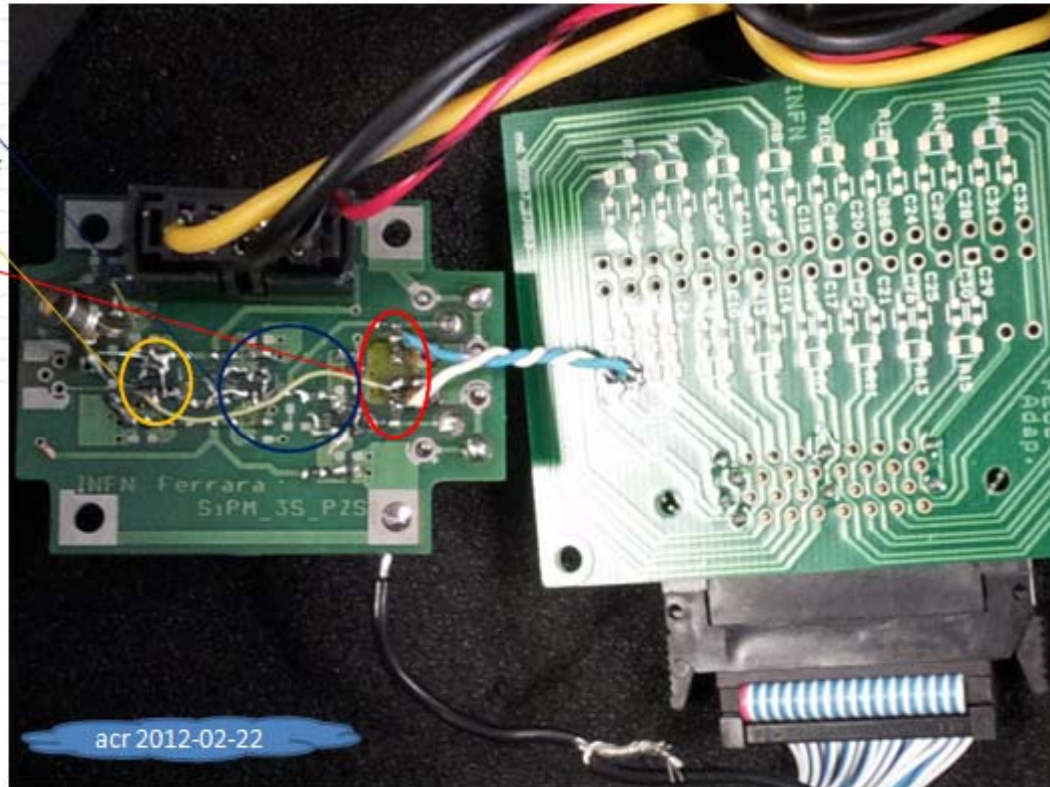
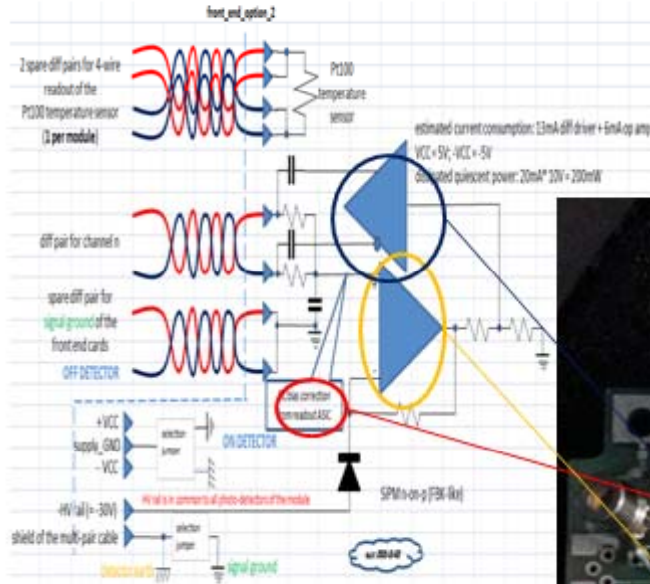


features of the current baseline for the IFR detector design with "binary mode" readout :

Test of active differential option for "picking-up" the signals from SiPM (by A.C.R., INFN-FE)



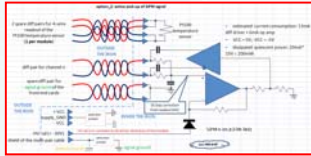
buffer/adattatore di polarita' per SiPM:
trasmettitore differenziale con recupero del livello in DC di modo comune



Angelo Cotta Ramusino INFN-Ferrara Feb 21 2012

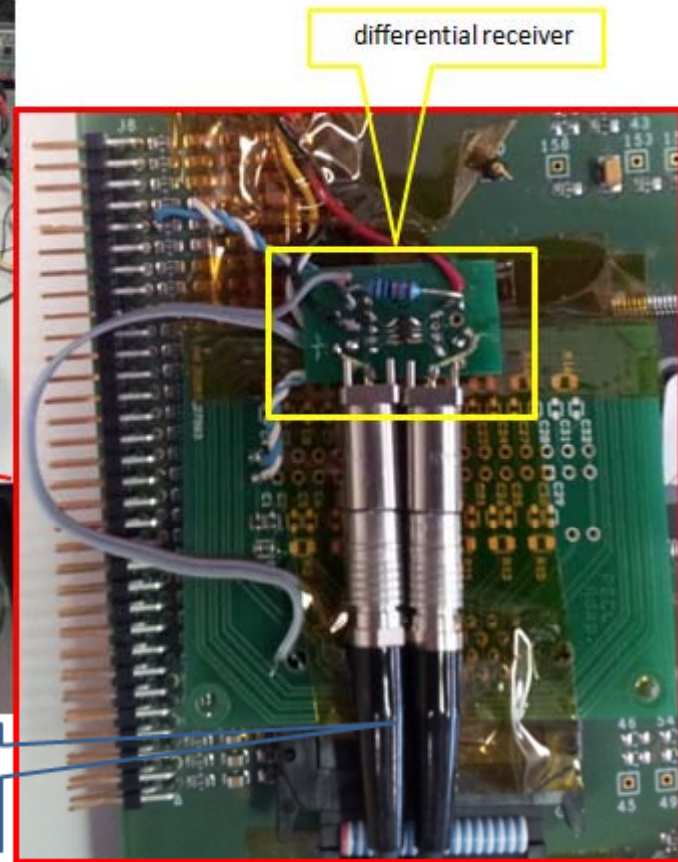
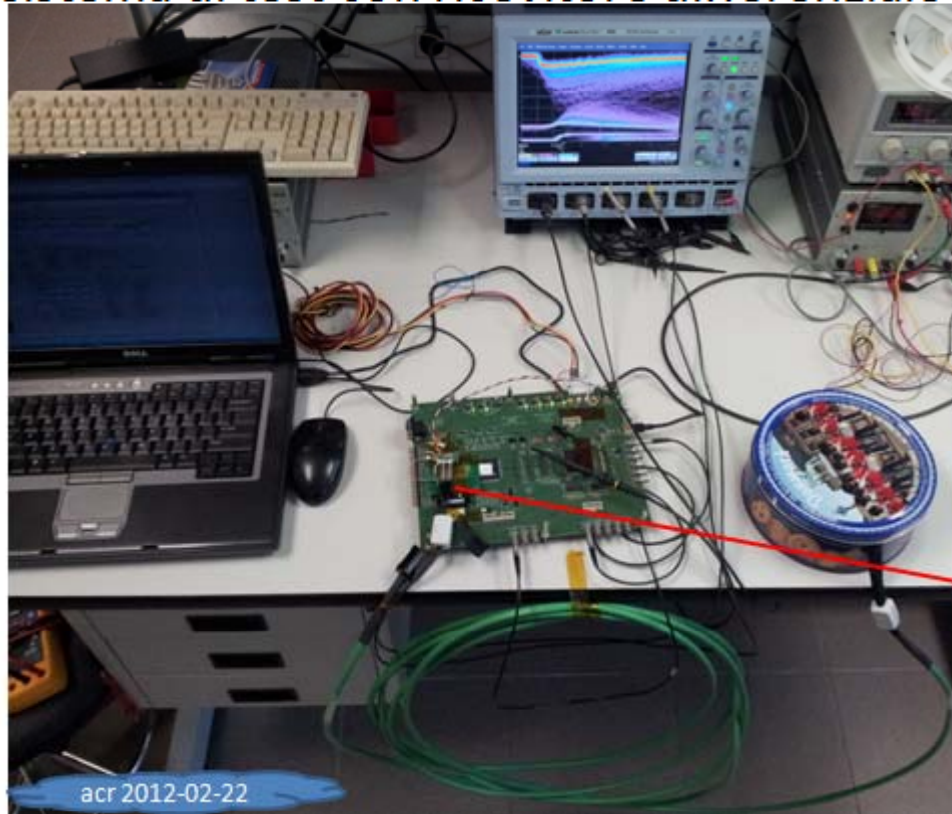
features of the current baseline for the IFR detector design with "binary mode" readout :

Test of active differential option for "picking-up" the signals from SiPM (by A.C.R., INFN-FE)



buffer/adattatore di polarita' per SiPM:

sistema di test con ricevitore differenziale applicato alla scheda EASIROC



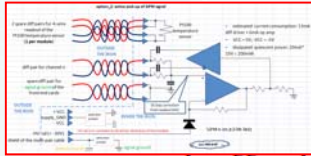
Coaxial LEMO cables connected to scope (AC coupling, ext 50 Ohm termination) for monitoring the differential signals at the input of the receiver

Angelo Cotta Ramusino INFN-Ferrara Feb 21 2012

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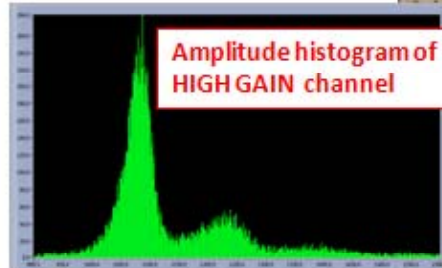
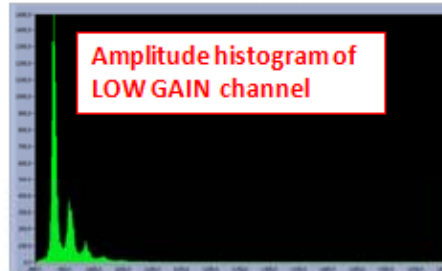
features of the current baseline for the IFR detector design with "binary mode" readout :

Test of active differential option for "picking-up" the signals from SiPM (by A.C.R., INFN-FE)

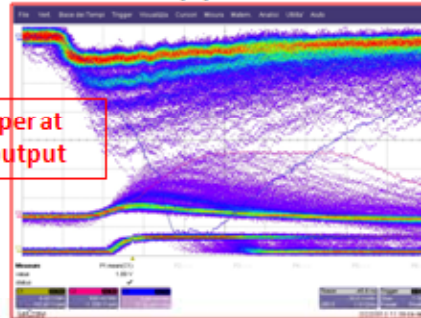


buffer/adattatore di polarita' per SiPM: applicazione alla scheda EASIROC: test results

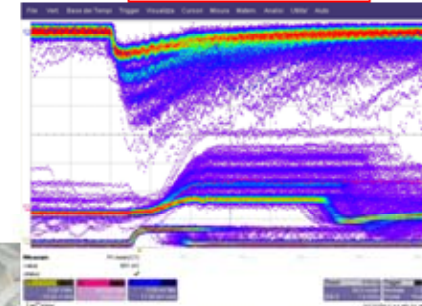
histogramming program
by R. Malauci, May 2011



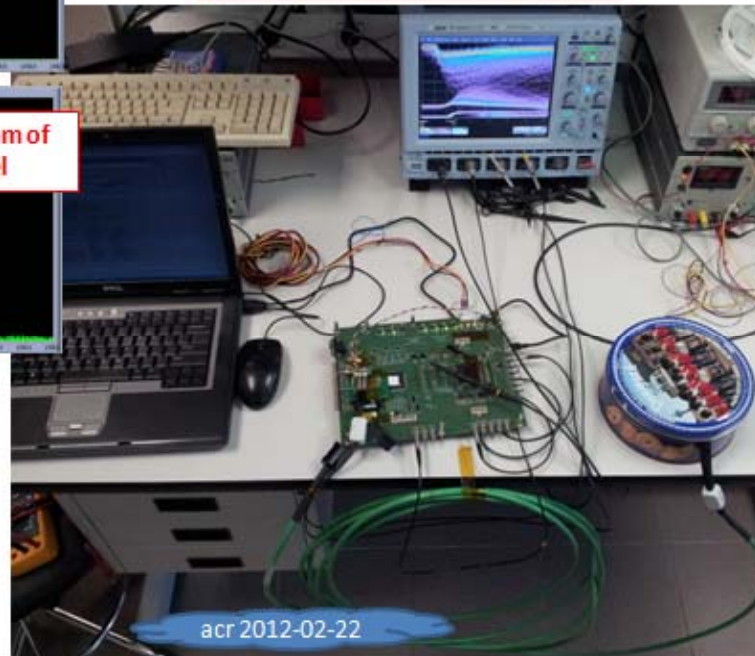
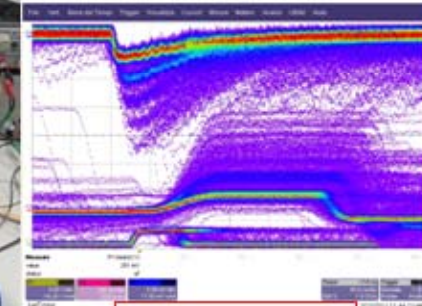
Fast Shaper at
PROBE output



LOW GAIN output
HOLD enabled



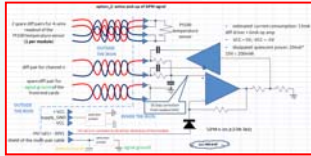
HIGH GAIN output
HOLD enabled



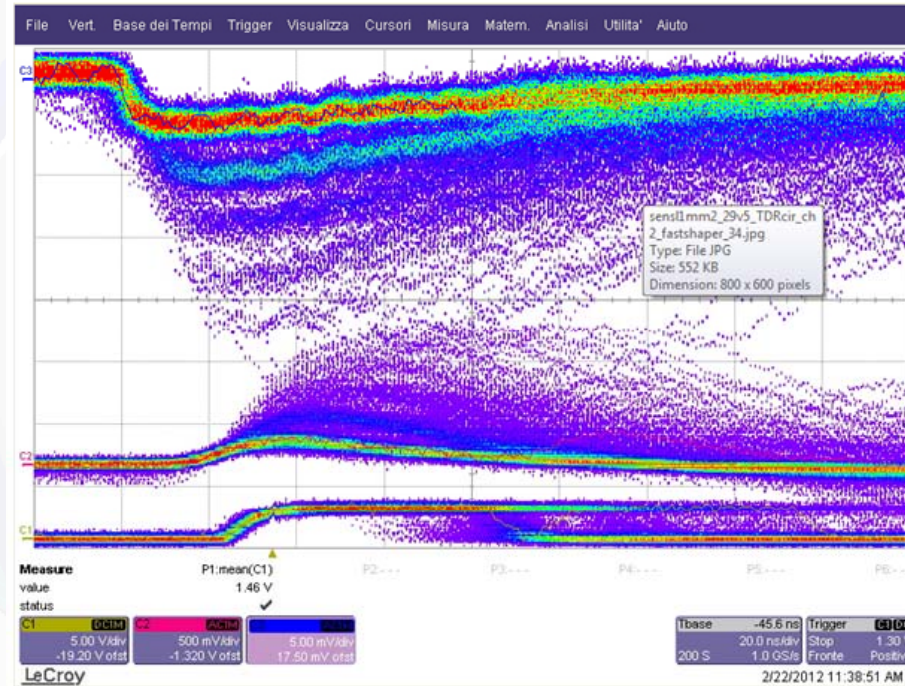
Test results for a reference
system with 8m of shielded
twisted pair cable between
driver and receiver

features of the current baseline for the IFR detector design with "binary mode" readout :

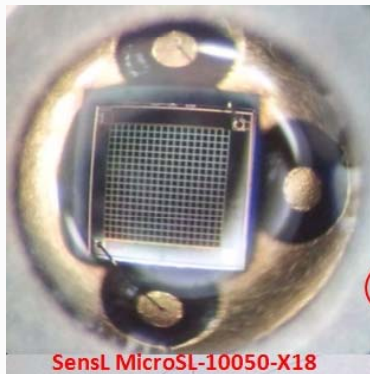
Test of active differential option for "picking-up" the signals from SiPM (by A.C.R., INFN-FE)



buffer/adattatore di polarita' per SiPM: applicazione alla scheda EASIROC: test results qualche forma d'onda



Test results for a reference system with 8m of shielded twisted pair cable between driver and receiver



Angelo Cotta Ramusino INFN-Ferrara Feb 21 2012

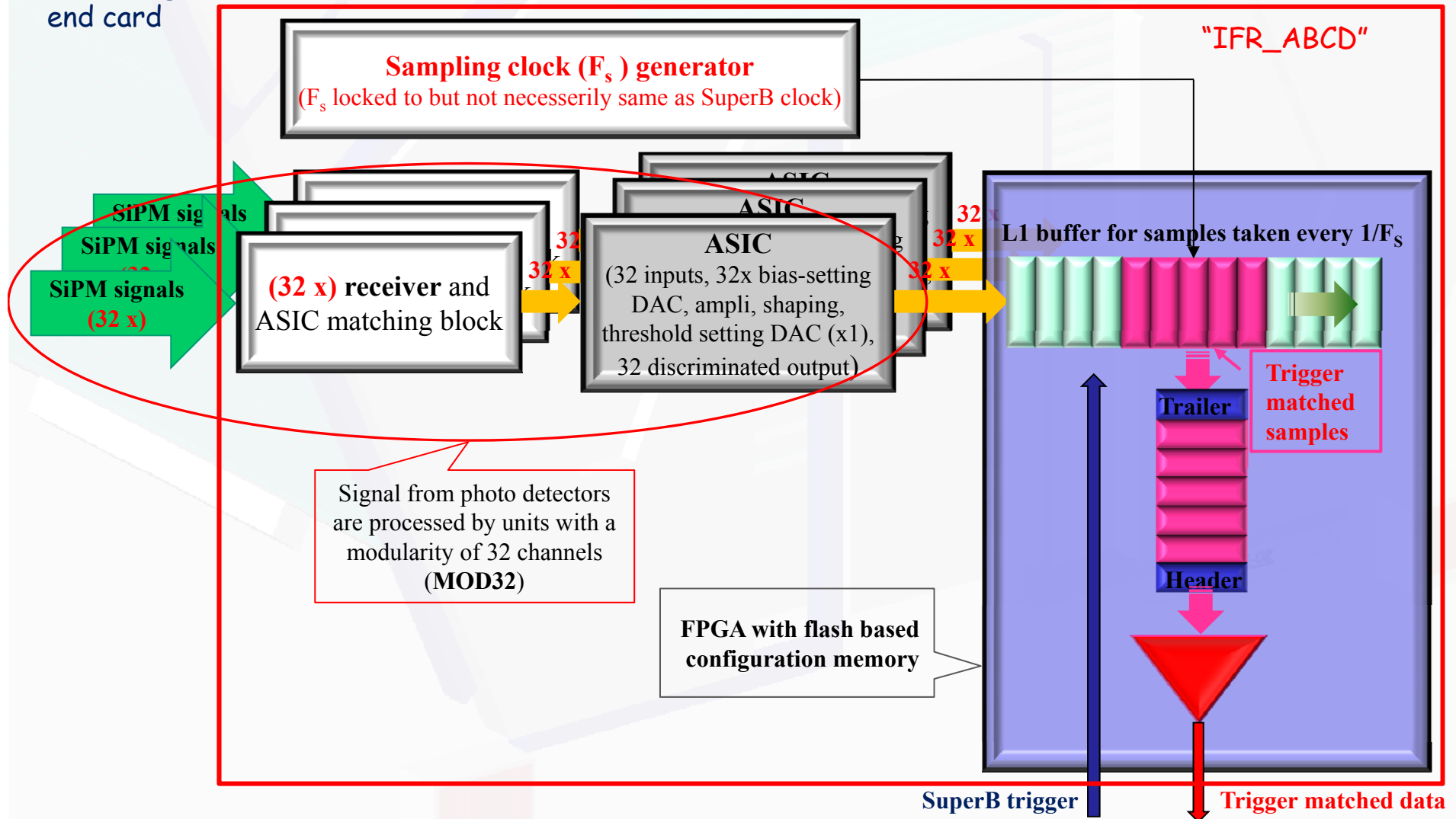
14

The test was carried out by connecting a SensL MicroSL-10050-X18 through the proposed active buffer to the EASIROC development board and looking at the amplitude histogram of the dark current pulses.

Also in this configuration the result is that THERE IS LITTLE DIFFERENCE WITH THE HISTOGRAMS OBTAINED by connecting the SiPM to the EASIROC WITH A 0.25m LONG COAXIAL CABLE

features of the current baseline IFR detector design with "binary mode" readout:
 block diagram of the "IFR_ABCD" front end card

Presented at the nov16/17 ETD meeting at CERN

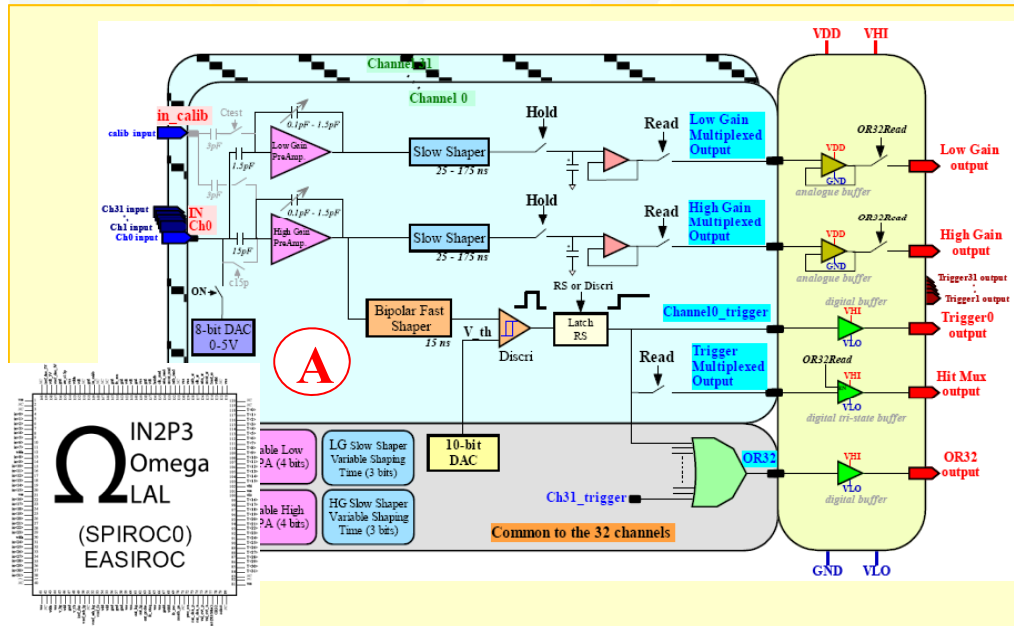


Signal from photo detectors are processed by units with a modularity of 32 channels (MOD32)

FPGA with flash based configuration memory

Two "CONCENTRATOR / DATA LINK DRIVER" cards in the "IFR-ABCD" front end crates are connected to the FCTS and to the ROM: they distribute the trigger to the "IFR_ABCD" cards, collect the matched data, merge the streams into the de-randomizer FIFO and drive the data link (1 or 2 per concentrator) toward the ROMs

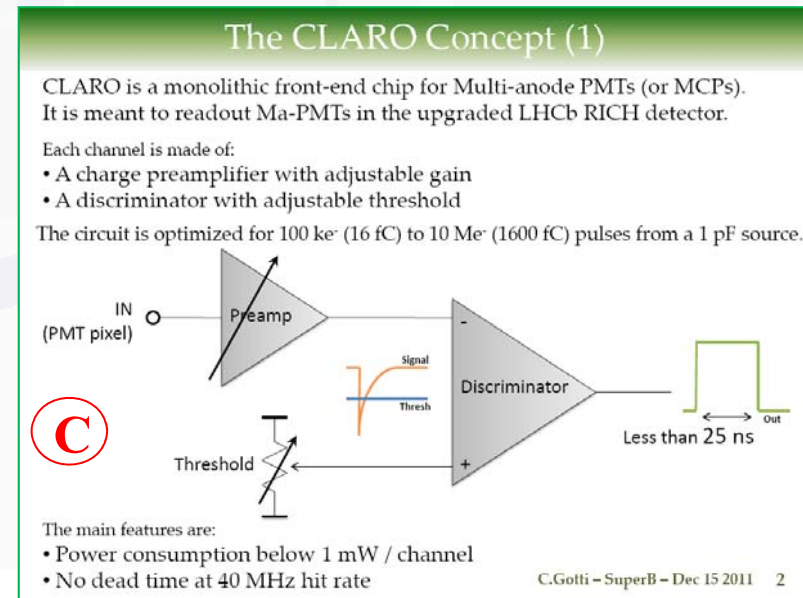
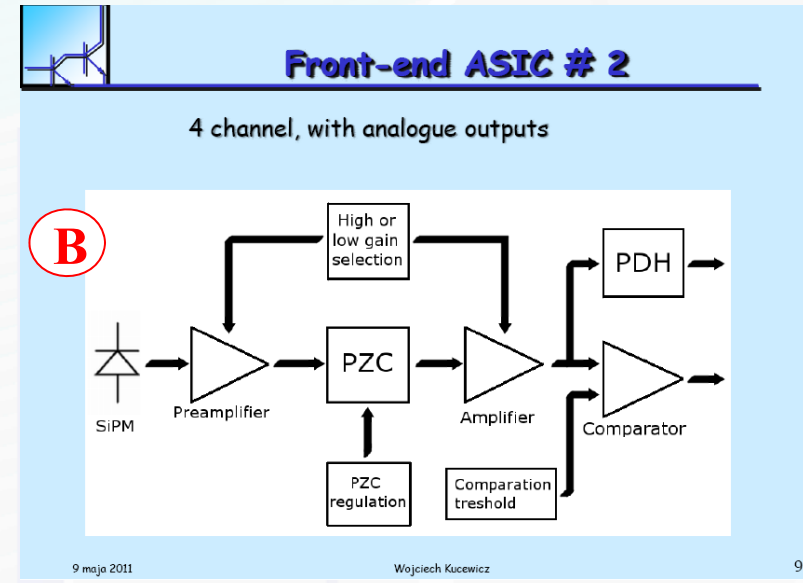
features of the current baseline IFR detector design with "binary mode" readout:
Candidate ASICs at present date



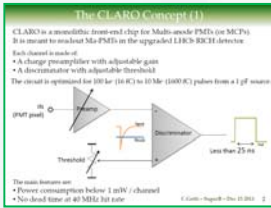
(A) The EASIROC has been designed by the Omega group of LAL and it has been extensively used and tested in Ferrara thanks to evaluation board provided by LAL. It has already described in previous presentations

(B) The RAPSODI ASIC#2 has been designed by Wojciech Kucewicz of AGH University in Cracov Poland. It has already been introduced in previous presentations

(C) The CLARO ASIC has been designed by Gianluigi Pessina and Claudio Gotti and presented at the 2nd SuperB meeting last December.



features of the current baseline IFR detector design with "binary mode" readout: Candidate ASICs at present date

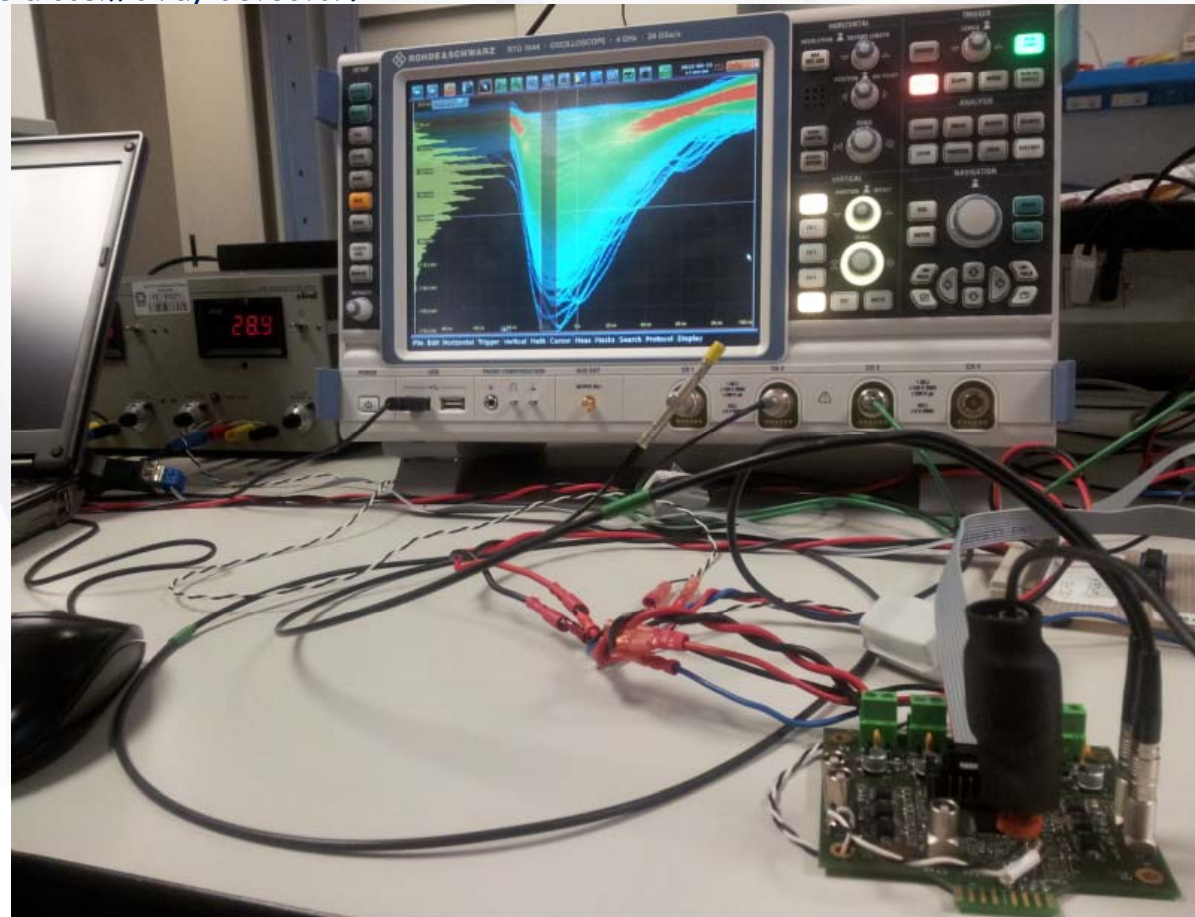


The **CLARO ASIC** has been recently tested in Ferrara on a PCB laid out by R. Malaguti of INFN-Ferrara.

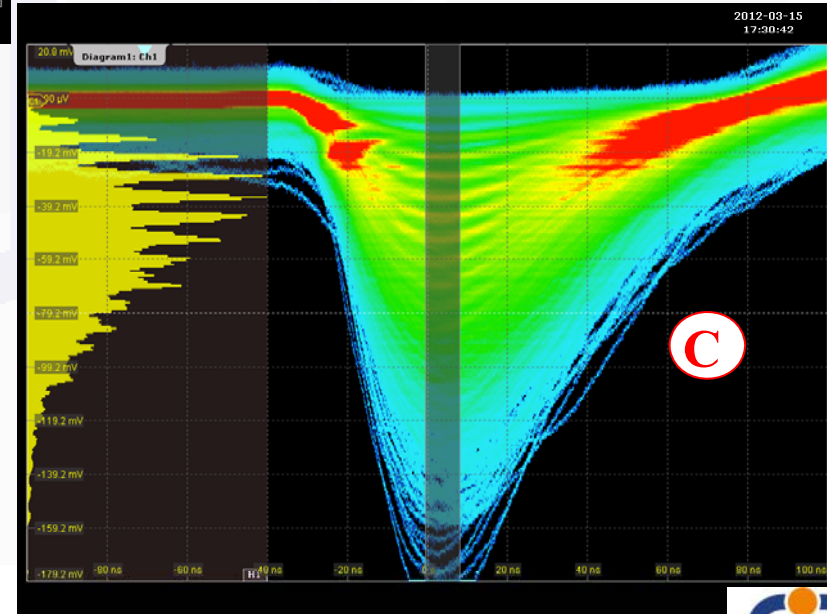
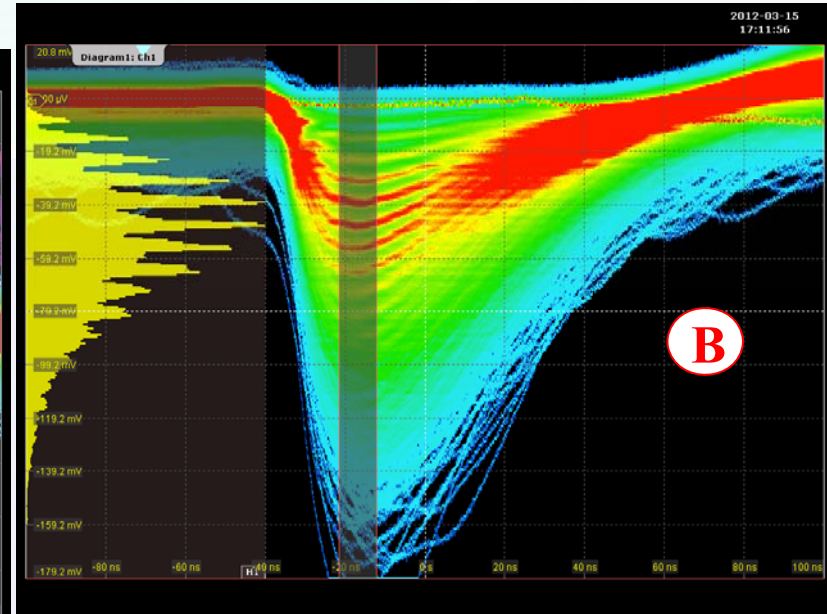
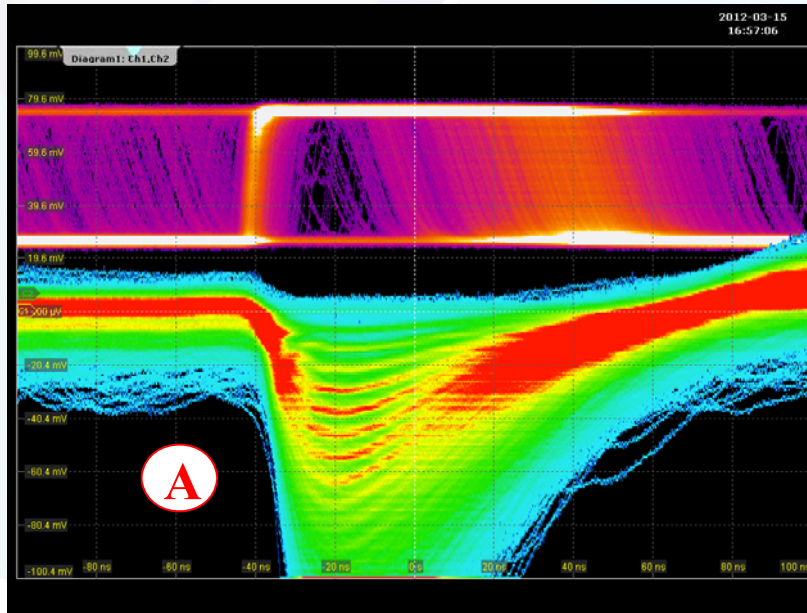
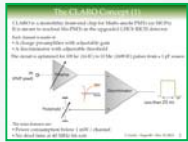
The CLARO was connected to a **SensL MicroSL-10050-X18 1mm²**, directly or through a 1m long coaxial cable. A **SensL MicroSL-30035 9mm²**, was also tested to see the effect of higher input capacitance on the ASIC peaking time and noise performances.

In order to better evaluate the noise performances of the ASIC, a digital scope with a very low noise floor was used (Rohde & Schwarz RTO 1044). The SiPM connected to the ASIC has been first stimulated by photons from a blue LED and then coupled to a scintillator/WLS fiber assembly and operated as a cosmic ray detector.

The details of the tests performed on the **CLARO ASIC** are being presented at this meeting by Claudio Gotti.



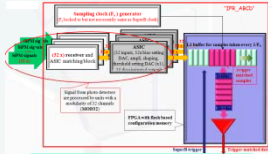
features of the current baseline IFR detector design with "binary mode" readout:
Candidate ASICs at present date



The details of the tests performed on the **CLARO ASIC** are being presented at this meeting by Claudio Gotti.

- (A) The CLARO digital and analog outputs
- (B) The CLARO ASIC is connected to the SiPM directly
- (C) The CLARO ASIC is connected to the SiPM via a 1m long coax cable; the peak is late wrt previous case

features of the current baseline IFR detector design with "binary mode" readout:
specification of a dedicated ASIC for SuperB IFR front end

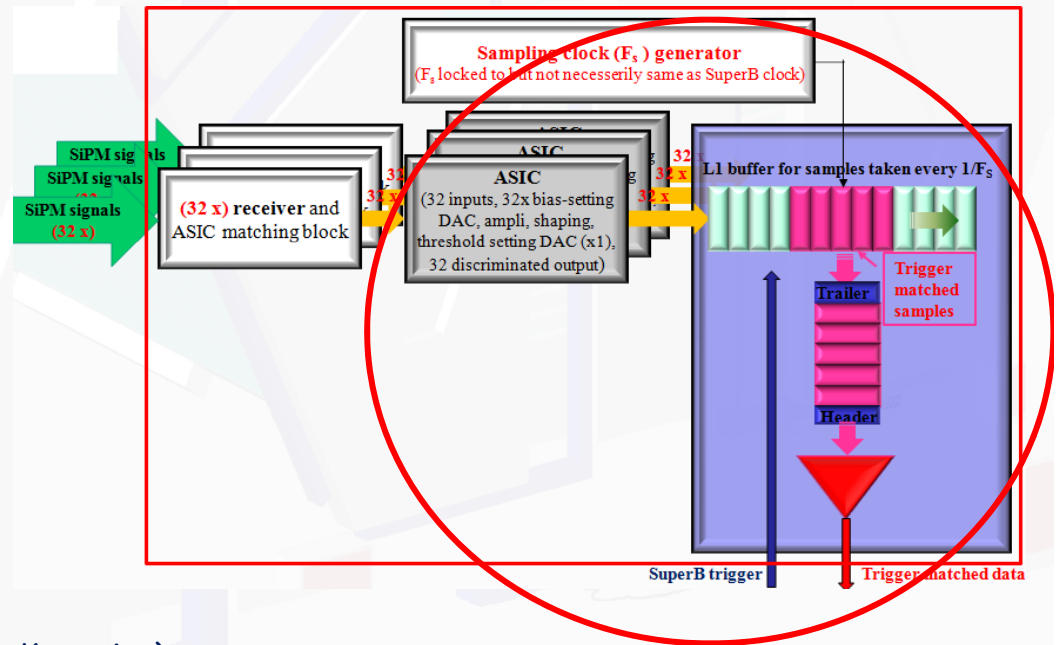


The basic building blocks of the baseline IFR readout system are available.

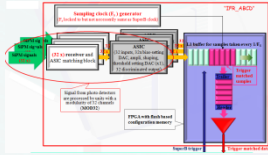
Since new groups with expertise in ASIC design have joined the SuperB collaboration we are considering to develop a new ASIC targeting the SuperB specifications in terms of power dissipation and radiation tolerance.

The new ASIC would be built by the following groups :

- Analog blocks (AB):
 - AGH University in Cracovia, Poland (Wojciech Kucewicz)
 - INFN and Dipartimento di Fisica di Ferrara (Angelo Cotta Ramusino)
 - INFN di Milano-Bicocca (Gianluigi Pessina)
- Digital blocks (DB):
 - INFN and Dipartimento di Fisica di Torino (Simonetta Marcello)



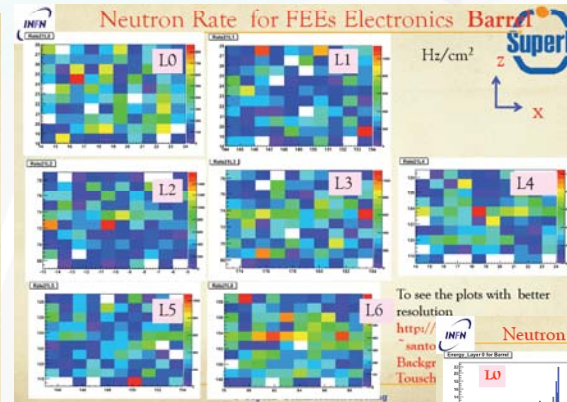
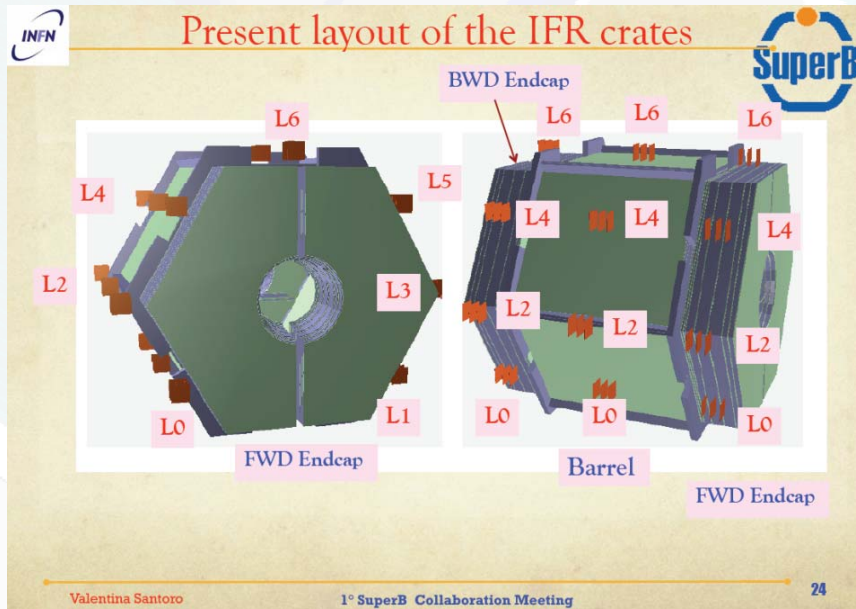
features of the current baseline IFR detector design with "binary mode" readout:
specification of a dedicated ASIC for SuperB IFR front end



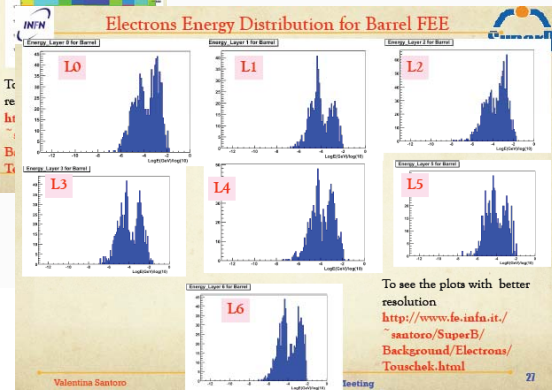
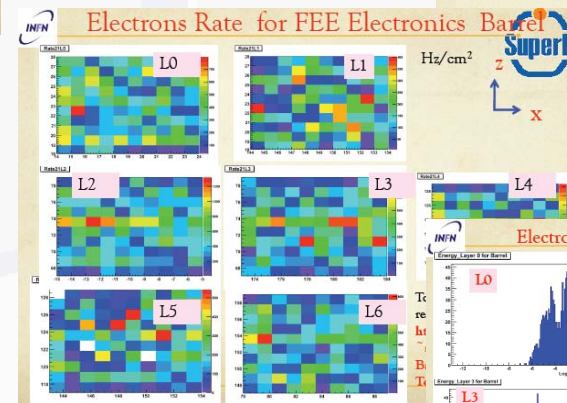
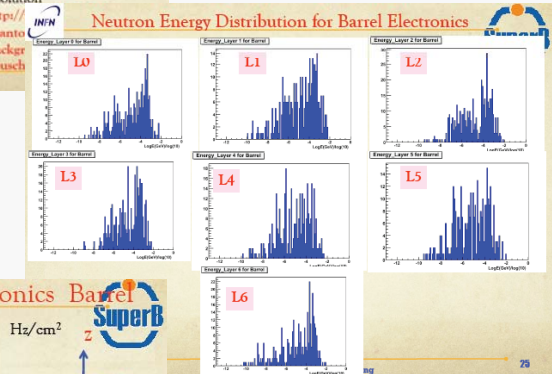
- (AB) input amplifier design suited for positive and negative signals ; linear dynamic range ≈ 100 p.e. equivalent signal
- (AB) a fast shaper design with peaking time in the range of a few ns, to minimize the pulse pile-up effects at high input rates
- (AB) individual bias setting DACs: range of a few Volts; resolution up to 8 bit; external or an internal voltage reference
- (AB) high speed comparator with differential topology to reduce the switching noise
- (AB) one common threshold setting DAC: range of a few Volts; resolution up to 10 bit; external or an internal voltage reference
- (AB) configurable test pulse injection circuitry
- (DB) SEU protected registers for all configurable features of the ASIC
- (DB) SEU protected slow control interface logic
- (AB) auxiliary differential output buffers for diagnostic purposes
- (AB) clock interface unit to generate all internal timing signals from the SuperB clock
- (DB) configurable latency buffer, based on a dual ported memory, holding the data during the trigger decision time
- (DB) trigger interface: to perform the extraction of the data from the proper window of the latency buffer upon the trigger request
- (AB) suitable low power serializers to transmit the trigger match data to the downstream readout stages
- (DB) Trigger primitives generator: a SEU protected configurable look-up table to generate trigger signals from the inputs

addressing the radiation issues: background rates estimation at the location of detectors
Presented at the nov16/17 ETD meeting at CERN

From: "IFR Background Status" Valentina Santoro INFN Ferrara



To see the plots with better resolution
<https://santoro.infn.it/Background/Neutron/Touschek>



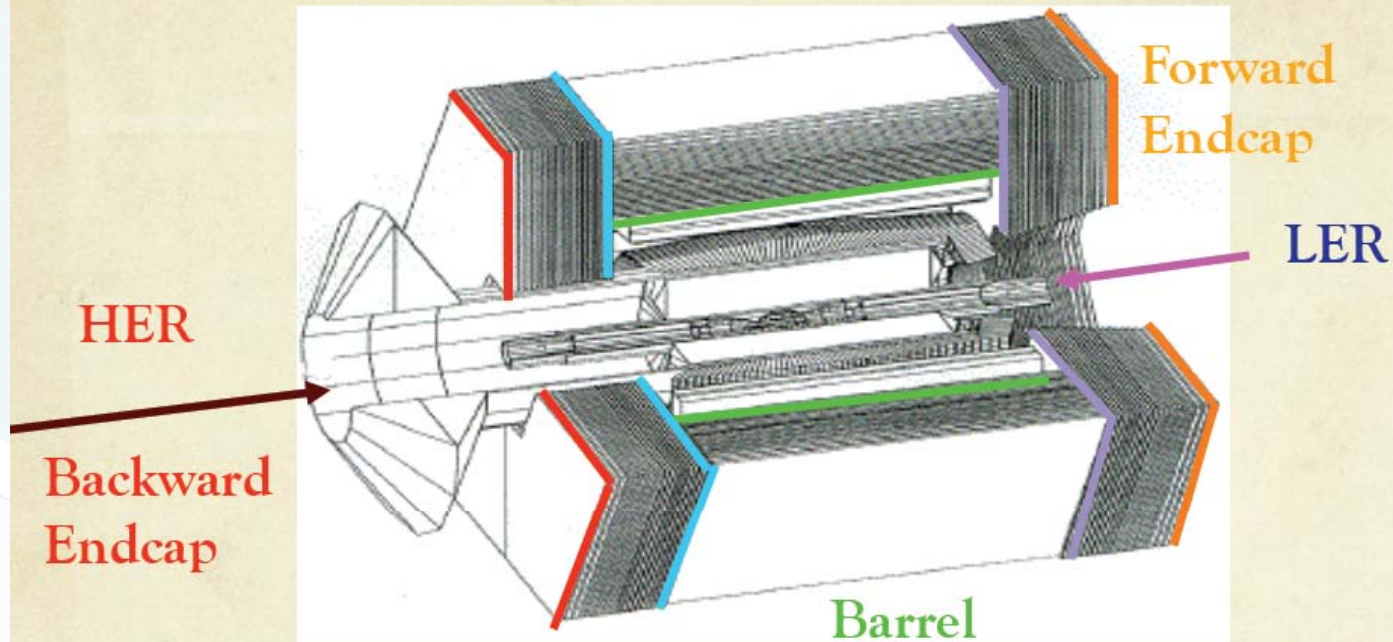
To see the plots with better resolution
<http://www.infn.it/~santoro/SuperB/Background/Electrons/Touschek.html>

Thanks to this work we have now an estimate of the expected radiation doses at the locations of the front end electronics crates, according to the baseline design.

This will allow us to properly plan the irradiation tests of the "compact" front end design based on the EASIROC.

addressing the radiation issues: background rates estimation at the location of detectors

Hot regions



Barrel: innermost layers, mostly neutrons

FWD encaps (hottest region) : inner layers and outer layers (BEAM halo), electron and photons

BWD encaps: inner layers and small radii

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SuperB Background Meeting

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addressing the radiation issues: background rates estimation at the location of detectors

What's new from the Frascati CM Meeting



Frascati

- ✓ Beam Composition for the IFR background
- ✓ Radiative Bhabha Background Studies (neutrons, photons and electron)
- ✓ Touschek background (neutrons, photons and electron)
- ✓ Pair background (neutrons, photons and electron)
- ✓ Background Studies and Absorbed dose on our FEEs

For all the detector rates see

<http://agenda.infn.it/contributionDisplay.py?contribId=132&sessionId=29&confId=4107>

New

- ✓ Proton study
- ✓ FEEs studies improved

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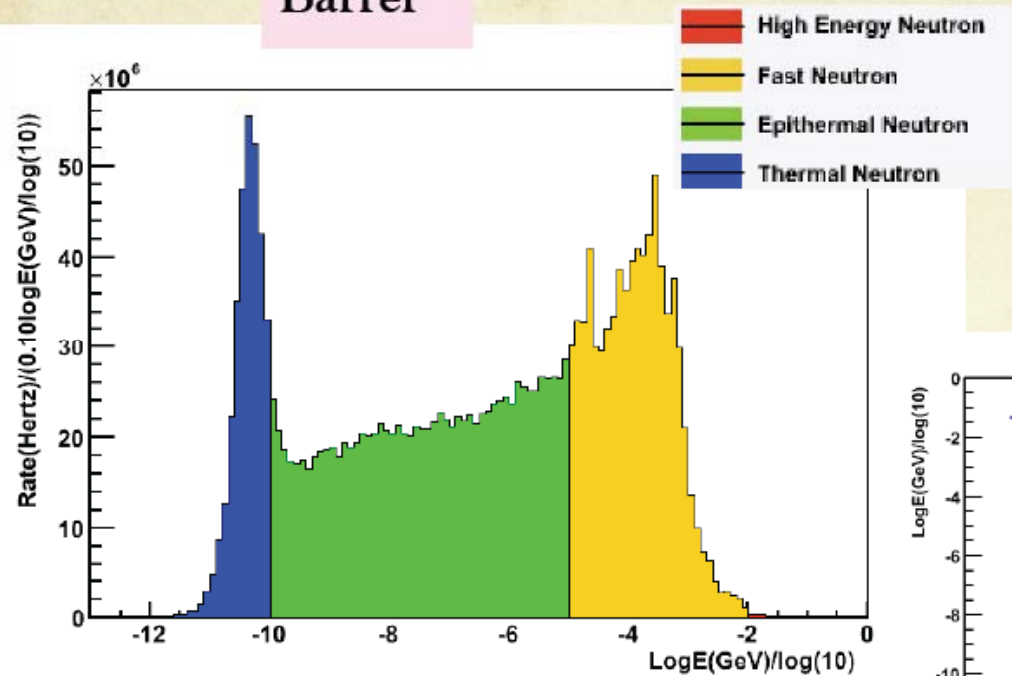
3

addressing the radiation issues: background rates estimation at the location of detectors

Neutron Energy Distributions for Radiativa Bhabha events

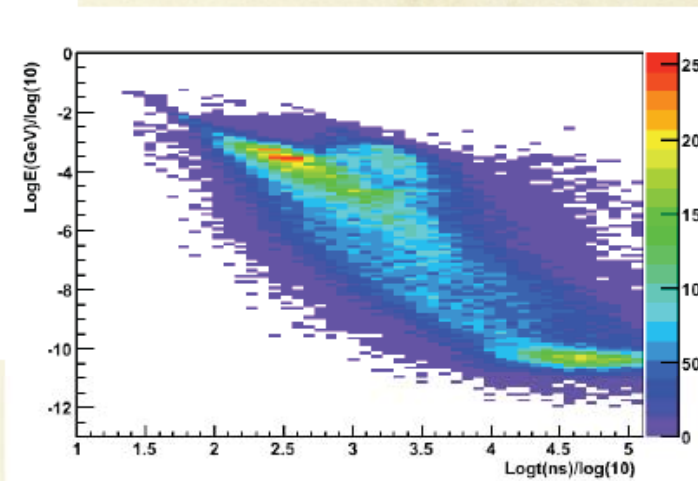


Barrel



Barrel

Energy vs time distributions



Frascati

The Energy distribution for FWD and BWD Endcap are similar

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addressing the radiation issues: background rates estimation at the location of detectors

Neutron Rates

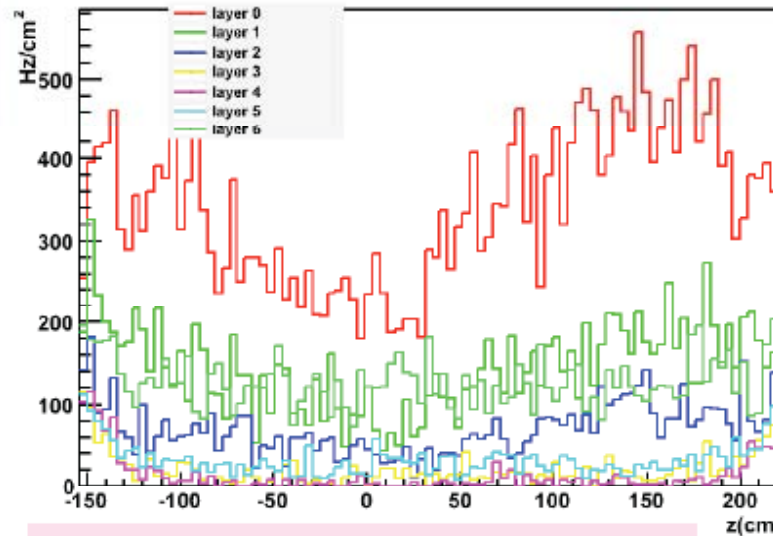


Frascati

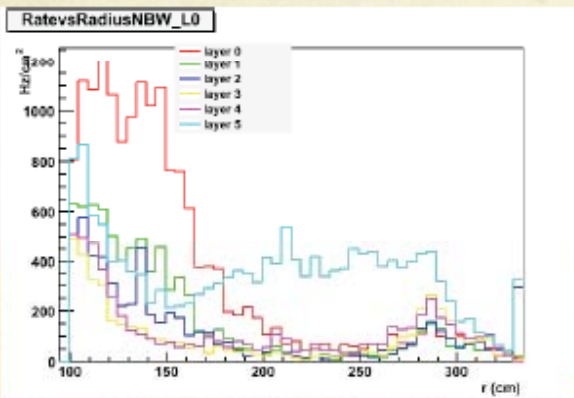
Rate vs Z-coordinate for Barrel

Rate of 450 Hz/cm^2 - \rightarrow about 3×10^9 neutrons/cm² for a year

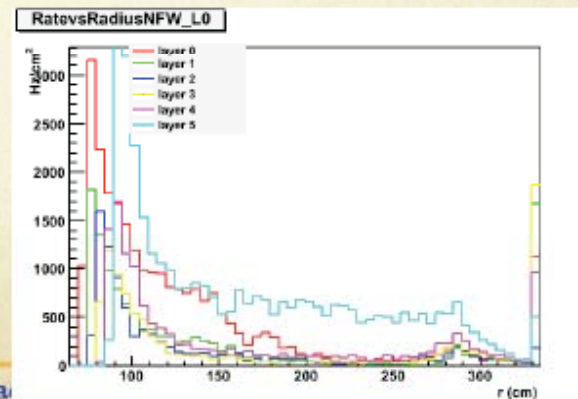
All the rate are normalized to 1MeV energy



Rate vs radius for BWD Endcap



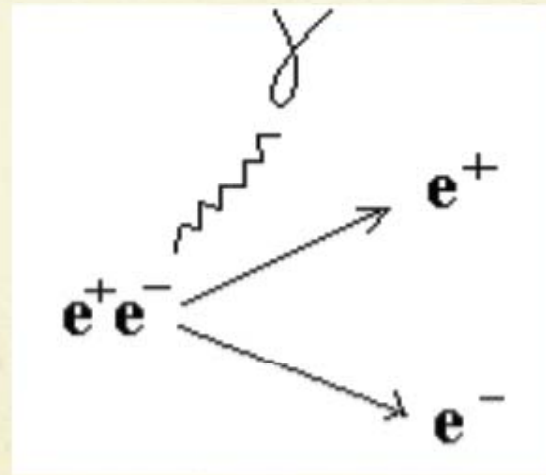
Rate vs radius for FWD Endcap



SuperB Ba

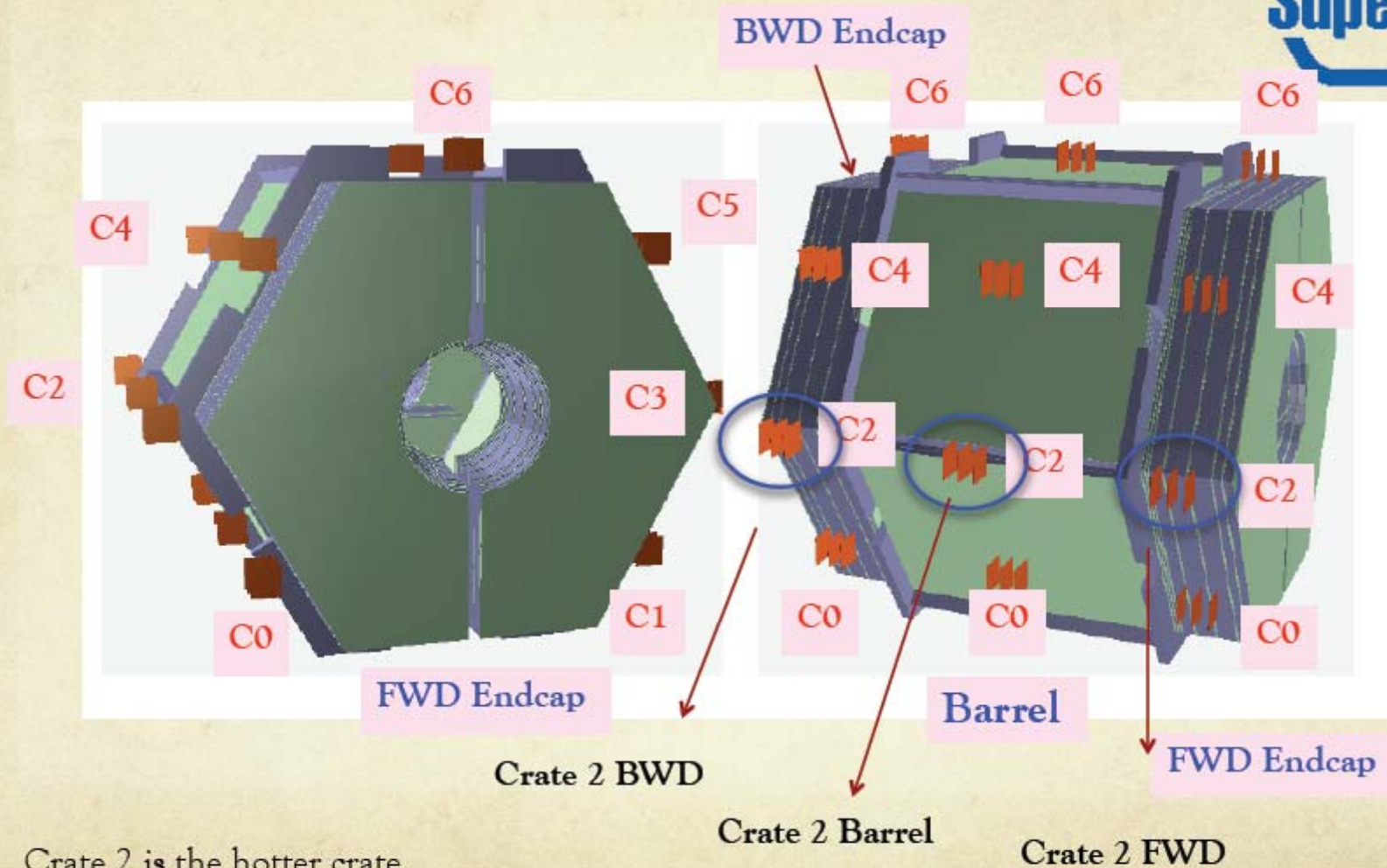


Radiative Bhabha background crossing the IFR FEE boards



addressing the radiation issues: background rates estimation at the location of IFR front end electronics

Present layout of the IFR crates



Crate 2 is the hotter crate

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Neutron Rates for FEEs Electronics

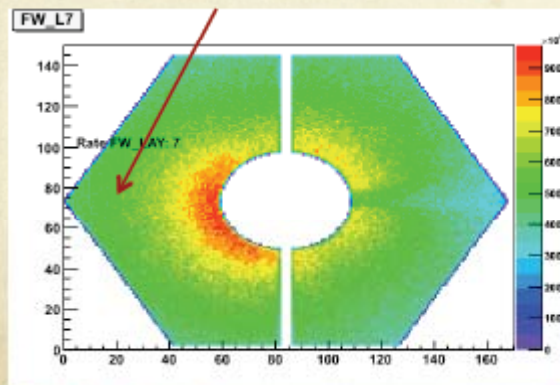
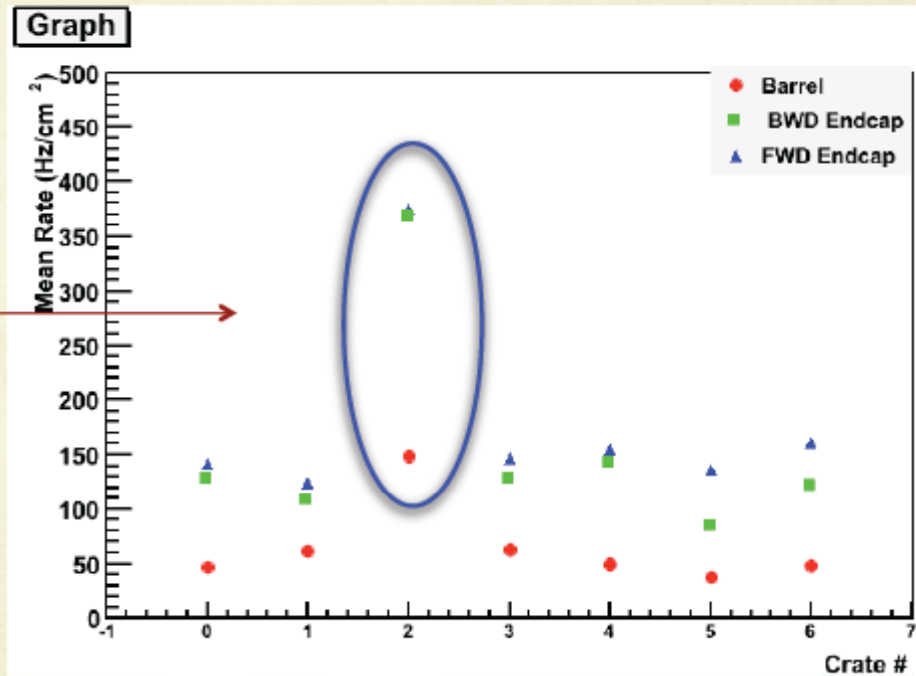


- Rate on electronics comparable to that one on the last IFR layer)

Mean Rate for each FEE in different Crates

Crates located in the FWD have systematically higher rates compared to that one in the Barrel

Crate 2 very hot compared to other one the crate 2 is located on beam plane negative X



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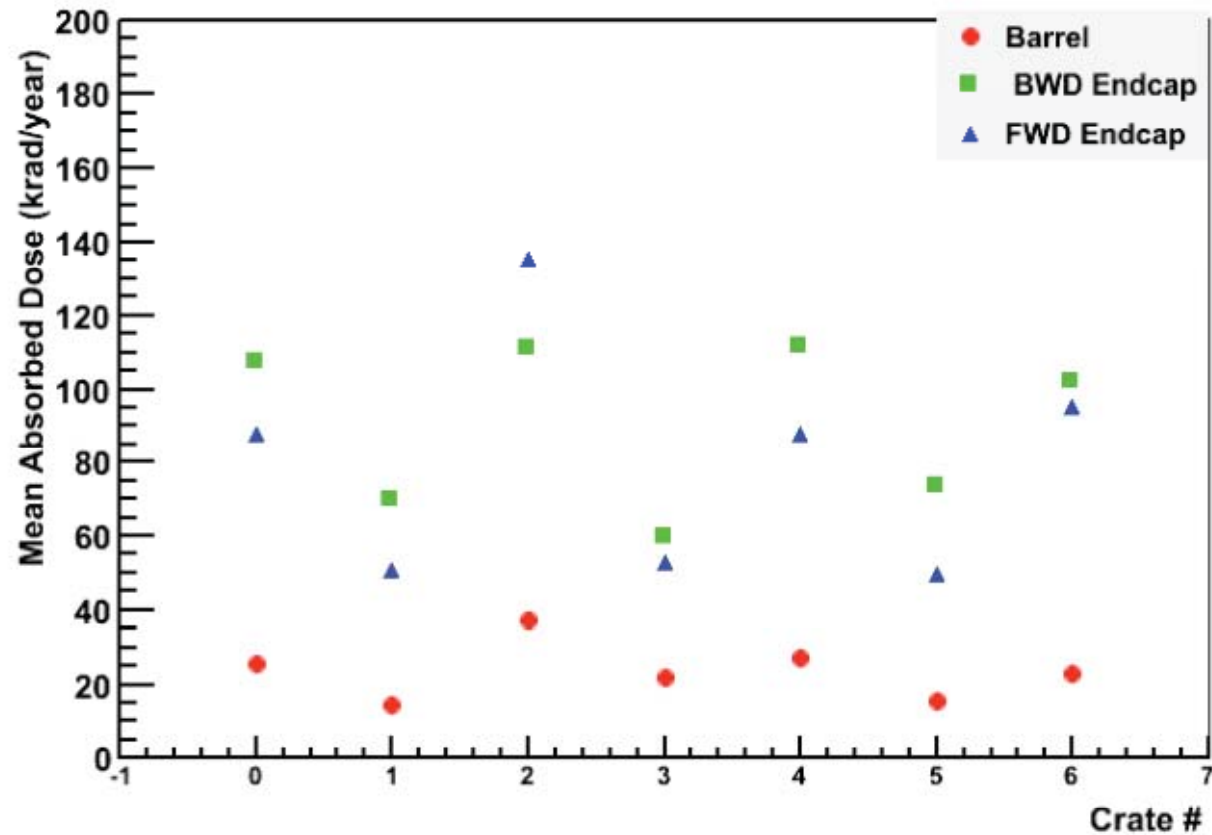
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addressing the radiation issues: background rates estimation at the location of IFR front end electronics



Absorbed Dose for each FEE Crates

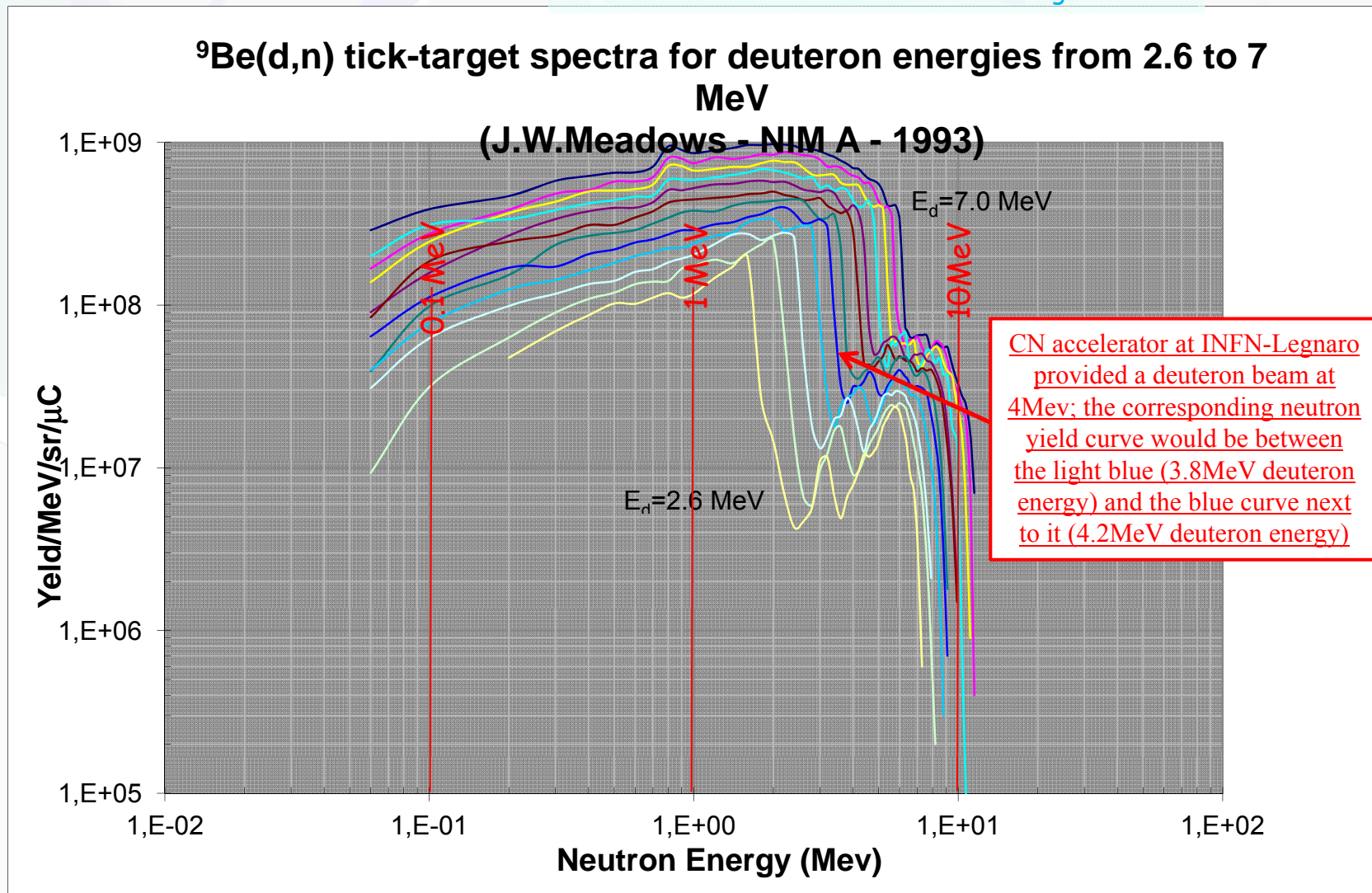


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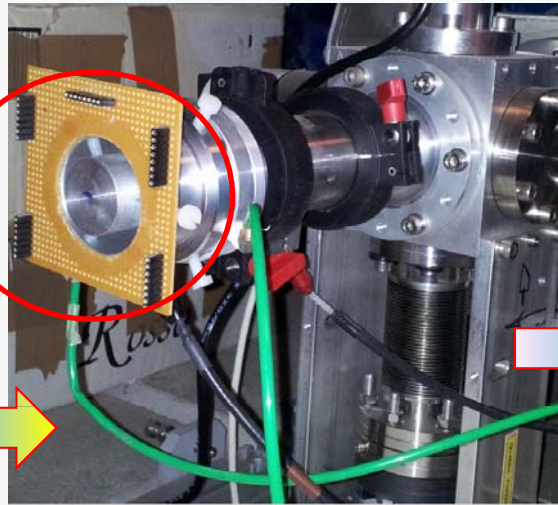
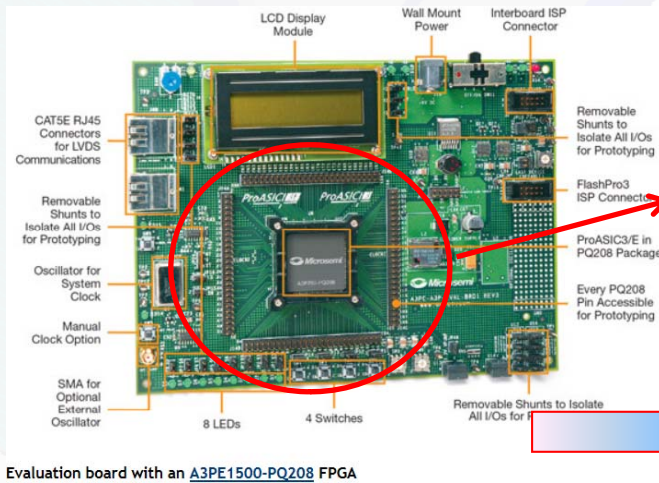
17

addressing the radiation issues:
measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro
Presented at the nov16/17 ETD meeting at CERN

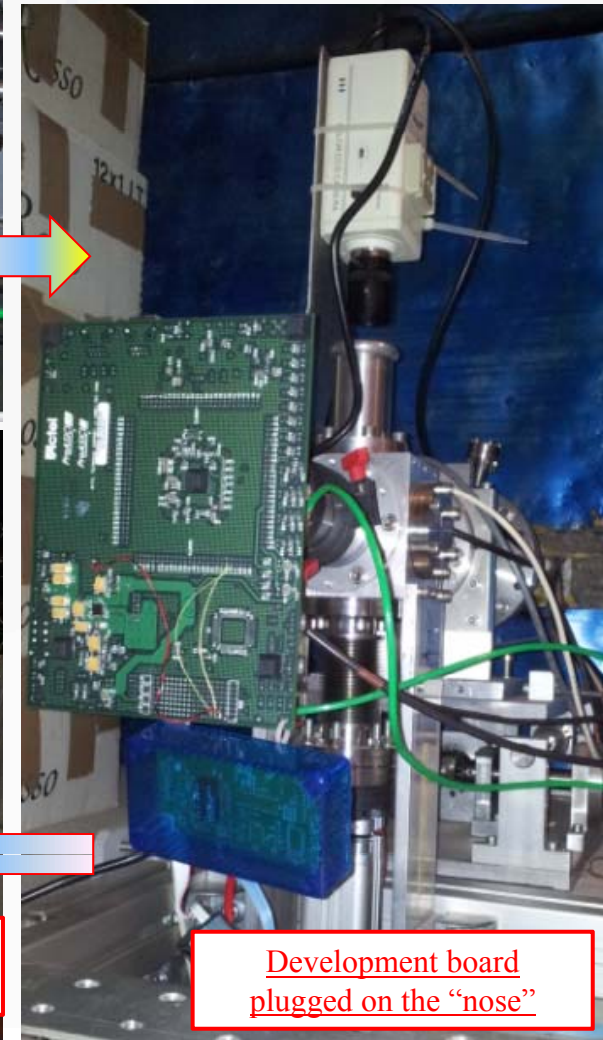


([excel file by Flavio Dal Corso](#))

addressing the radiation issues:
 measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro

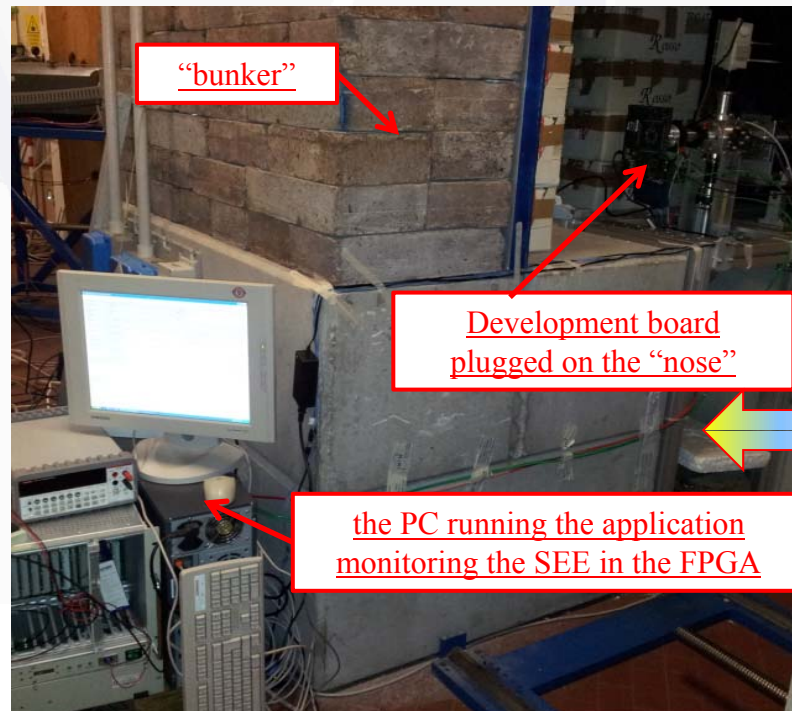


Presented at the nov16/17 ETD meeting at CERN



Acknowledgements:

We exploited beam time which had been allocated by our colleagues Roberto Stroili and Flavio Dal Corso who also provided the information needed to estimate the neutron flux.



addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: **preliminary results**

Prior to the irradiation tests:

1) the EASIROC ASIC provided by LAL/OMEGA was characterized (thanks to Roberto Malaguti) in order to record:

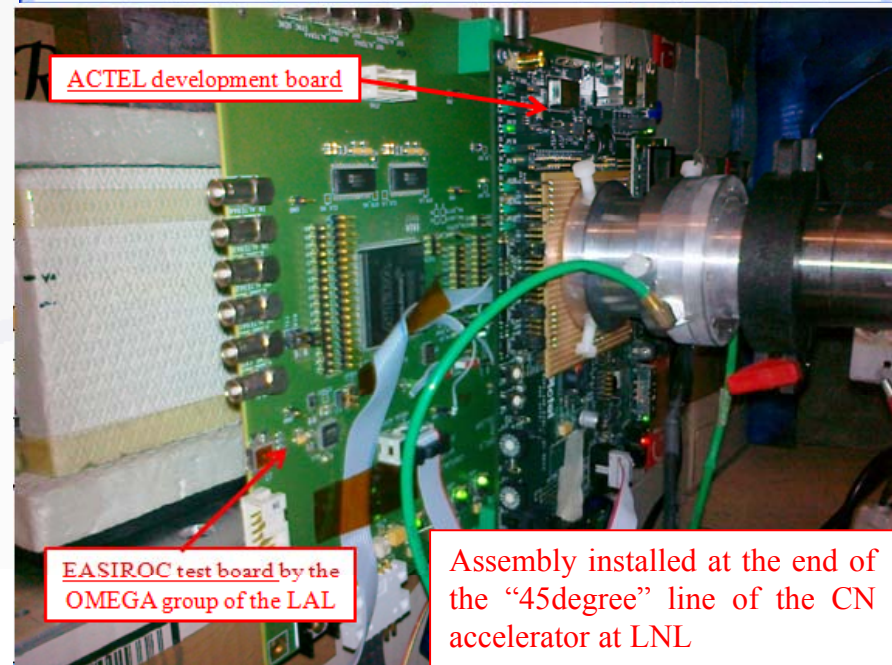
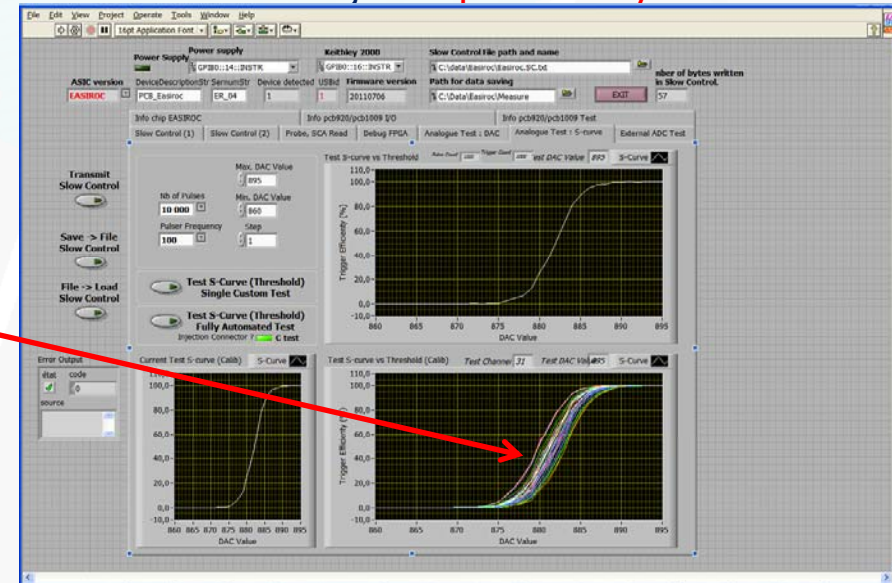
- the transfer curve of the input DACs
- the S-curve for a set of input channels
- the current consumption

2) the EASIROC test board was **modified to isolate the ASIC from the on-board FPGA** in such a way that the serial programming stream for the initialization of the chip could be provided by a microcontroller board located outside the bunker

3) the firmware for the microcontroller (R.M.) and a Labview program (A.C.R.) were prepared to allow an operator to **periodically send and readback the configuration stream to the configuration registers of the EASIROC (57 words of 8 bit each for a total of 456 bit): these registers were written and checked after a period of about ½ hour to look for SEU**

4) a suitable support was realized to couple the EASIROC board to the FPGA board in such a way that **the FPGA and the ASIC were aligned (and separated by about 13mm)**; the FPGA board was used in this case as a neutron fluence monitor

5) finally a set of op-amp to be used in the front end differential driver has been fastened on top of the FPGA



addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: preliminary results

SOLID ANGLE OMEGA	ACTEL	EASIROC
OMEGA =	1,187020 767	0,040584586
alfa (cm)	0,9	0,41
beta (cm)	0,9	0,4
alfa * beta = (cm^2)	0,81	0,164
distance d = (cm)	0,7	2
denominator (cm^2)	2,648924 31	16,1632175

Data extracted from the "irraggiamento.xls" spreadsheet by Flavio Delella

integrated irradiation time (sec)	charge (µC)	total errors in the FIFO section of the FPGA design	total errors in the shift register section of the FPGA design
60683	4104	752	26
total Yeld/sr/uC @ Ed=4 MeV	hardness factor @ Ed=4 MeV		
1,02E+09	1,146		

	ACTEL	EASIROC
numero totale di neutroni attraverso DUT per tutta la durata del test	4,96E+12	1,69E+11
numero di neutroni attraverso 1 cm^2 in per tutta la durata del test = fluenza@DUT	6,12E+12	1,03E+12
FIFO depth:	4096	
Shift Reg. depth:	728	
word width:	8	
<numero di bit flip in FIFO> :	752,0000 22949,218	
per Mb:	8	
<numero di bit flip in Shift Reg> :	26,0000	
per Million Flip Flop:	4464,2857	

If the estimation of neutron flux at the CN facility in Legnaro is correct then we have exposed the devices to a total flux of :

- $\approx 4,9 * 10^{12}$ neutrons at the FPGA location
- $\approx 1,7 * 10^{11}$ neutrons at the EASIROC location

in about 17 hours, during which we have detected:

- NO SINGLE EVENT EFFECTS HAVE BEEN OBSERVED FOR THE EASIROC
- 752 errors in the RAM based section of the design
- 26 errors in the shift register instantiated in the FPGA fabric

(the beam intensity was lower than that of the previous tests because the deuterium bottle became almost exhausted during the last day)

vedi: "Overview of iRoC Technologies Report "Radiation Results of the SER Test of Actel FPGA December 2005"

da: "Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances"

cross section per chip: $\text{Sigma}_C = \text{No_of_errors} / (\text{fluence} * C)$ with C = number of chips

reference fluence: fluence at ground level in New York City: fluence_NYC = 14 n/cm^2/hour
FIT: Failure In Time: failures in 10^9 hours. FIT = $\text{Sigma}_C * \text{fluence_NYC} * 10^9$

g.c.p. 2011-11-02

nel nostro caso:

a3p250-FIFO section
a3p250-SHIFT Register section

	FIFO	SHIFT REGISTER
Sigma_C [cm^2]	1,229E-10	4,250E-12

ref_fluence/hour
1,400E+01

FIT
1,721E+00
5,950E-02

definisco:

cross section per FIFO Mb: $\text{Sigma_Mb} = \text{No_of_errors} * 10^6 / (\text{fluence} * N_FIFO_bit)$

our test at LNL on a ProASIC3 device a3p250 IROC test on a ProASIC3 E device a3pE600

FIT per million bit of embedded RAM	
RAM	FIT per million bit of embedded RAM
5,252E+01	1580
FIT per million flip flop	
	FIT per million flip flop
1,022E+01	889
5,141E+00	1,7

a3p250: Fifo cross section per Mbit

Sigma_Mb
3,75131E-09

definisco:

cross section per M flipflops: $\text{Sigma_Mff} = \text{No_of_errors} * 10^6 / (\text{fluence} * N_flipflops)$

Sigma_Mff
7,29738E-10

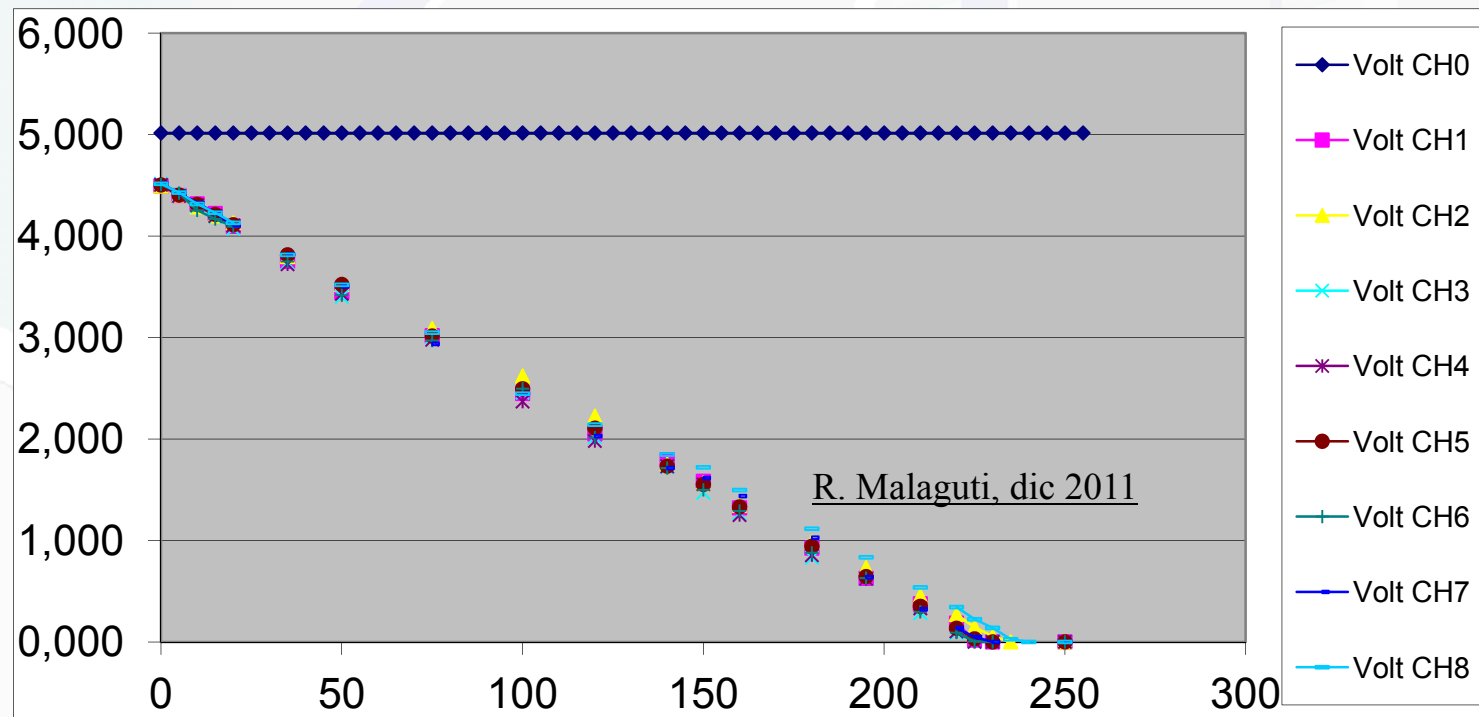
a3p250: ShiftRegister cross section per Mfliplop

FIT (Failure in Time) figure resulting from our test is 30 times smaller than that published by ACTEL for a similar FPGA tested with 14MeV neutrons.

addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: **preliminary results**

□ **EASIROC test results:**

- **integrated neutron fluence at the EASIROC location : $\approx 1.7 * 10^{11}$ neutrons**
- **TID effects: **change in DAC characteristics due to irradiation : undetectable****



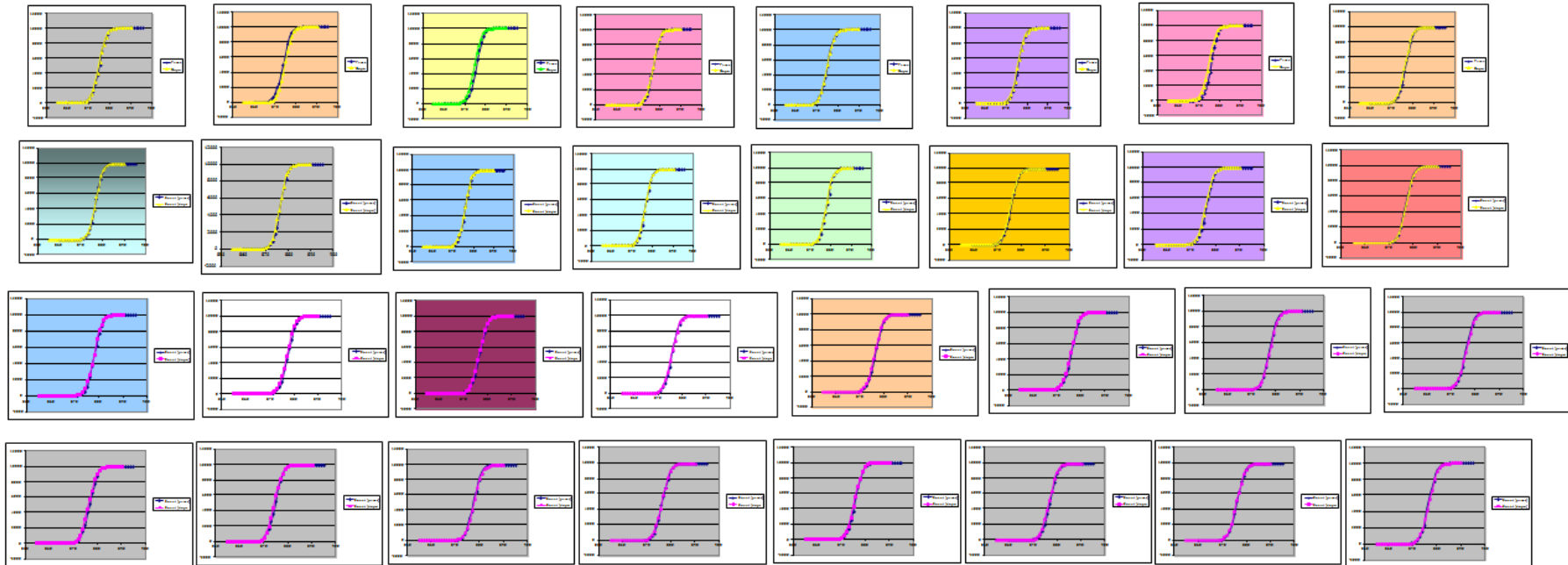
The plot shows the transfer curves, taken BEFORE irradiation, for the input DACs for the channels 0 through 8. Channel 0 was damaged by us at the beginning of the test and can be neglected.

The plots created after irradiation show no detectable differences; just one measurement point, at DAC count 140 for channel 7, was off by 130mV. At all other points the differences were within the systematic error range

addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: **preliminary results**

□ **EASIROC test results:**

- **integrated neutron fluence at the EASIROC location : $\approx 1.7 * 10^{11}$ neutrons**
- **TID effects: **change in S-curves due to irradiation : minor****



R. Malaguti, dic 2011

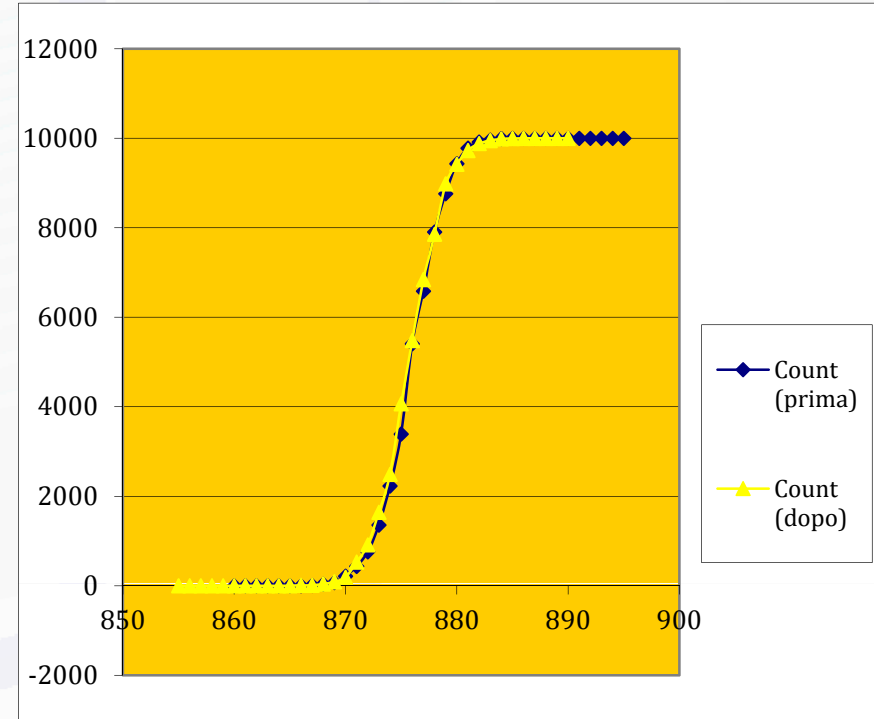
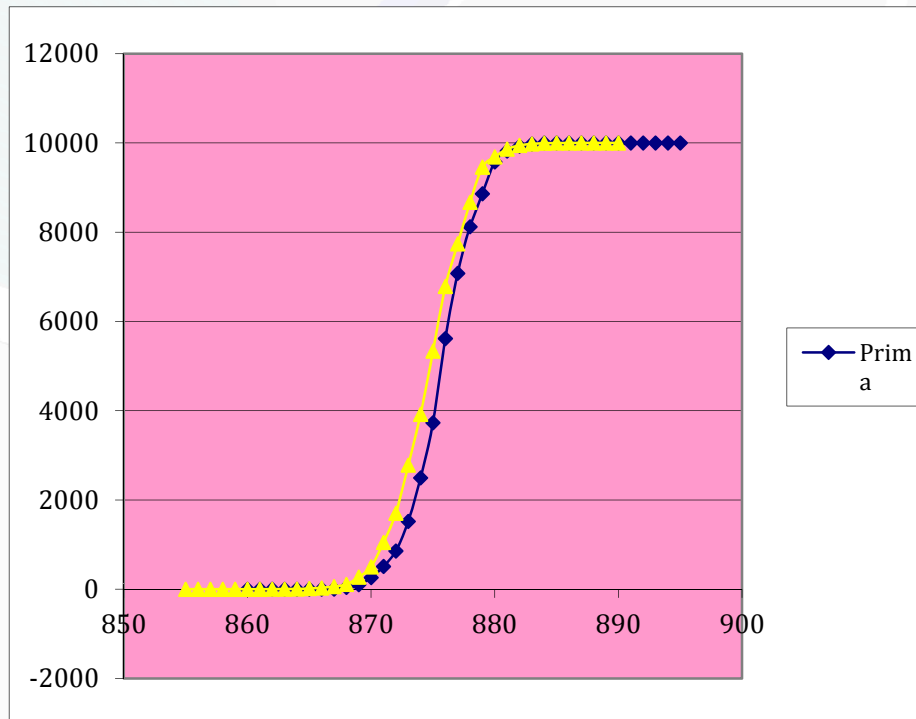
The plots, by R. Malaguti, show the S-curves, taken BEFORE and AFTER irradiation. In general they show shifts which could be compatible with systematic errors.

A couple of S-curves are shown in more details on the next slide

addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: **preliminary results**

□ **EASIROC test results:**

- **integrated neutron fluence at the EASIROC location : $\approx 1.7 * 10^{11}$ neutrons**
- **TID effects: **change in S-curves due to irradiation : minor****



The plots shown are representative of channel with little (**left, channel 6**) or no (**right, channel 13**) difference between BEFORE and AFTER irradiation.

addressing the radiation issues: preparation for next irradiation tests

For the coming irradiation tests we are developing dedicated carrier cards (LEFT) for the EASIROC ASIC and auxiliary cards (RIGHT) to detect (and protect) Single Event LatchUp. The auxiliary card could be used also for the CLARO and the RAPSODI ASIC#2

