ROM Status

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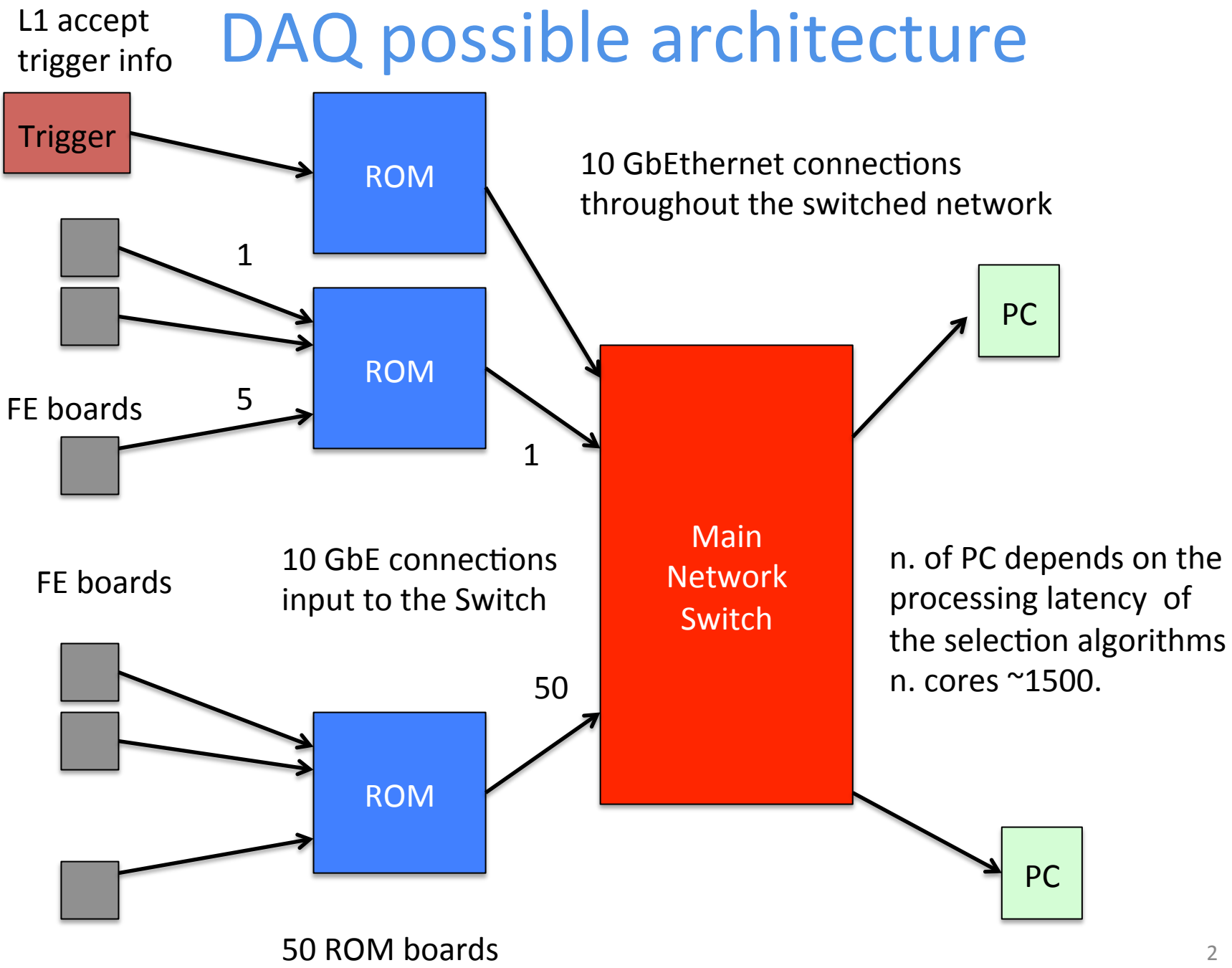
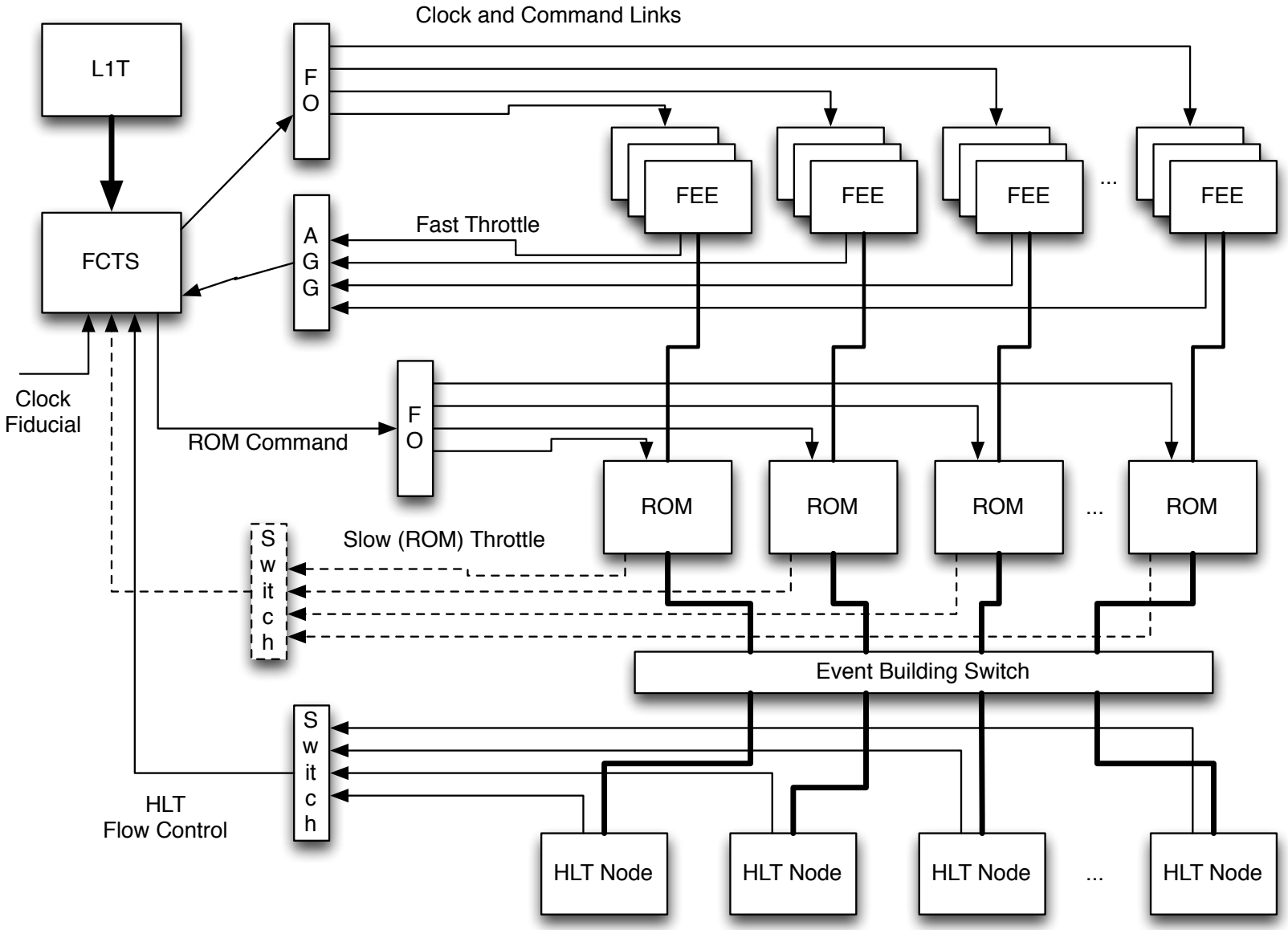
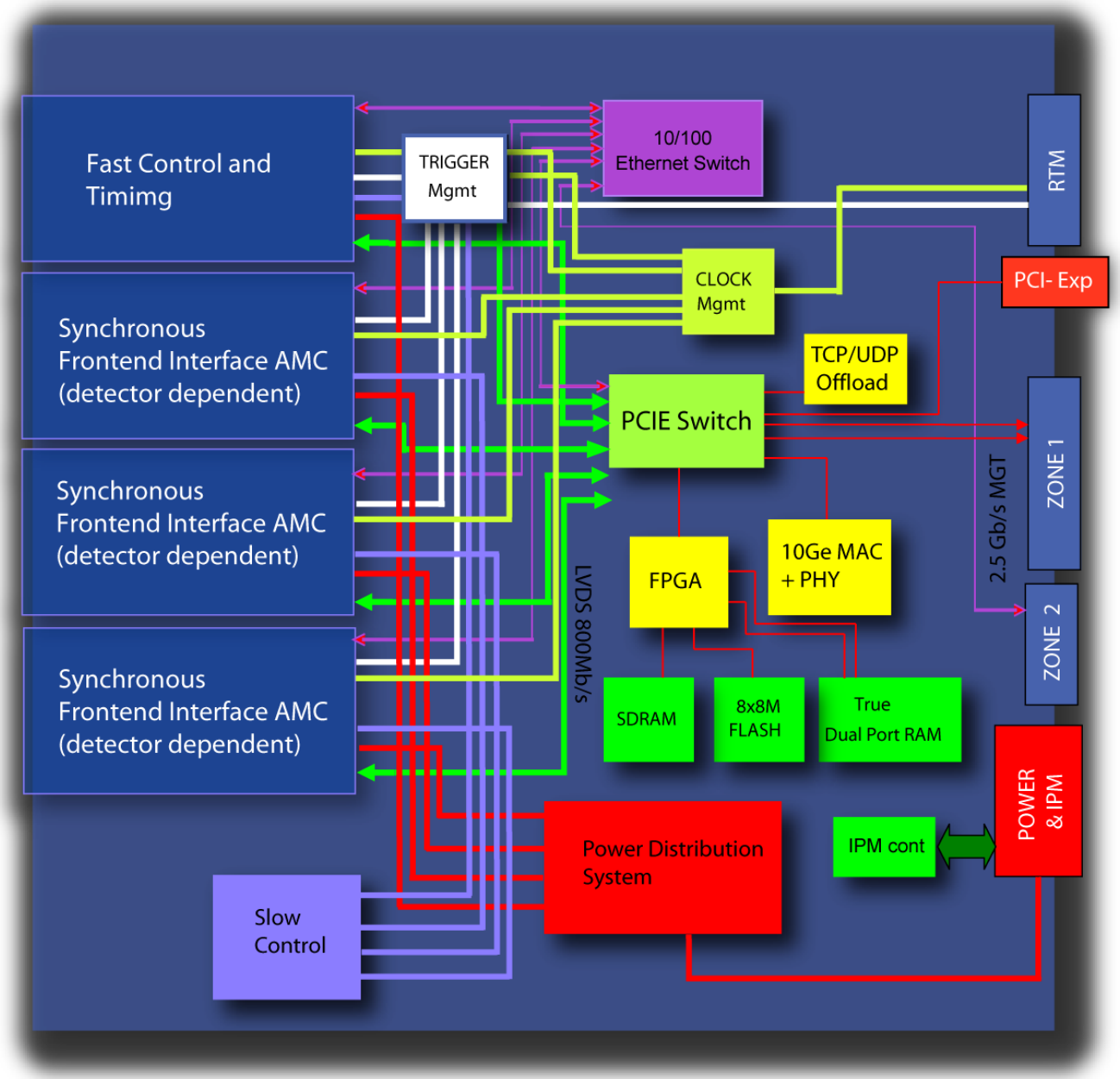
DAQ possible architecture




Clock and Command Links
L1T
FCTS
F
O
A
G
G
Fast Throttle
FEE
FEE
FEE
...
FEE
Clock
Fiducial
ROM Command
F
O
ROM
ROM
ROM
...
ROM
Slow (ROM) Throttle
S
w
it
c
h
Event Building Switch
S
w
it
c
h
HLT
Flow Control
HLT Node
HLT Node
HLT Node
...
HLT Node

ROM PCIe board Block Diagram



Electronics

- The Xilinx ML605 evaluation board hosting a Virtex-6 has been a good tool to start playing with PCIe.

4x lanes PCIe Gen2, 5 Gb/s per lane
4 GB/s in total
8x lanes PCIe Gen1, 2.5 Gb/s per lane

The setup

- **PCI Express card: ML605 board**
  It enables hardware and software developers to create or evaluate designs, programming Virtex®-6 XC6VLX240T-1FFG1156 FPGA. It includes an 8-lane PCI Express® interface gen1 . It's possible to add desired features by means of mezzanine cards attached to the onboard high-speed VITA-57 FPGA Mezzanine Connector (FMC).

- **First-type of PC architecture:**
  - Mother board: for Intel® Xeon® X3400 e L3400, Intel® Core™ i3-540, i3-530 and Intel® Pentium® G6950; chipset Intel® 3420, until 32GB ram, 2 slot PCI-Express x8. By the hyper-threading, It corresponds to 8 CPUs.
  - Processor: Intel® Core X3470 Quad-Core - 2,93GHz, 8MB extern cache, memory rate 1333MHz (DDR3 only), 8 elaboration threads.
  - Ethernet board: 1 x Qlogic 10Gb QLE3142 SR Server Dual Port

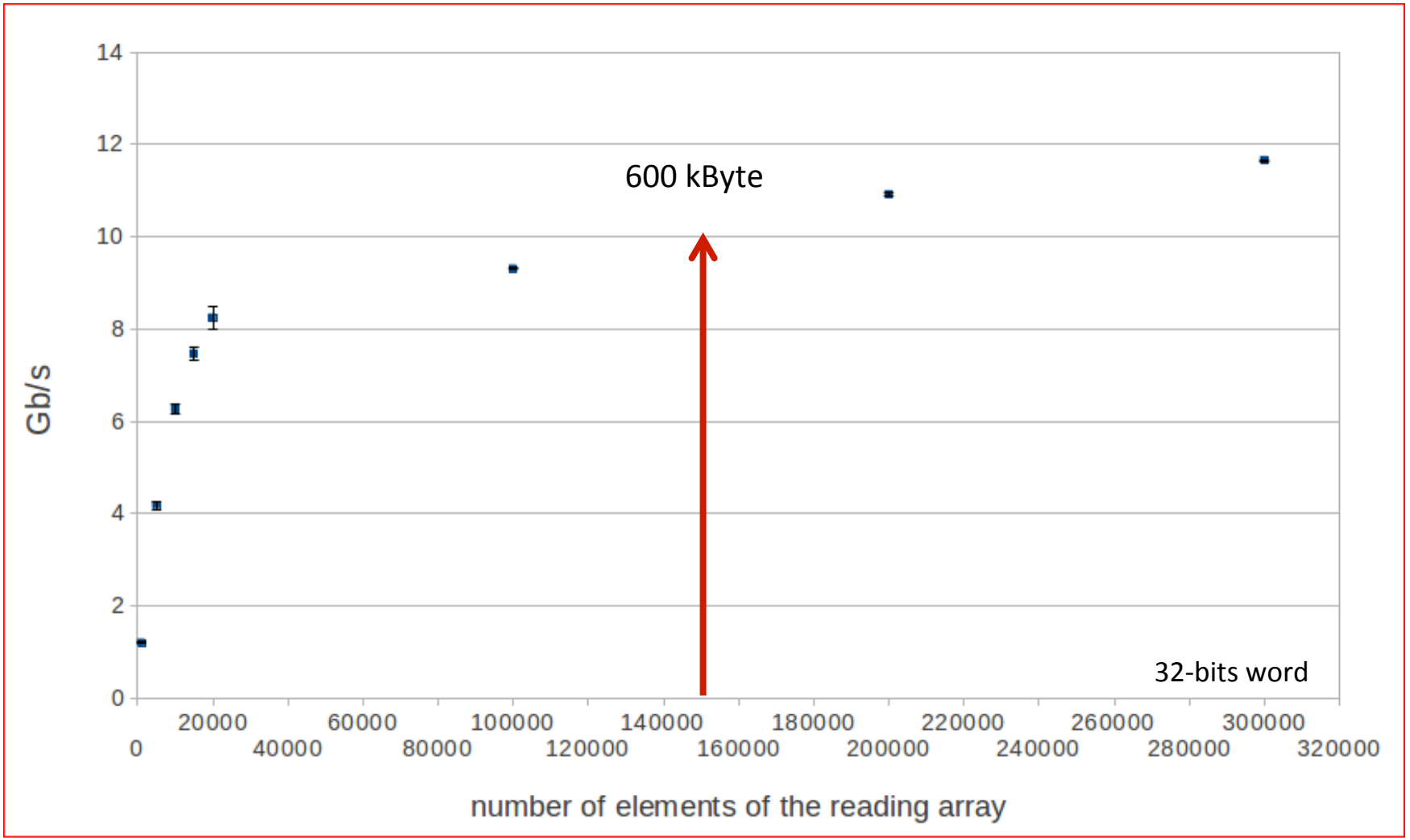
- **Second-type of PC architecture (NUMA Technology):**
  - Mother board: for Intel® Xeon® serie 5500, system bus Quick Path Interconnect (until 6.4 GT/s); chipset Intel® 5520 Express IOH; until 48GB ram, 2 slot PCI-Express x 8
  - Processor: 2 x Intel® Xeon E5620 Quad-Core - 2,40GHz, QPI rate 5,86GT/sec., 12Mb extern cache, memory rate 1066MHz (DDR3 only), 8 elaboration threads. By the hyper-threading, It corresponds to 16 CPUs.
  - Ethernet board: 1 x Solarflare 10Gb SinglePort SFP+.

The software

- Linux driver (by D. Bortolato-INFN Padova) specifically designed to data acquisition from a PCI express , employing the hyper-threading features and pre-emptibility of the 2.6.38-11-generic kernel version.
- The driver has been installed and tested on Ubuntu 4.5.2-8 and on Scientific Linux 6. The simulated input data was produced by the ML605 board on specific VHDL design. The control of the PCIe is maintained by a process one at a time.
- C programs using PCIe driver to read simulated data: measuring reading and transmitting times needed sending the data to a second PC exploiting UDP/IP protocol.
  Implementation and driver debug by L. Carota –INFN Bologna.
- Scripts to start parallel run of many processes.
  Implementation by L. Carota –INFN Bologna.

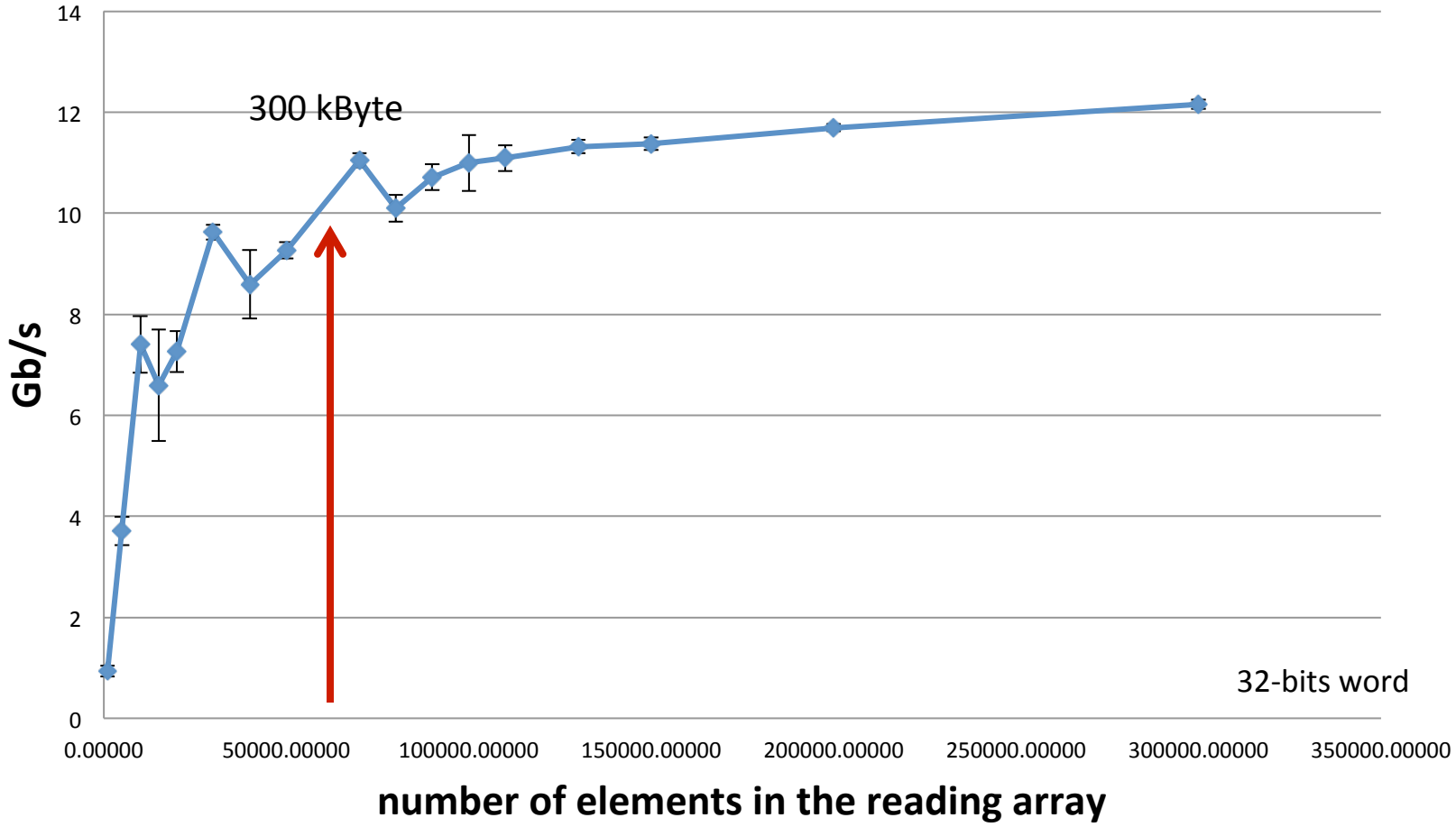
Input rate versus the event size.

Results achieved with the first-type of mother-board architecture.
The 10 Gb/s throughput can be reached when the size is about 1.5×10^5 (32-bit words).



Input rate versus the event size.

Results achieved with the second-type of mother-board architecture.
The 10 Gb/s throughput can be reached when the size is about 7.0×10^4 (32-bit words).

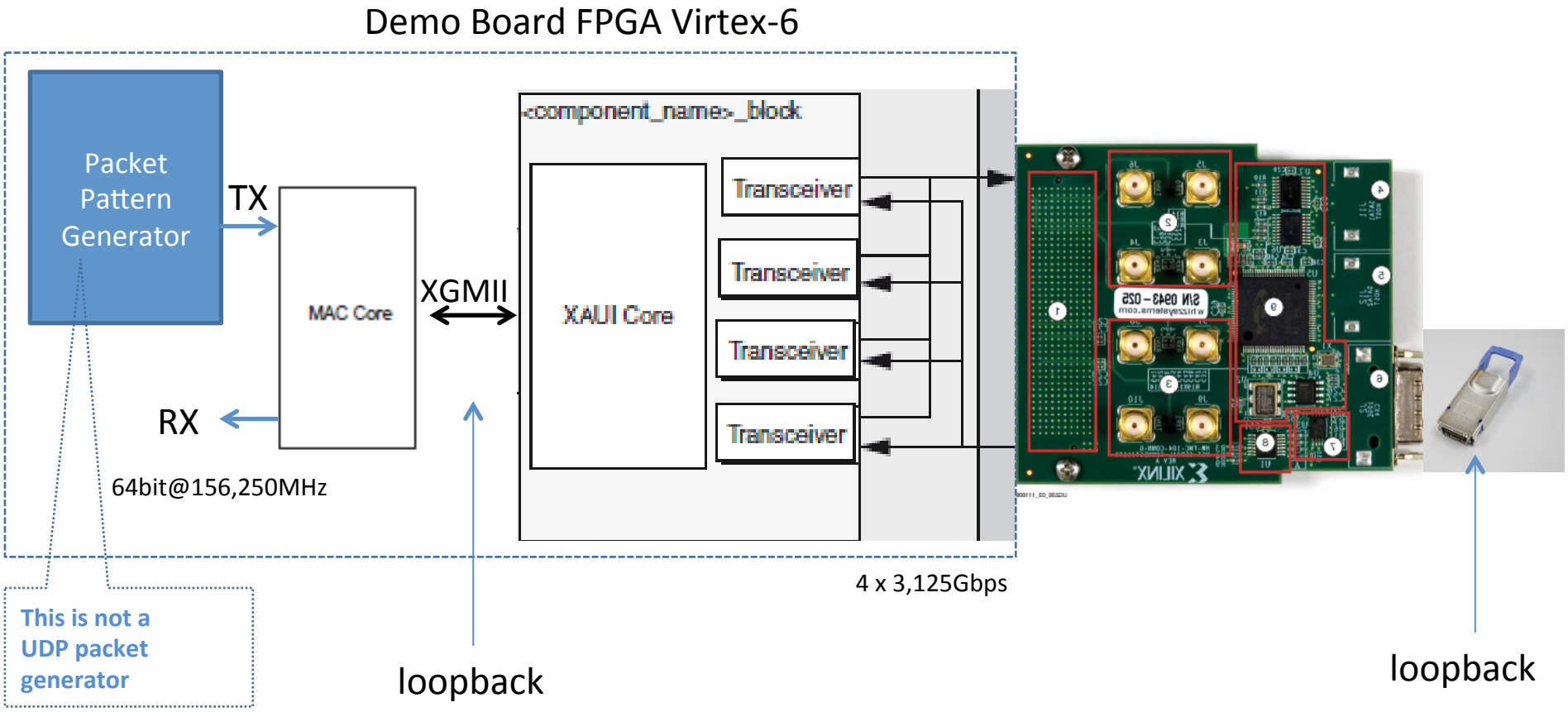


Ongoing activities

- Testing a relatively more complex chain:
  Data moved from the PCIe interface to the host PC to another PC.
  We want to check 10 Gb/s flows throughout the chain.
- Data between PCs goes through 10 GbEthernet NIC.
- A NIC board (receiver PC) has shown an incompatibility of the firmware and the driver of the Scientific Linux 6.
  - Probably we need to flash the board with a new firmware, or recompile the driver, or buy a new Ethernet board.
  - Driver for Scientific Linux 6 are not supported for this NIC board.
  - We reached 4 Gb/s.
- We plan to develop a software architecture with a single process continuously transmitting data, while reading is performed by several processes running in parallel.
  - We have to develop a strategy to minimize the transferring time of the data between a reading process and the sending process.

10 GbEthernet on FPGA Virtex-6

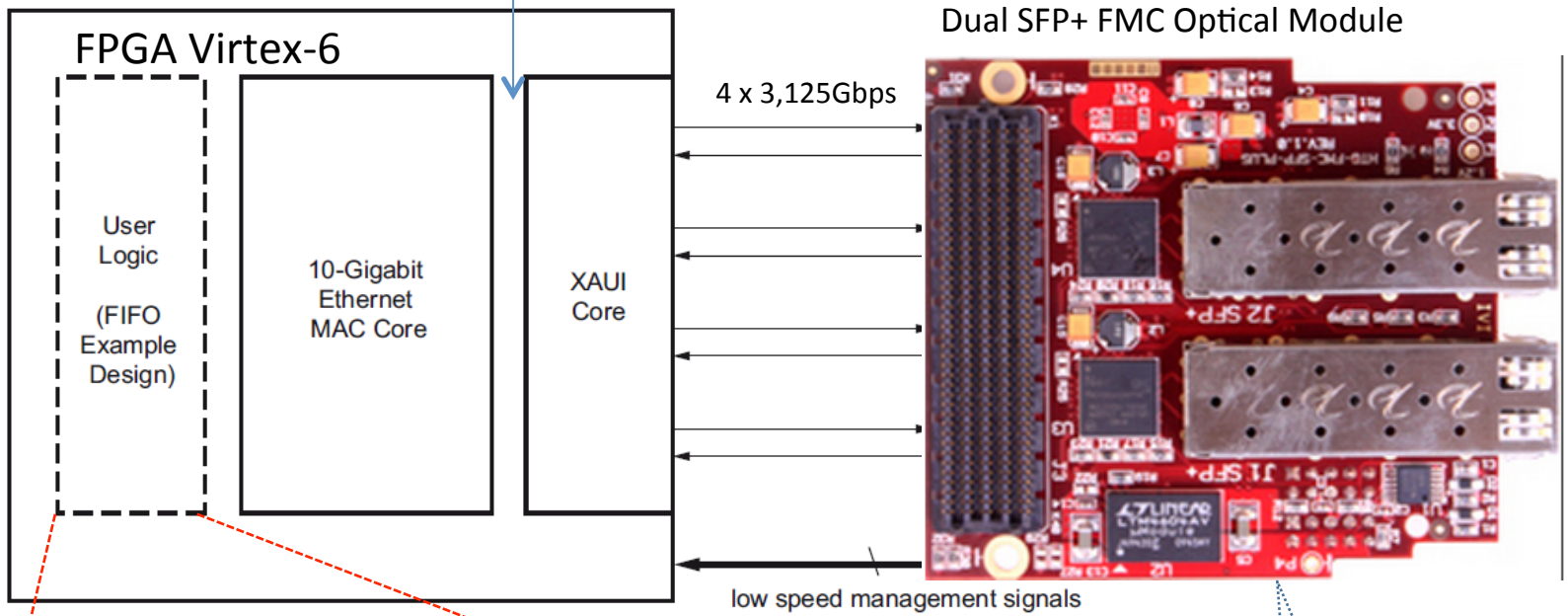
Simulation and implementation on a Xilinx demo-board equipped with Virtex-6 FPGA

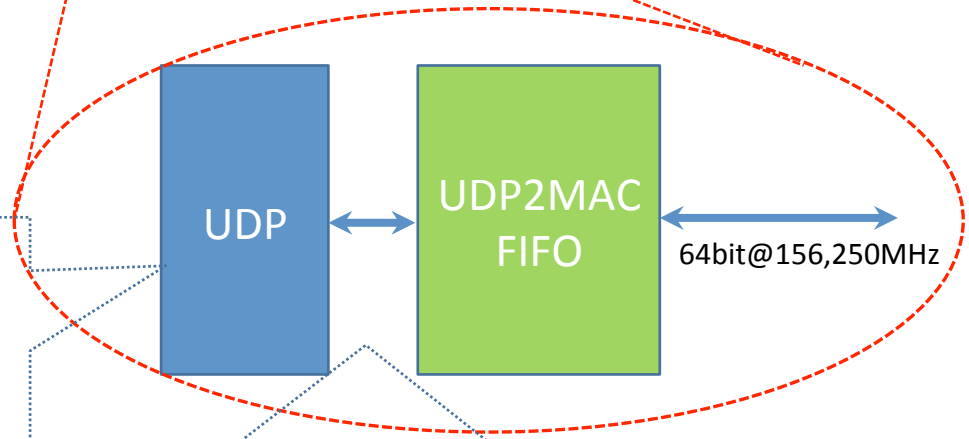


Data flows through the MAC core (Ethernet physical layer) to come back through the RX.
Test data consistency at the RX using Chipscope.

10 GbEthernet on FPGA Virtex-6

Simulazione con loopback in questo punto





Ordered.
Not available yet

UDP packet generator . Variable packet size. Random pattern.

Attualmente generiamo pacchetti UDP a 8bit@125MHz. Per raggiungere i 10G si pensa di moltiplicare x10 questo modulo

Xilinx Virtex-7 FPGA VC707 Evaluation Kit

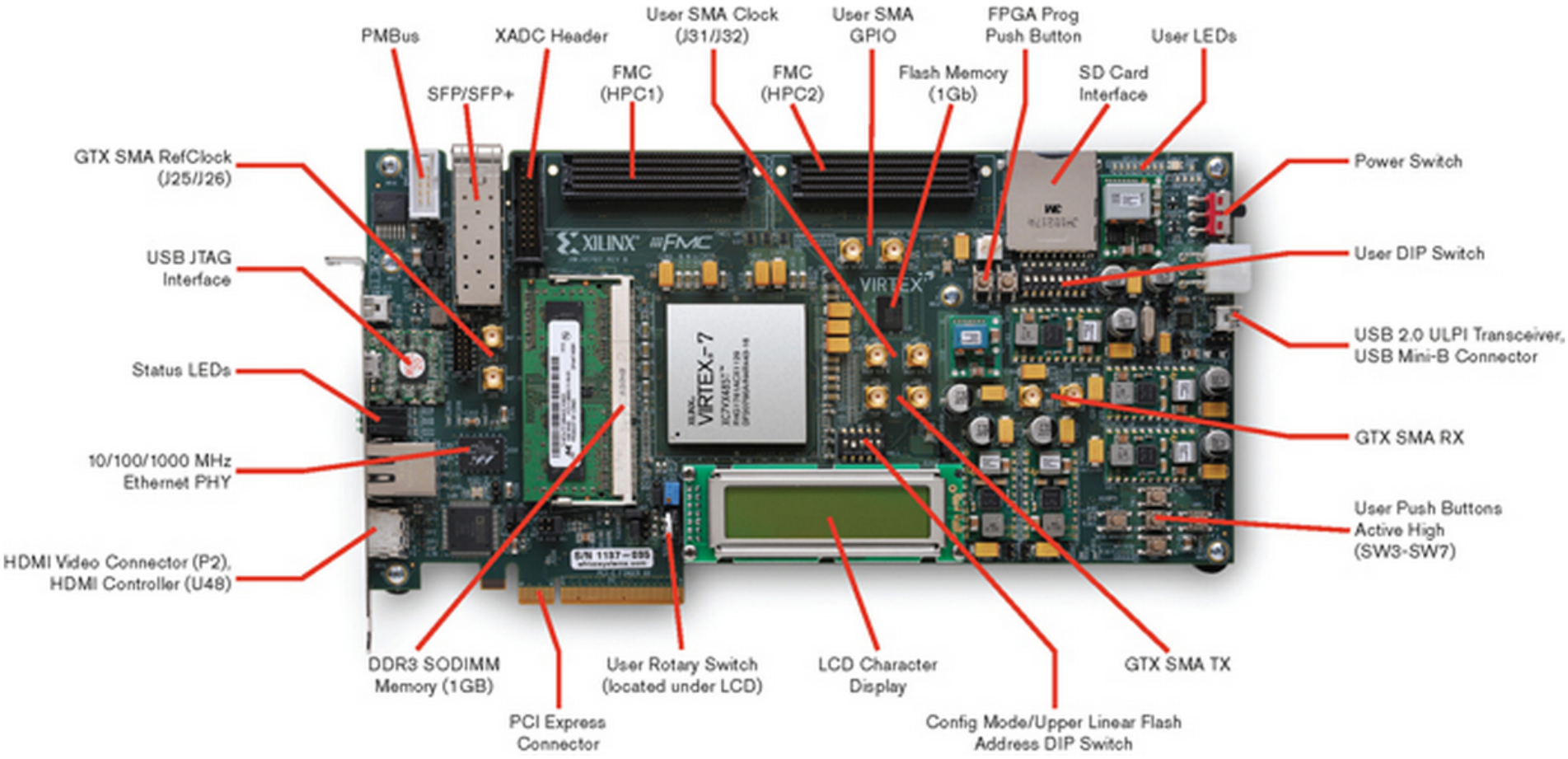
Click to Enlarge Image
View Partner Profile
$3,495

Overview | Boards | Tools & IP

- VC707 Base Board
  - Key Features
- Agile Mixed Signal Evaluation Card
  - Key Features

VC707 Base Board

VC707 Base Board



Test on 10 GbE

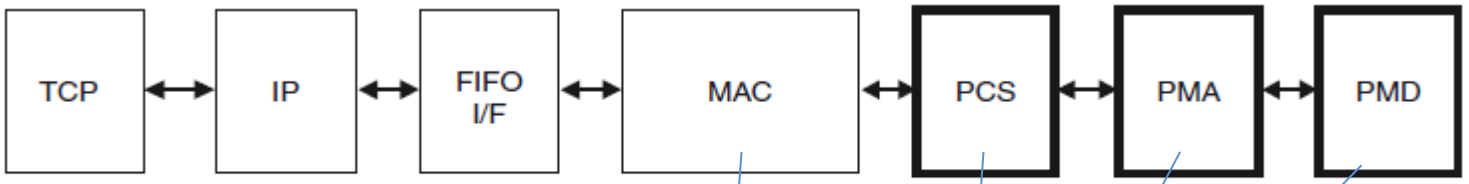


Figure 3-3: **Typical Ethernet System Architecture**

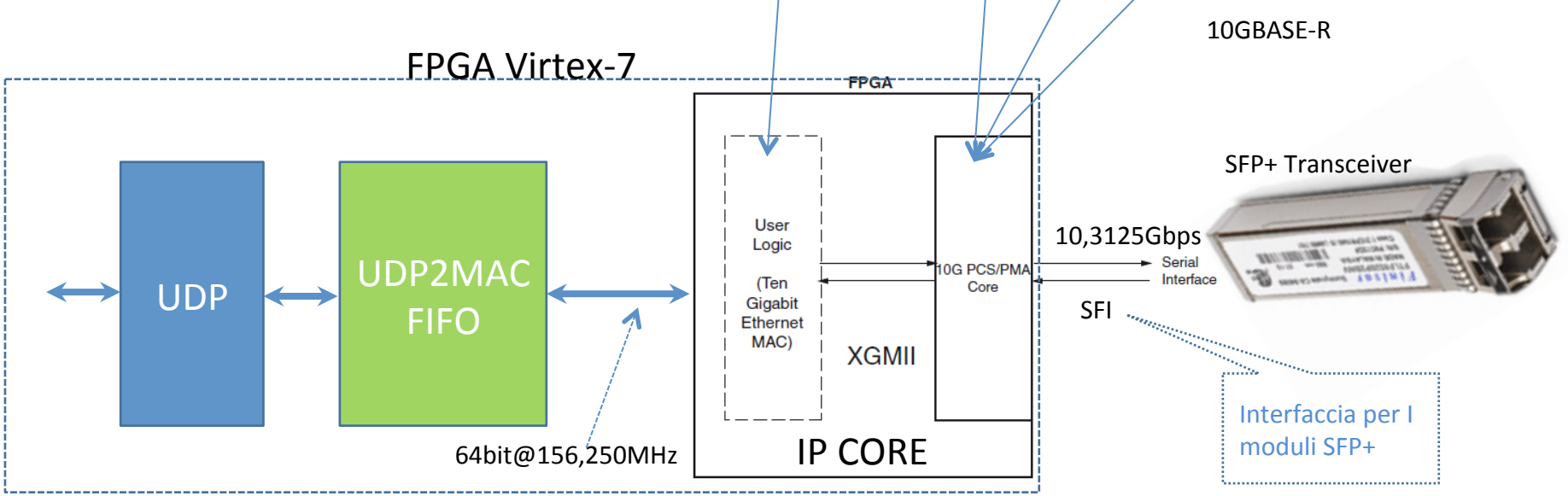


Figure 3-4: **10-Gigabit Ethernet PCS/PMA Core Connected to MAC Core Using XGMII Interface**