FDIRC prototype status

J. Va' vra

SuperB collaboration meeting in Frascatti, March 2012

Content

- **Status of optics.**

- **Status of Fbox & CRT mechanics.**

- **Comments of FDIRC prototype electronics.**

- **Comments on background & shielding.**

Problems

- **We had to decide how to deal with the plating problem.**

- **Matt was on medical leave for a month (hernia operation).**

- **When he came back, the lab took him away to help some other experiment, which had higher priority at that moment.**

- **We effectively started on March 15.**

- **Now I see the end of the tunnel and we can start planning again.**
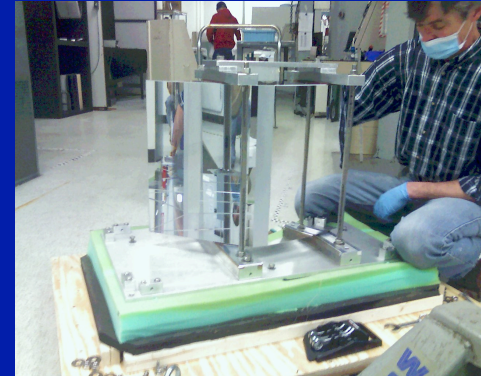
FBLOCK: plating problem

J. Va'vra

Tape took some plating off in one corner:
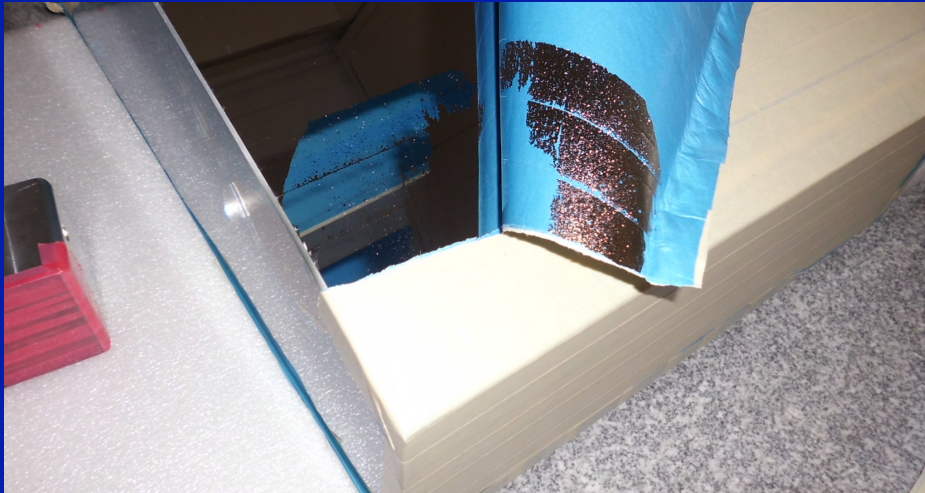
Plating shop, EMF, Ithaca, N.Y.:

- **Cosmo company insisted that all surfaces must be protected by a tape.**
- **They did some tests on aluminized coupons. I repeated them and indeed the tape would not remove plating from well-plated surface.**
- **However, there may have been some pollution introduced when handling heavy optical piece and the plating would be weaker in this section.**
- **Did some tests with 4 different tapes. All of them would remove the plating from this "weaker" section. So it was not a choice of bad or good tape.**
- **The only tape which would work OK even here: electrostatic Grafix tape.**

FDIRC: Definitions of names

(A new beautiful drawing from Massimo)
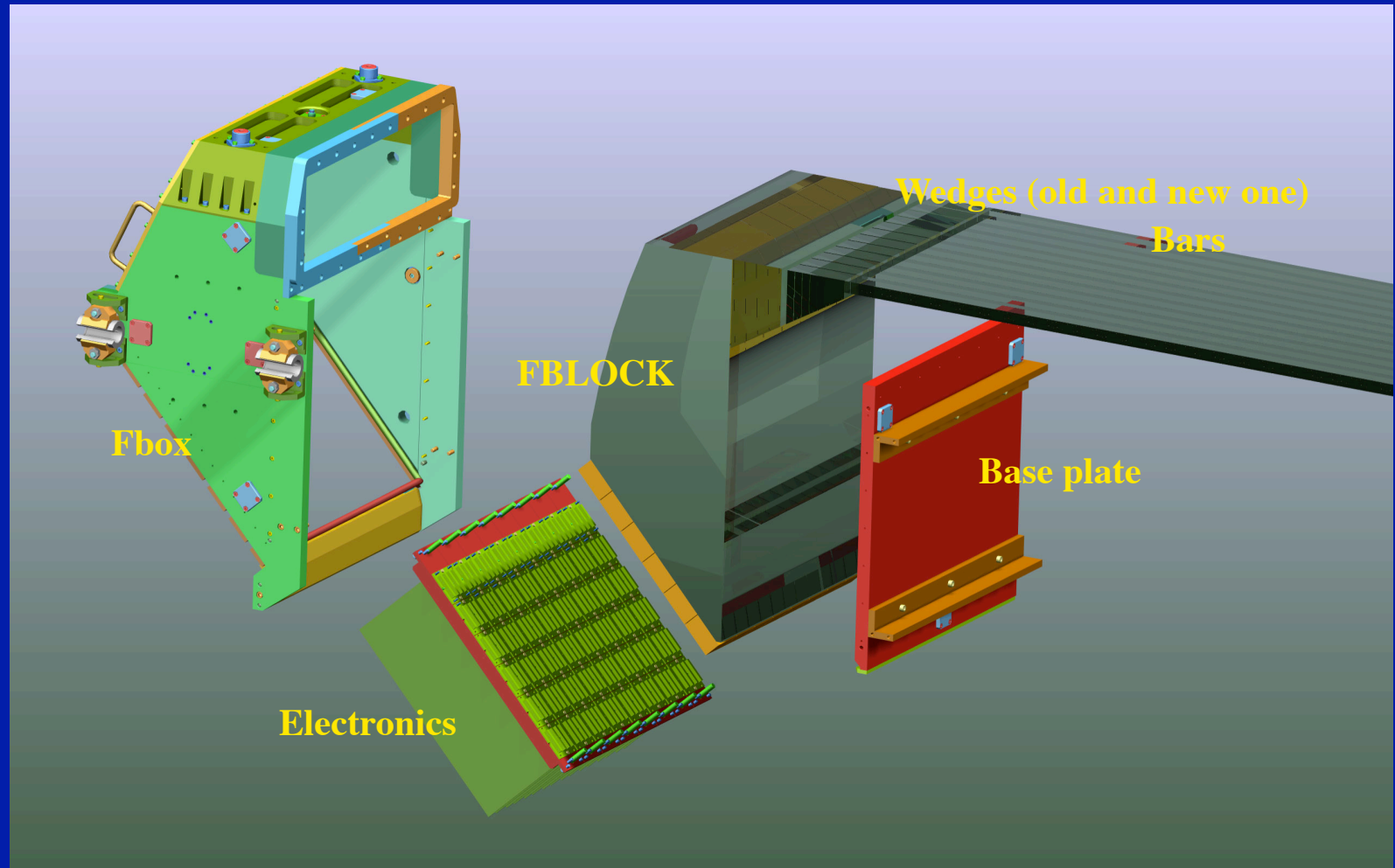
QC of FBLOCK

SLAC alignment group

Use the FERO digital arm to measure coordinates of points:

- **Measure 20-30 points on each surface.**
- **Determine angles between surfaces, and rms deviation of each point from a given surface, distance between surfaces, radius of cylinder, etc.**
- **We found the alignment within tolerances on all critical numbers, clearly proving that this kind of optics is doable.**

Difference between designed and "as-built" values

J. Va'vra, G. Gassner (head of alignment group)

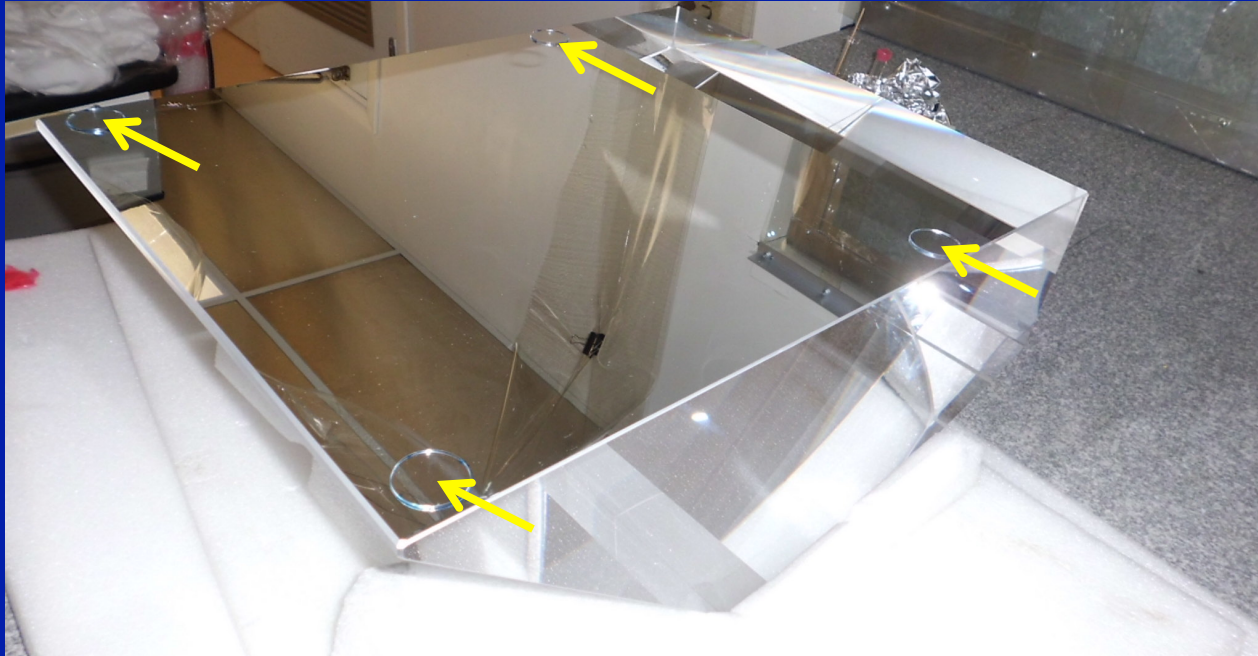**Graphical summary of numbers "as-built":**

Numbers relative to my original design (in red are measured numbers):
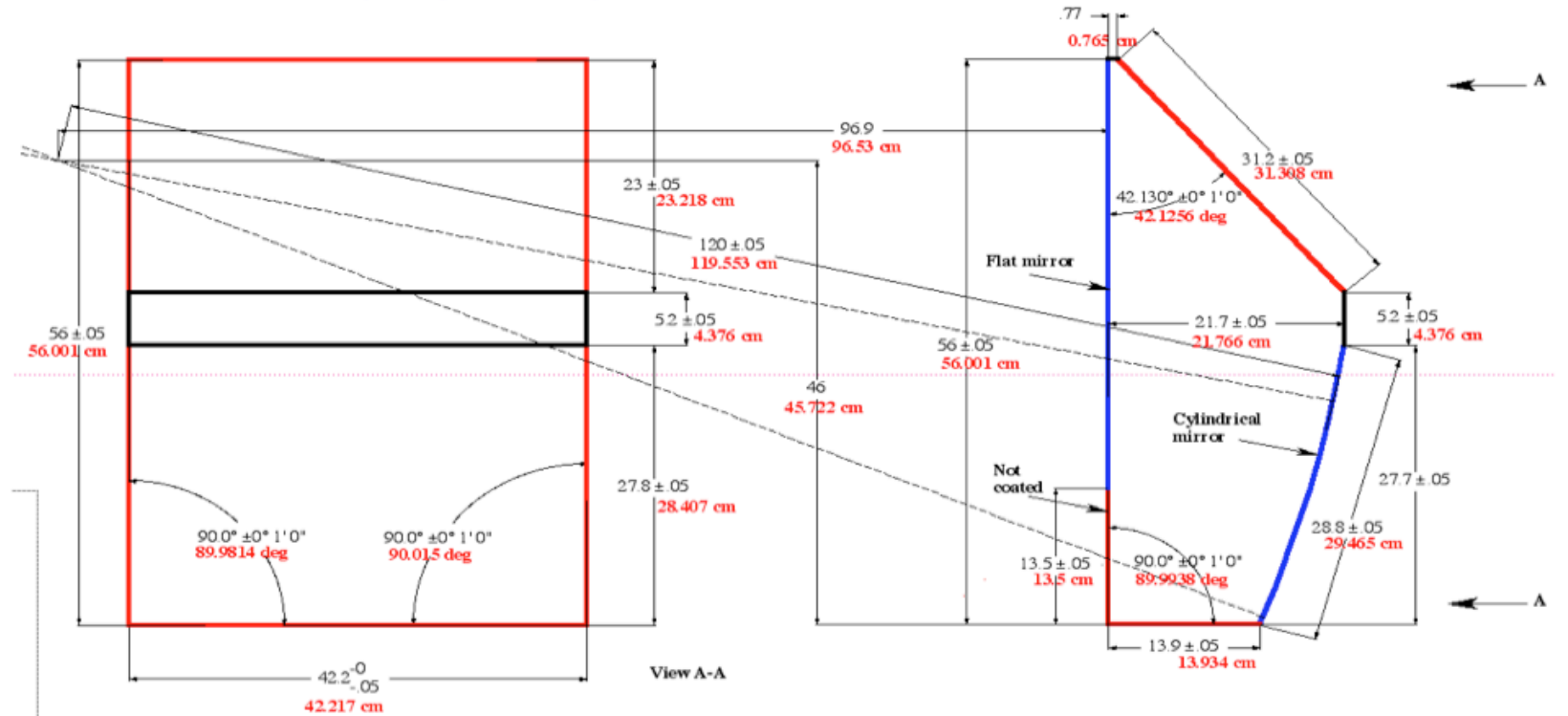
- **Update file of critical numbers: " Critical_dimensions_v5.pdf ".**
- **Doug has been implementing them in the FDIRC MC simulation.**

Preparing FBLOCK for next steps
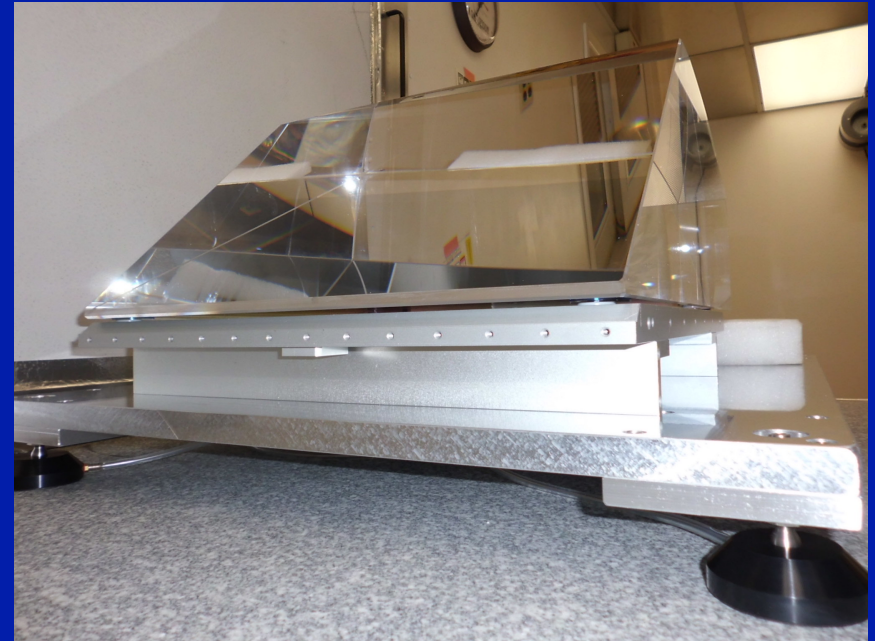
M. McCulloch and J. Va'vra

- **Glue quartz cookies to four corners of FBLOCK.**
- **Cookie is made of natural quartz, 1/16" thick and 1 1/4" dia.**
- **It has been glued with Epotek 301-2 epoxy on entire surface of cookie.**

FBLOCK placed on Fbox base

M. McCulloch and J. Va'vra

- **This is the most difficult step in the Fbox assembly. Done perfectly.**
- **Next step: start assembling Fbox.**

Electronics for the prototype

J. Va'vra, G. Varner

- **<u>Boundary conditions:</u>**

a) **Hawaii BLAB3 electronics had an amplifier built in. Unfortunately, this electronics does not work.**

b) **French electronics will not be ready until next year.**

- <u>**TWO OPTIONS TO PROCEED**</u>:

  a) **With help of SLAC electronics group, I am pushing building SLAC amplifiers.**
     Gary will supply IRS-2 waveform digitizer boards
     We are planning for a readout of 12 H-8500 tubes, i.e., need 60 boards
     Target date: June 15

  b) **If this will not not work, then we will put in 7 BLAB2 electronics packages.**
     This package has known timing resolution problems, but it would get us going.

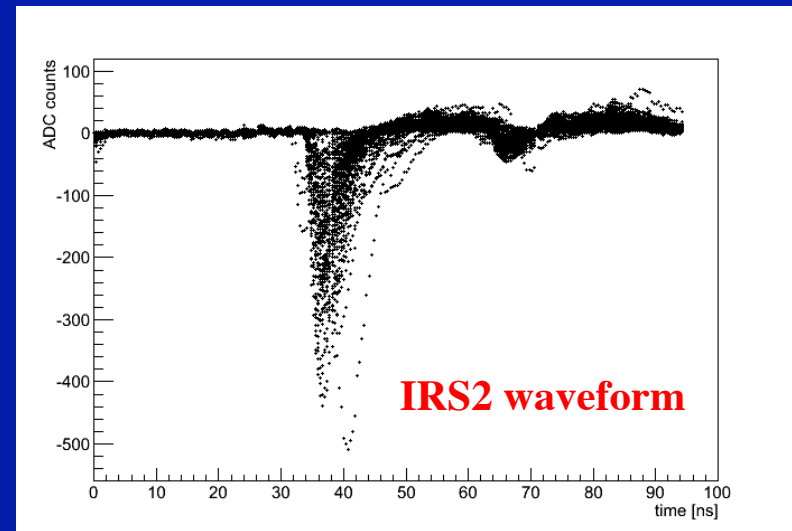# Test of IRS2 electronics with SLAC amplifier on H-8500 PMT

K. Nishimura

Jerry – SLAC amplifier in scanning setup:
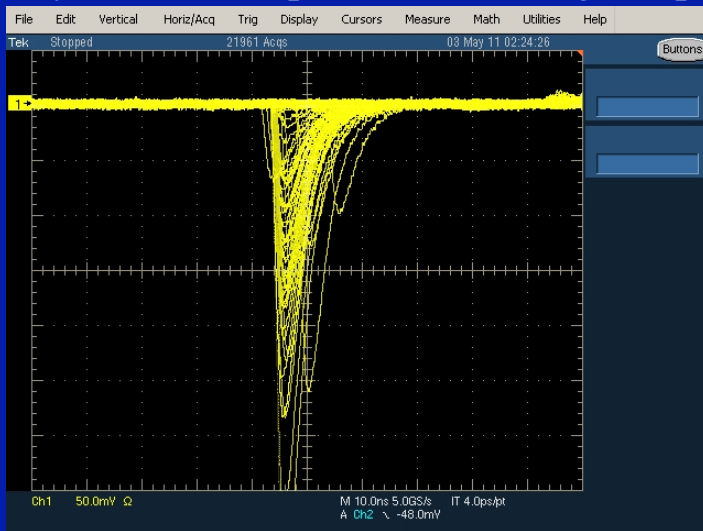
(Single photoelectrons in SLAC scanning setup)

Kurtis – Check of IRS2 in Hawaii laser setup:
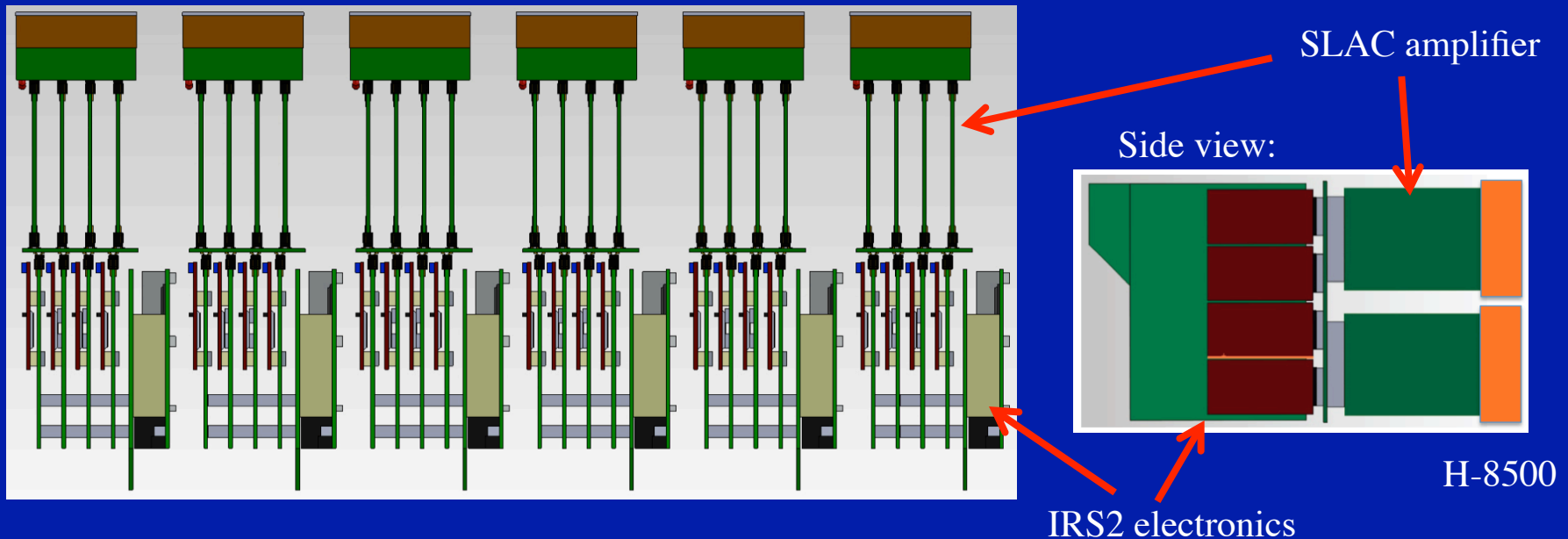

IRS2 waveform

(Wiggles due to poor setup, I am told)

- **Verify that the IRS2 digitizer would work with the SLAC amplifier.**
- **Test done with single photoelectrons.**
- **Based on this result we have decided to go ahead and build 65 boards.**

SLAC amplifier + Hawaii IRS2 digitizer

M. Andrew, J. Va'vra

Top view:

SLAC amplifier

Side view:

IRS2 electronics

H-8500

- **12 H-8500 tubes altogether.**
- **Each IRS2 package handles 2 SLAC amplifiers & 2 H-8500 tubes.**
- **Benefit of this electronics: will have time & pulse height on every pixel.**
- **It is crucial to have timing work to a level of ~200 ps, otherwise it is wasted effort.**
- **Can use the already built G-10 detector holder.**

FDIRC electronics with IRS2 digitizer

J.Va'vra with input from D. Roberts & M. Andrew

Overlay a
G-10 detector
holder drawing
with Doug's
MC display
drawing
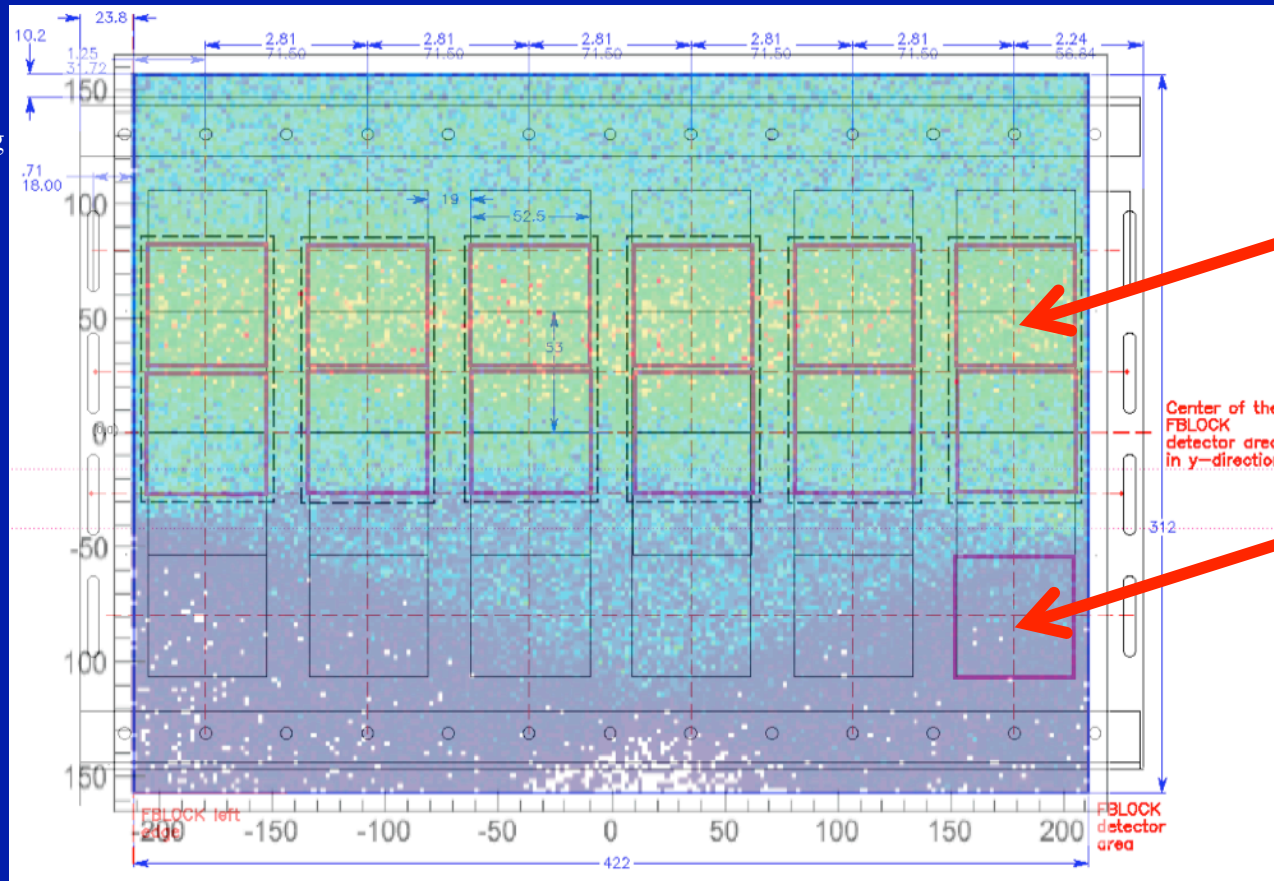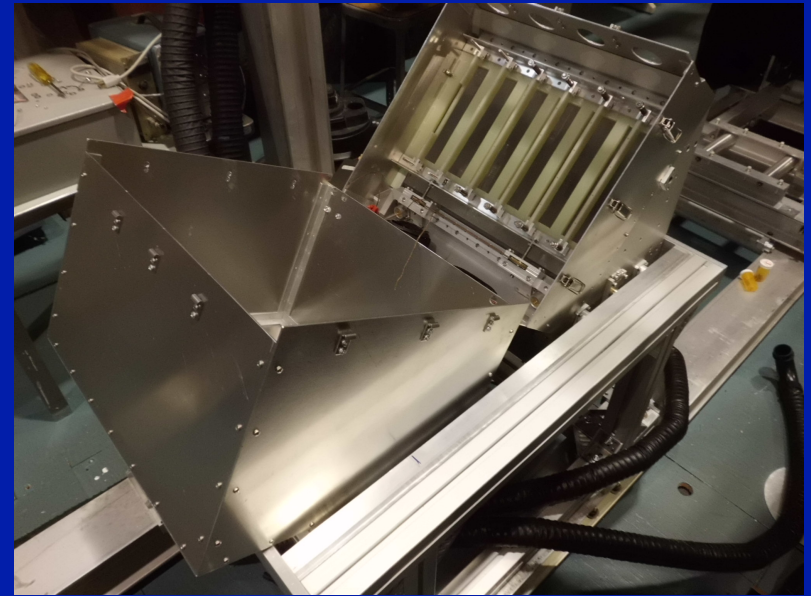

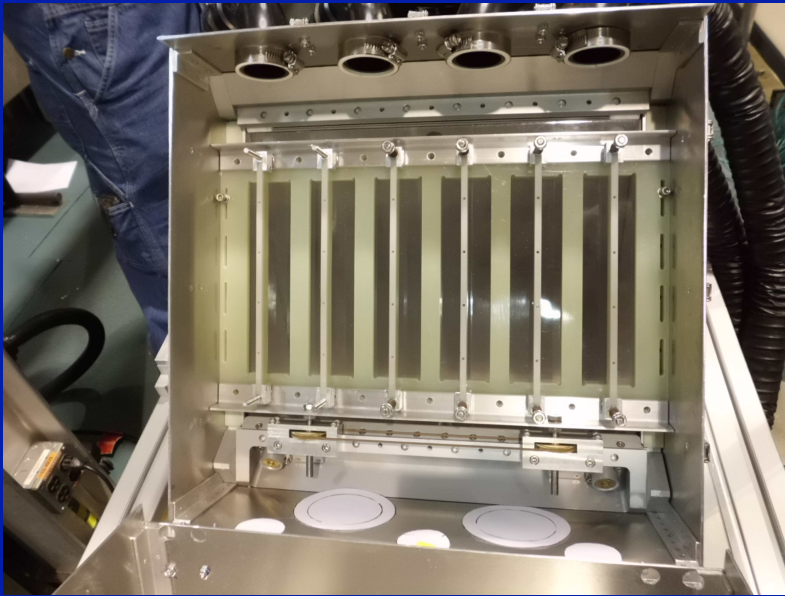IRS2 double-package handles two H-8500 tubes

H-8500 tube for analog monitoring

- **12 H-8500 tubes, one tube for analog monitoring.**
- **Pixel location will be available in " Critical_dimensions_v6.pdf ".**

Mechanical trial test of Fbox in CRT

M. McCulloch and J. Va'vra

G-10 holder and enclosure:

- **IRS2 electronics would be compatible with already built G-10 holder.**
- **In this trial test used the Fbox with the plastic FBLOCK built in Padova and Bari.**

FDIRC background at full luminosity

J.Va'vra, last collaboration meeting

| Method	Person	Rate per double-pixel from the bar box, i.e., <u>from active volume</u>	Rate per double-pixel from the Photon camera <u>if not shielded</u>
Real MC simulation using a proper treatment of optical photons	Alejandro, Doug, Andrea	~ 85 kHz	~ 550 kHz
MC simulation using a simple treatment of optical photons	Riccardo	~ 67 kHz *	~ 400 kHz *
Empirical scaling from Belle-I by quartz volume and as Lumi-term	Jerry	~ 75 kHz *	~ 120 kHz *

* Apply a factor of 2 reduction for a photon loss on optical surfaces

• **We clearly need to shield the photon camera contribution.**
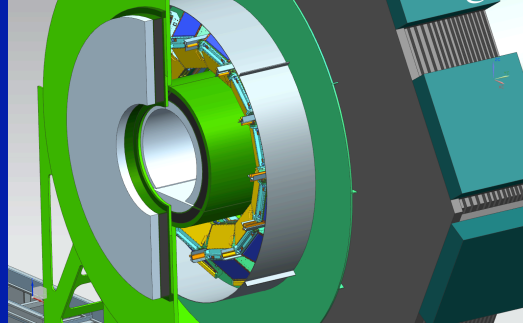
FDIRC shielding

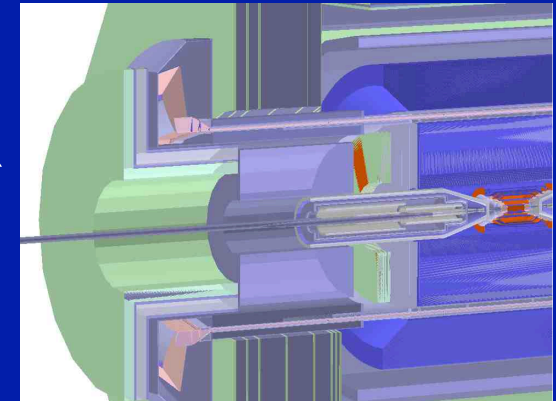J. Va'vra, M. Benettoni, A. Perez

Jerry: concept
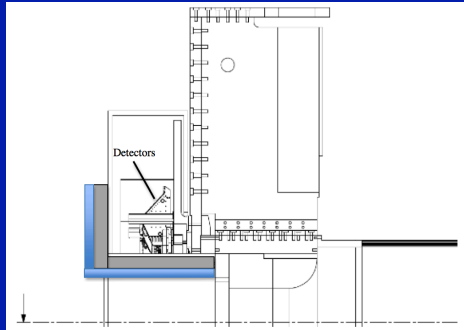
- 10 cm thick Boron-loaded polyethylene
- 10 cm lead in between two 2.5 cm-thick steel plates

Massimo: mechanical design
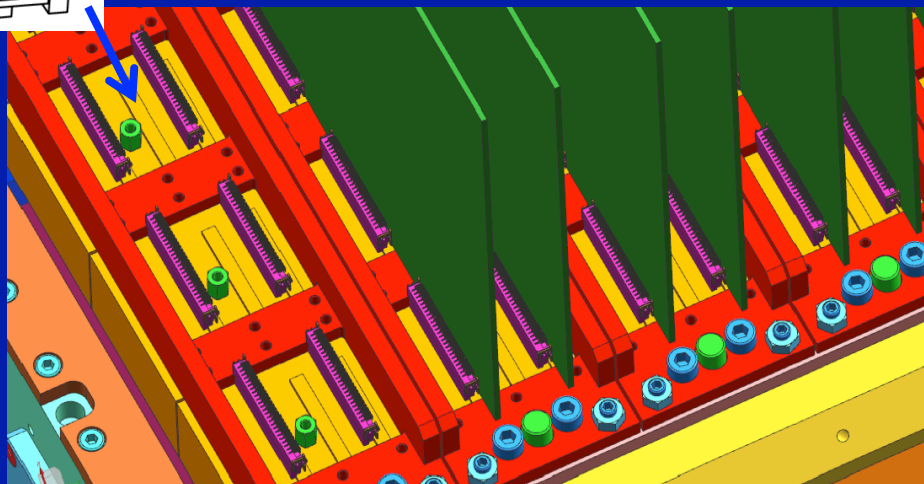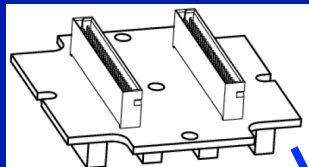

Alejandro: Bruno implementation

Requirement:

a) Reduce photoelectron rate from the FBLOCK.

b) Protect FPGA electronics from neutrons.

c) Need easy access to electronics.

Note: To handle neutrons correctly one needs to cover much larger area with neutron absorbers.
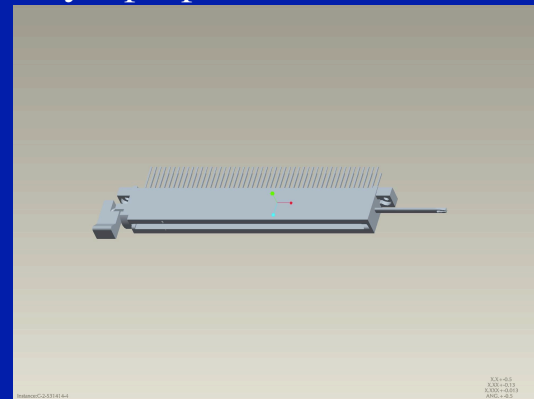
Discussion about the motherboard

Ch. Beibeder, M. Benettoni, G. Simi, J. Va'vra


Jerry's proposal: ZIF connector

- **Each PMT will have its own motherboard, which will be aligned so we can insert a large size electronics card.**

- **We has discussion whether we need to have ZIF connectors (zero-insertion-force connectors). We used it on CRID detectors.**

- **Christophe is assuring me that there is not going to have a problem since the cards will have rails and insertion tools.**
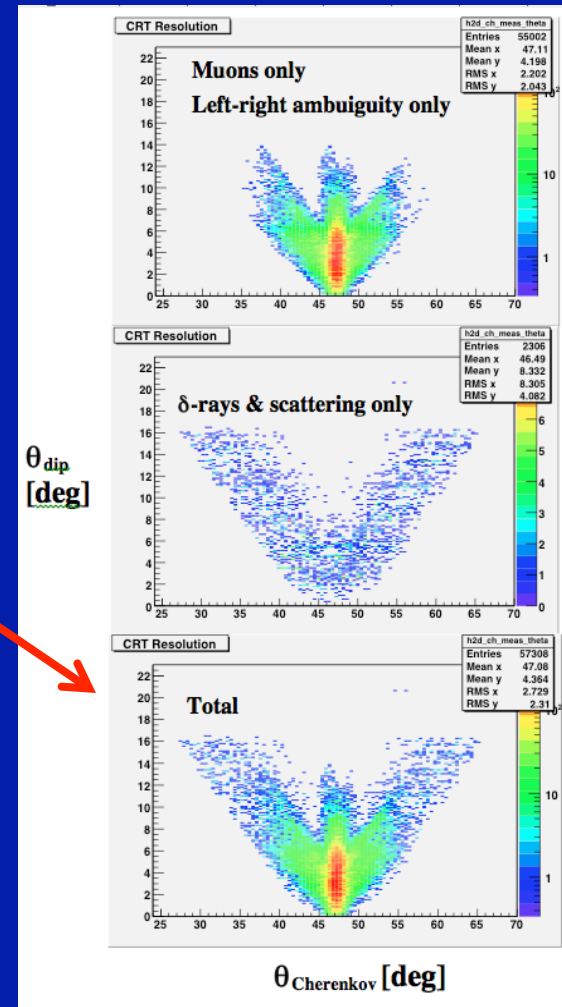
Analysis of the 1st FDIRC prototype

B. Bay, D. Shtol, J. Va'vra

Jerry: CRT data analysis

B. Day: CRT MC simulation
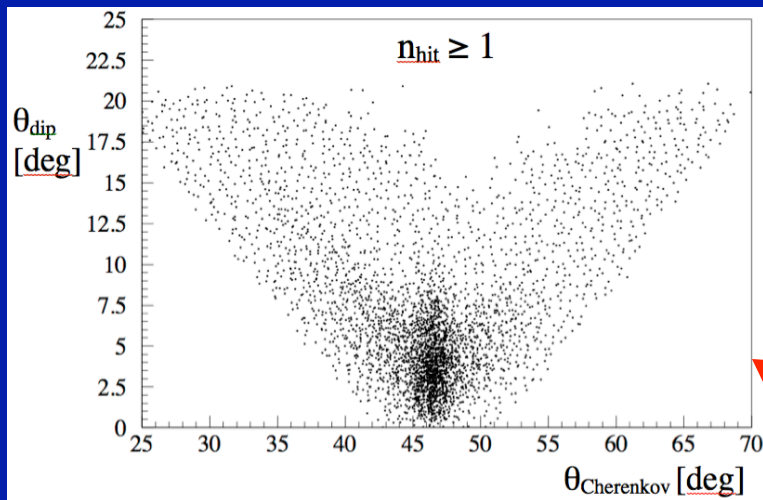
- **Tails arise <u>mostly</u> from left-right ambiguity.**
- **In addition there is contribution from the background from showers accompanying muons, delta-rays, and scattering in the bar.**
- **In the 1st FDIRC prototype we have only 2 ambiguities (there is no wedge).**

FDIRC optics published in "SLAC Today"

https://news.slac.stanford.edu/features/slac-physicists-build-prototype-particle-identification-detector

FBLOCK:

Summary

- **QC the FBLOCK and Wedge finished.**
- **Learned how to handle heavy & fragile FBLOCK optics.**
- **Started to assemble Fbox.**
- **The target dates:**
    - Fbox assembly: April
    - FDIRC assembly in CRT: May
    - SLAC/IRS2 electronics: June 15.
    - Hope to start initial taking some data in June: July.