March 20th, 2012
SuperB meeting
Frascati

Update on Strasbourg activities

on CMOS pixel sensor (CPS) developments for the SuperB SVT

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current work plan: chip design

1. Status

- The Strasbourg PICSEL group is involved in several projects (ALICE...).
- **New specifications by ALICE** for their CDR

  ➛ impact the ITS pixel sensor developments:

  · former 8 kHz Pb-Pb collisions: requiring a read-out time of 50 µs,

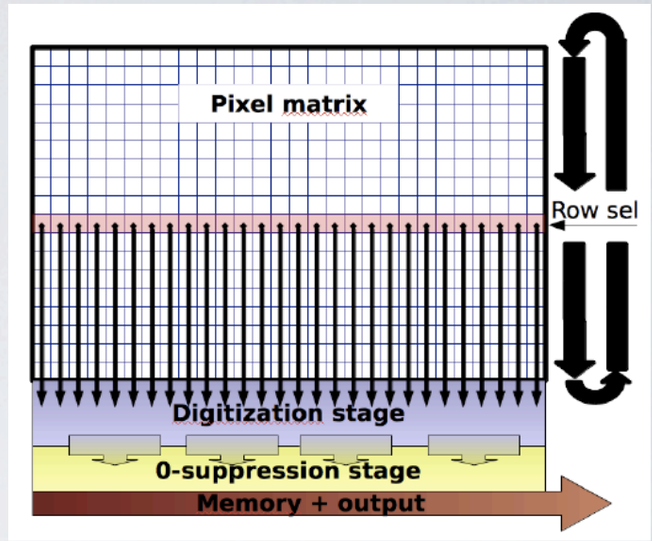
  · have become now 50 kHz Pb-Pb: read-out time has to be < 10 µs.

➛ focus on 0.18 µm HR CPS with r.o. time < 2 µs (AROM sensor),

in very good synergy with what is also required by the SuperB Layer-Ø.

current work plan: chip design

2. State-of-the-art CPS



- MIMOSA-26 equipping the EUDET beam telescope (FP-6),
  MIMOSA-28 currently assembled on the STAR-PXL detector at RHIC.
  - 0.35 µm process with high resistivity epitaxy.
  - fabricated in 2008-2010: > 90 sensors tested with different features.
  - detection efficiency ~ 100 % for very low fake rate (~10^{-4}).
  - in-pixel amplification and CDS.
  - end-of-column discrimination and 0 suppression (digital output).
  - **rolling shutter read-out:** pixels grouped in columns, readout in // ➔ no dead-time
  - read-out time: **200 ns/row** ➔ ~ 100 µs ➔ suited for > 10^6 particles/cm^2/s
  - power dissipation: **150-250 mW/cm^2**

sensor name	sensitive area (mm^2)	pixel pitch (µm)	spatial resol. (µm)	number of rows	read-out time (µs)	power dissipation (mW/cm^2)
MIMOSA-26	10.6x21.2	18.4	~ 3	576	~100	150
MIMOSA-28	19.2x19.9	20.7	~ 3.5	928	~200	250

current work plan: chip design

3. AROM

- Performances of a given architecture
  = global optimisation.

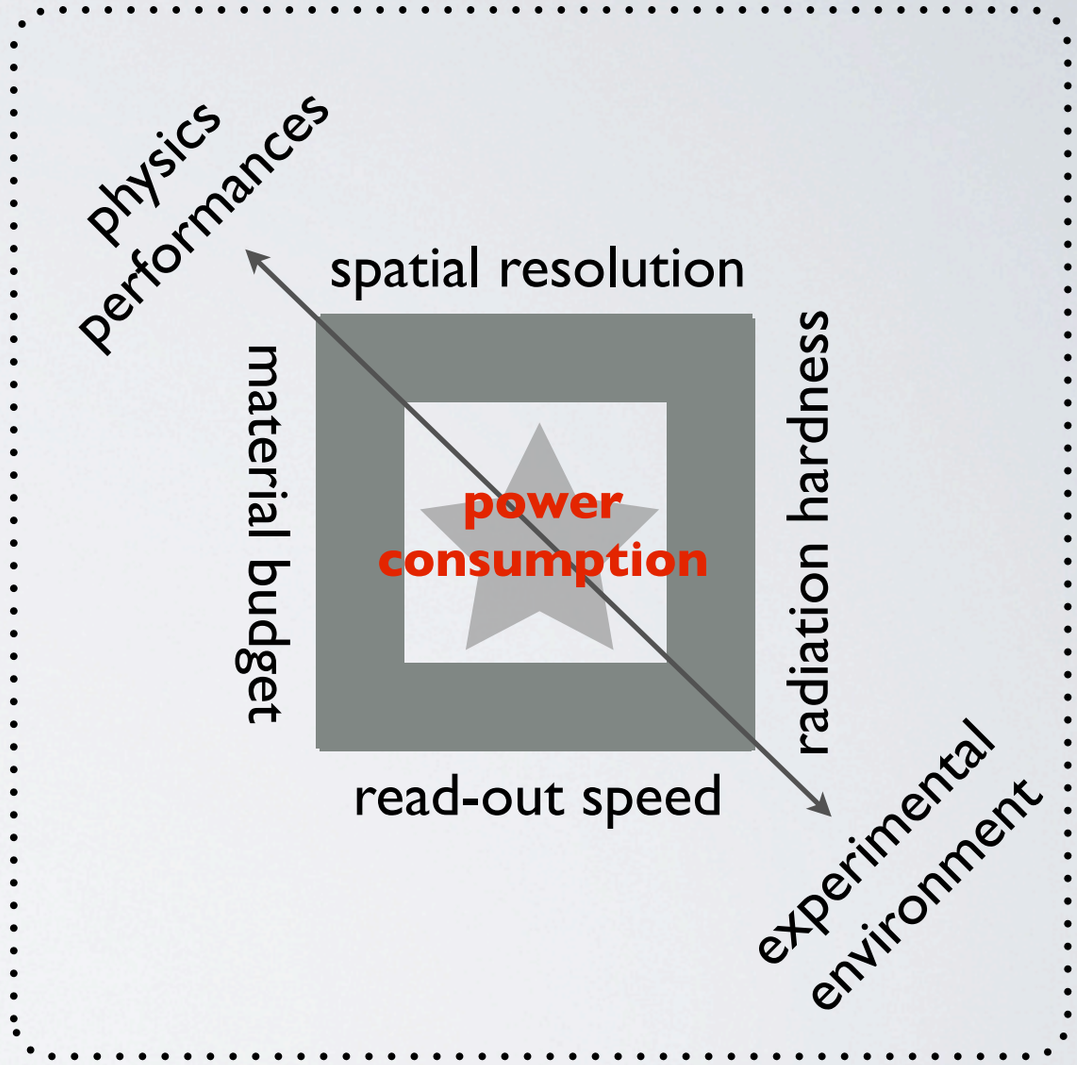
- Rolling-shutter architecture
  ➛ low power consumption

➛ **Modify MIMOSA to shorten the r.o. time to a few µs while keeping the power dissipation low = AROM:**

Accelerated ROlling-Shutter Mimosa chip

- The road to design AROM:
  - start from the state-of-the-art CPS (MIMOSA),
  - migrate to 0.18 µm process,
  - elongate the pixel ➛ less rows in the pixel array
  - do in-pixel discrimination,
  - optimise the rolling-shutter.

➛ **aimed read-out time < 2 µs adapted to hit rates > 10^7 hits/cm^2.**

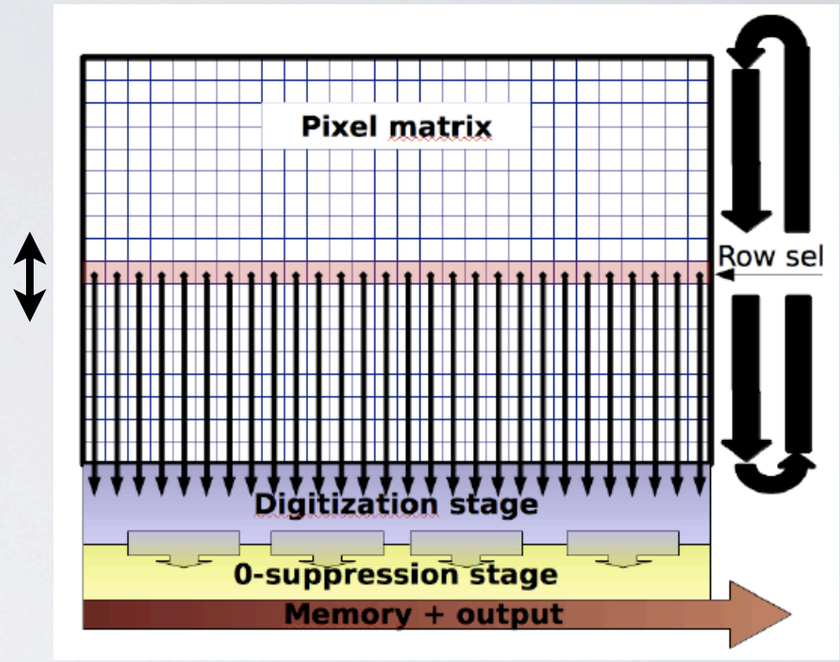


This is an extrapolation from achieved and beam-tested chips + simulations:

current work plan: chip design

4. Elongated pixels

- Larger pixel size in one dimension
  ➛ less rows to be read-out.
- Pixel length of 80 µm (instead of 20 µm)
  ➛ **r.o. speed increased by a factor of 4**.



Main limitations:

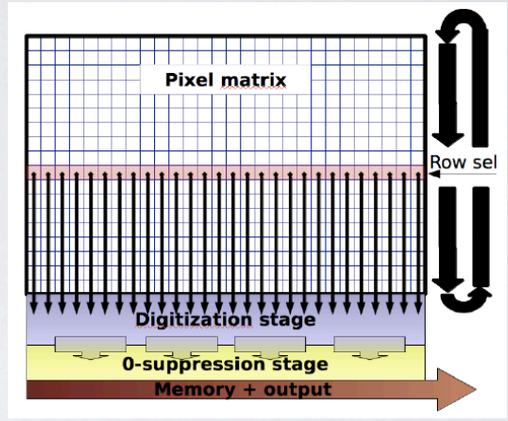
· Loss in spatial resolution ?
  - test of 18.4x73.2 µm^2 pixels with SPS 100 GeV beam
    ➛ $\sigma_{s.p.}$ = 5-6 µm in both direction (diodes are staggered).
  - **use of a double-sided ladder** ➛ factorisation of the requirements:
    · one side is optimised for time stamping,
    · the other side takes over the spatial accuracy.

· Charge collection efficiency and radiation tolerance ?
  - large pixel sizes ➛ more charge carrier recombinations (non-ionising rad.)
  - lower sensing diodes density ➛ leakage current increases (ionising rad.)
    ➛ optimise the balance between number of sensing diodes & S/N.

current work plan: chip design

5. In-pixel signal discrimination

- Larger pixel size and 0.18 µm process ➛ space to incorporate a discri. in each pixel
  ➛ **r.o. speed increased by a factor of ~2:**
  200 ns becomes ≲100 ns needed to read one row.



- Power consumption remains low:
  - only signal above threshold is being transferred,
  - signals are binary,
  - rolling-shutter: only read-out column is powered.

  ➛ estimation: **< 70 mW/cm** = f(number of columns) at a given time.
  Independent of the number of pixels/columns (i.e. number of rows).

- In MIMOSA CPS, discriminators are at the end of each column (~0.3 mm wide band)
  ➛ in-pixel discriminators result in more sensitive area surface.

- Pixel signals transmitted to the periphery through metal layers
  ➛ need enough metal layers.

current work plan: chip design

6. Optimised rolling-shutter architecture (1)

- **Subdivide the sensitive area in several sub-arrays read-out in //:**

· Results in reducing the number of pixels in a column: i.e. reducing the number of rows to be read-out successively.

· N sub-arrays ➛ r.o. time shortened by a factor N.

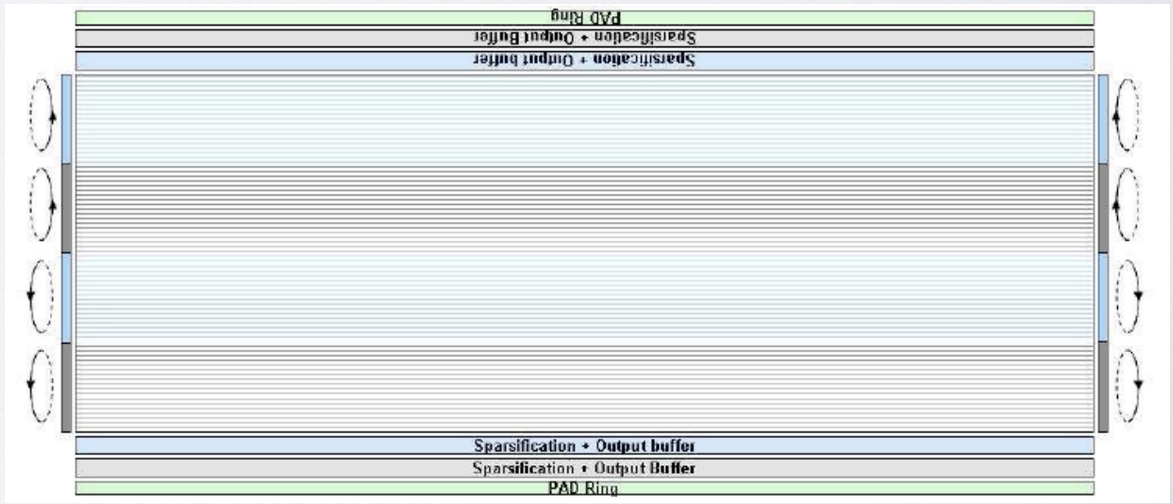
· Need of several sequencers to steer these sub-arrays:
implementation outside the sensitive area ➛ ~100 µm insensitive wide band.
Not an issue because of double-sided layers with only one side (time-stamp side) with this insensitive band.

· Zero-suppression is more complicated.

· Power consumption = f(sub-arrays).

➛ optimise the number of sub-arrays:
- r.o. time vs. power consumption,
- r.o. time vs. sparsification circuitry.

2 sub-arrays double-sided read-out: r.o speed accelerated by a factor of 2.



current work plan: chip design

6. Optimised rolling-shutter architecture (2)

- **Read several rows simultaneously:**

  rolling shutter architecture: r.o. time = number of rows x 200 ns.

  ➛ accelerate the frame read-out by encoding several rows simultaneously:
  expected acceleration: **factor of 4** (4 rows simultaneously).

- Without in-pixel discrimination:

  · 10 µm wide discriminators at the end of each column

  ➛ pixel size (i.e. column width) constrains the number of discri. we can implement:
  10 µm x number of rows read-out simultaneously ~ pitch (pixel width).

- With in-pixel discrimination:

  · Limitation of the number of rows r.o. simultaneously comes from the data processing and data transmission rate (capabilities of the sparsification circuitry).

  · Could be improved:

  - by using an external trigger signal,
  - by changing the current logic of the sparsification: address pictograms formed by the signal clusters over several consecutive rows.

current work plan: chip design

7. AROM expected performances

- Concrete example to achieve a **~1.6 µs read-out time** with rolling-shutter:
  - Pitch 20x80 µm^2, in-pixel discrimination (100 ns/row),
  - 2 sub-arrays read-out in // from 2 opposite sides of the sensor, each sub-array = 72 rows ➛ 5.76 mm in height,
  - 4 consecutive rows read-out simultaneously in each sub-array.
  - Dimension of sensitive area: 11.5x30 mm^2.

    due to number of rows
    ➛ if increased: will increase the read-out time
    and the power dissipation

  - Power dissipation of the whole sensor: ~ 900 mW/cm
    sharing between pixel array and periphery is 2/1.

- For large surfaces (outer layers):

power dissipation may limit the number of rows read-out simultaneously

➛ read-out time of 6-7 µs may cope with lower background hit rate at larger radii.

Several possibilities:

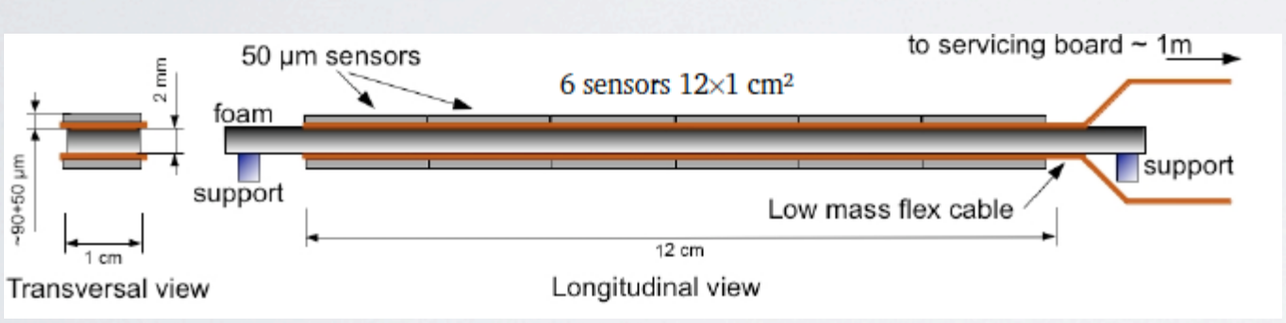
- 6.4 µs for a sensitive area of 20x30 mm^2 (more rows but same pitch, same number of sub-arrays and of consecutive rows read-out).
- Only read-out 2 consecutive rows ➛ r.o. time ~ 3 µs.
- Enlarge the pitch to 40 µm ➛ r.o. time ~ 3 µs.

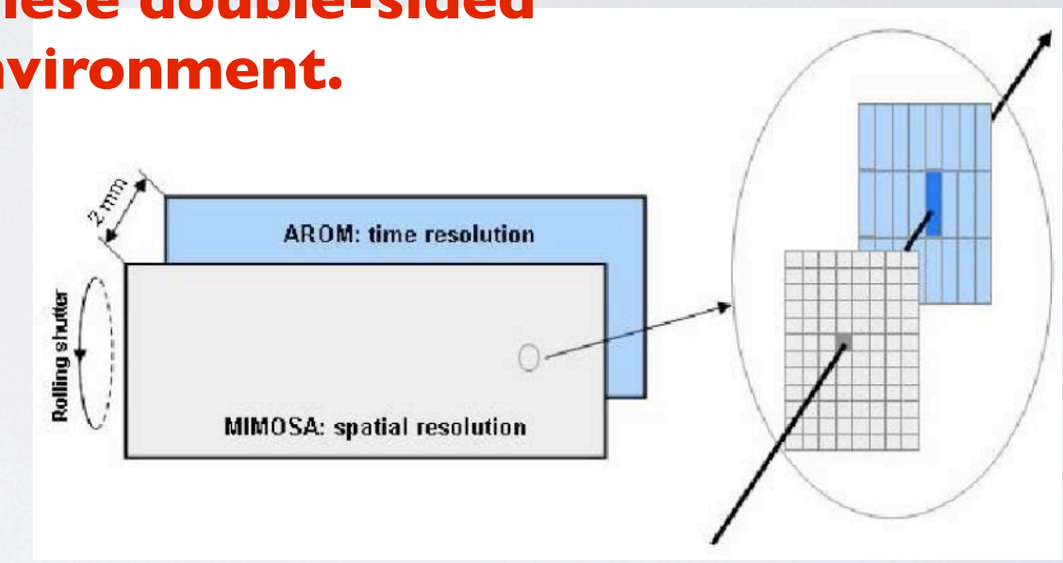
current work plan: system integration

- AROM chip with ~2 μs read-out time ➛ $\sigma_{s.p.}$~6 μm only.

➛ **double-sided ladder equipped with AROM chips on one side and MIMOSA chips on the other side** ($\sigma_{s.p.}$~3 μm if 20 μm pitch).

➛ **work on new tracking algorithms using these double-sided ladders, more efficient in high densitiy environment.**





- PLUME double-sided ladder: **total material budget ~0.35 % of X_0** for 2 points.

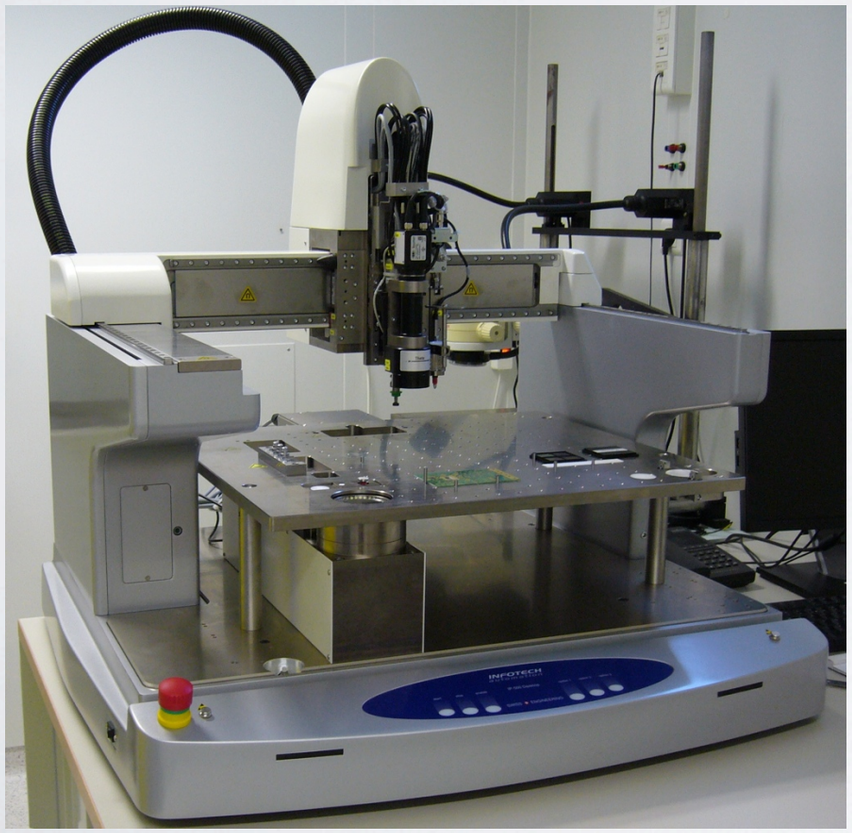
more information:

- http://www.iphc.cnrs.fr/PLUME.html
- previous report at SuperB collab. meeting from Dec. 2012:
  - 2010 prototype equipped with MIMOSA CPS,
  - material budget 0.6 % of X_0,
  - results from Nov-2011 test with CERN-SPS beam.

latest news and next steps

1. System integration aspects

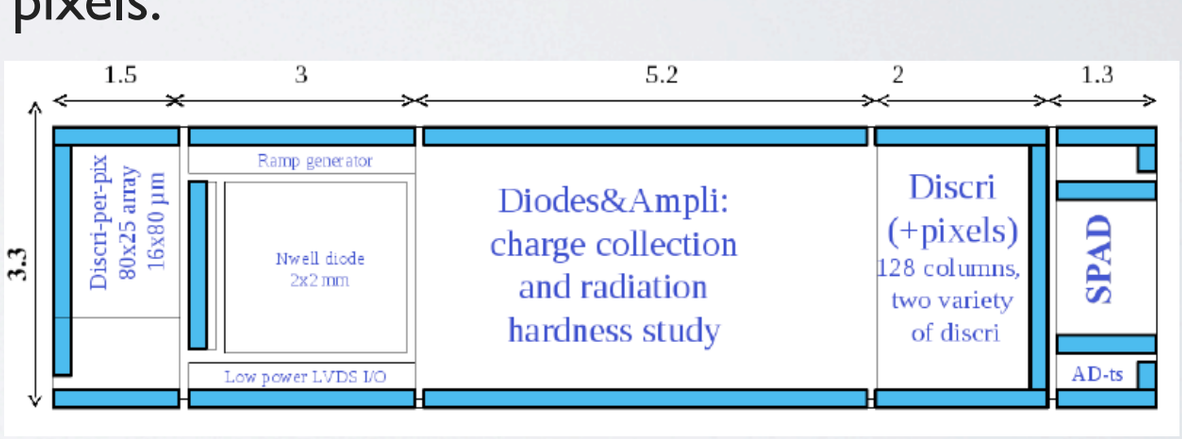
- System integration aspects:
  - New machine to place and glue the sensors.
  - Assembling under way of the 2012 prototype with new cable (copper traces) to reach 0.3 % of X_0.
    ➛ achievement in Summer 2012,
    test with CERN-SPS beam foreseen end of 2012 / early 2013.



latest news and next steps

2. Chip developments

- MIMOSA-32: **validation of the 0.18 µm technology**
  - Submitted in Oct. 2011, delivered in January 2012.
  - Prototype subdivided in several blocks:
    - Explore pixel sizes (20x20, 20x40 and 20x80 µm^2) and charge amplification / collection system (diode sizes, diode types, pre-amplifiers).
    - Explore radiation hardness: 1 sub-array of 128 columns with discriminators at their end.
    - Explore in-pixel discrimination: 16x80 µm^2 pixels.
  - Test plans:
    - lab. tests in April 2012,
    - analog output in beam test in June 2012,
    - digital output in beam test in Aug. 2012.



- MIMOSA-22 THR: **validation of the optimised rolling-shutter architecture**
  - Submission foreseen July 4th, 2012.
  - 2 different chips: 2 rows read-out simultaneously in rolling-shutter mode, w/ and w/o in-pixel discrimination (pixel pitch 22x44 µm^2).
- Next submission: foreseen in Oct./2012 or Dec./2012 to test sparsification for 2 and 4 // rows.

conclusion

- Strasbourg activities focused on modifying MIMOSA in order to:
  - shorten the read-out time to **1.5 µs**,
  - while keeping the power consumption low: < 1 W for 1 cm of row read-out with rolling-shutter.

➢ AROM CMOS pixel sensor.

Such an optimisation is based on the rolling-shutter read-out method.

- Proof of principle has to be done.
  Several submissions already done or foreseen.

- Advantage of double-sided ladders equipped with CMOS pixel sensors on both sides:
  - one side provides the time stamp,
  - the other side is optimised for spatial resolution.

➢ develop new tracking algorithm to take advantage of (several) layers of double-sided CPS ladders:
  - more efficient in a high density environment,
  - allow to relax some performances of the sensors.

more material

tracking with double-sided CPS ladders

Example of ILC-VTX