



3rd SuperB Collaboration Meeting



SVT activities at Valencia

(introduction and plans)

Arantza Oyanguren
(IFIC – Valencia)

associated with



Outline

- Infrastructure: the IFIC (ATLAS) installations
- Purpose
- People
- Conclusions

The IFIC's lab.

80m² clean room *class 10000* (ISO7) with 25m² *class 1000* (ISO6), 1°C controlled temperature and ±5% humidity:



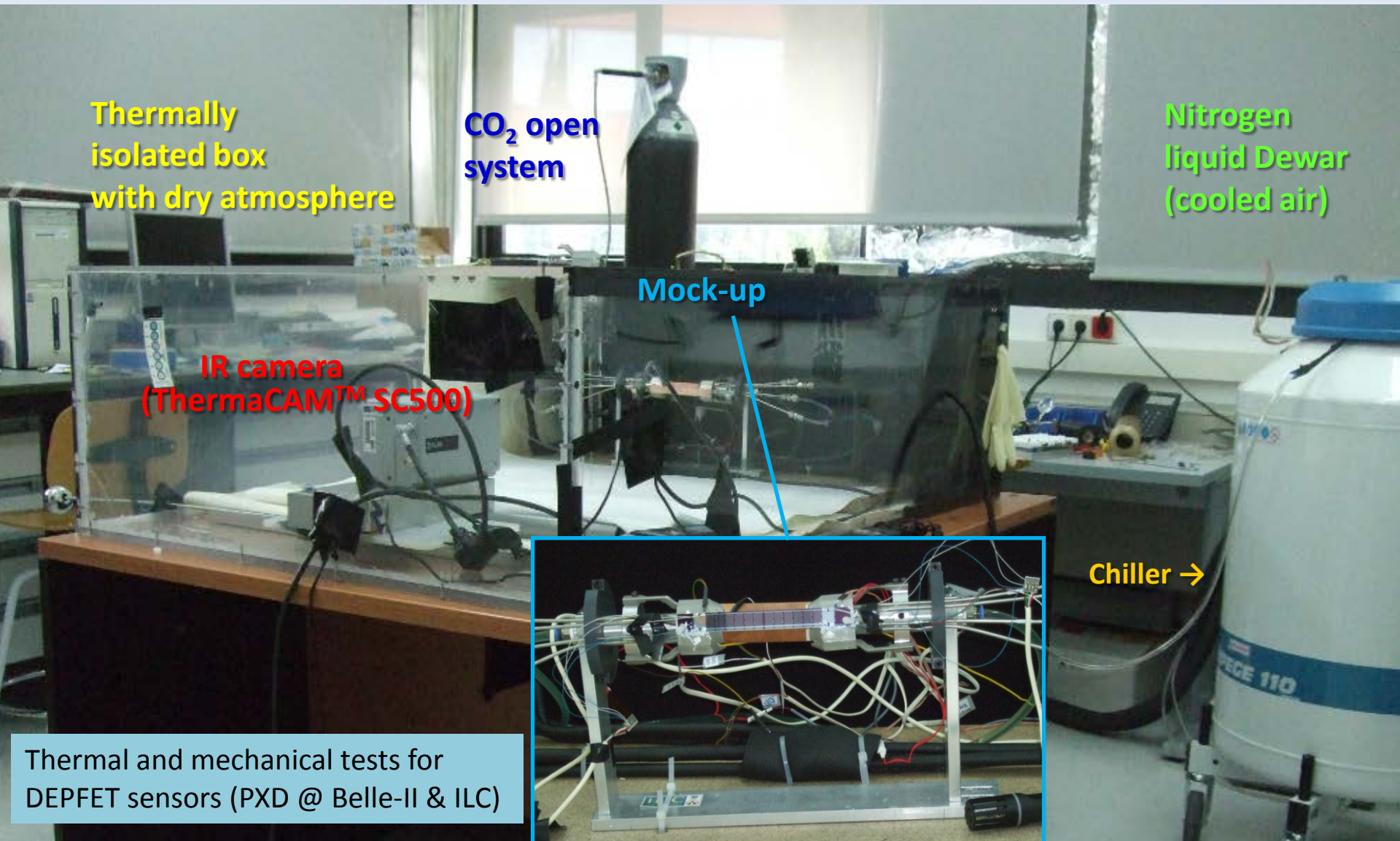
Two wafer probe stations: 1 manual, the other automatic/programmable
Wire-bonders: one fully automatic, one manual and one test bonder
Laser interferometer system, glue dispenser, sensor test cage

→ detector characterization, module assembly, bonding, metrology and electrical QA test

[ATLAS-SCT endcap module testing, assembly and³QC]

The IFIC's lab.

+ dedicated laboratory room with an open CO₂ cooling system, N₂ dewar, climatic chamber and thermal camera: [thermal tests](#)



Thermally isolated box with dry atmosphere

CO₂ open system

Nitrogen liquid Dewar (cooled air)

Mock-up

IR camera (ThermaCAM™ SC500)

Chiller →

Thermal and mechanical tests for DEPFET sensors (PXD @ Belle-II & ILC)

The IFIC's lab.

Mechanics workbench



CNC lathers and grinders with $\sim 5\mu\text{m}$ precision
MIG and TIG soldering machines,
3D CAD design
Visual and contact CMM with $\sim 1\mu\text{m}$ prec.

Electronics workshop



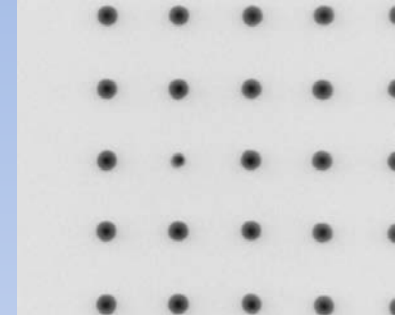
PCB design and fabrication (up 7 layers)

The IFIC's lab.

BONUS:

- To be delivered in June:

- A X ray machine
- Flip chip reworking station (TRESKY T-3000-FC3)

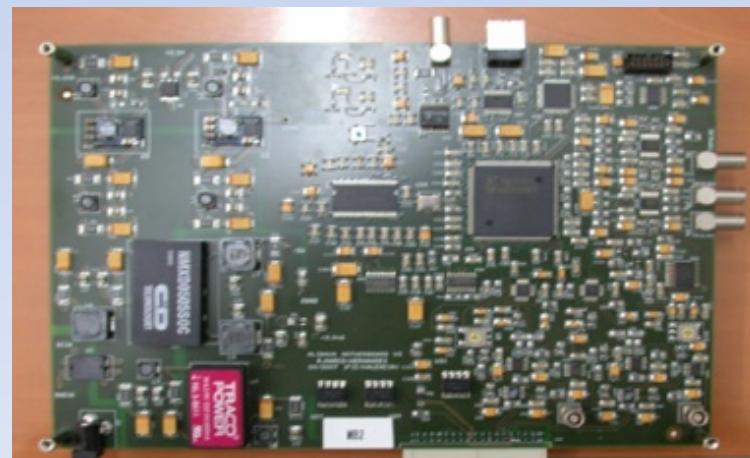
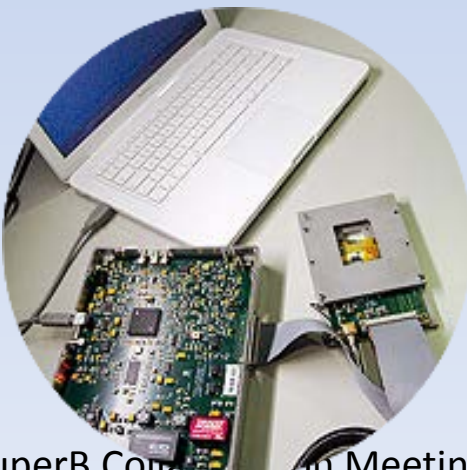


(Purchased by the U. Valencia, ordered by the DEPFET group)

- In addition:

A portable readout system for silicon microstrip sensors: **ALIBAVA**
(may be suitable for testing, test beams ...)

<http://www.alibavasystems.com/>



Purpose

- **Electronics** : FEE design and simulation

(eng. Jose Mazorra)

- Analog readout circuit design:

→ Development of peripheral blocks (voltage regulators and references)? .

→ Adaptation from CERN IP blocks?

- Electrical tests and characterization

At present:

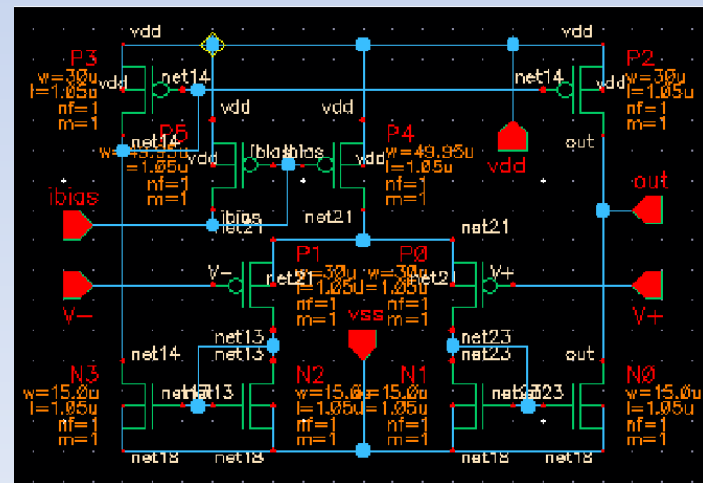
→ CADENCE IC Package (v6.1 & v5.10) license purchased at EUROPRACTICE

→ IBM CMOS8RF-DM (v1.8) design kit acquired from CERN

→ Software installed, configured and working

We want to contribute to the QC and QA of 1st prototype expected for end 2012

Technical support from the U. Barcelona engineers (LHCb group)



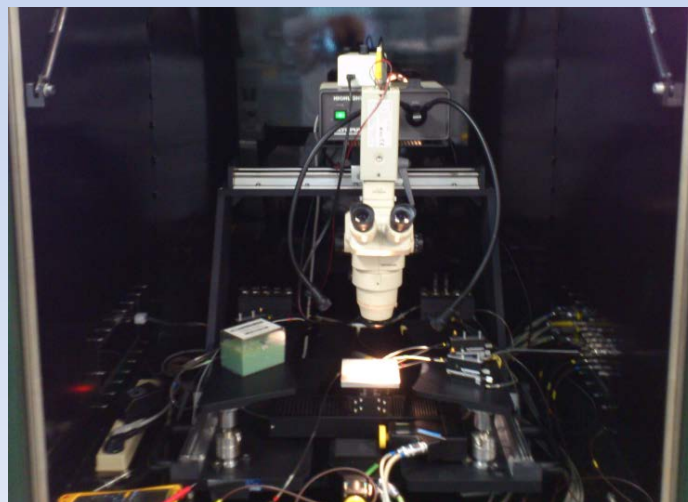
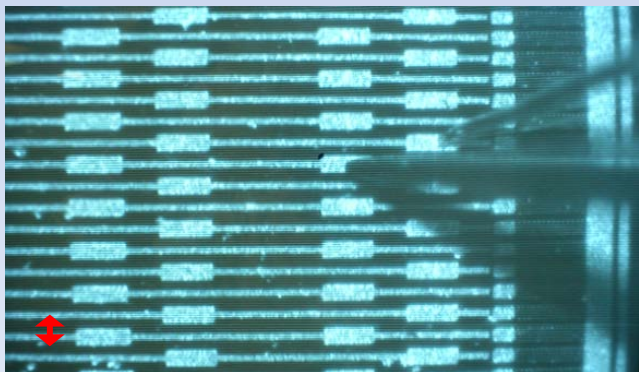
Purpose

- Microstrip sensors (SVT layers 1-5)

- Contribute to the sensor development for L1-L5
 - Electrical test and characterization
 - Fanouts?

At present:

- Setting the clean room up for our work
- Learning to work with 1st) the manual wafer probe station 2nd) the automatic one
 - Using damaged Si wafers from ATLAS, aiming to get practice with the tools
 - Defining actuation protocol
- Asking for a BaBar spare from Pisa for testing and re-characterizing



People (Valencia + U. Barcelona)

Valencia:

-Seniors:

Fernando Martínez-Vidal **(IP)** [Prof.]

Arantza Oyanguren [Ten. Track]

Victoria Castillo [Full Prof.]

Emilio Higón [Full Prof.]

Oscar Vives [Prof., theorist co-convener
 τ group]

-Engineers:

José Mazorra de Cos

-PhD students:

Pablo Ruiz Valls

U. Barcelona associates:

Lluís Garrido [Full Prof.]

Eugeni Graugés [Prof.]

David Gascón

Albert Comerma

Conclusions

- We are willing to contribute to the SuperB SVT layers L1-L5
 - FEE: Design, simulation and test
 - Sensors: Test and characterization, ...
- We have got the adequate installations, we need to get some practice with them
- We count with the support and expertise of the UB group
- Other topics where we could contribute:
 - Software
 - Thermal and mechanical tests