Peripheral Electronics

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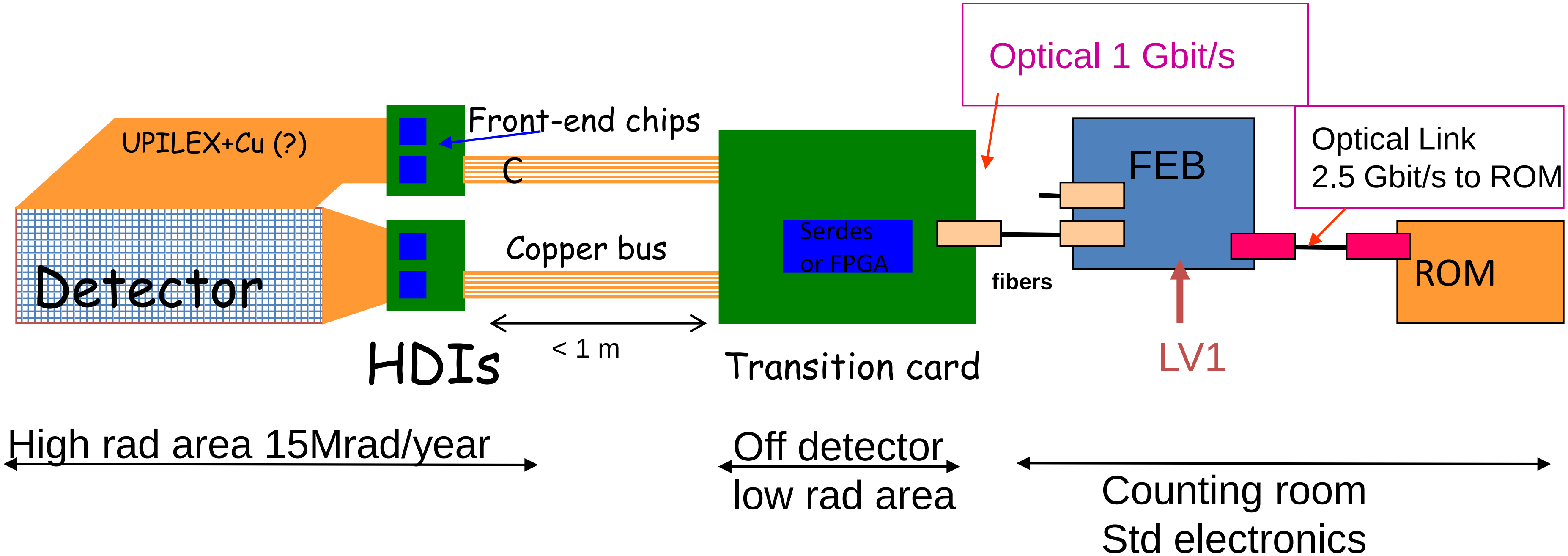
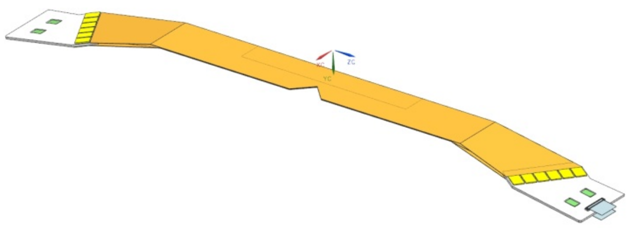
DAQ reading chain for L0-L5

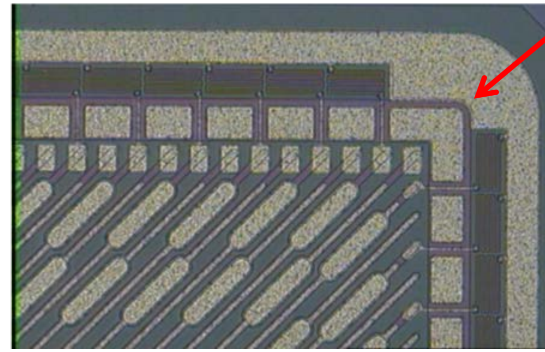


Area of interest

- → **fanout (layer0)**
- → **Copper bus**
- → **Estimate of "power lines" on Copper bus**
- → **Number of LVDS lines on Copper Bus**
- → **Transition card**
  - **numbers**
  - **what is on the transition card ....**

Fanout (layer 0)



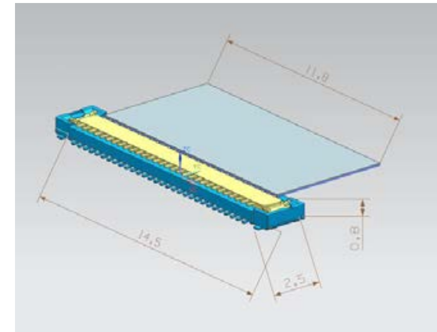


Absolute reference point (0,0) in scaling detector size

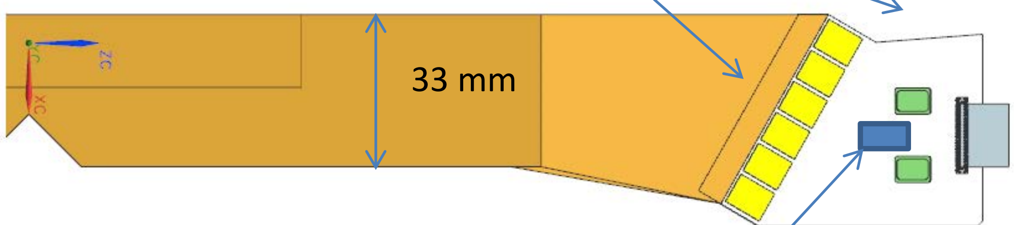
Design progressing on Aluminum/Kapton 2 layer fanout

- → Fanout min. pitch proposed is 71 um
- → Bonding always toward detector side
- → Some constraints applied on how traces match IC channel sequence
- → Fanout resistance estimate is still approximate ~ 0.85 ohm/cm (assuming Aluminum resistivity ~ 33 ohm x m x 10^{-9}). Capacitance not yet estimated.
- → Narrow pitch needed over a length of ~ 50 mm
- → Cern suggestions:
  - Minimize the area where the pitch is 71 um
  - Perform a test on one layer to verify reliability/consistency of pitch
  - Concern about bending such a fine lines (perform resistance test before and after bending) on first sample
  - Spread lines before reaching bonding
- → Overall fanout width 33 mm → It should fit in the existing CAD model of detector

Output connector has 0,4 mm pitch.
Goal is to use 70 contacts connector.
It could be increased to 80 contacts.
It will carry all copper lines (13 LVDS + power LV).
Not rated for HV.



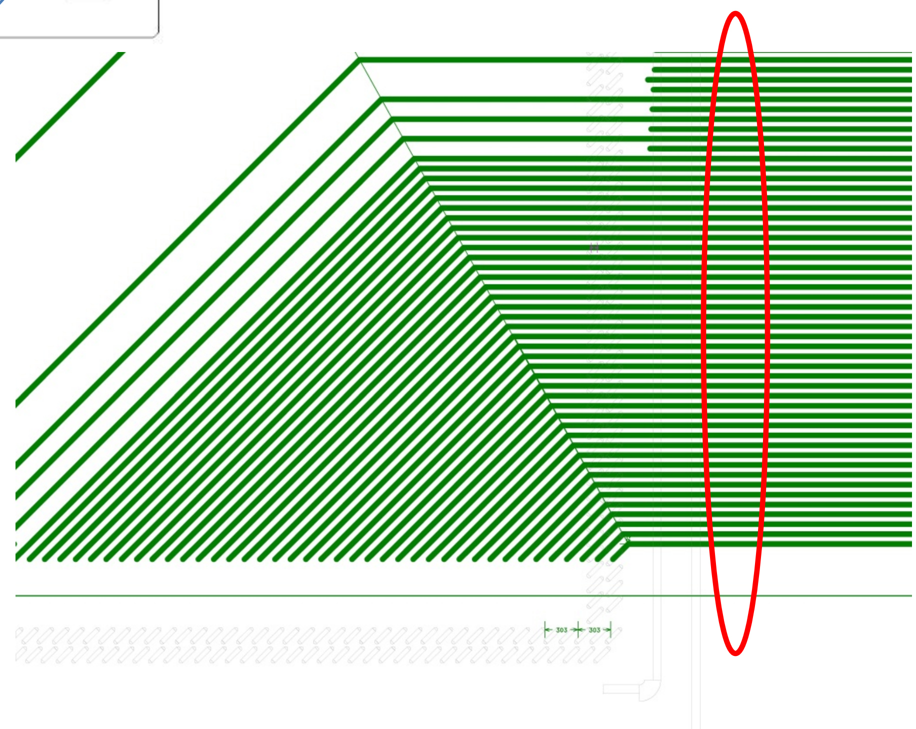
Larger pitch used near IC (~ 100 um)



Serializer

Simple geometry requested by CERN

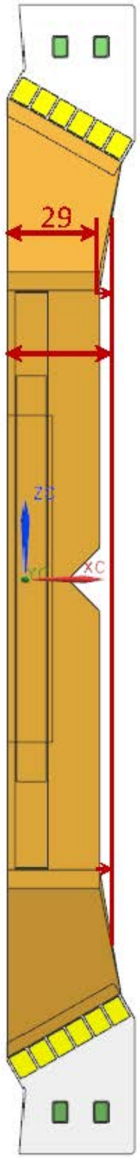
Mimimum pitch ~ 70 um

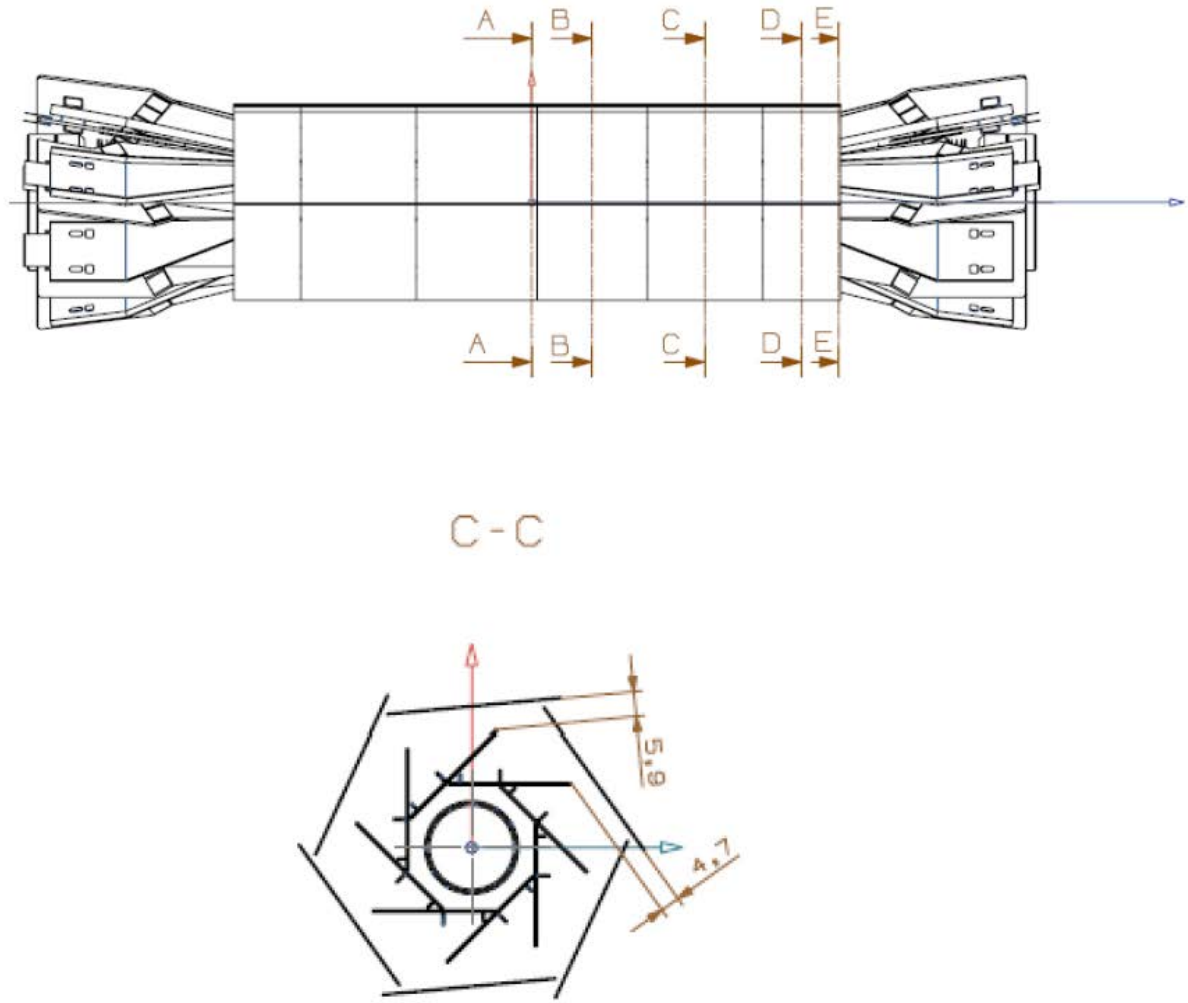


The layout of the fanout requires ~ 33 mm.
The artwork on the right will be discussed with CERN and eventually a prototype will be produced:

- Various pitches in same sample
- Important to have a corner and perform bending tests

Dimensional Studies

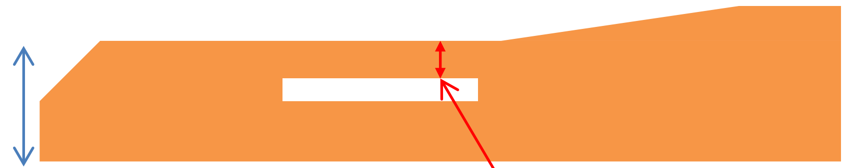




Two Layers Al Fanout: layout requires 33 mm

L1 - 30.5 mm

L2 - 29.9 mm



Bosi Design (mm)	29
Maximum Lateral Dimension (mm)	**33**
Cut out (mm)	1
Later dimension above Cut-out (mm)	13.1

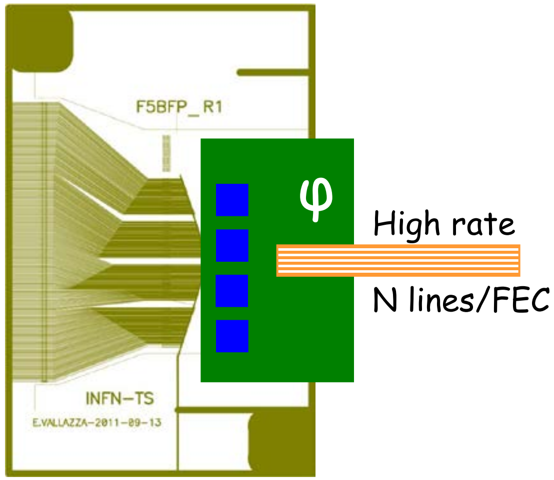
Additional Constraints

Layers	L1 (bottom Layer)	L2 (top Layer)	128 ch on L1 (over sensor)	128 ch on L2 (over sensor)
Overall Widht	33.00	33.00	13.1	13.1
Distance of last trace to border (2 sides)	0.60	0.60	0.3	0.3
Clearance around Cut-out (common to both Layers)	0.90	0.90	0.6	0.6
Clearance around Cut-out (additional for L2)		0.60		0.6
Cut-out	1.00	1.00		
Total "available" widht/layer	30.50	29.90	12.20	11.60

Pitch calculation with constraints applied

		L1 + L2 (over sensor)	Remaining widht	L2 (over sensor)
Overall Available widht (mm)	60.40	23.80	36.60	11.6
Number of traces	768	256	512.00	128
HV + GND traces	2			
Pitch (mm)	0.0784	0.0930	**0.0715**	0.0906

HDI and output bus



Minimal number of elements on HDI
(ideally only FE chips and possibly a serializer)

6 shared input lines:
Reset, Clock, FastClock,
Timestamp, Trigger, RegIn
1 shared output line:
RegOut
N lines x M chips in output
Ground and powering on the bus
Signal lines in standard LVDS
(CMOS to/from LVDS required on HDI if not provided on FE)

- HDI elements should be:
- Rad-hard characteristics dependent on chips
  - Requirement: > 5 Mrad/year
- Power dissipation: < 1 W/chip (guess-estimate, past values)
- *Option for a serializer on HDI*

Number of Transition Cards and Copper Bus

Layer		Module	HDI	Chip	Output Lines (180MHz) on 1 Face of the HDI	Copper Bus	Transition Card (TC)	Optical Fiber on Transition Card	GROS
L0	Top Bottom	8	16	6 6	12 12	32	16	32	32
L1	Z Phi	6	12	7 7	7 14	24	12	24	24
L2	Z Phi	6	12	7 7	7 7	24	12	24	24
L3	Z Phi	6	12	10 6	10 6	24	12	24	24
L4	Z Phi	16	32	5 4	5 4	64	16	32	32
L5	Z Phi	18	36	5 4	5 4	72	18	36	36
Total			**120**			**240**	**86**	**172**	**172**

2 copper bus for TC Layer 0,1,2,3

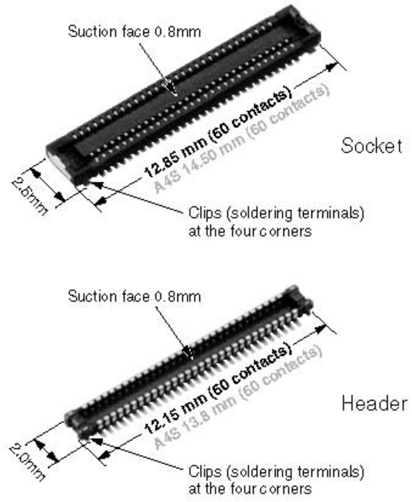
2 Fiber for TC

4 copper bus for TC Layer 4,5

Proposal: 1 Transition Card accept at least 2 Copper Bus !!!
Why? To increase size of TC → shown later
Number of LVDS lines on copper bus is limited !!!

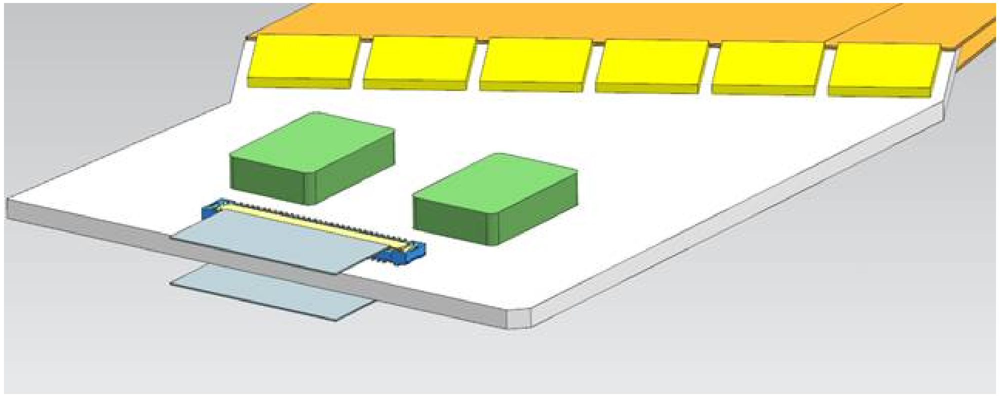
Copper Bus Structure

1.The world's smallest size* (width: 2.5 mm, Terminal pitch: 0.35 mm and Mated height: 0.8 mm)
The footprint when mated is down approx. 10% from our existing A4S model (60 contacts), contributing to the functionality enhancement and size reduction of target equipment.



Only rated 150 Volt

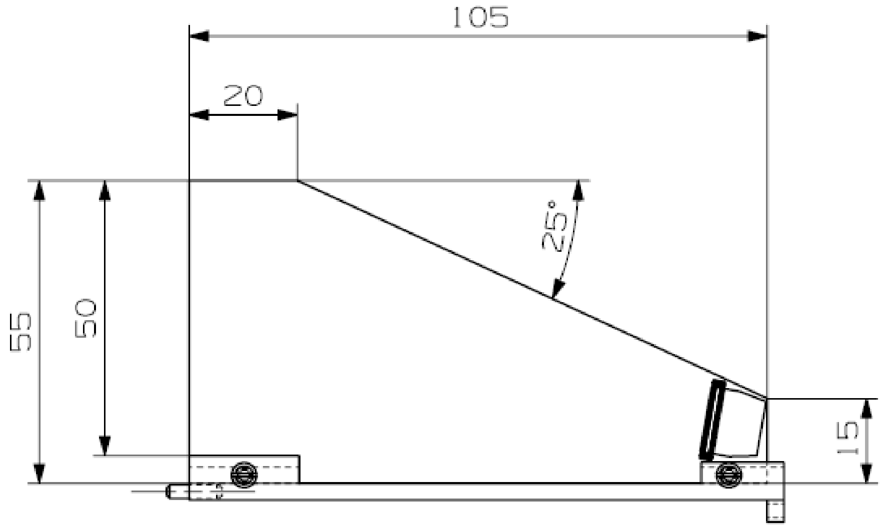
For various reasons the wisted pair wire solution I proposed in the past (magnet wires) is not as simple as I thought.
We will continue to study it but we need to investigate a different solution:

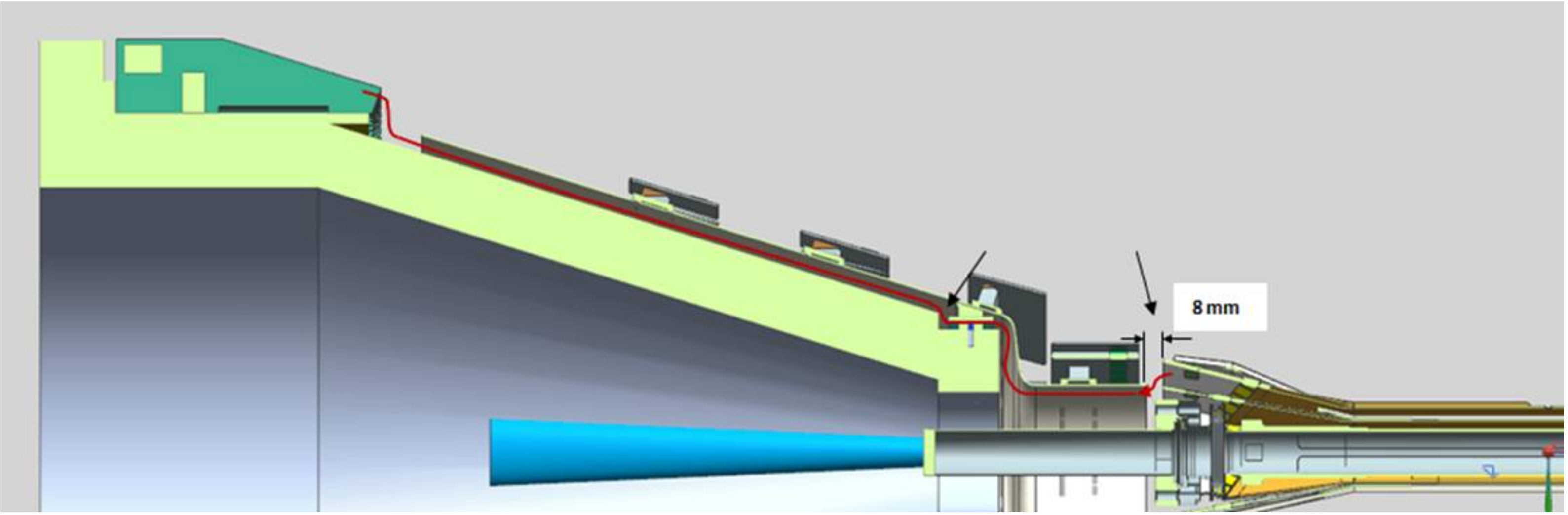


The copper bus is becoming a 3 layer Copper/Kapton Tape.
Aspect ratio: ~ 10 mm x 400-500 mm
At the connector the tape is ~ 17 mm wide

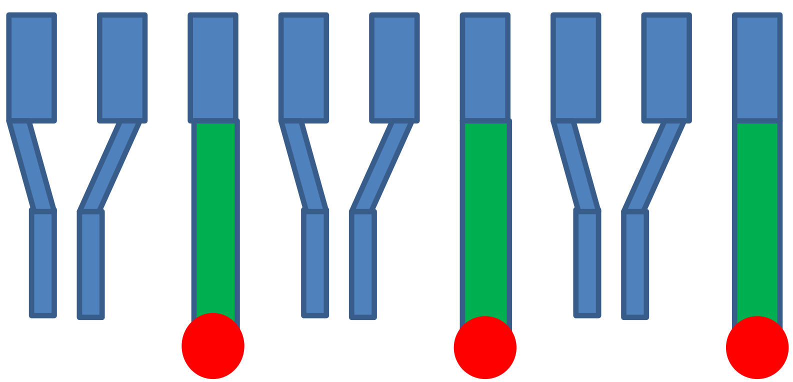
Width of Copper bus is determined by geometrical reasons:

- **Dimension of Transition Card**
- **Routing of Bus (an example is shown on bottom)**





Copper Bus Structure



Stack-up Design Rules:

LVDS Lines: Strip lines
LVDS Lines: 4 mils
LVDS Space: 4 mils
LVDS Copper Thickness ~ 20 um (~½ ounce)

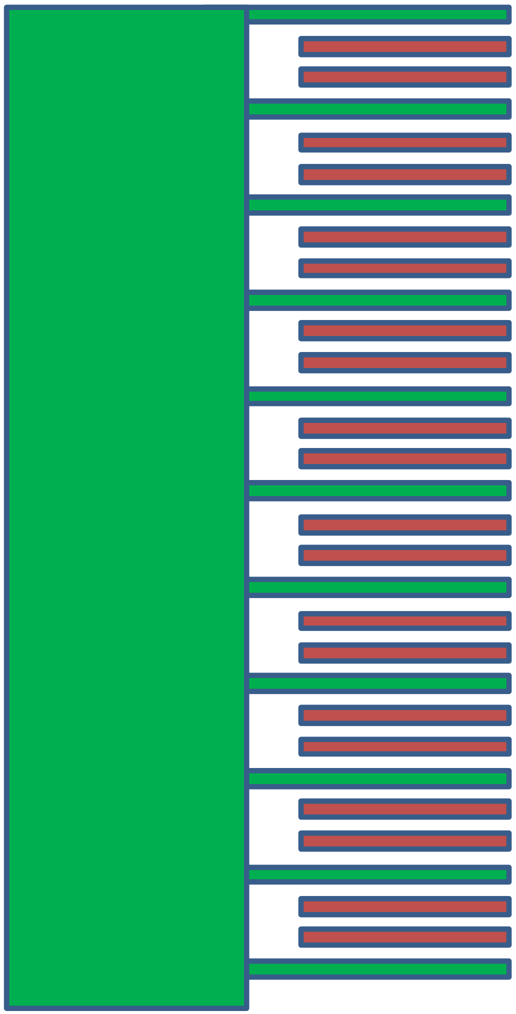
Dielectric Thickness: ~ 100 mils
Zdiff ~ 100 Ohm
To be optimized

Kapton Thickness: 2 mils (?)

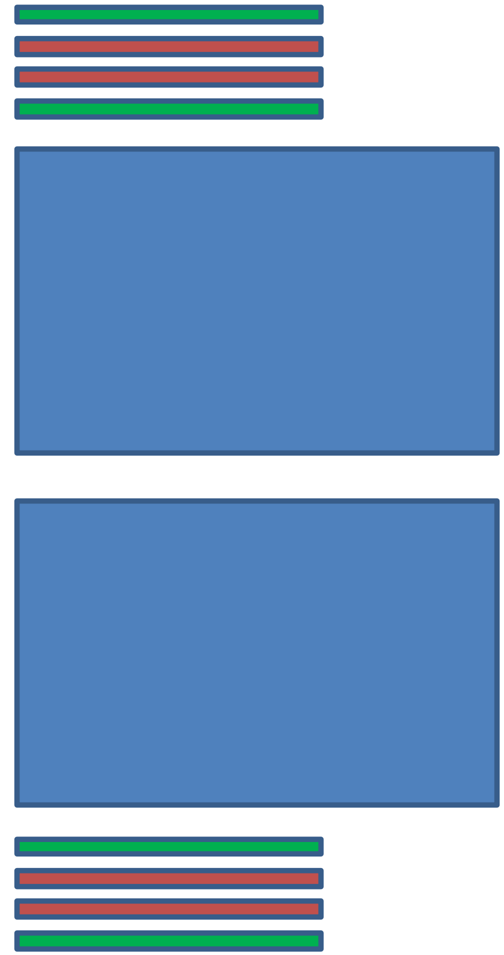
Via Diameter: 10-12 mils
Via Clearance: 6 mils

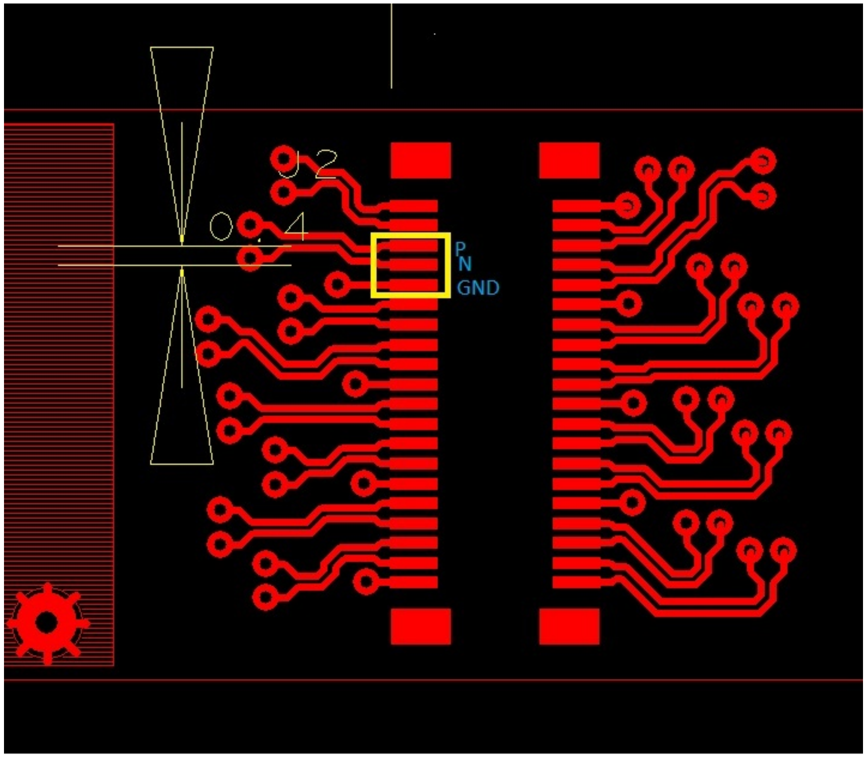
Power/Gnd Planes:
Widht ~ 4.7 mm (almost double for GND !!)
Thickness > 50 um (or 2 ounces)
Current capability ~ 3-3.5 Amps
Voltage drop (both ways) ~ 250 mV

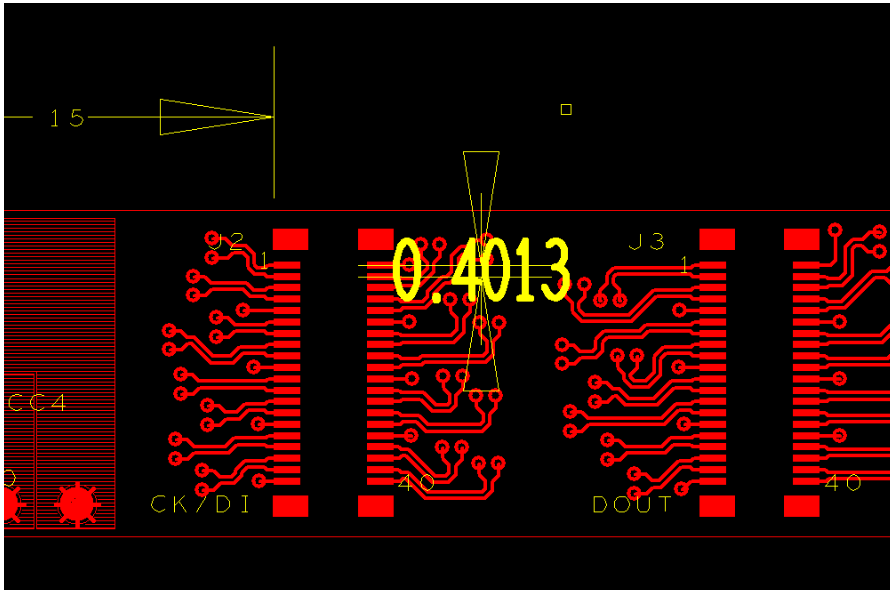
Copper Bus Structure



GND	1	36	GND
D1+	2	37	Reg Out +
D1-	3	38	Reg Out -
GND	4	39	GND
D2+	5	40	Power 1
D2-	6	41	Power 1
GND	7	42	Power 1
D3+	8	43	Power 1
D3-	9	44	Power 1
GND	10	45	Power 1
D4+	11	46	Power 1
D4-	12	47	Power 1
GND	13	48	Power 1
D5+	14	49	Power 1
D5-	15	50	Power 1
GND	16	51	Power 1
D6+	17	52	Power 1
D6-	18	53	
GND	19	54	Power 2
Trigger +	20	55	Power 2
Trigger -	21	56	Power 2
GND	22	57	Power 2
TimeStamp +	23	58	Power 2
Time Stamp -	24	59	Power 2
GND	25	60	Power 2
Clock +	26	61	Power 2
Clock -	27	62	Power 2
GND	28	63	Power 2
Fast Clock +	29	64	Power 2
Fast Clock -	30	65	Power 2
GND	31	66	Power 2
Reset +	32	67	GND
Reset -	33	68	Reg In +
GND	34	69	Reg In -
Not Assigned	35	70	GND







Courtesy of C. Gemme – IBL Flex Project

Still a serious puzzle …..

Even with the proposed design → not enough LVDS lines to match the HDI Data output lines:

→ 7 shared lines
→ 6 Data Output Lines

Increasing number of contacts on Panasonics?

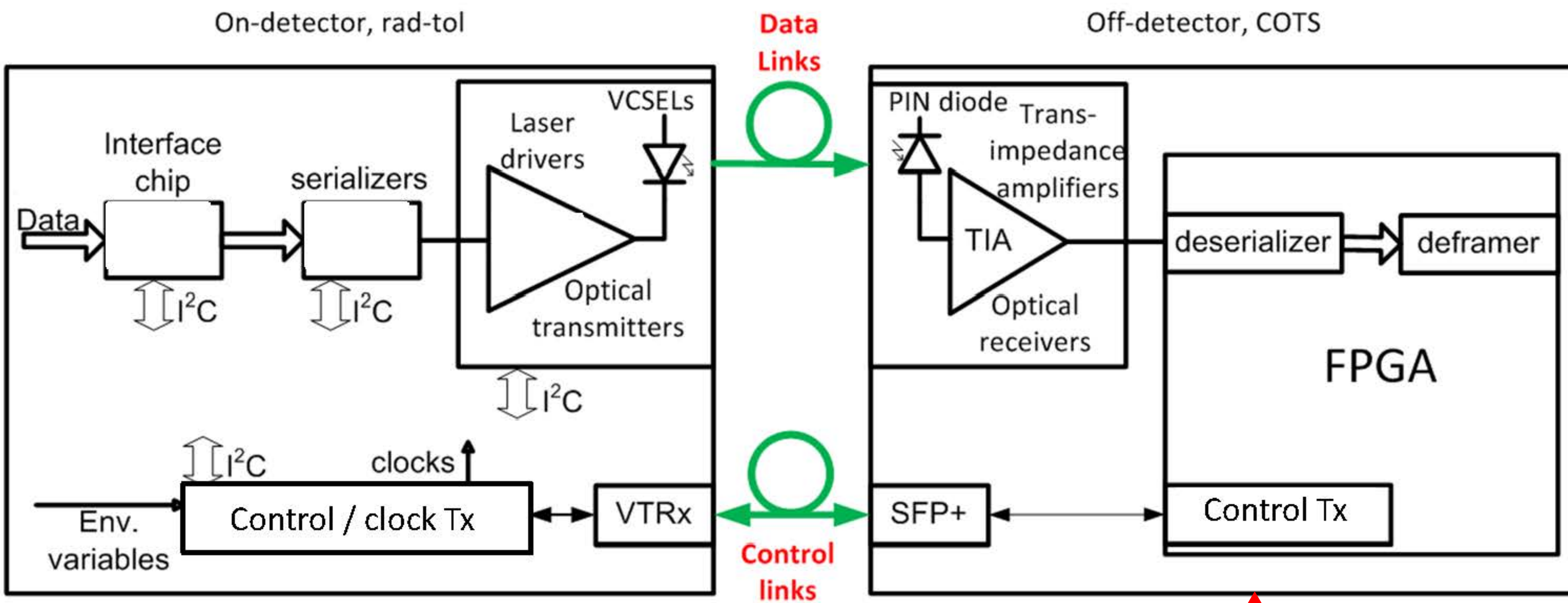
→ Max number of contacts is 80
→ Max data out lines will become 9

From previous table Number of HDI Data lines which are critical
→ 12 on L0
→ 14 on L1 Phi
→ 10 on L3 Z

Possible Solution …..

Having a 1:2 MUX on each HDI
Chip with 256 channels
- Frequency on LVDS increases → to be verified

Where are the logic blocks located…..



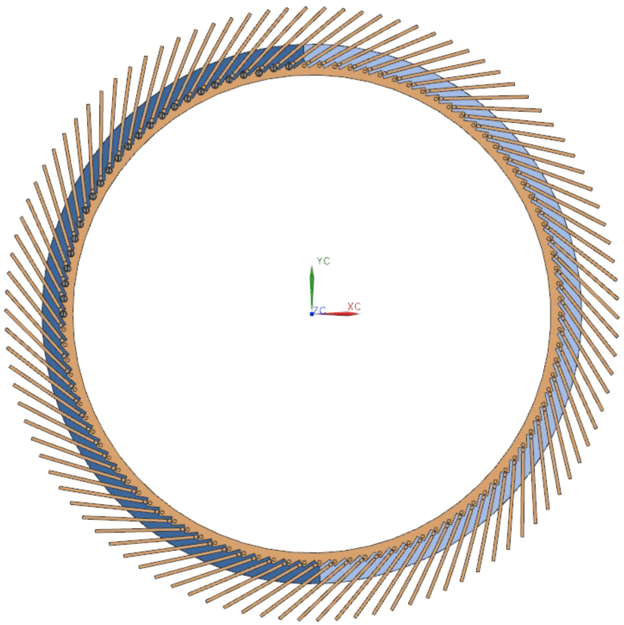
We do not have yet this block:
- Design our own except Optical Package and mount it on HDI
- Get GBT (fall 2012) and mount it on Transition Card (size 15x15 mm)
- FPGA based interface → mountable only on Transition Card

Separate Optical Fibers for controls and data ?

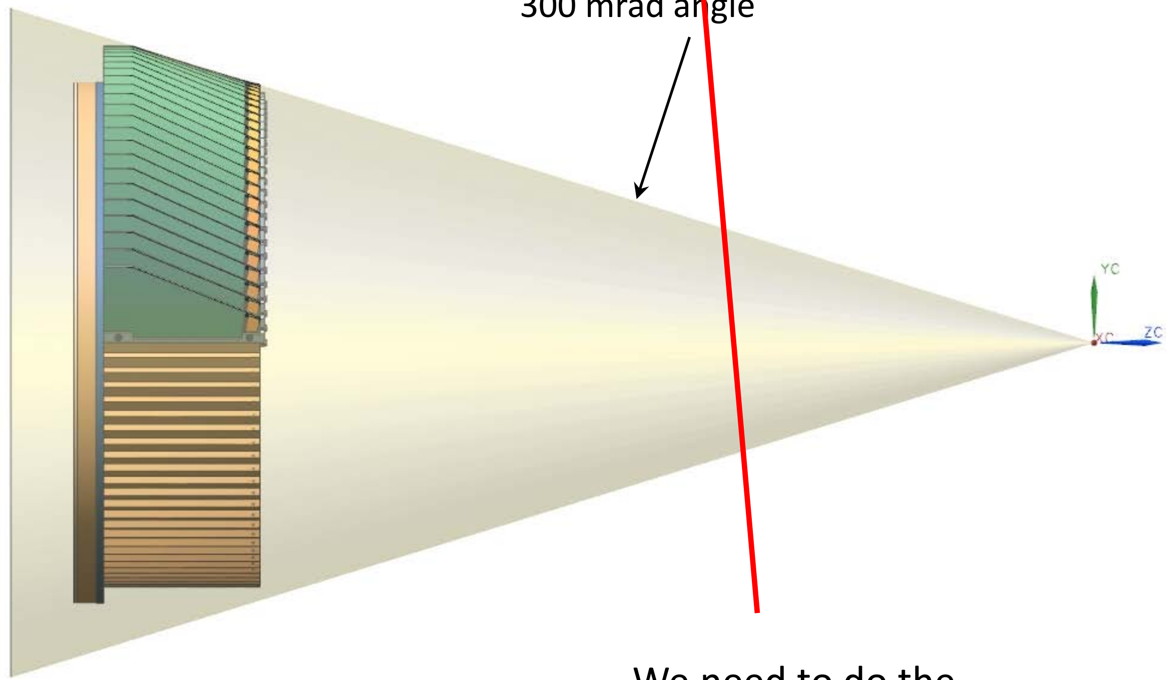
Very simple Cartoon …. Not to be taken very seriously

Istituto Nazionale
di Fisica Nucleare
Sezione di Milano

Transition cards
Alternative design: Turbine layout – n. 102 cards
(Hypothesis: only 18 cards for layer 5 instead of 36)



300 mrad angle



We need to do the same on L4 and reduce to 86 cards

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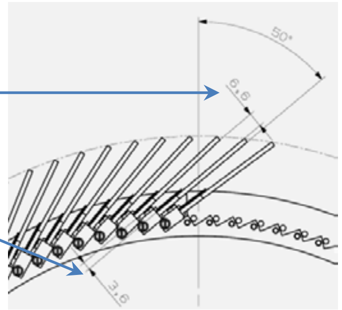
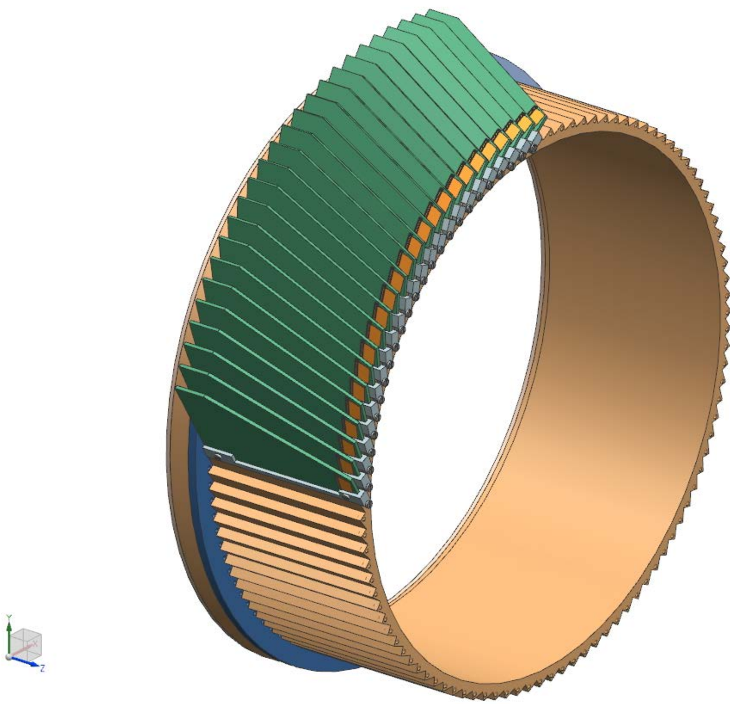
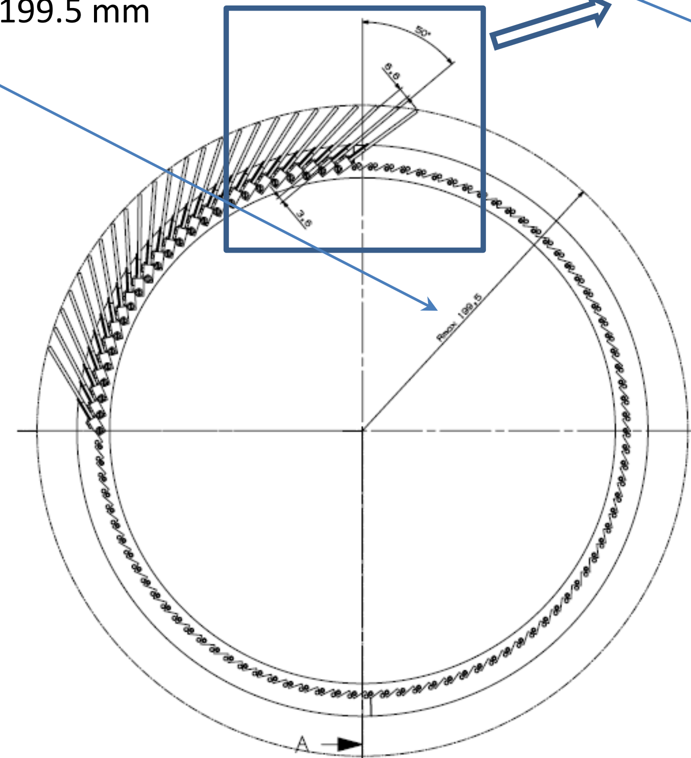
Transition cards – Turbine layout

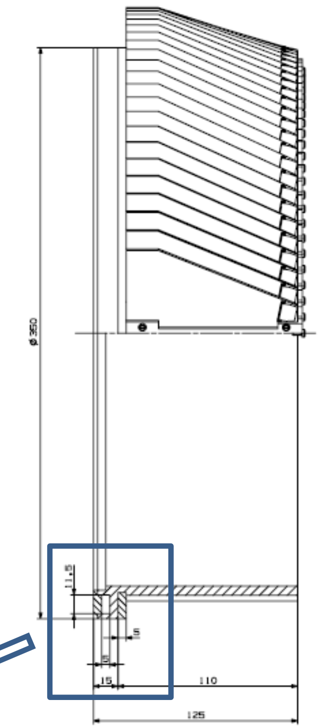
Max gap: 6.6 mm
Min gap : 3.6 mm



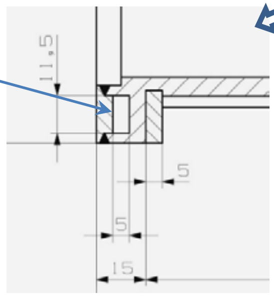
Max envelope radius : 199.5 mm





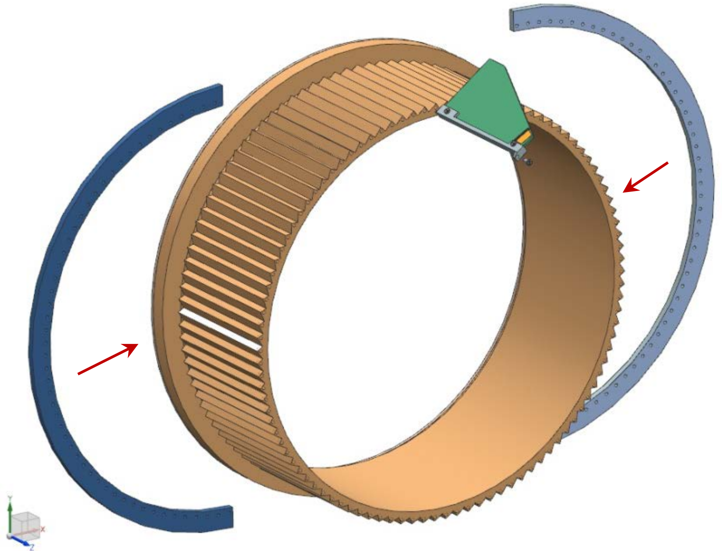


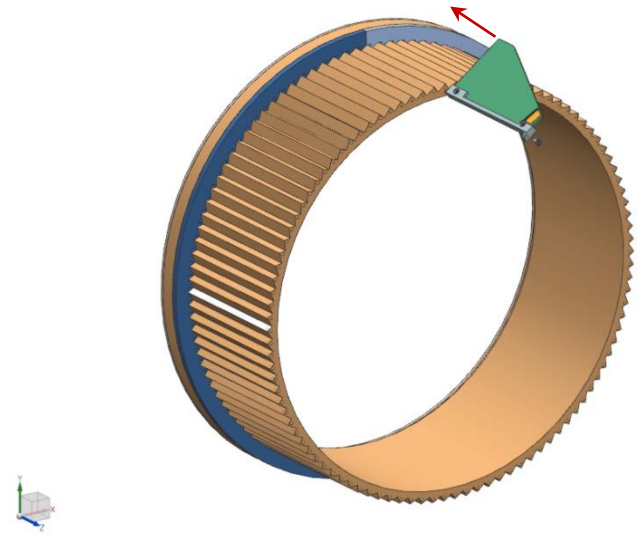
cooling space in back flange



16 March 2012

Transition cards – Turbine layout assembling





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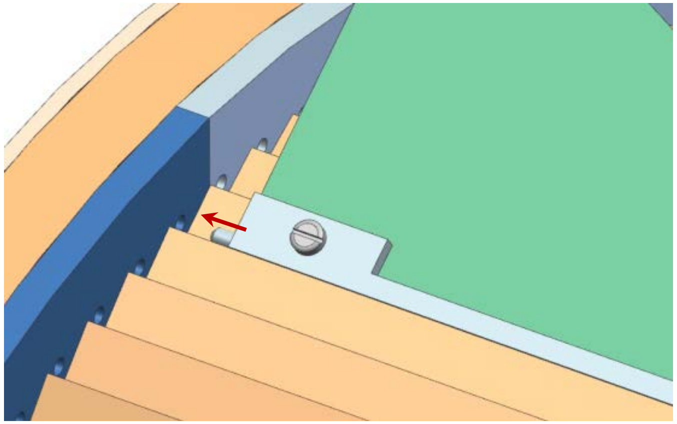
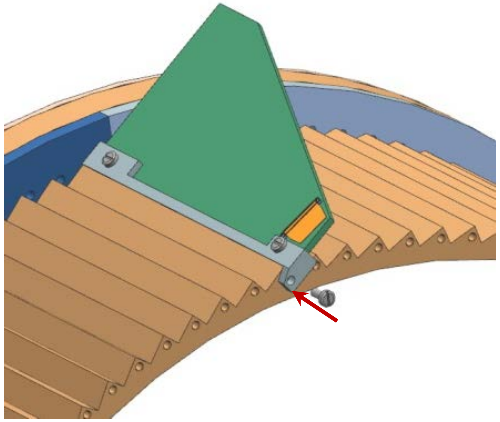
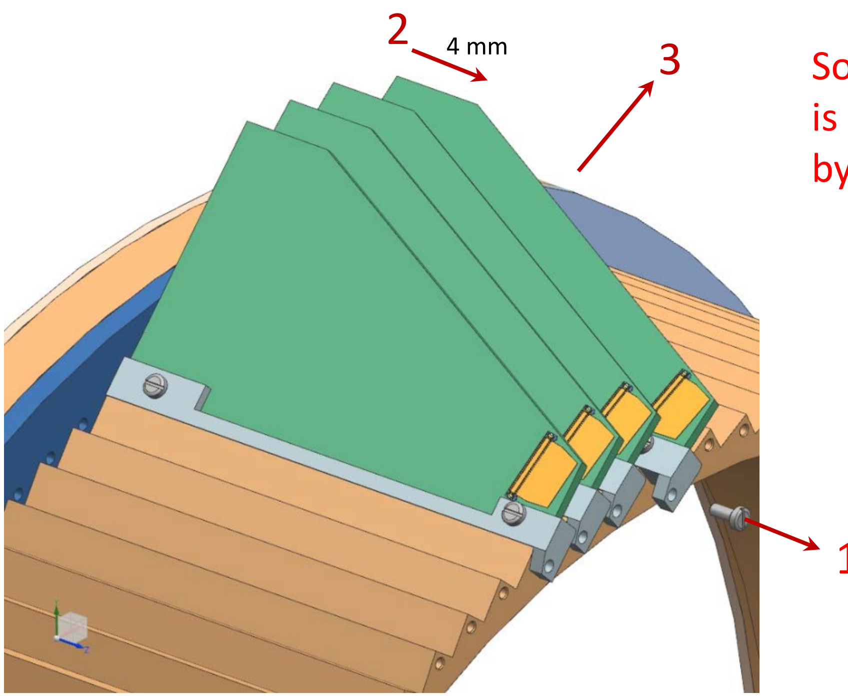


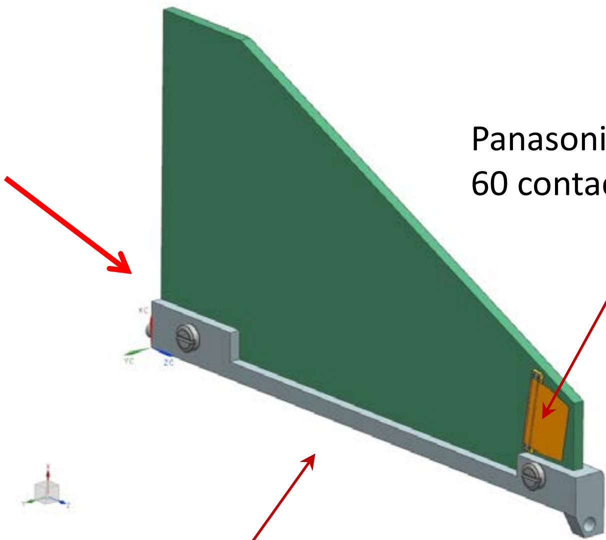


Transition cards – Turbine layout



Transition Card dismantling

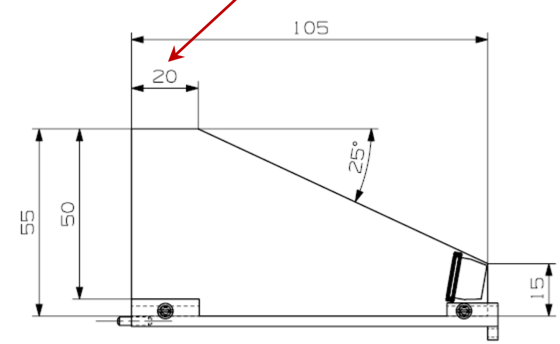
Some area
is blocked
by the ring



Panasonic connector
60 contacts

Transition Card support

Length to be increased
moving back cryostat



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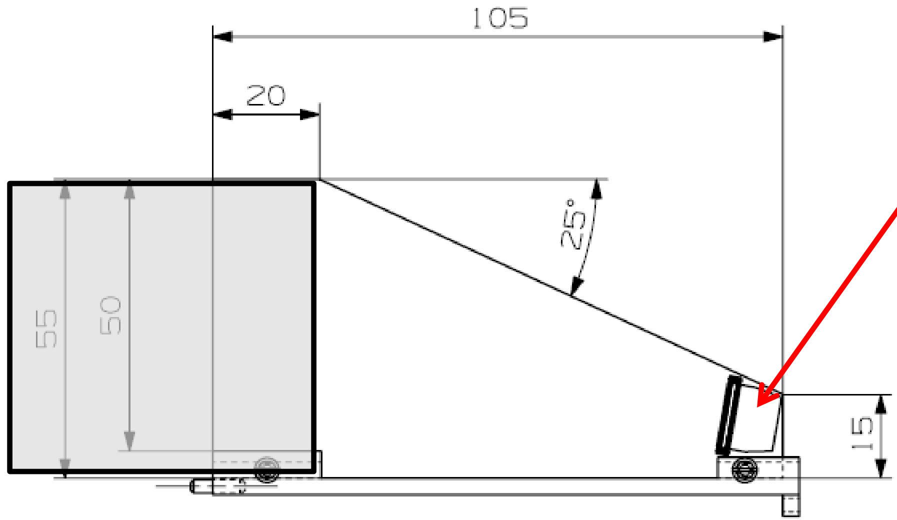
How much space is needed …..

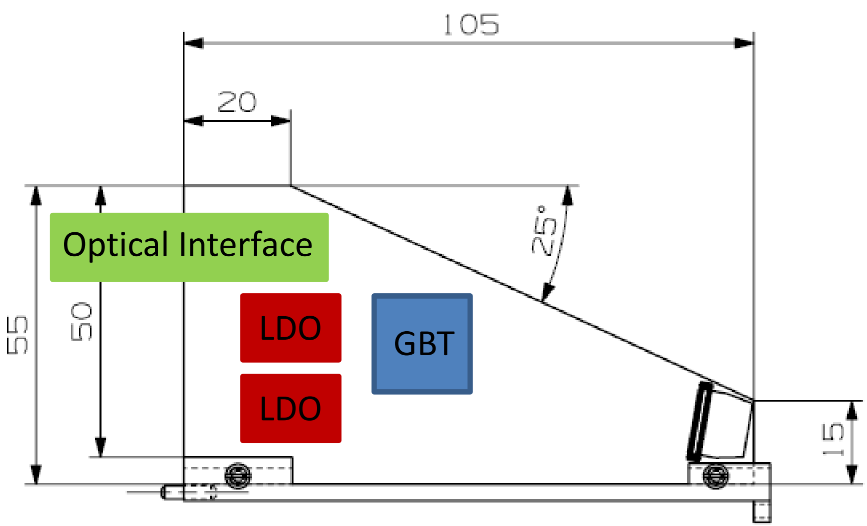
The "component" blocks have approximately the right dimensions:

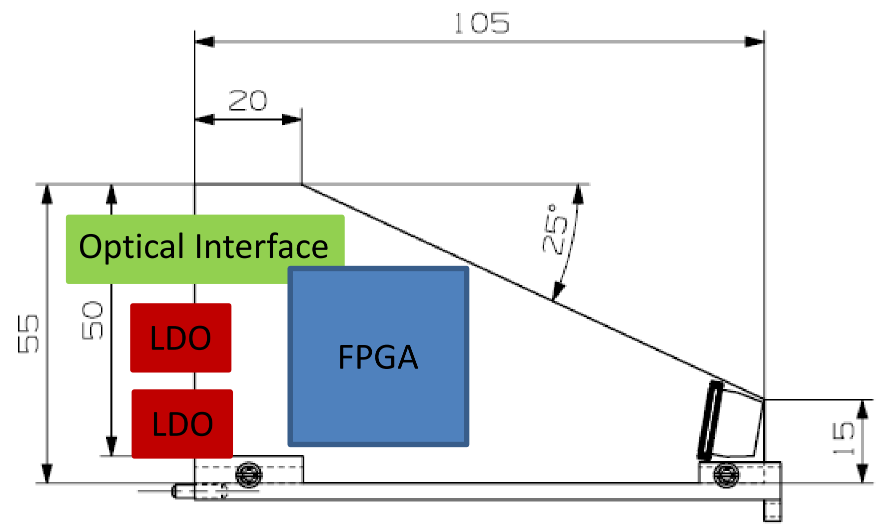
→ We need to get more spaces ~ 3-4 cm (grey box)

→ The turbine structure is helping on one side only



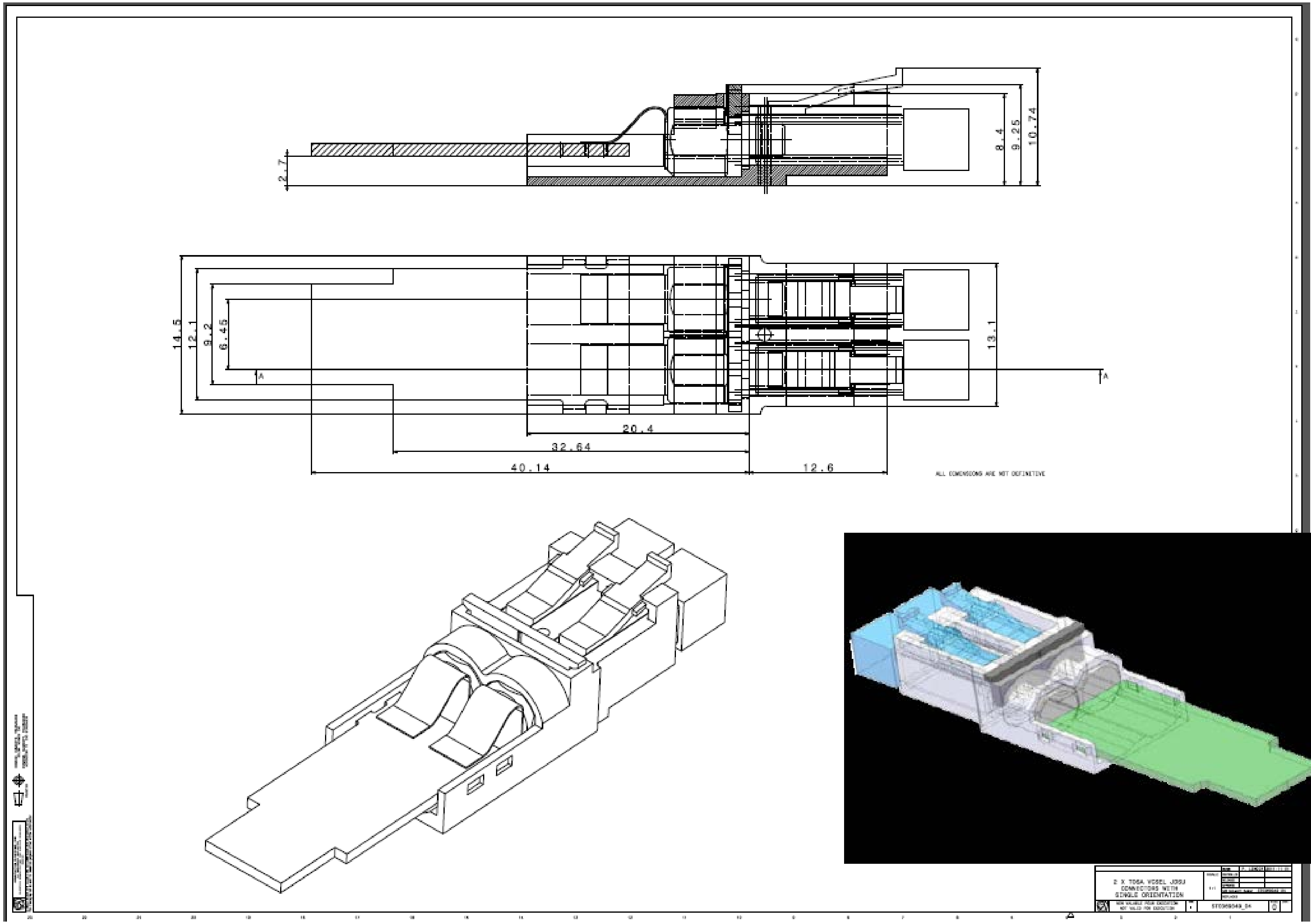
Only one copper bus shown





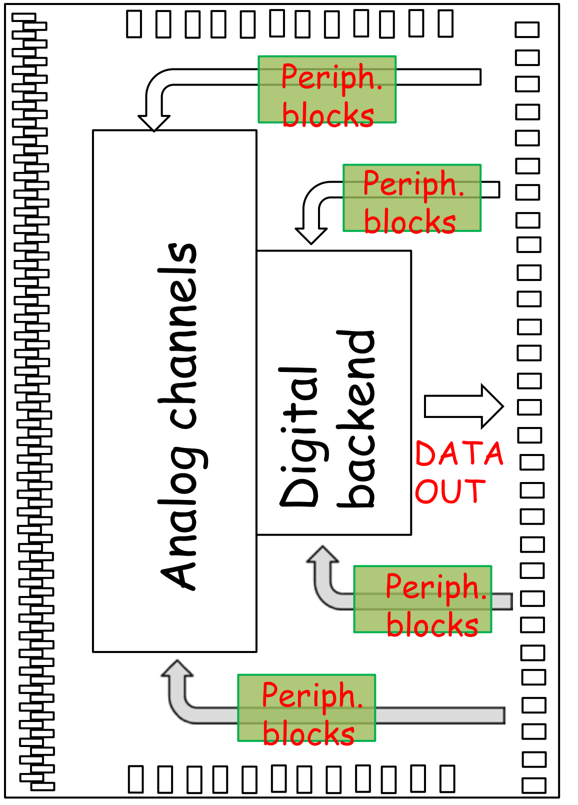
Input Power Cables NOT shown

Courtesy of the Versatile Project - CERN

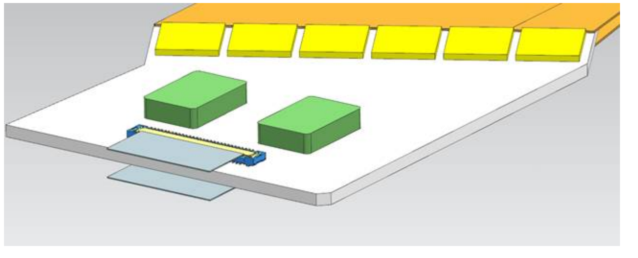


HDI

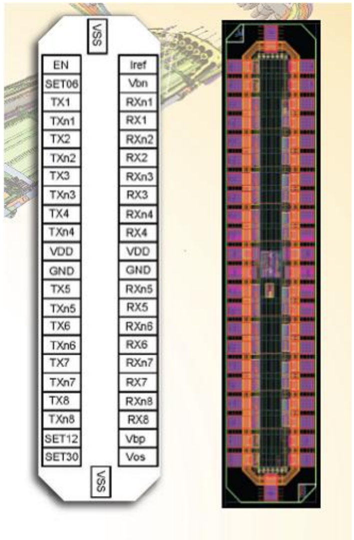
- → Layer 0 HDI dimensions
  - → We should "freeze" the dimensions
  - → I have started to draw a real "schematic and layout".
    - → In the coming days we should agree on some "tentative" pad layout
  - → No show-stopper up to now
    - → Still need to understand if we need to "shielding" between LVDS lines close to the connector
    - → Clock routing not yet addressed
  - → Number of layers seems similar to Babar HDI



  - → Summary of LVDS lines
    - → 3 clocks (System clock, Time Stamp clock, readout clock)
    - → 1 REG In
    - → 1 REG out
    - → 1 Reset
    - → 1 Trigger
    - → Max 9 Data lines



LVDS test in preparation



- → IC acquired from CERN (8 receivers and 8 transmitters, 6x1.5 mm)
  - → Extract of info from CERN:
    - → IBL loads 5.6m of twisted pair cable with this LVDS (FE-I4).
    - → Baud rate is 160Mb/s, transmission quality is marginal. Eye-plot is small mostly due to NO pre-empjasis
    - → nSPQ uses the same LVDS over a cable lenght (bunch of magnet wires) of 6.3m with a baud rate of 80Mb/s. Bit error rate is < 10E-14.
    - → With only one magnet wires baud rate could increase up to 120-130Mb/s, but if a bunch is used «mutual impedance» creates a problem

    - → We are bonding the IC to a board
    - → We will retest performance with multiple magnet wires
      - → we would need to interpose shields ?
    - → In parallel we will test an LVDC driver designed by Bergamo group
    - → As soon as the Copper Bus is ready we will repeat the test