

# Super*B* Detector Technical Design Report

## Abstract

This report describes the technical design detector for Super*B*.

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# 1 Electronics, Trigger, DAQ and Online

Breton/Marconi/Luitz Pages : 7-10

## 1.1 Overview of the Architecture

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SL + DB + UM Note: To be rewritten in a less tentative and more “absolute” style, i.e. “the design is” but includes lessons learned from BaBar and LHC

The architecture proposed for the SuperB [1] Electronics, Trigger, Data acquisition and Online systems (ETD) has evolved from the BABAR architecture, informed by the experience gained from running BABAR [2] and building the LHC experiments [3], [4], [5]. The detector side of the system is synchronous and all sub-detector readouts are now triggered, leading to improved reliability and uniformity. In SuperB, standard links like Ethernet are the default; custom hardware links are only used where necessary. The potential for high radiation levels makes it mandatory to design radiation-safe on-detector electronics.

Figure 1.1 shows an overview of the trigger and the event data chain:

A first-level hardware trigger uses dedicated data streams of reduced primitives from the sub-detectors and provides decisions to the fast control and timing system (FCTS) which is the centralized bandmaster of the system. The FCTS distributes the clock and the fast commands to all elements of the architecture and controls the readout of the events in the detector front-end electronics (FEE). The FEE send event fragments to the Reaout Modules (ROMs) which perform a first stage event build and send the partially constructed events through a network event builder to the processing farm running a high-level trigger (HLT). The HLT acts on complete events and reduces the data stream to an acceptable rate for permanent logging.

The ETD includes all the elements in the architecture: The FCTS, sub-detector-specific and common parts (CFEE) of the front-end electronics for data readout and control, the Level 1 hardware trigger, the ROMs, the Experiment Control System (ECS), and the various links that interconnect these components.

The trigger, data acquisition and Online components of the ETD system are described in this chapter, the common and subdetector-specific components of the electronics are described in the next chapter.

### 1.1.1 Trigger Strategy

PB + UM + SL

The BABAR and Belle [6] experiments both chose to use “open triggers” that preserved nearly 100% of  $B\bar{B}$  events of all topologies, and a very large fraction of  $\tau^+\tau^-$  and  $c\bar{c}$  events. This choice enabled very broad physics programs at both experiments, albeit at the cost of a large number of events that needed to be logged and reconstructed, since it was so difficult to reliably separate the desired signals from the  $q\bar{q}$  ( $q = u, d, s$ ) continuum and from higher-mass two-photon physics at trigger level. The physics program envisioned for SuperB requires very high efficiencies for a wide variety of  $B\bar{B}$ ,  $\tau^+\tau^-$ , and  $c\bar{c}$  events, and depends on continuing the same strategy, since few classes of the relevant decays provide the kinds of clear signatures that allow the construction of specific triggers.

All levels of the trigger system should be designed to permit the acquisition of prescaled samples of events that can be used to measure the trigger performance.

The trigger system consists of the following components <sup>1</sup>:

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<sup>1</sup> While at this time we do not foresee a “Level 2” trigger that acts on partial event information in the data path, the data acquisition system architecture would



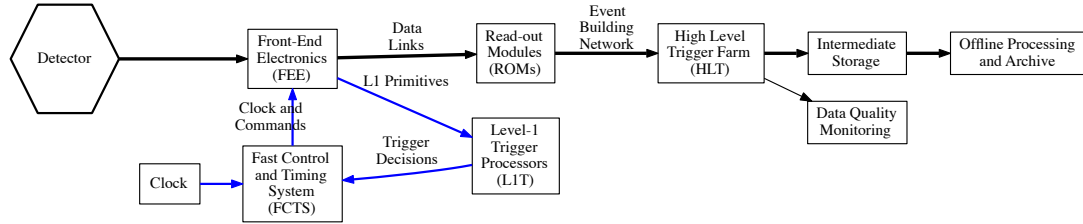


Figure 1.1: Overview of the Trigger and Data Chain

**Level 1 (L1) Trigger:** A synchronous, fully pipelined L1 trigger receives continuous data streams from the detector independently of the event readout and delivers readout decisions with a fixed latency. While we have yet to conduct detailed trigger studies, we expect the L1 trigger to be similar to the *BABAR* L1 trigger, operating on reduced-data streams from the drift chamber and the calorimeter. We will study the possibilities of improving the L1 trigger performance by including SVT information, taking advantage of larger FPGAs, faster drift chamber sampling, the faster forward calorimeter, and improvements to the trigger readout granularity of the EMC.

**High Level Triggers (HLT)—Level 3 (L3) and Level 4 (L4):** The L3 trigger is a software filter that runs on a commodity computer farm and bases its decisions on specialized fast reconstruction of complete events. An additional “Level 4” filter may be implemented to reduce the volume of permanently recorded data if needed. Decisions by L4 would be based on a more complete event reconstruction and analysis. Depending on the worst-case performance guarantees of the reconstruction algorithms, it might become necessary to decouple this filter from the near-realtime requirements of L3—hence, its designation as a separate stage.

allow the addition of such a trigger stage at a later time, hence the nomenclature.

### 1.1.2 Trigger Rates and Event Size Estimation

The present L1-accept rate design standard is 150 kHz. It has been increased from the *SuperB*

CDR [1] design of 100 kHz to allow more flexibility and add headroom both to accommodate the possibility of higher backgrounds than design (e.g. during machine commissioning), and the possibility that the machine might exceed its initial design luminosity of  $10^{36} \text{ cm}^{-2}\text{sec}^{-1}$ .

The event size estimates still have large uncertainties. Raw event sizes (between front-end electronics and ROMs) are understood well enough to determine the number of fibres required. However, neither the algorithms that will be employed in the ROMs for data size reduction (such as zero suppression or feature extraction) nor their specific performance for event size reduction are yet known. Thus, while the 75 kbytes event size extrapolated from *BABAR* for the CDR remains our best estimate, the event size could be significantly larger due to new detector components such as Layer 0 of the SVT and/or the forward calorimeter. **In this document we will use 150 kHz L1-accept rate and 100 kbytes per event as the baseline.**

**Note:** Consider increasing the event size to 150-200 kbyte to take into account requirement for permanent storage of EMC barrel waveforms

With the prospect of future luminosity upgrades up to 4 times the initial design luminosity, and the associated increases in event size and rate, we also must define the system upgrade path, including which elements need to be designed upfront to facilitate such an upgrade,

which can be deferred until a later time, and, ultimately, what the associated costs would be.

### 1.1.3 Dead Time and Buffer Queue Depth Considerations

#### SL + DB + UM

The readout system is designed to handle an average rate of 150 kHz and to absorb the expected instantaneous rates, both without incurring dead time of more than 1% under normal operating conditions at design luminosity. Dead time is generated and managed centrally by the FCTS which will drop valid L1 trigger requests that would not fit into the readout system’s envelope for handling of average or instantaneous L1 trigger rates. The average rate requirement determines the overall system bandwidth; The instantaneous trigger rate requirement affects the FCTS, the data extraction capabilities of the front-end-electronics, and the depth of the de-randomization buffers. The minimum time interval between bunch crossings at design luminosity is about 2.1 ns—so short in comparison to detector data collection times that we assume “continuous beams” for the purposes of trigger and FCTS design. Therefore, the burst handling capabilities (minimum time between triggers and maximum burst length) to achieve the dead time goal are dominated by the capability of the L1 trigger to separate events in time and by the ability of the trigger and readout systems to handle events that are partially overlapping in space or time (pile-up, accidentals, etc.). Detailed detector and trigger studies are needed to determine these requirements.

## 1.2 Trigger and Event Data Chain

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The systems in the trigger and event data chain manage event selection, event filtering and end-to-end data flow from the detector to the intermediate buffer.

**Note:** The previous sentence needs better wording. We try to avoid the traditional architectural distinction between “TDAQ” (or Odf in BaBar) and “Online”. The idea is to design and present the system architecture as an integrated

end-to-end “push” data flow chain all the way from the detector to data logging. A number of auxiliary systems supports the primary data logging function.

### 1.2.1 Level-1 Trigger

#### PB (+ SL?)

The current baseline for the L1 trigger is to re-implement the *BABAR* L1 trigger with state-of-the-art technology. It would be a synchronous machine running at 59 MHz (or multiples of 59 MHz) that processes primitives produced by dedicated electronics located on the front-end boards or other dedicated boards of the respective sub-detector. The raw L1 decisions are sent to the FCTM boards which applies a throttle if necessary and then broadcasts them to the whole experiment. The standard chosen for the crates would most likely be either ATCA for Physics (Advanced Telecommunications Computing Architecture) for the crates and the backplanes, or a fully custom architecture.

The main elements of the L1 trigger are shown in Fig. 1.3 (see [8] for detailed descriptions of the *BABAR* trigger components):

**Drift chamber trigger (DCT):** The DCT consists of a track segment finder (TSF), a binary link tracker (BLT) and a  $p_t$  discriminator (PTD).

**Electromagnetic Calorimeter Trigger (EMT):** The EMT processes the trigger output from the calorimeter to find clusters.

**Global Trigger (GLT):** The GLT processor combines the information from DCT and EMT (and possibly other inputs such as an SVT trigger or a Bhabha veto) and forms a final trigger decision that is sent to the FCTS.

**Note:** Update this with the current L1 trigger design proposal

We will study the applicability of this baseline design at SuperB luminosities and backgrounds, and will investigate improvements, such as adding a Bhabha veto or using SVT information in the L1 trigger. We will also study faster sampling of the DCH and the new fast

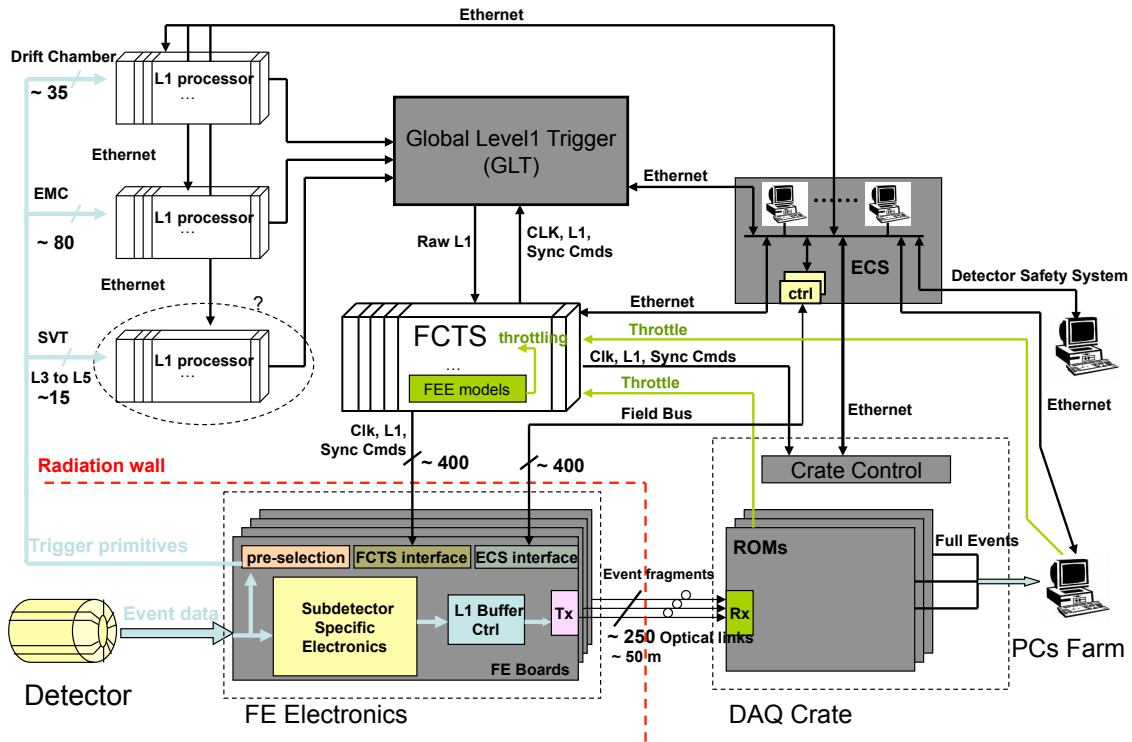


Figure 1.2: Overview of Level-1 Trigger, FCTS, FEE and ROMs. **Note: Figure needs to be updated!**

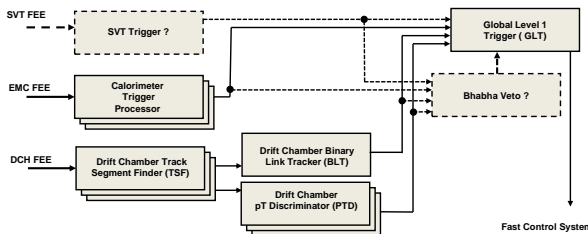


Figure 1.3: Level 1 Trigger Overview

forward calorimeter. In particular for the barrel EMC we will need to study how the L1 trigger time resolution can be improved and the trigger jitter can be reduced compared to BaBar. In general, improving the trigger event time precision should allow a reduction in readout window and raw event size. The L1 trigger may also be improved using larger FPGAs (e.g. by implementing tracking or clustering algorithm improvements, or by exploiting better readout granularity in the EMC).

**L1 Trigger Latency:** The *BABAR* L1 trigger had  $12 \mu\text{s}$  latency. However, since the size, and cost, of the L1 data buffers in the sub-detectors scale directly with trigger latency, it should be substantially reduced, if possible. L1 trigger latencies of the much larger, more complex, ATLAS, CMS and LHCb experiments range between 2 and  $4 \mu\text{s}$ , however these experiments only use fast detectors for triggering. Taking into consideration that the DCH adds an intrinsic dead time of about  $1 \mu\text{s}$  and adding some latency reserve for future upgrades, we are currently estimating a total trigger latency of  $6 \mu\text{s}$  (or less). More detailed engineering studies will be required to validate this estimate.

**Monitoring the Trigger:** To debug and monitor the trigger, and to provide cluster and track seed information to the higher trigger levels, trigger information supporting the trigger decisions is read out on a per-event basis through

the regular readout system. In this respect, the low-level trigger acts like just another sub-detector.

### 1.2.2 Fast Control and Timing System

#### DC + CB + DB + a little bit of SL

The Fast Control and Timing System (FCTS, Fig. 1.4) manages all elements linked to clock, trigger, and event readout, and is responsible for partitioning the detector into independent sub-systems for testing and commissioning.

The FCTS will be implemented in a crate where the backplane can be used to distribute all the necessary signals in point-to-point mode. This permits the delivery of very clean synchronous signals to all boards—avoiding the use of external cables. The Fast Control and Timing Module (FCTM, shown in Fig. 1.5) provides the main functions of the FCTS:

**Clock and Synchronization:** The FCTS synchronizes the experiment with the machine and its bunch pattern, distributes the clock throughout the experiment, buffers the clock, and generates synchronous reset commands.

**Note:** We somewhere need to discuss “synchronization” in more detail, here some potential topics:

- Fixed-latency implementation in FPGA (verify) - can’t forget this!
- Timing of the various delays during commissioning so that the analog signals are placed correctly within the readout windows. Where is the adjustable delay? On the sender side or the receiver side (i.e. sub-detector). DC proposes receiver (it’s a per-subdetector thing. Also could potentially adjust latency buffer depth in FEE + adjust phase). What is the hardware support needed in CFEE to measure the offset. Is there a common implementation? Probably not, FEE will have to deal with this problem.
- The ability to reset all clock dividers and state machines in the (C)FEE at system initialization to ensure that divided versions of the 59MHz global clock and state

machines are also “in phase”. This probably needs some sort of a “reset” or “sync” command to be broadcast to all FEE in a partition via the clock/command link.

- Protocol to detect, report and recover from “loss of lock” in CFEE. Return path of command link (also used for fast throttle) for reporting? Can we recover an individual channel / channel group or do we need to globally reset / resync the detector?

**Trigger Handling:** The FCTS receives the raw L1 trigger decisions, throttles them as necessary, and broadcasts them to the sub-detectors.

**Note:** We should somewhere have a brief discussion of the command word length and content. To consider:

- Number of bits available in the command word (quite limited on a 1 GBit link given the dead time constraints. 2GBit/s would be much more comfortable!)
- content of the command word and related issues: Do we broadcast information derived from the trigger type (probably at least a few bits)? If yes, how many bits? The full trigger information can be included in the event by reading out the L1 trigger processors. How many bits or the HLT node address (10-12 is probably about right)? How many bits for an event tag? How to we reconstitute / construct a globally unique event identifier at the ROM level if we don’t have enough bits available in the command word? Separate link? Ethernet? ...?
- Can we “reuse” the HLT node address as part of the event tag (thus saving some bits?) Probably not, since we need to support running with very small number of HLT nodes.

**Note:** We need a discussion of the implementation of a fast throttle. Some issues

- The FCTS needs one bit per subdetector to do the fast throttle

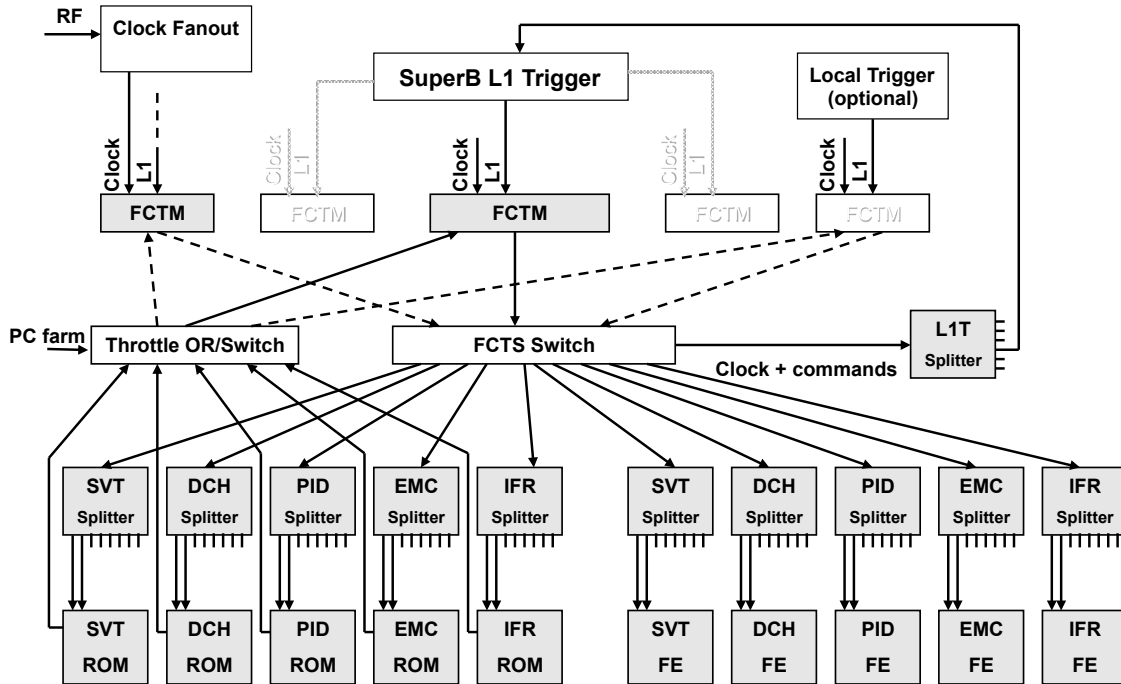


Figure 1.4: Fast Control and Timing System

- Aggregation of throttles from different front-end boards within one subdetector is not subdetector-specific
- For diagnostic purposes it is mandatory that we record which front-end board throttled when (“Logic analyzer on the throttle lines”)
- need to define throttle latency (depends on derandomizer depth) - should be as fast as possible to be able to utilize the derandomizer as efficiently as possible (i.e. where do we set the “almost full” level?)

**Calibration and Commissioning:** The FCTS can trigger the generation of calibration pulses and flexibly programmable local triggers for calibration and commissioning.

**Note:** How do we handle the EMC source calibration where by definition a meaningful global calibration trigger can not be constructed.

**Event Handling:** The FCTS generates event identifiers, manages the event routing, and dis-

tributes event routing information to the ROMs. It also keeps a trace of all of its activity, including an accounting of triggers lost due to dead time or other sources of throttling and event-linked data that needs to be included with the readout data.

The FCTS crate includes as many FCTM boards as required to cover all partitions. One FCTM will be dedicated to the unused sub-systems in order to provide them with the clock and the minimum necessary commands.

Two dedicated switches are required in order to be able to partition the system into independent sub-systems or groups of sub-systems. One switch distributes the clock and commands to the front-end boards, the other collects throttling requests from the readout electronics or the ECS. These switches can be implemented on dedicated boards, connected with the FCTMs, and need to receive the clock. To reduce the number of connections between ROM crates and

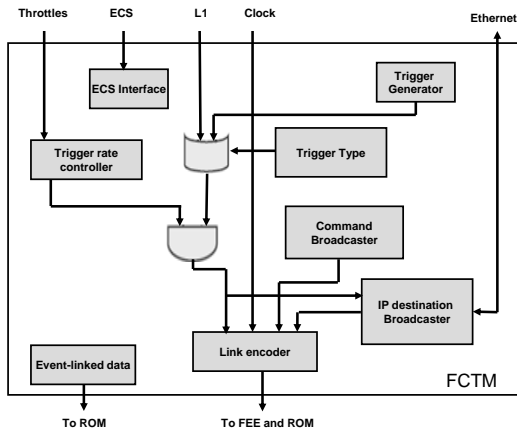


Figure 1.5: Fast Control and Timing Module

the global throttle switch board, throttle commands could be combined at the ROM crate level before sending them to the global switch.

**Note:** Describe fast throttle (from FEE to FCTS) here.

The FCTM also manages the distribution of events to the HLT farm for event building, deciding the destination farm node for every event. There are many possible implementations of the event building network protocol and the routing of events based on availability of HLT farm machines, so at this point we can provide only a high-level description. We strongly prefer to use the FCTS to distribute event routing information to the ROMs because it is simple and provides natural synchronization. Management of event destinations and functions such as bandwidth management for the event building network or protocols to manage the event distribution based on the availability of farm servers can then be implemented in FCTM firmware and/or software.

“Continuation events” to deal with pile-up could either be reconstituted the ROMs or in the high-level trigger farm, but we strongly prefer to reconstitute them in the ROMs. Doing this in the trigger farm would complicate the event builder and require the FCTS to maintain event state and adjust the event routing to send all parts of a continuation event to the same HLT farm node.

### 1.2.3 Control Links

AA

**Note:** per agreement at Fall 2011 CERN workshop

### 1.2.4 Common Front-End-Electronics

DB + ?

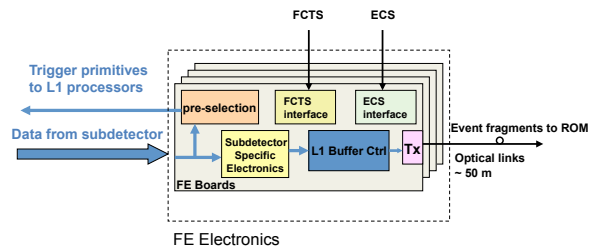


Figure 1.6: Common Front-End Electronics

Common Front-End Electronics (CFEE) designs and components allow us to exploit the commonalities between the sub-detector electronics and avoid separate design and implementation of common functions for each sub-detector.

In our opinion, the separate functions required to drive the FEE should be implemented in dedicated independent elements. These elements will be mezzanines or circuits directly mounted on the front-end modules (which act as carrier boards) and will be standardized across the sub-systems as much as possible. For instance, as shown in Fig. 1.6, one mezzanine can be used for FCTS signal and command decoding, and one for ECS management. To reduce the number of links, it may be possible to decode the FCTS and ECS signals on one mezzanine and then distribute them to the neighbouring boards.

A common dedicated control circuitry inside a radiation-tolerant FPGA may also drive the L1 buffers. It would handle the L1 accept commands and provide the signals necessary to manage the data transfers between latency buffers, derandomizer buffers and the fast multiplexers feeding the optical link serializers. If required by the system design, it would also provide logic for special treatment of pile-up events

and/or extending the readout window back in time after a Bhabha event has been rejected.

The latency buffers can be implemented either in the same FPGA or directly on the carrier boards. One such circuit can drive numerous data links in parallel, thus reducing the amount of electronics on the front-end.

One intriguing, possible advantage of this approach is that *analog* L1 buffers might be implemented in an ASIC, though the analog output of the ASIC then must be able to drive an internal or external ADC that samples the signal.

Serializers and optical link drivers will also reside on carrier boards, mainly for mechanical and thermal reasons. Fig. 1.6 shows a possible implementation of the L1 buffers, their control electronics (in a dedicated FPGA), and their outputs to the optical readout links.

**Note: Serializer clock not necessarily identical to front-end clock. Derandomizer buffer input synchronized with latency buffer, output runs at link clock speed. This allows flexible choice and upgrade of data link technology. Derandomizer could be located on link carrier board.**

All (rad-tolerant) FPGAs in the FEE have to be reprogrammable without dismounting a board. This could be done through dedicated front panel connectors, which might be linked to numerous FPGAs, but it would be preferable if the reprogramming could be done through the ECS without any manual intervention on the detector side.

Sampling of the analog signals in the FEEs is done with the global clock or a clock signal derived from the global clock (typically by dividing it down). To maintain the timing required by the fixed latency design, the latency buffers in the FEEs must be read with the same sampling frequency as they are written. In addition, when initializing the FEE boards, care must be taken that all dividers are reset synchronously with those of the first level trigger (by a global signal) in order to maintain a constant phase between them.

### 1.2.5 Data Links

AA

**Note: per agreement at Fall 2011 CERN workshop**

### 1.2.6 Read-out Modules

MB + UM

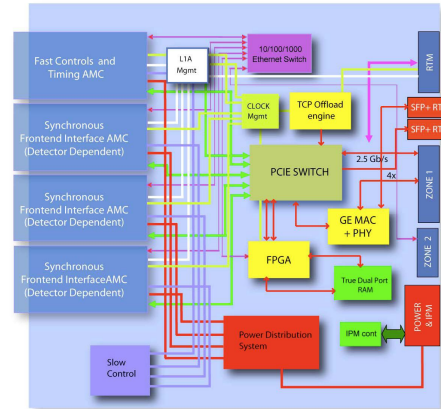


Figure 1.7: Readout Module

The Readout Modules (ROM, Fig. 1.7) receive event fragments from the sub-detectors' front-end electronics, tag them with front-end identifiers and absolute time-stamps, buffer them in de-randomizing memories, perform processing (still to be defined) on the fragment data, and eventually inject the formatted fragment buffers into the event builder and HLT farm. Connected to the front-end electronics via optical fibres, they will be located in an easily accessible, low radiation area.

A modular approach will maximize standardization across the system to simplify development and keep costs low—different sub-detector requirements can then be accommodated by using sub-detector-specific “personality modules”.

On the ROM boards, signals from optical receivers mounted on mezzanine cards will be routed to the de-serializers (in commercial FPGAs) where data processing can take place. Special requirements from the sub-detector systems will be accommodated by custom-built mezzanines mounted on common carriers. One of the mezzanine sites on the carrier will host an interface to the FCTS to receive global timing and trigger information. The carrier itself will

host memory buffers and 1 Gbit/s or 10 Gbits/s links to the event building network.

A baseline of 8 optical fibres per card currently seems like a good compromise between keeping the number of ROM boards low and adding to their complexity. This density is sufficient so that there needs to be only one ROM crate per sub-detector, and corresponds nicely to the envisaged FCTS partitioning.

### 1.2.7 Network Event Builder

SL + GM

**Note: To be rewritten — add more detail about proposed node management and load balancing protocol — update the numbers**

Assuming a L1 trigger rate of 150 kHz and an event size of 75 kbytes, the bandwidth in the network event builder is about 12 Gbytes/s, which corresponds to about 120 Gbits/s with network overhead included. It seems prudent to retain an additional safety factor of  $\sim 2$ , given the event size uncertainty and the immaturity of the overall system design. Thus, we will take 250 Gbits/s as the baseline for the Online system input bandwidth.

The ROMs read out event fragments in parallel from sub-detector front-end electronics—buffering the fragments in deep de-randomizing memories. The event-related information is then transferred into the ROM memories, and sent over a network to an event buffer in one of the machines of the HLT farm. This collection task, called event building, can be performed in parallel for multiple events, thanks to the depth of the ROM memories and bandwidth of the event building network switch (preferably non-blocking). Because of this inherent parallelism, the building rate can be scaled up as needed (up to the bandwidth limit of the event building network). We expect to use 10 Gbits/s Ethernet as the basic technology of the event builder network.

### 1.2.8 High Level Trigger Farm

SL

The HLT farm needs to provide sufficient aggregate network bandwidth and CPU resources to handle the full Level 1 trigger rate on its in-

put side. The Level 3 trigger algorithms should operate and log data entirely free of event time ordering constraints and be able to take full advantage of modern multi-core CPUs. Extrapolating from *BABAR*, we expect 10 ms core time per event to be more than adequate to implement a software L3 filter, using specialized fast reconstruction algorithms. With such a filter, an output cross-section of 25 nb should be achievable.

To further reduce the amount of permanently stored data, an additional filter stage (L4) could be added that acts only on events accepted by the L3 filter. This L4 stage could be an equivalent (or extension) of the *BABAR* offline physics filter—rejecting events based either on partial or full event reconstruction. If the worst-case behavior of the L4 reconstruction code can be well controlled, it could be run in near real-time as part of, or directly after, the L3 stage. Otherwise, it may be necessary to use deep buffering to decouple the L4 filter from the near real-time performance requirements imposed at the L3 stage. The discussion in the *SuperB* CDR [1] about risks and benefits of a L4 filter still applies.

### 1.2.9 Data Logging

SL + ?

The output of the HLT is logged to disk storage. We assume at least a few Tbytes of usable space per farm node, implemented either as directly attached low-cost disks in a redundant (RAID) configuration, or as a storage system connected through a network or SAN. We do not expect to aggregate data from multiple farm nodes into larger files. Instead, the individual files from the farm nodes will be maintained in the downstream system and the book-keeping system and data handling procedures will have to deal with missing run contribution files. A switched Gigabit Ethernet network separate from the event builder network is used to transfer data asynchronously to archival storage and/or near-online farms for further processing. It is not yet decided where such facilities will be located, but network connectivity with adequate bandwidth and reliability will need to be



provided. Enough local storage must be available to the HLT farm to allow data buffering for the expected periods of link down-time.

While the format for the raw data has yet to be determined, many of the basic requirements are clear, such as efficient sequential writing, compact representation of the data, portability, long-term accessibility, and the freedom to tune file sizes to optimize storage system performance.

## 1.3 Support Systems

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### 1.3.1 Experiment Control System

*Author to be assigned*

The complete SuperB experiment (power supplies, front-end, DAQ, etc.) must be controlled by an Experiment Control System (ECS). As shown in Fig. 1.1, the ECS is responsible both for controlling the experiment and for monitoring its functioning.

**Configuring the Front-ends:** Many front-end parameters must be initialized before the system can work correctly. The number of parameters per channel can range from a only a few to large per-channel lookup tables. The ECS may also need to read back parameters from registers in the front-end hardware to check the status or verify that the contents have not changed. For a fast detector configuration and recovery turnaround in factory mode, it is critical to not have bottlenecks either in the ECS itself, or in the ECS' access to the front-end hardware. If technically feasible and affordable, front-end electronics on or near the detector should be shielded or engineered to avoid frequent parameter reloads due to radiation-induced single event upsets—reconfiguring through the ECS should only be considered as a last resort.

**Calibration:** Calibration runs require extended functionality of the ECS. In a typical calibration run, after loading calibration parameters, event data collected with these parameters must be sent through the DAQ system and analyzed. Then the ECS must load

the parameters for the next calibration cycle into the front-ends and repeat.

**Testing the FEE:** The ECS may also be used to remotely test all FEE electronics modules using dedicated software. This obviates the need for independent self-test capability for all modules.

**Monitoring the Experiment:** The ECS continuously monitors the entire experiment to insure that it functions properly. Some examples include (1) independent spying on event data to verify data quality, (2) monitoring the power supplies (voltage, current limits, etc.), and (3) monitoring the temperature of power supplies, crates, and modules. Support for monitoring the FEE modules themselves must be built into the FEE hardware so that the ECS can be informed about FEE failures. The ECS also acts as a first line of defense in protecting the experiment from a variety of hazards. In addition, an independent, hardware-based detector safety system (part of the Detector Control System, see 1.3.4) must protect the experiment against equipment damage in case the software-based ECS is not operating correctly.

The specific requirements that each of the sub-systems makes on ECS bandwidth and functionality must be determined (or at least estimated) as early as possible so that the ECS can be designed to incorporate them. Development of calibration, test, and monitoring routines must be considered an integral part of sub-system development, as it requires detailed knowledge about sub-system internals.

**Possible ECS Implementation:** The field bus used for the ECS has to be radiation tolerant on the detector side and provide very high reliability. Such a bus has been designed for the LHCb experiment: it is called SPECS (Serial Protocol for Experiment Control System) [7]. It is a bidirectional 10 Mbits/s bus that runs over standard Ethernet Cat5+ cable and provides all possible facilities for ECS (like JTAG (Joint Test Action Group) and I2C (Inter IC)) on a small mezzanine. It could be easily adapted to the SuperB requirements. Though SPECS was initially based on PCI boards, it is currently being

translated to an Ethernet-based system, as part of an LHCb upgrade, also integrating all the functionalities for the out-of-detector elements.

For the electronics located far from the detector, Ethernet will be used for ECS communication.

### 1.3.2 Event Data Quality Monitoring and Display

SL

Event data quality monitoring is based on quantities calculated by the L3 (and possibly L4) trigger, as well as quantities calculated by a more detailed analysis on a subset of the data. A distributed histogramming system collects the monitoring output histograms from all sources and makes them available to automatic monitoring processes and operator GUIs.

### 1.3.3 Run Control System

GM

The control and monitor of the experiment is performed by the Run Control System (RCS), providing a single point of entry to operate and monitor the entire experiment. It is a collection of software and hardware modules that handle the two main functions of this component: controlling, configuring, and monitoring the whole Online system, and providing its user interface. The RCS interacts both with the Experiment Control System (ECS) and with the Detector Control System (DCS). We expect the RCS to utilize modern web technologies.

### 1.3.4 Detector Control System

SL

The Detector Control System (DCS) is responsible for ensuring detector safety, controlling the detector and detector support system, and monitoring and recording detector and environmental conditions.

Efficient detector operations in factory mode require high levels of automation and automatic recovery from problems. The DCS plays a key role in maintaining high operational efficiency, and tight integration with the Run Control System is highly desirable.

Low-level components and interlocks responsible for detector safety (Detector Safety System, DSS) will typically be implemented as simple circuits or with programmable logic controllers (PLCs).

The software component will be built on top of a toolkit that provides the interface to whatever industrial buses, sensors, and actuators may be used. It must provide a graphical user interface for the operator, have facilities to generate alerts automatically, and have an archiving system to record the relevant detector information. It must also provide software interfaces for programmatic control of the detector.

We expect to be able to use existing commercial products and controls frameworks developed by the CERN LHC experiments.

### 1.3.5 Other Components

SL

**Electronic Logbook:** A web-based logbook, integrated with all major Online components, allows operators to keep an ongoing log of the experiment's status, activities and changes.

**Databases:** Online databases such as configuration, conditions, and ambient databases are needed to track, respectively, the intended detector configuration, calibrations, and actual state and time-series information from the DCS.

**Configuration Management:** The configuration management system defines all hardware and software configuration parameters, and records them in a configuration database.

**Performance Monitoring:** The performance monitoring system monitors all components of the Online.

**Software Release Management:** Strict software release management is required, as is a tracking system that records the software version (including any patches) that was running at a given time in any part of the ETD/Online system. Release management must cover FPGAs and other firmware as well as software.

**Computing Infrastructure Reliability:** The Online computing infrastructure (including the specialized and general-purpose networks, file,

database and application servers, operator consoles, and other workstations) must be designed to provide high availability, while being self-contained (sufficiently isolated and provided with firewalls) to minimize external dependencies and downtime.

### 1.3.6 Software Infrastructure

#### GM + SL

The data acquisition and online system is basically a distributed system built with commodity hardware components. Substantial manpower will be needed to design the software components—taking a homogeneous approach in both the design and implementation phases. An Online software infrastructure framework will help organize this major undertaking. It should provide basic memory management, communication services, and the executive processes to execute the Online applications. Specific Online applications will make use of these general services to simplify the performance of their functions. Middleware designed specifically for data acquisition exists, and may provide a simple, consistent, and integrated distributed programming environment.

## 1.4 R&D

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For the overall ETD/Online system, substantial R&D is needed to better understand the global system requirements, develop solutions, and probe the possible upgrade paths to handle luminosities of up to  $4 \times 10^{36} \text{ cm}^{-2}\text{sec}^{-1}$  during the lifetime of the experiment.

**Data Links:** The data links for SuperB require R&D in the following areas: (1) studying jitter related issues and filtering by means of jitter cleaners; (2) coding patterns for effective error detection and correction; (3) radiation qualification of link components; and (4) performance studies of the serializers/de-serializers embedded in the new generation of FPGAs (Virtex6, Xilinx, etc.)

**Readout Module:** Readout Module R&D includes investigation of 10 Gbits/s Ethernet tech-

nology, and detailed studies of the I/O subsystem on the ROM boards. The possibility of implementing the ROM functions in COTS computers by developing suitable PCIe boards (such as optical link boards for FCTS and FEE links, or personality cards to implement sub-detector-specific functions) should also be investigated.

**Trigger:** For the L1 trigger, the achievable minimum latency and physics performance will need to be studied. The studies will need to address many factors including (1) improved time resolution and trigger-level granularity of the EMC and a faster DCH than *BABAR*; (2) potential inclusion of SVT information at L1; (3) the possibility of a L1 Bhabha veto; (4) possibilities for handling pile-up and overlapping (spatially and temporally) events at L1; and (5) opportunities created by modern FPGAs to improve the trigger algorithms.

For the HLT, studies of achievable physics performance and rejection rates need to be conducted, including the risks and benefits of a possible L4 option.

**ETD Performance and Dead Time:** The design parameters for the ETD system are driven by trigger rates and dead time constraints, and will need to be studied in detail to determine the requirements for (1) trigger distribution through the FCTS, (2) the FEE/CFEE buffer sizes, and (3) for handling pile-up and overlapping events. Input from the L1 trigger R&D and from background simulation studies will be required.

**Event Builder and HLT Farm:** The main R&D topics for the Event Builder and HLT Farm are (1) the applicability of existing tools and frameworks for constructing the event builder; (2) the HLT farm framework; and (3), event building protocols and how they map onto network hardware.

**Software Infrastructure:** To provide the most efficient use of resources, it is important to investigate how much of the software infrastructure, frameworks and code implementation can

be shared with Offline computing. This requires us to determine the level of reliability-engineering required in such a shared approach. We also must develop frameworks to take advantage of multi-core CPUs.

## 1.5 Conclusions

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The architecture of the ETD system for Super*B* is optimized for simplicity and reliability at the lowest possible cost. It builds on substantial in-depth experience with the *BABAR* experiment, as well as more recent developments derived from building and commissioning the LHC experiments. The proposed system is simple and safe. Trigger and data readout are fully synchronous—allowing them to be easily understood and commissioned. Safety margins are specifically included in all designs to deal with uncertainties in backgrounds and radiation levels. Event readout and event building are cen-

trally supervised by a FCTS system which continuously collects all the information necessary to optimize the trigger rate. The hardware trigger design philosophy is similar to that of *BABAR* but with better efficiency and smaller latency. The event size remains modest.

The Online design philosophy is similar—leveraging existing experience, technology, and toolkits developed by *BABAR*, the LHC experiments, and commercial off-the-shelf computing and networking components—leading to a simple and operationally efficient system to serve the needs of Super*B* factory-mode data taking.

## 1.6 Organizational Structure of Electronics, Trigger, DAQ and Online

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DB + UM + SL



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## 2 Electronics

Breton/Marconi/Luitz Pages ? 12-15 pages

### 2.1 Electronics overview

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The general design approach is to standardize components across the system as much as possible, to use mezzanine boards to isolate sub-system-specific functions differing from the standard design, and to use commercially available common off-the-shelf (COTS) components where viable.

### 2.2 Common components

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#### 2.2.1 Clock, Control and Data Links

- [To be updated to CERN workshop 11/2011 outcome](#)

Designing and validating the different serial links required for SuperB (for data transmission, timing, and control commands distribution and read-out) will require substantial effort during the TDR phase. Because of fixed latency and low jitter constraints, simple solutions relying on off-the-shelf electronics components must be thoroughly tested to validate them for use in clock and control links. Moreover, because radiation levels on the detector side are expected to be high, R&D will be necessary to qualify the selected chip-sets for radiation robustness. Since requirements for the various link types differ, technical solutions for different link types may also differ.

The links are used to distribute the frequency-divided machine clock (running at 59 MHz) and fast control signals such as trigger pulses, bunch crossing, and event IDs or other qualifiers to all components of the ETD system. Copper wires are used for short haul data transmission

(< 1m), while optical fibres are used for medium and long haul. To preserve timing information, suitable commercial components will be chosen so that the latency of transmitted data and the phase of the clock recovered from the serial stream do not change with power cycles, resets, and loss-of-locks. Encoding and/or scrambling techniques will be used to minimize the jitter on the recovered clock. The same link architecture is also suitable for transmitting regular data instead of fast controls, or a combination of both.

Link types can be divided into two classes:

**A-Type:** The A-type links are homogeneous links with both ends off-detector. Given the absence of radiation, they might be implemented with Serializer-De-serializers (SerDes) embedded in FPGAs (Field Programmable Gate Arrays). Logic in the FPGA fabric will be used to implement fixed latency links and to encode/decode fast control signals. A-Type links are used to connect the FCTS system to the DAQ crate control and to the Global Level 1 Trigger. A-Type links run at approximately 2.2 Gbits/s.

**B-Type:** The B-type hybrid links have one end on-detector and the other end off-detector. The on-detector side might be implemented with off-the-shelf radiation-tolerant components—the off-detector end might still be implemented with FPGA-embedded SerDes. B-Type links connect the FCTS crate to the FEE and the FEE to ROMs. The B-Type link speed might be limited by the off-the-shelf SerDes performance, but is expected to be at least 1 Gbit/s for the FCTS to FEE link and about 2 Gbits/s for the FEE to ROM link.

All links can be implemented as plug-in boards or mezzanines, (1) decoupling the development of the user logic from the high-speed



link design, (2) simplifying the user board layout, and (3) allowing an easy link upgrade without affecting the host boards. Mezzanine specifications and form-factors will likely be different for A-Type and B-Type links, but they will be designed to share a common interface to the host board to the maximum possible extent.

### 2.2.2 FCTS Links

### 2.2.3 Data Links

### 2.2.4 Common Front-End Electronics

### 2.2.5 Power supplies (?)

### 2.2.6 Grounding and Shielding (?)

### 2.2.7 Cable Plant (?)

## 2.3 Subsystem-specific Electronics

7-10 pages

### 2.3.1 SVT Electronics

The SVT electronics shown in Fig. 2.1 is designed to take advantage, where possible, of the data-push characteristics of the front-end chips. The time resolution of the detector is dominated by the minimal time resolution of the FSSR2 chip, which is 132 ns. Events are built from packets of three minimal time slices (396 ns event time window). The readout chain in layer 0 starts from a half-module holding two

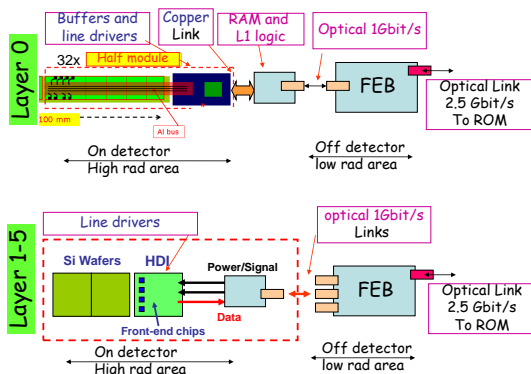


Figure 2.1: SVT Electronics

sets of pixel chips (2 readout sections, ROS). Data are transferred on copper wires to boards located a few meters away from the interaction region where local buffers will store the read hits. As discussed in the SVT chapter, for layer 0, the data rate is dominated by the background. The bandwidth needed is about 16 Gbits/s/ROS. This large bandwidth is the main reason to store hits close to the detector and transfer only hits from triggered events.

For events accepted by the L1 trigger, the bandwidth requirement is only 0.85 Gbits/s and data from each ROS can be transferred on optical links (1 Gbit/s) to the front-end boards (FEB) and then to ROMs through the standard 2 Gbits/s optical readout links. Layers 1-5 are read out continuously with the hits being sent to the front-end boards on 1 Gbit/s optical links. On the FEBs, hits are sorted in time and formatted to reduce event size (timestamp stripping). Hits of triggered events are then selected and forwarded to the ROMs on 2 Gbits/s standard links.

Occupancies and rates on layers 3-5 should be low enough to make them suitable for fast track searching so that SVT information could be used in the L1 trigger. The SVT could provide the number of tracks found, the number of tracks not originating from the interaction region, and the presence of back-to-back events in the  $\phi$  coordinate. A possible option for SVT participation to the L1 trigger would require two L1 trigger processing boards each one linked to the FEBs of layers 3-5 with synchronous optical links.

In total, the SVT electronics requires 58 FEBs and 58 ROMs, 58 optical links at 2 Gbits/s, 308 links at 1 Gbit/s (radiation hard) and, optionally, two L1 trigger processing boards and about 40 links at 1.25 Gbits/s for L1 trigger processing.

### 2.3.2 DCH Electronics

The design is still in a very early stage, so we only provide a baseline description of the drift chamber front-end electronics. It does not include additional front-end features currently un-

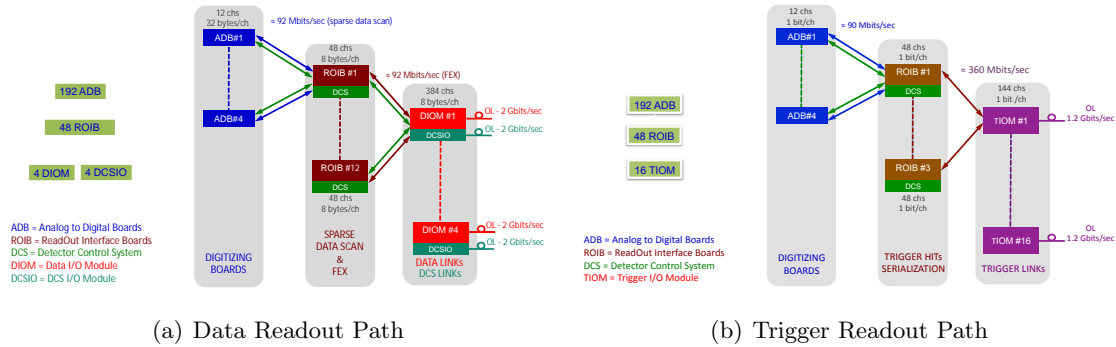


Figure 2.2: DCH Electronics

der study (such as a cluster counting capability).

The DCH provides charged particle tracking,  $dE/dx$ , and trigger information. The front-end electronics measures the drift time of the first electron and the total charge collected on the sense wires, and generates the information to be sent to the L1 trigger.

The DCH front-end chain can be divided into three different blocks:

**Very Front End Boards (VFEB):** The VFEBs contain HV distribution and blocking capacitors, protection networks and preamplifiers. They could also host discriminators. The VFEBs are located on the (backward) chamber end-plate to maximize the S/N ratio.

**Data Conversion and Trigger Pattern Extraction:** Data conversion incorporates both TDCs (1 ns resolution, 10 bits dynamic range) and continuous sampling ADCs (6 bits dynamic range). Trigger data contain the status of the discriminated channels, sampled at about 7 MHz (compared to 3.7 MHz in *BABAR*). This section of the chain can be located either on the end-plate (where power dissipation, radiation environment, and material budget are issues) or in external crates (where either micro-coax or twisted cables must be used to carry out the preamplifier signals).

**Readout Modules:** The ROMs collect the data from the DCH FEE and send zero-suppressed data to DAQ and trigger.

The number of links required for data transfer to the DAQ system can be estimated based on the following assumptions: 150 kHz L1 trigger rate, 10k channels, 15% chamber occupancy in a  $1 \mu\text{s}$  time window, and 32 bytes per channel. At a data transfer speed of 2 Gbits/s per link, about 40 links are needed. 56 synchronous 1.25 Gbits/s links are required to transmit the trigger data sampled at 7 MHz. The topology of the electronics suggests that the number of ECS and FCTS links should be the same as the number of readout links.

### 2.3.3 PID Electronics

**Forward PID Option:** There are currently two detector options be considered for the forward PID.

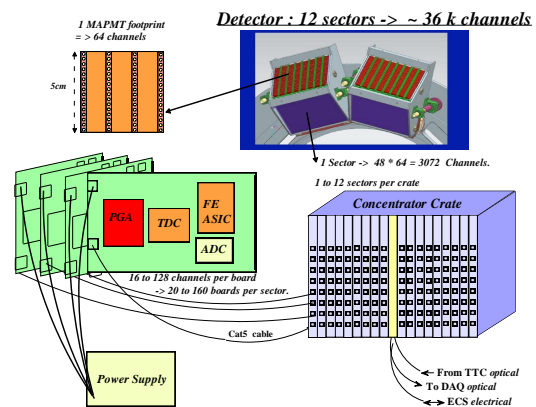


Figure 2.3: PID Electronics

The first option is to measure the time of flight (TOF) of particles from the interaction point to the PID detector. Two implementations are under consideration—a pixel detector which would lead to a large number of read-out channels (7200), or a DIRC-like detector with fused silica bars (plates) which would require a much smaller (192) channel count. Both implementations make use of fast Micro Channel Plate PMTs (MCPMT) and have to provide a measurement of the hit time with a precision of  $\sim 10$  ps. The readout would probably use fast analog memories which, as of today, are the most plausible solution for a picosecond time measurement in this environment. To achieve this time resolution, the clock distribution will have to be very carefully designed and will likely require direct use of the machine clock at the beam crossing frequency.

A second option is a Focusing Aerogel Cherenkov detector. Though the timing requirements are less severe, its  $\sim 115,000$  channels would also have to come from MCPMTs, since standard multi-anode PMTs cannot be used in the high magnetic field where it resides. Since the time precision needed is similar to that of the barrel, the same type of electronics could be used. At least 50 links would be the minimum necessary for the data readout, while the ECS and FCTS would require a maximum of about 50 additional links.

**Barrel PID:** The barrel PID electronics must provide the measurement of the arrival time of the photons produced in the fused silica bars with a precision of about 100 ps rms. The SuperB detector baseline is a focusing DIRC, using multi-anodes photo multipliers. This optical design (smaller camera volume, and materials) reduces the background sensitivity by at least one order of magnitude compared to BABAR thus reducing the rate requirements for the front-end electronics.

The baseline design is implemented with 16-channel TDC ASICs—offering the required precision of 100 ps rms. A 12-bit ADC can provide an amplitude measurement, at least for calibration, monitoring and survey, which is transmit-

ted with the hit time. A 16-channel front-end analog ASIC must be designed to sample and discriminate the analog signal. Both ASICs would be connected to a radiation-tolerant FPGA which would handle the hit readout sequence and push data into the L1 trigger latency buffers.

This front-end electronics must all sit on the MAPMT base, where space is very limited and cooling is difficult. However, crates concentrating front-end data and driving the fast optical links can be located outside the detector in a more convenient place where space is available. They would be connected to the front-end through standard commercial cables (like Cat 5 Ethernet cables). The readout mezzanines would be implemented there, as well as the FCTS and ECS mezzanines from where signals would be forwarded to the front-end electronics through the same cables.

The system would be naturally divided into 12 sectors. Using the baseline camera with 36,864 channels, 150 kHz trigger rate, 100 kHz/channel hit rate, 32 data bits/hit, and 2 Gbits/s link rate, the readout link occupancy should be only  $\sim 15\%$ , thus offering a pleasant safety margin. A camera using another model of PMTs with one-half the number of channels is also being studied.

An alternative readout option would be to use analog memories instead of TDCs to perform both time and amplitude measurements. This option retains more information on the hit signals but would likely be more expensive. Its advantages and disadvantages are still under study.

### 2.3.4 EMC Electronics

Two options have been considered for the EMC system design—a BABAR-like push architecture where all calorimeter data are sent over synchronous optical 1 Gbit/s links to L1 latency buffers residing in the trigger system, or a “triggered” pull architecture where the trigger system receives only sums of crystals (via synchronous 1 Gbit/s links), and only events accepted by the trigger are sent to the ROMs through standard 2 Gbits/s optical links.

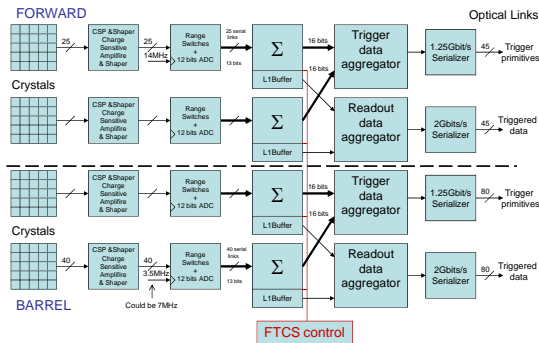


Figure 2.4: EMC Electronics

The triggered option, shown in Fig. 2.4, requires a much smaller number of links and has been chosen as the baseline implementation. The reasons for this choice and the implications are discussed in more detail below.

To support the activated liquid-source calibration, where no central trigger can be provided, both the barrel and the end-cap readout systems need to support a free running “self-triggered” mode where only samples with an actual pulse are sent to the ROM. Pulse detection may require digital signal processing to suppress noisy channels.

**Forward Calorimeter** The 4500 crystals are read out with PIN or APD photodiodes. A charge preamplifier translates the charge into voltage and the shaper uses a 100 ns shaping time to provide a pulse with a FWHM of 240 ns.

The shaped signal is amplified with two gains ( $\times 1$  and  $\times 64$ ). At the end of the analog chain, an auto-range circuit decides which gain will be digitized by a 12 bit pipeline ADC running at 14 MHz. The 12 bits of the ADC plus one bit for the range thus cover the full scale from 10 MeV to 10 GeV with a resolution better than 1%. A gain is set during calibration using a programmable gain amplifier in order to optimize the scale used during calibration with a neutron-activated liquid-source system providing gamma photons around 6 MeV.

Following the *BABAR* detector design, a push architecture with a full granularity readout scheme was first explored. In this approach, the information from 4 channels is grouped, using

copper serial links, reaching an aggregate rate of 0.832 Gbits/s per link to use up most of the synchronous optical link’s 1 Gbit/s bandwidth. A total of 1125 links are required. The main advantage of this architecture is the flexibility of the trigger algorithm that can be implemented off-detector using state of the art FPGAs without constraining their radiation resistance. The main drawback is the large cost due to the huge number of links.

The number of links can be reduced by summing channels together on the detector side, and only sending the sums to the trigger. The natural granularity of the forward detector is a module which is composed of 25 crystals. In this case, data coming from 25 crystals is summed together, forming a word of 16 bits. Then the sums coming from 4 modules are aggregated together to produce a payload of 0.896 Gbits/s. In this case, the number of synchronous links toward the trigger is only 45. The same number of links would be sufficient to send the full detector data with a 500 ns trigger window. This architecture limits the trigger granularity, and implies more complex electronics on the detector side, but reduces the number of links by a large factor (from 1125 down to 90). However, it cannot be excluded that a faster chipset will appear on the market which could significantly reduce this implied benefit.

**Barrel Calorimeter** The EMC barrel reuses the 5760 crystals and PIN diodes from *BABAR*, with, however, the shaping time reduced from 1  $\mu$ s to 500 ns and the sampling rate doubled from 3.5 MHz to 7 MHz. The same considerations about serial links discussed above for the forward EMC apply to the barrel EMC. If full granularity data were pushed synchronously to the trigger, about 520 optical links would be necessary.

The number of synchronous trigger links can be drastically reduced by performing sums of  $4 \times 3$  cells on the detector side, so that 6 such energy sums could be continuously transmitted through a single optical serial link. This permits a reduction in the number of trigger links so as to match the topology of the calorimeter elec-

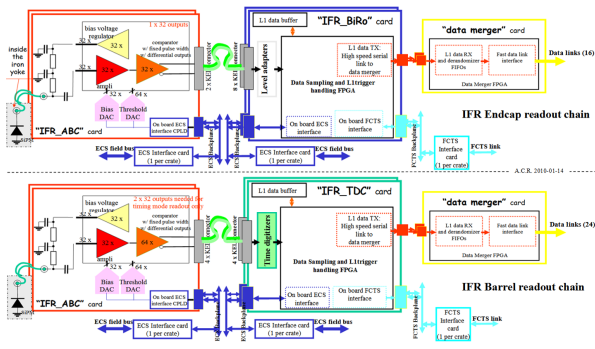


Figure 2.5: IFR Electronics

tronics boxes, which are split into 40  $\phi$  sectors on both sides of the detector. Therefore, the total number of links would be 80 both for the trigger and the data readout toward the ROMs, including a substantial safety margin ( $> 1.5$ ).

### 2.3.5 IFR Electronics

The IFR is equipped with plastic scintillators coupled to wavelength shifting fibres. Although different options have been explored, it is currently assumed that single photon counting devices (SiPM) will be located “inside” the iron, as close as possible to the scintillating assemblies. Each SiPM will be biased and read out through a single coaxial cable.

A schematic diagram of the IFR readout electronics is shown in Fig. 2.5. The first stage of the readout chain is based on the IFR\_ABC boards which provide (for 32 channels each):

- Amplification, presently based upon off-the-shelf components (COTS).
- Individually programmable bias voltages for the SiPMs.
- Comparators with individually programmable thresholds, presently based on COTS.

To minimize the length of the coaxial cables from the SiPMs to the IFR\_ABC boards, these boards need to be placed as close to the iron yoke as possible. The digital outputs of the IFR\_ABC boards will then be processed in different ways for the IFR barrel and end-caps.

**IFR Barrel** The barrel scintillation elements are mounted parallel to the beam axis. The time of arrival of pulses from both ends of the scintillating elements must be recorded so that the z-position of particle hits can be determined during reconstruction. The signals are read out with IFR\_TDC 64-channel timing digitizer boards.

The total TDC channel count estimate for the barrel is 14,400, which comes from the 3600 scintillating assemblies in the barrel that are read out at both ends with 2 comparators (with different thresholds) per end to improve timing (and position) resolution.

**IFR End-caps:** The signals from the scintillators in the IFR end-caps (which are positioned vertically and horizontally) are read out with IFR\_BiRO 128 channel “Binary Readout” boards, which sample the status of the input lines and update a circular memory buffer from which data are extracted upon trigger request.

The total channel count estimate for the end-caps is 9,600 BiRO channels coming from the two end caps, each with 2,400 scintillating assemblies in X, and 2,400 scintillating assemblies in Y read out into a single comparator per channel.

The IFR\_TDC and IFR\_BiRO digitizers should be located as closely as possible to the IFR\_ABC boards to minimize the cost of the interconnecting cables, preferably in an area of low radiation flux. In this case, commercial TDC ASICs could be used in the design. Alternatively, radiation-tolerant TDCs could be used closer to the detector. The FPGAs used in the digitizers should be protected against radiation effects by architecture and by firmware design.

The output streams from the IFR\_TDC and IFR\_BiRO boards go through custom “data concentrators” to merge the data coming from a number of digitizers, and send the resulting output data to the ROMs via the standard optical readout links.

In total, 225 IFR\_TDC boards (12 crates) and 75 IFR\_BiRO boards (4 crates) are needed. The total number of links to the ROMs is presently

estimated to be 24 for the barrel (2 links per digitizer crate), and 16 for the end-caps (4 links per digitizer crate).

To optimize the electronics topology, the number of ECS and FCTS links should match the number of readout links.

### 2.3.6 Level-1 Trigger Electronics