SVT detector Electronics Status

On behalf of the SVT community

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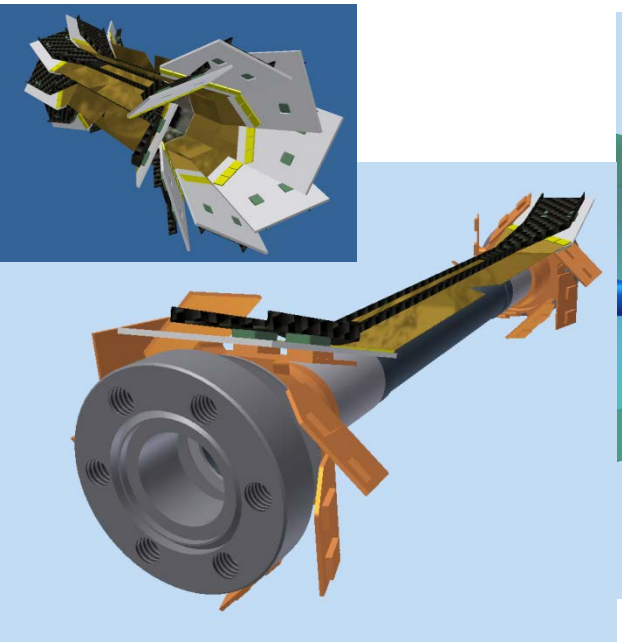
Overview:

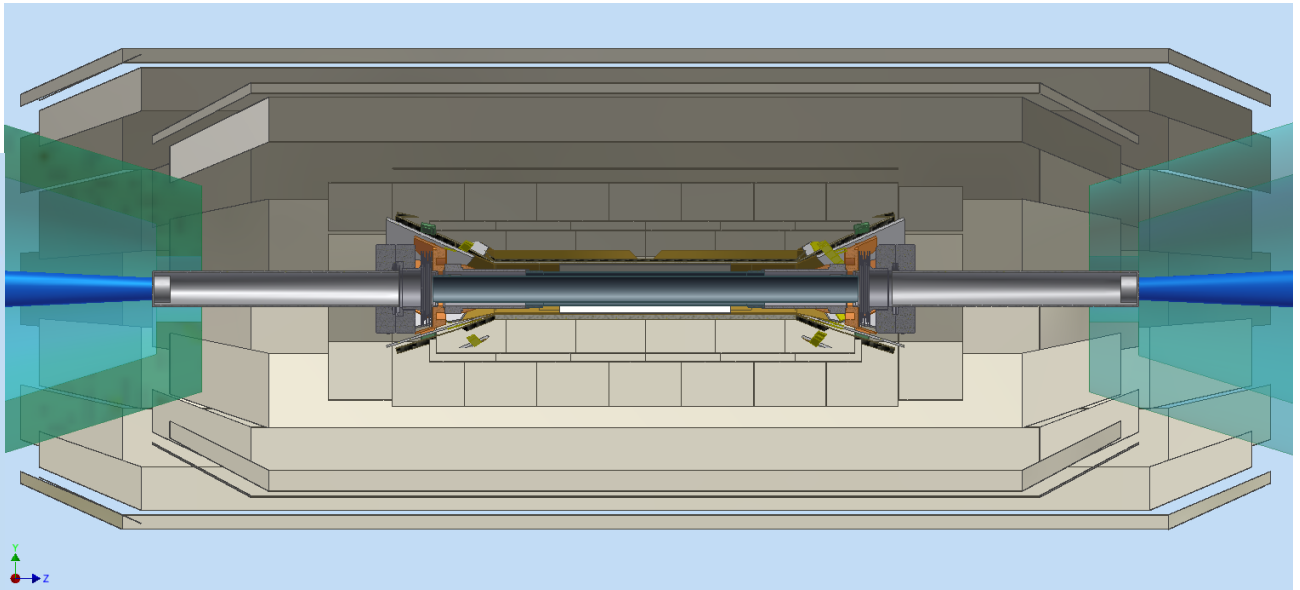
- SVT design status
- F.E. chips
- Electronic design
- Hit rates and data volumes

SVT Design

Detectors: 5 Layers with Si Strips (z, phi, L1-L5); one high precision inner layer (L0)

Open options *for L0*: striplets (45° strips), Hybrid pixels, MAPS

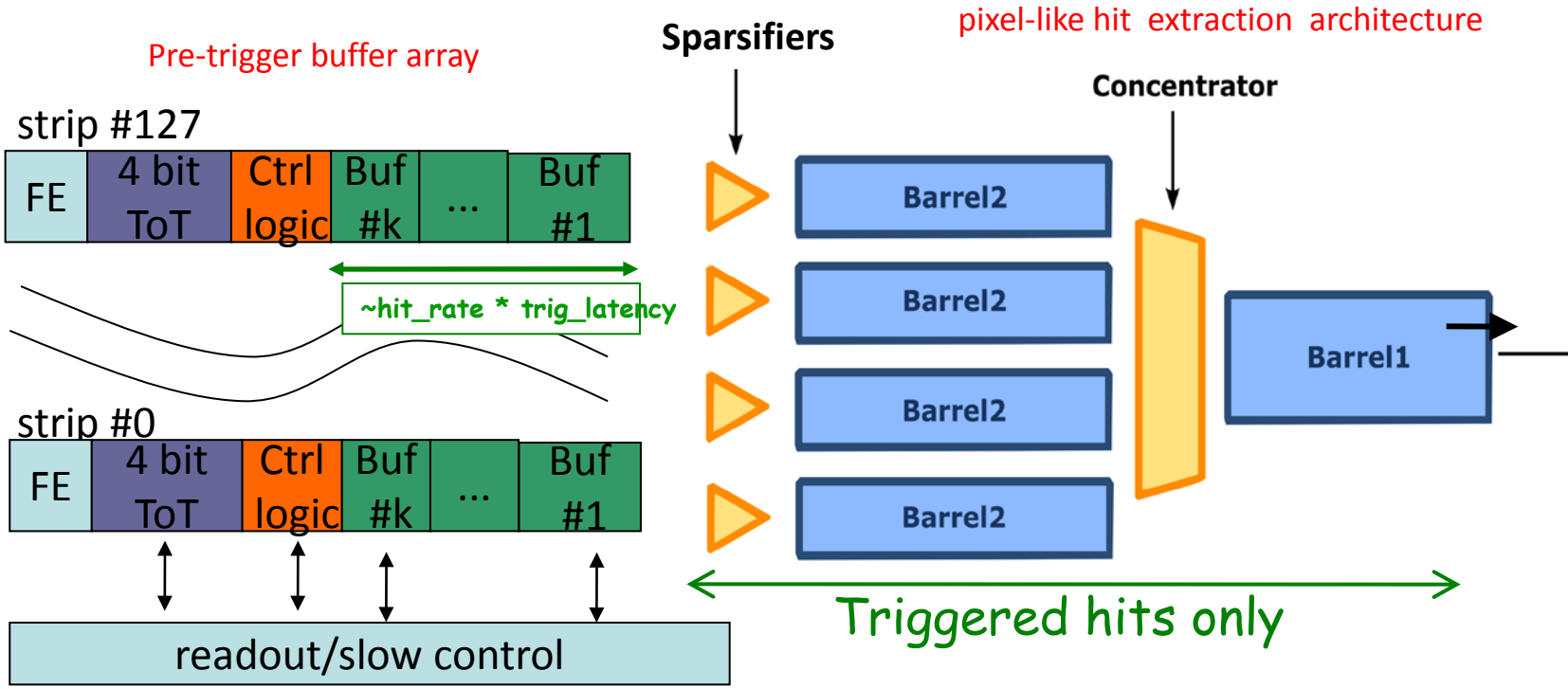




Front-End Chips: 128 channels ASIC for strips, large (>10k) pixel area chip

ROS: Layers are segmentend in phi (8-18) and z (2): 240 Read-Out Sections (ROS)

Strip readout architecture under development



How many buffers?
How many barrels?

Asynchronous logic assumed:
Triggered event size not known a-priori
(thus readout time as well)

Simulation status

- All elements have been modeled on both sides
  - *VHDL* for **hit extraction system** and **slow control**
  - *SystemVerilog* for the **strip FE logic** and **buffers**

- Test Bench developed:
  - Elements:
    - **Monte Carlo** hit generator
    - **Slow control vectors** for chip configuration and opearation
    - **Hit-IN / Hit-OUT** lists for efficiency evaluation.
    - **Device Under Test**
  - Simulation Tool: **ModelSim SE** (allows mixed-code simulations)

- So Far
  - Whole architecture integrated in simulation
  - Simulated with L0 and L1 expected rates (safety factor included)

Simulations

- Tens of ms of operation simulated
- MC hit rate trimmed to **2 MHz/strip (L0)** and **760 kHz/strip (L1)**
- Trigger latency **6 us** / trigger rate **200 kHz**.
- Time stamp resolution: **30 ns**
- Trigger buffer depth scan (8→16→32→64)
- Efficiency evaluation $\left(1-\frac{\mathrm{HitIn}-\mathrm{HitOut}}{\mathrm{HitIn}}\right)$

NB:
No multiple hits allowed on the **same strip** for the **same time interval**.
Only digital readout efficiency taken into account

Simulation results (L0/L1)

2 MHz/strip : Layer 0

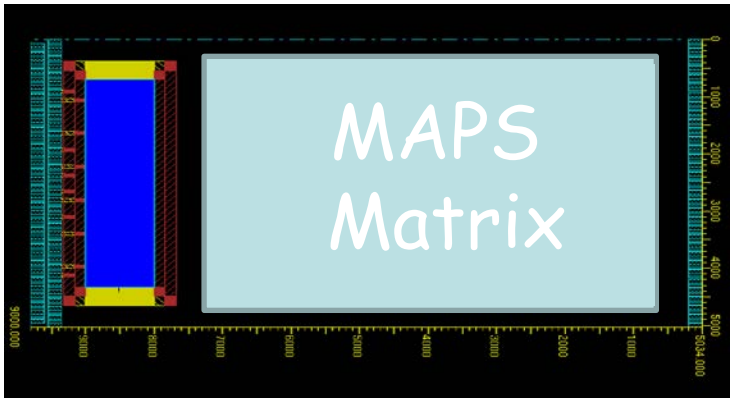
buffer size	16	32	64
buffered hits	3.8 M	12.9 M	12.9 M
of which triggered	23363	76850	23363
output triggered hits	14679	76849	23363
triggered hit lost	8684	1	0
Efficiency (%)	**62.8**	**99.9987**	**100**

760 kHz/strip : Layer 1

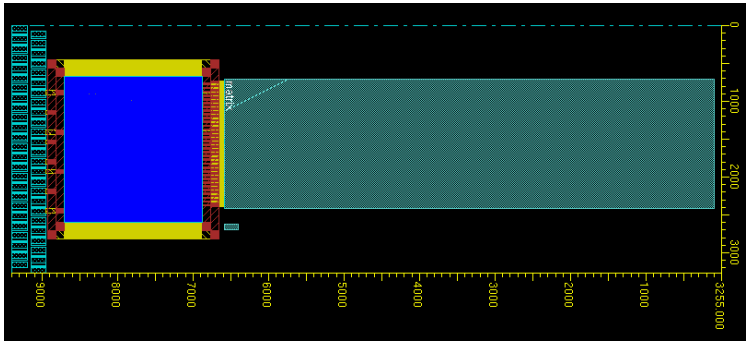
buffer size	8	16	32
buffered hits	1.4 M	7 M	7 M
of which triggered	8748	28829	28829
output triggered hits	6788	28825	28829
triggered hit lost	1960	4	0
Efficiency (%)	**77.6**	**99.986**	**100**

R&D on Pixel chip options for L0

- **Apsel-VI (MAPS)**
  - MATRIX 96x128 (2 sub-m. 48 x128)
  - **5034** um x **9800** um die area
  - 70 k Std-Cell readout
    - Core density = 25%



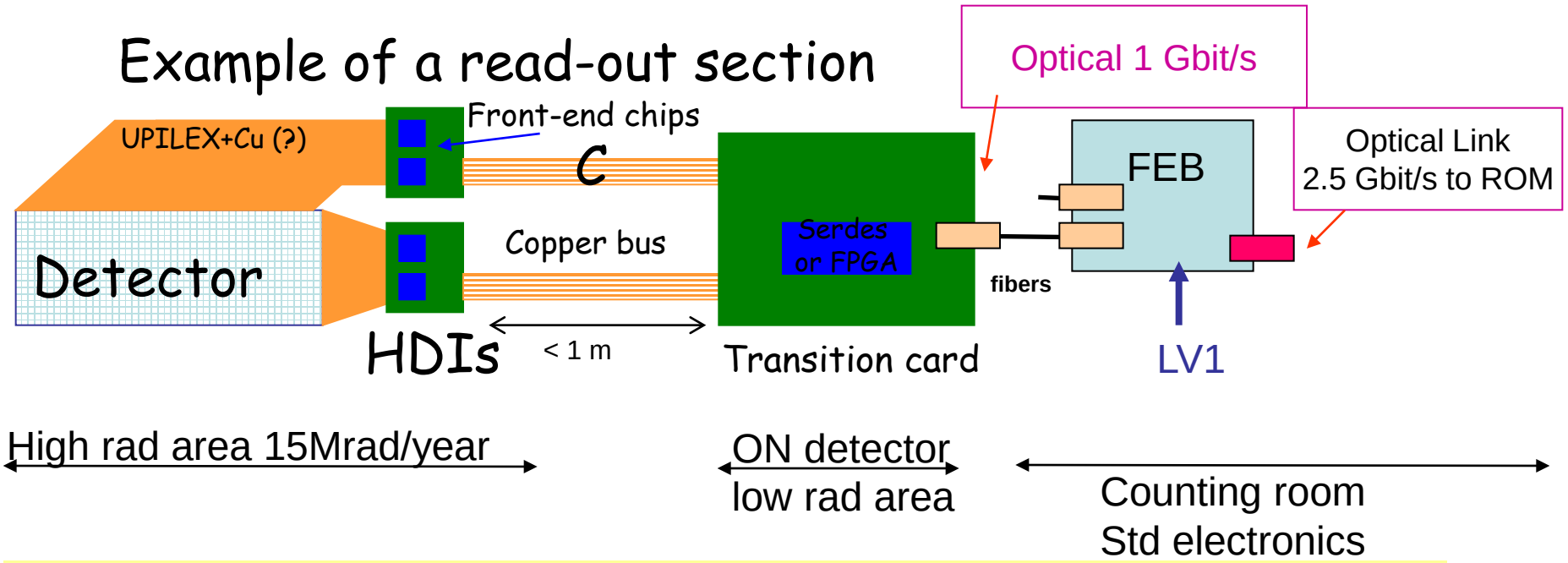
- **SuperPix1 (hybrid pixels)**
  - MATRIX 32x128 (2 sub-m. 16x128)
  - **3255** um x **9421** um die area
  - 40k Std-Cell readout
    - Core density = 20%



- **Triggered chips; L1 latency on pixels; efficiencies >98%;**
- **Output rate max: 200 MHit/s;**

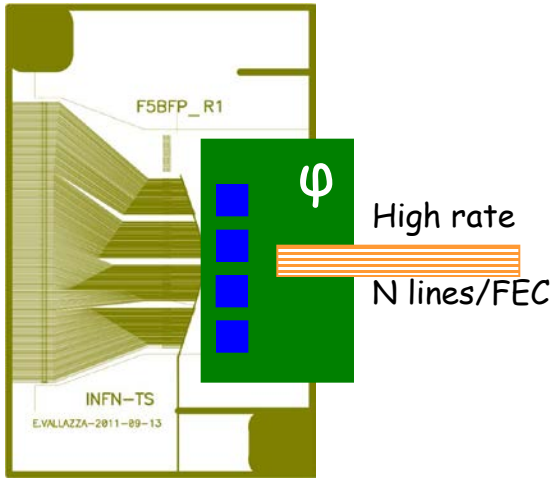
DAQ reading chain for L0-L5

DAQ chain independent on the chosen FE options



HDI card design is ongoing
Data Encoder IC .... Specs are under discussion
Rad-hard serializer to be finalized
→ looking into a low power/low speed version
Copper tail: lenght vs data transfer are under study
FEB + ROM as before

HDI and output bus



Minimal number of elements on HDI
(FE chips a data 'organizer' + serializer 2:1-4:1)

6 shared input lines:
Reset, Clock, FastClock,
Timestamp, Trigger, RegIn
1 shared output line:
RegOut
N lines x M chips in output
Ground and powering on the bus
Signal lines in standard LVDS
(CMOS to/from LVDS required on HDI if not provided on FE)

- HDI elements should be:
- Rad-hard characteristics dependent on chips
  - Requirement: > 5 Mrad/year
- Power dissipation: < 1 W/chip (guess-estimate, past values)

Number of Transition Cards and Output Bus

Layer		Module	HDI	Chip	Output Lines (180MHz) on 1 Face of the HDI	Copper Bus	Transition Card (TC)	Optical Fiber on Transition Card	GROS
L0	Top Bottom	8	16	6 6	12 12	32	32	32	32
L1	Z Phi	6	12	7 7	7 14	24	24	24	24
L2	Z Phi	6	12	7 7	7 7	24	24	24	24
L3	Z Phi	6	12	10 6	10 6	24	24	24	24
L4	Z Phi	16	32	5 4	5 4	64	32	32	32
L5	Z Phi	18	36	5 4	5 4	72	18	36	36
Total			**120**			**240**	**86+86= 172**	**172**	**172**

- **Proposal:**
- **1 Transition Card accept 1 Output Bus for L0,L1,L2,L3**
- **1 Transition Card accept 2 Output Bus for L4, L5**

1 copper bus for TC Layer 0,1,2,3

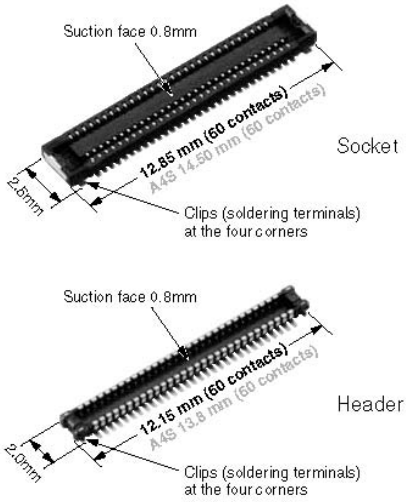
1 Fiber for TC

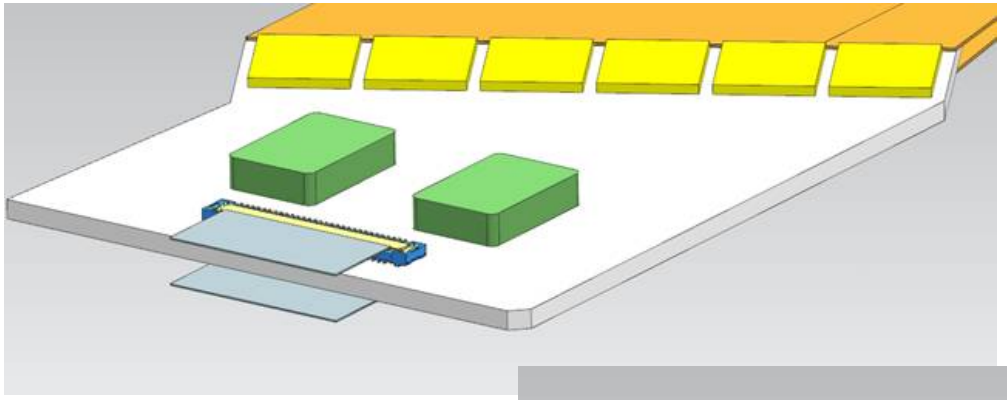
- **To reduce No of TC and to increase the size**
- **Number of LVDS lines on Output bus is limited to 8-9**

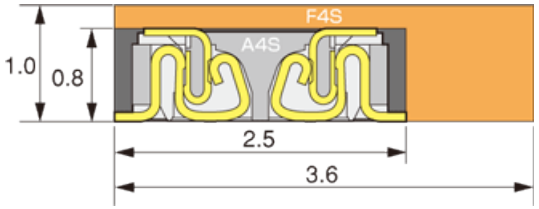
2 copper bus for TC Layer 4,5

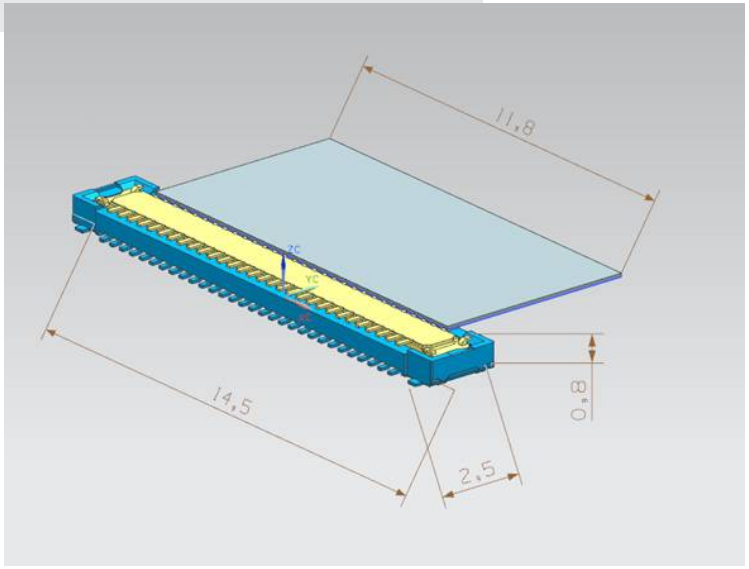
Output Bus Structure

1. The world's smallest size* (width: 2.5 mm, Terminal pitch: 0.35 mm and Mated height: 0.8 mm)
The footprint when mated is down approx. 10% from our existing A4S model (60 contacts), contributing to the functionality enhancement and size reduction of target equipment.



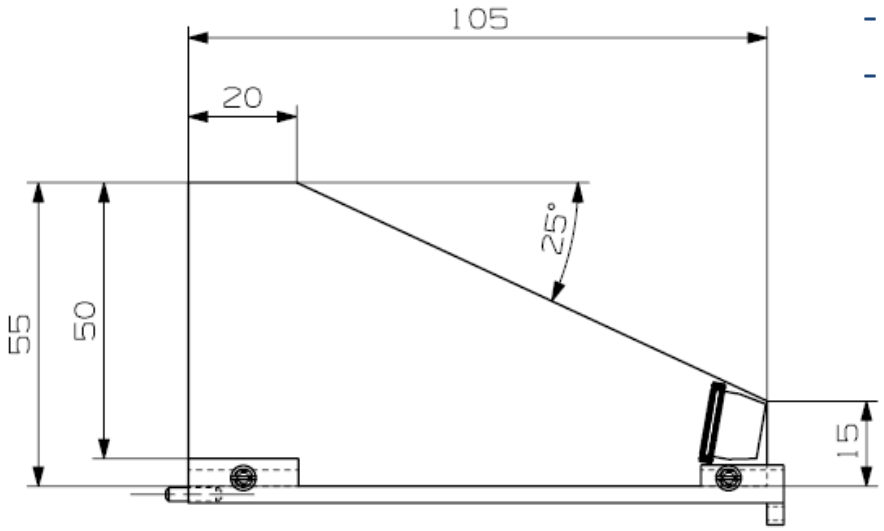






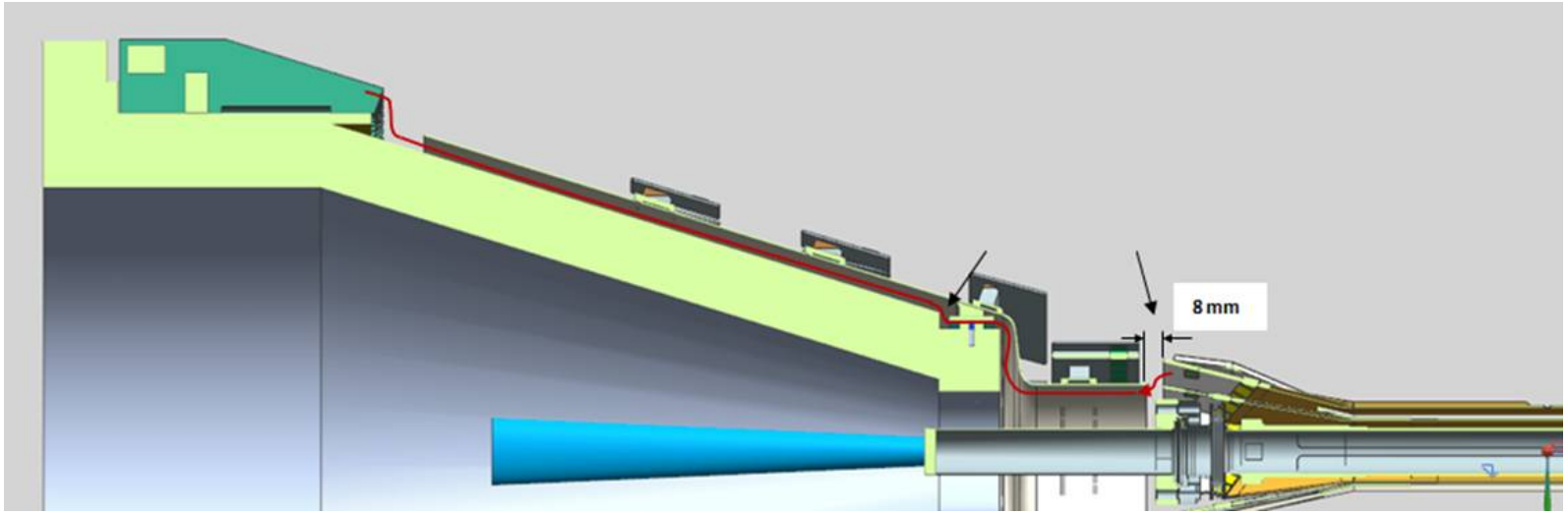
Only rated 150 Volt

The Output Bus: 3 layer Copper/Kapton Tape.
Aspect ratio: ~ 10 mm x 400-500 mm
At the connector the tape is ~ 17 mm wide

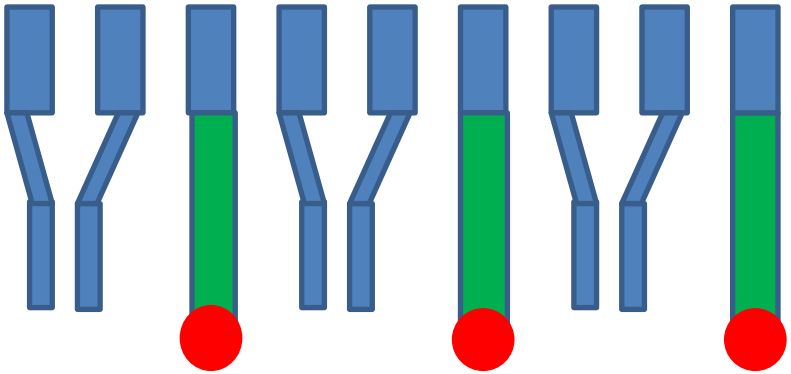


Width of Output Bus is determined by geometrical reasons:

- **Dimension of Transition Card**
- **Routing of Bus through available openings (an example is shown on bottom)**



Copper Bus Structure



Stack-up Design Rules:

LVDS Lines: Strip lines
LVDS Lines: 4 mils
LVDS Space: 4 mils
LVDS Copper Thickness ~ 20 um (~½ ounce)

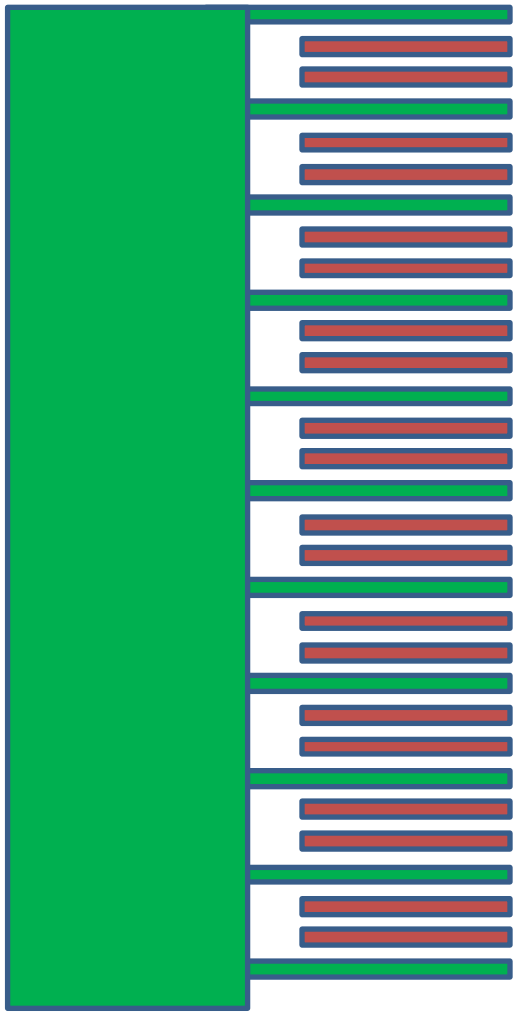
Dielectric Thickness: ~ 100 mils
Zdiff ~ 100 Ohm
To be optimized

Kapton Thickness: 2 mils (?)

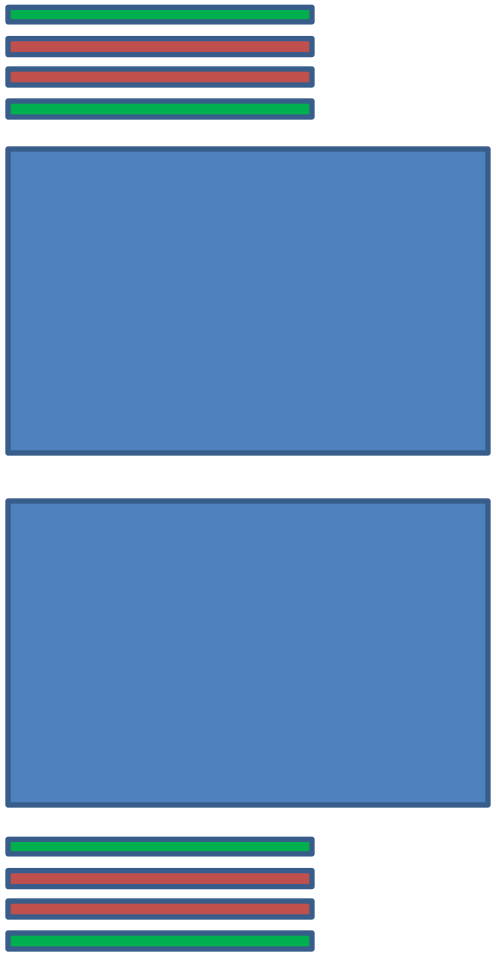
Via Diameter: 10-12 mils
Via Clearance: 6 mils

Power/Gnd Planes:
Widht ~ 4.7 mm (almost double for GND !!)
Thickness > 50 um (or 2 ounces)
Current capability ~ 3-3.5 Amps
Voltage drop (both ways) ~ 250 mV

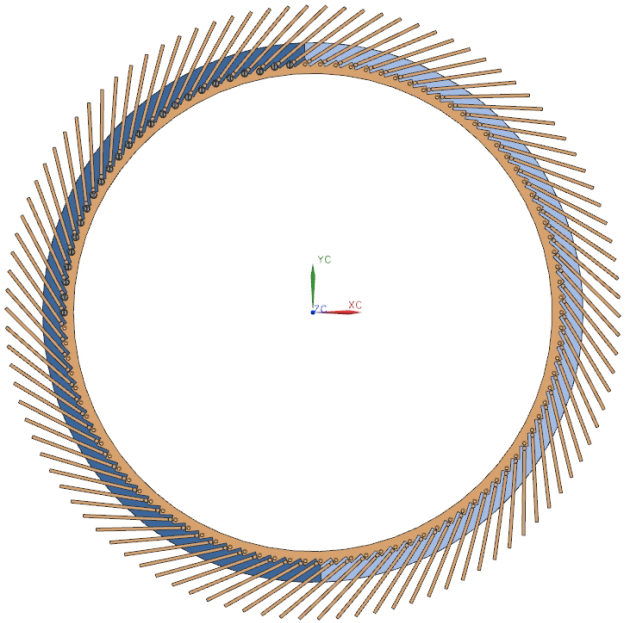
Copper Bus Structure

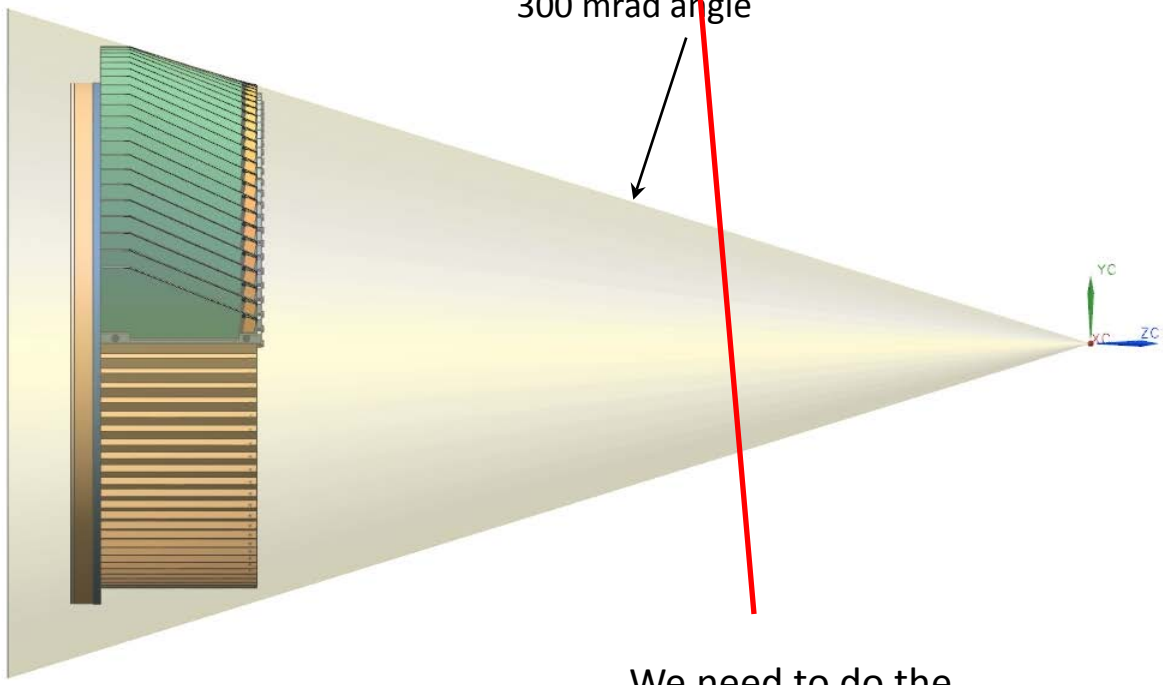


GND	1	36	GND
D1+	2	37	Reg Out +
D1-	3	38	Reg Out -
GND	4	39	GND
D2+	5	40	Power 1
D2-	6	41	Power 1
GND	7	42	Power 1
D3+	8	43	Power 1
D3-	9	44	Power 1
GND	10	45	Power 1
D4+	11	46	Power 1
D4-	12	47	Power 1
GND	13	48	Power 1
D5+	14	49	Power 1
D5-	15	50	Power 1
GND	16	51	Power 1
D6+	17	52	Power 1
D6-	18	53	
GND	19	54	Power 2
Trigger +	20	55	Power 2
Trigger -	21	56	Power 2
GND	22	57	Power 2
TimeStamp +	23	58	Power 2
Time Stamp -	24	59	Power 2
GND	25	60	Power 2
Clock +	26	61	Power 2
Clock -	27	62	Power 2
GND	28	63	Power 2
Fast Clock +	29	64	Power 2
Fast Clock -	30	65	Power 2
GND	31	66	Power 2
Reset +	32	67	GND
Reset -	33	68	Reg In +
GND	34	69	Reg In -
Not Assigned	35	70	GND



Transition cards
Alternative design: Turbine layout – n. 102 cards
(Hypothesis: only 18 cards for layer 5 instead of 36)



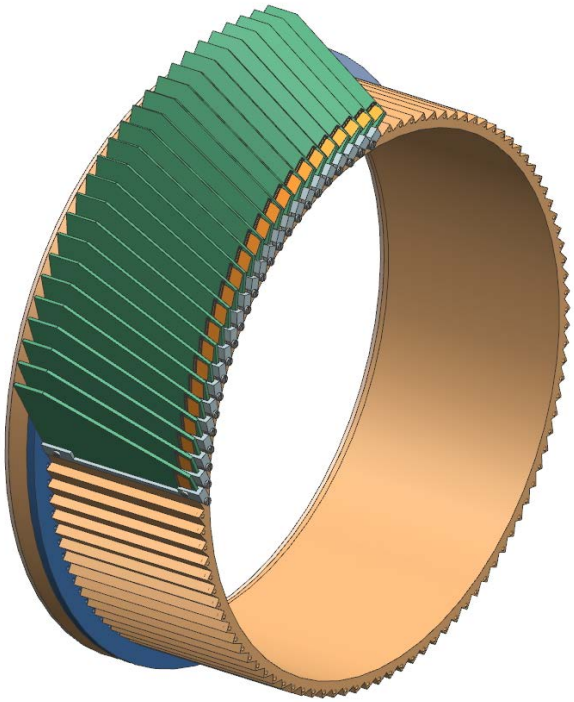


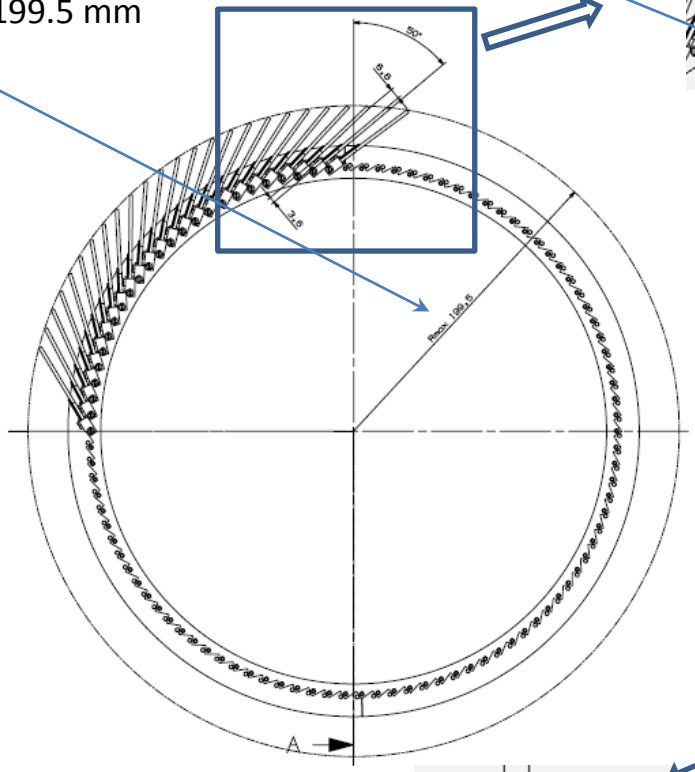
We need to do the same on L4 and reduce to 86 cards

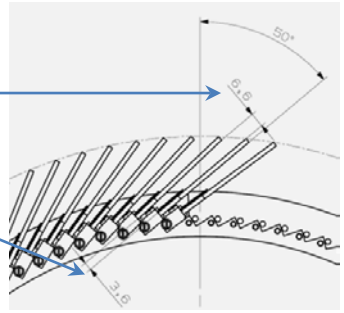
Transition cards – Turbine layout

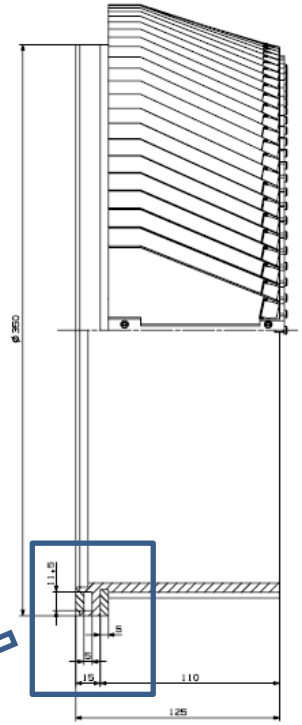
Max gap: 6.6 mm
Min gap : 3.6 mm

Max envelope radius : 199.5 mm

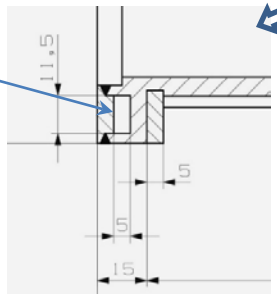




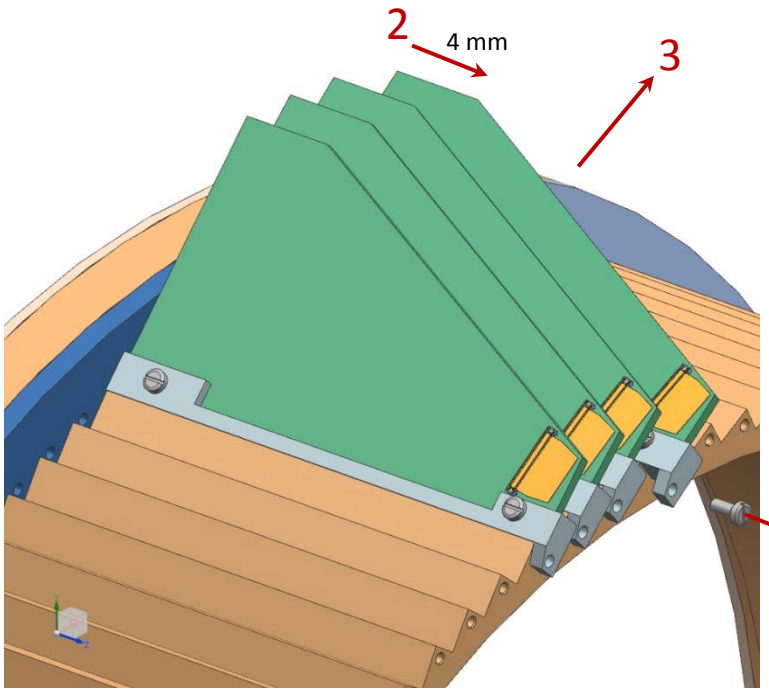




cooling space in back flange

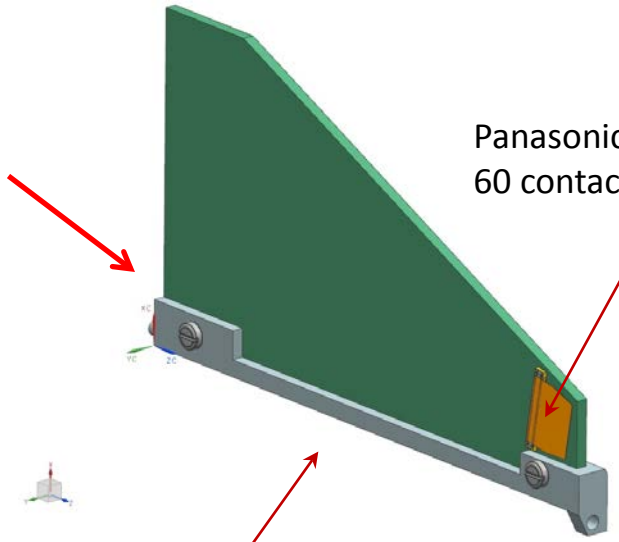


Transition cards – Turbine layout

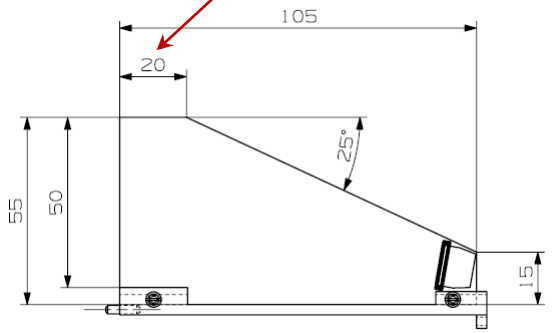


Transition Card dismantling

Some area
is blocked
by the ring



Length will be increased
by moving back the cryostat

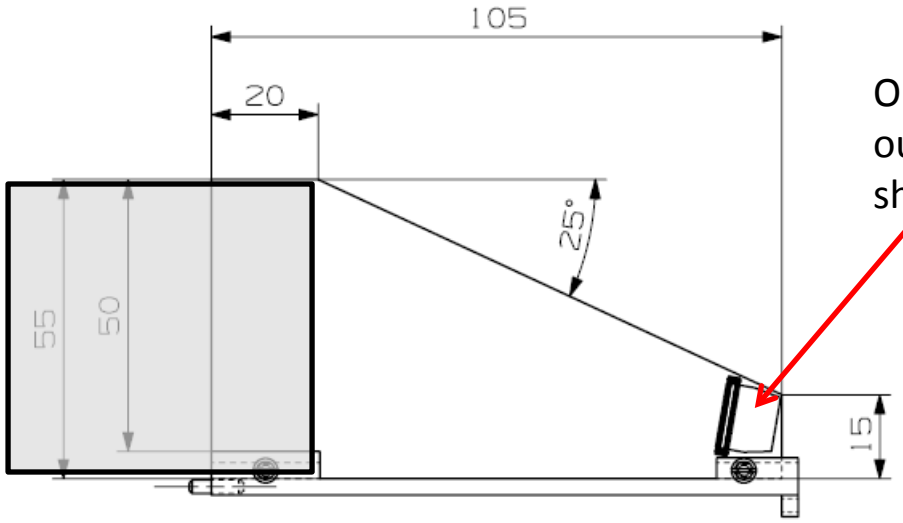


M. MONTI S. COELLI

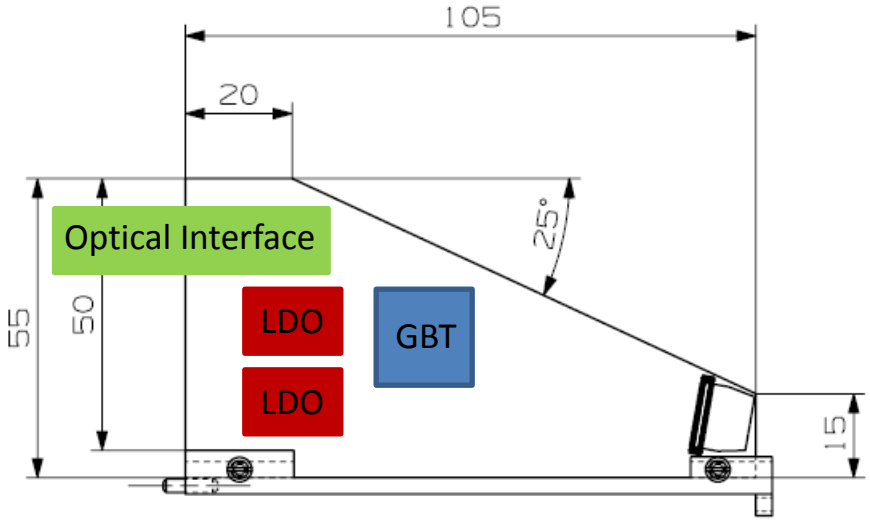
How much space is needed …..

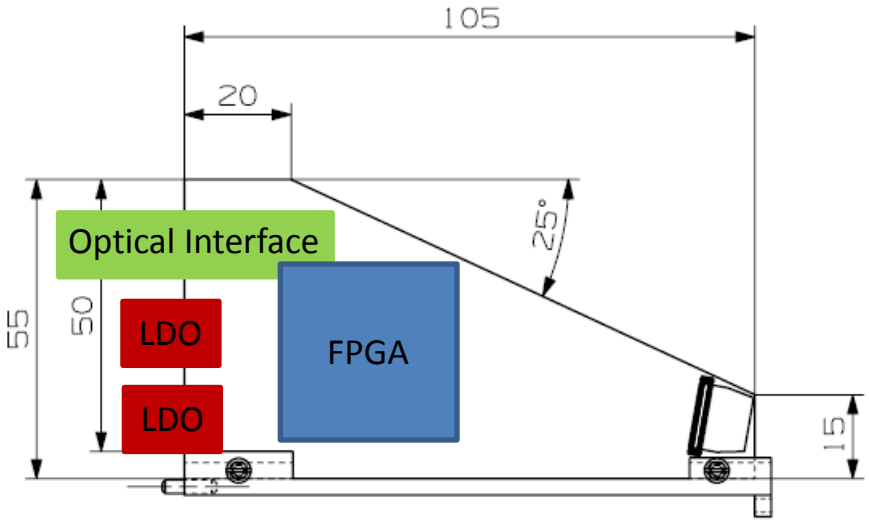
The "component" blocks have approximately the right dimensions:

- → more space considered ~ 3 cm (grey box)
- → The turbine structure is helping by increasing the other side to at least 55 mm
- → The Optical Interface 13x50x11 mm. The GBT 15x15 mm, the FPGA 32x32 mm



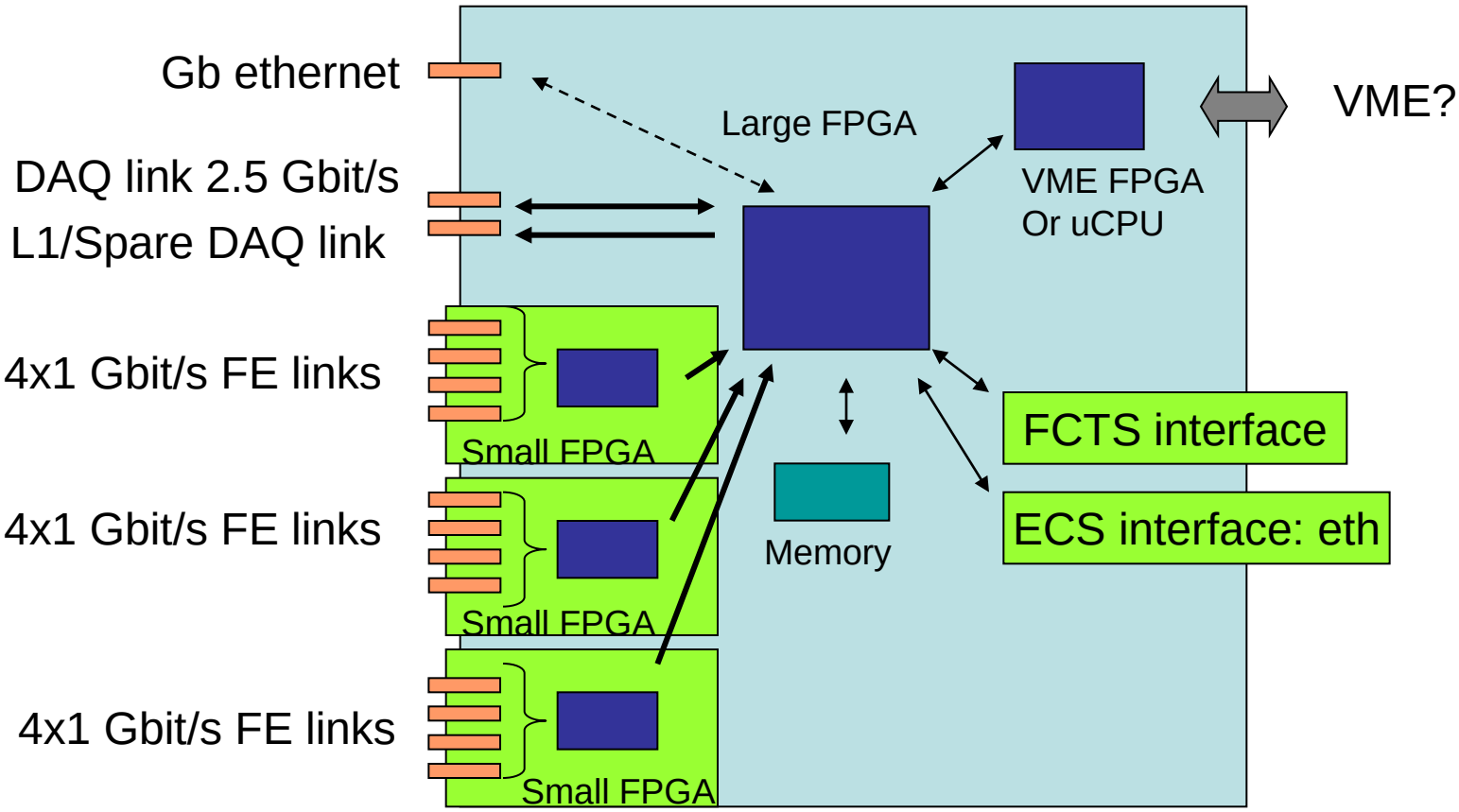
Only one output bus shown





Input Power Cables NOT shown

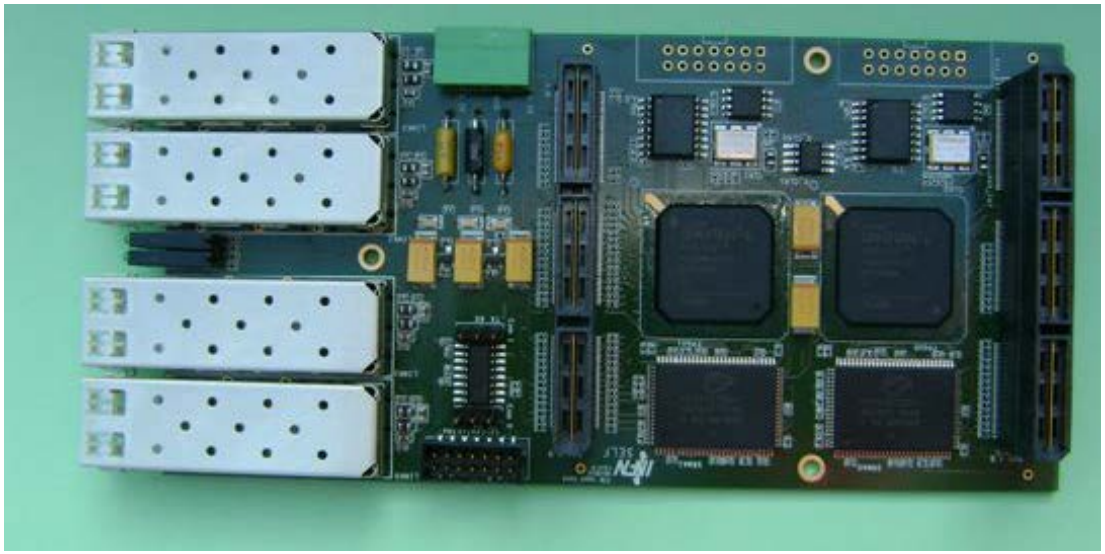
SuperB-FEB Board schematics



FCTS protocols to be decided experiment-wide
Large FPGA for data shipping and monitoring
VME FPGA or uCPU might be included in the large FPGA.

Optical link mezzanine card for EDRO

Developed as a part of ATLAS/FTK project (LNF)



4 optical links at 1 Gbit/s; FPGA Xilinx, 40/100 MHz clk (programmable)

First prototypes under tests.

Usable as link test mezzanine in SuperB

Electronic Data Load Evaluation
Design assumptions

- Detector geometry as from Luciano/Filippo
- Background rates from Cenci/Rizzo
- Fully Strip/striplet SVT – triggered
- FE chips with 128 channels
- FE word length: 20 bits (serialized)
- Trigger/DAQ
  - 150 kHz trigger rate;
  - L0-L3: 300 ns DAQ window, L4-L5: 1 us
  - 30 ns BCO Clock

Background rates

- Input rates per area

Layers	lato	Average total strip rate/area from Bruno (safety x5 included) MHz/cm2	Average total strip rate from SuperB dimensions including safety x5 and average ganging in z(Khz)
0	1	1.908E+02	1997.86
0	2	2.613E+02	1997.86
1	phi	1.497E+01	803.12
1	z	1.031E+01	507.91
2	phi	8.808E+00	572.37
2	z	6.885E+00	480.21
3	phi	2.348E+00	449.40
3	z	2.994E+00	283.24
4	phi	3.371E-01	98.49
4	z	2.180E-01	51.29
5	phi	1.593E-01	59.78
5	z	1.142E-01	33.68

- Average occupancies and total load

- Max strip rate

Layers	lato	Max strip rate for SuperB including safety x5 and average ganging in z (Khz)
0	1	1509.27
0	2	2525.38
1	phi	1445.00
1	z	726.96
2	phi	960.00
2	z	697.50
3	phi	775.00
3	z	675.78
4	phi	195.00
4	z	203.63
5	phi	135.00
5	z	133.29

- Peak chip load

Strip front-end chip

- Triggered, 128 channels, 60 MHz clock, 60/120/180 MHz output clock, serialized output.

2 Data word: Time-stamp-like and hit

Hit: 7 bits Channel ID, 4 bits ToT, 1 bit word type,
4 bits to be defined, for a total of **16 bits**
Timestamp: 10 bits Timestamp, 1 bit word type,
5 bits to be defined, for a total of **16 bits**

Guesswork: serialization using a 8b/10b protocol implies a **20 bit output word**

Layer	layer Type	Chip /ROS	Avai chan s	back. rate MHz/ cm2 (safety = 5)	Hits in BCO	Occup ancy in BCO	Group ing	Trigge red Gbit/s/ GROS	FE Board s	Event Size (hits)
0	Striplet u	6	768	230	50.2	6.54%	1	1.51	3	8037
0	Striplet v	6	768	230	50.2	6.54%	1	1.51	3	8037
1	Strip z	7	896	10.31	13.6	1.52%	1	0.41	1	1637
1	Strip phi	7	896	14.97	19.8	2.21%	1	0.59	1	2377
2	Strip z	7	896	6.88	12.9	1.44%	1	0.39	1	1550
2	Strip phi	7	896	8.81	16.5	1.85%	1	0.50	1	1985
3	Strip z	10	1280	2.994	12.0	0.94%	1	0.36	1	1438
3	Strip phi	6	768	2.35	9.4	1.22%	1	0.28	1	1129
4a	Strip z	5	640	0.218	1.0	0.15%	2	0.20	1	1038
4a	Strip phi	4	512	0.337	1.5	0.30%	2	0.30	1	1605
4b	Strip z	5	640	0.218	1.0	0.16%	2	0.20	1	1075
4b	Strip phi	4	512	0.337	1.6	0.31%	2	0.31	1	1662
5a	Strip z	5	640	0.114	0.6	0.10%	2	0.13	1	769
5a	Strip phi	4	512	0.159	0.9	0.18%	2	0.18	1	1073
5b	Strip z	5	640	0.114	0.7	0.10%	2	0.13	1	793
5b	Strip phi	4	512	0.159	0.9	0.18%	2	0.18	1	1106

- 172 GROS, 204 1-Gbps links, 20 FEBoards, <88 kB/evento

Maximum data lines per chip

		Max HIT strip rate (kHz)	DAQ Time window (us)	Hits/ chip per Trig.	Words per chip per trigger	Bits per chip per trig.	band width (Mbit /s)	Lines at 60 MHz	Lines at 120 MHz	**Lines at 180 MHz**	Chip/ ROS	Lines/ROS at 180 MHz
L0	U	2000	0.3	76.8	86.8	1736.0	260.4	6	3	**2**	6	**12**
L0	V	2000	0.3	76.8	86.8	1736.0	260.4	6	3	**2**	6	**12**
L1	Z	727	0.3	27.9	37.9	758.3	113.8	3	2	**1**	7	**7**
L1	PHI	1445	0.3	55.5	65.5	1309.8	196.5	4	2	**2**	7	**14**
L2	Z	697	0.3	26.8	36.8	735.3	110.3	3	2	**1**	7	**7**
L2	PHI	960	0.3	36.9	46.9	937.3	140.6	3	2	**1**	7	**7**
L3	Z	676	0.3	26.0	36.0	719.2	107.9	3	2	**1**	10	**10**
L3	PHI	775	0.3	29.8	39.8	795.2	119.3	3	2	**1**	6	**6**
L4	Z	204	1	26.1	36.1	722.2	108.3	3	2	**1**	5	**5**
L4	PHI	195	1	25.0	35.0	699.2	104.9	3	2	**1**	4	**4**
L5	Z	133	1	17.0	27.0	540.5	81.1	2	1	**1**	5	**5**
L5	PHI	135	1	17.3	27.3	545.6	81.8	2	1	**1**	4	**4**

1,2,4 lines **per chip** usable at 120 MHz on all SVT
14 lines **per module** max at 180 MHz (16 bits serializers)

Summary

- Strip/striplet front end chip defined.
- Digital efficiency evaluated estensively.
- Pixel options ongoing: two new chips designed.

- Definition of the DAQ Data Chain ongoing
- L0 requires 8 1-Gbit links per physical module (is space an issue?).

- FEboard-ROM links not yet decided (2-3.5-5 Gbit/s). We need up to a factor 3 compression for L0.