SuperB IFR electronics: update

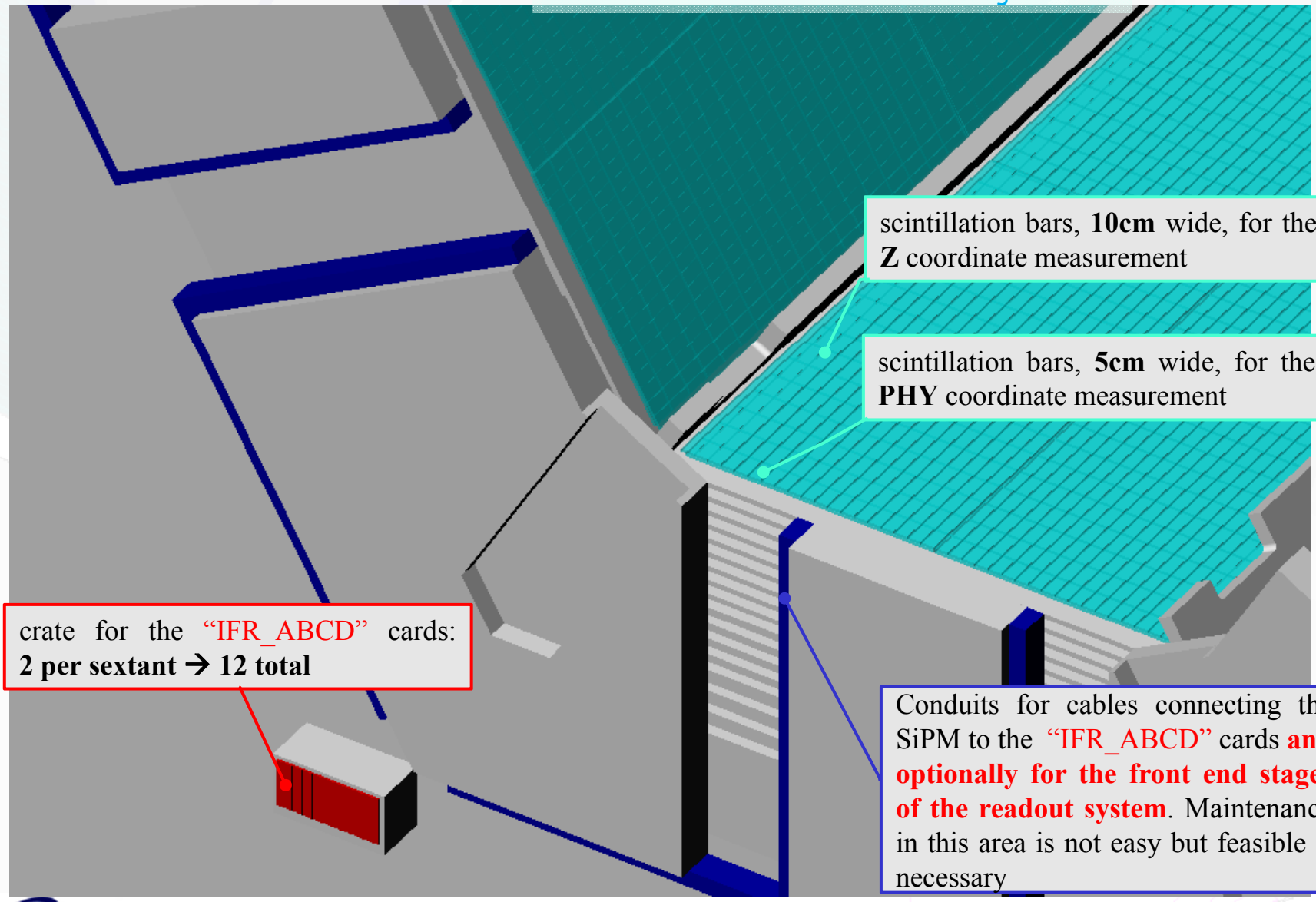
SuperB IFR electronics: update

- **features of the current baseline for the IFR detector design with "binary mode" readout**
  - layout of the scintillator bars in the barrel
  - layout of the scintillator bars in the endcaps updated
  - channel number and data bandwidth estimation updated
  - test of passive Single Ended and active Differential options for "picking-up" the signals from SiPM new
  - block diagram of the "IFR_ABCD" front end card
  - test of "CLARO" chip for SiPM readout new
- **addressing the radiation issues**
  - background rates estimates at the location of IFR front end electronics
  - results of measurements at the INFN Laboratori Nazionali di Legnaro of neutron induced effects on some key elements of the current baseline IFR readout electronics

a.c.r. 2011-11-02

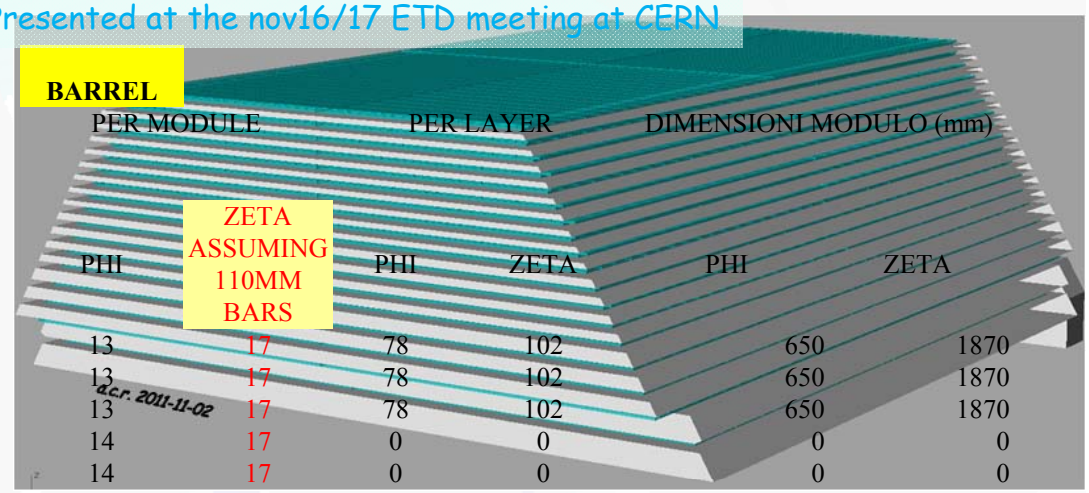
features of the current baseline IFR detector design with "binary mode" readout: barrel

Presented at the nov16/17 ETD meeting at CERN



channel number estimation: barrel

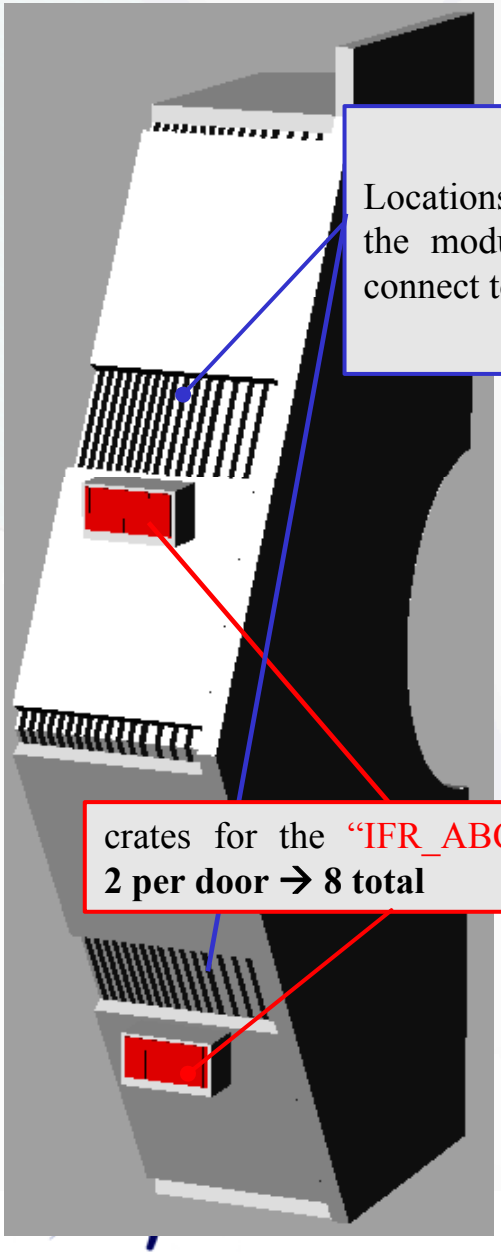
Presented at the nov16/17 ETD meeting at CERN



BARREL

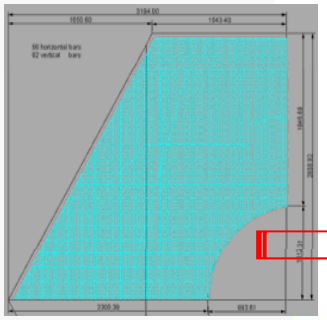
LAYER WIDTH	LAYER	No.Modules per layer	LAYER ENABLE	PER MODULE PHI	PER MODULE ZETA ASSUMING 110MM BARS	PER LAYER PHI	PER LAYER ZETA	DIMENSIONI MODULO (mm) PHI	DIMENSIONI MODULO (mm) ZETA
1963	1	6	1	13	17	78	102	650	1870
1987	2	6	1	13	17	78	102	650	1870
2050	3	6	1	13	17	78	102	650	1870
2113	4	6		14	17	0	0	0	0
2176	5	6		14	17	0	0	0	0
2240	6	6	1	14	17	84	102	700	1870
2304	7	6		15	17	0	0	0	0
2367	8	6		15	17	0	0	0	0
2431	9	6		16	17	0	0	0	0
2494	10	8	1	12	17	96	136	600	1870
2569	11	8		12	17	0	0	0	0
2641	12	8		13	17	0	0	0	0
2712	13	8	1	13	17	104	136	650	1870
2784	14	8		13	17	0	0	0	0
2879	15	8	1	14	17	112	136	700	1870
2973	16	8		14	17	0	0	0	0
3068	17	8		15	17	0	0	0	0
3144	18	8	1	15	16	120	128	750	1870
3296	19	8	1	16	16	128	128	800	1870
NUMBER OF MODULES per sextant:	64			TOTAL PER SEXTANT	1950	878	1072		
TOTAL NUMBER OF MODULES	**384**			**TOTAL CHANNELS PER BARREL**	**11700**	5268	6432		

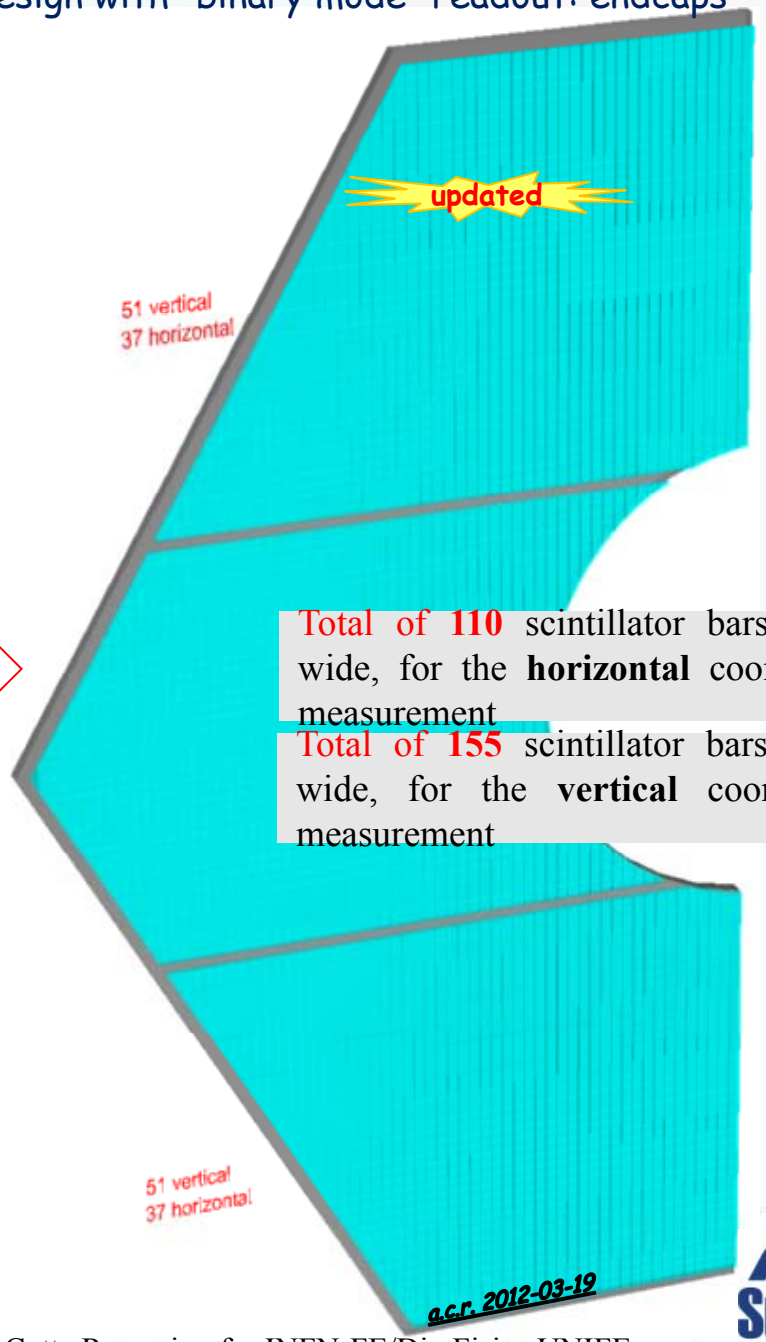
features of the current baseline IFR detector design with "binary mode" readout: endcaps



Locations at which the cables from the modules can exit the iron and connect to the "IFR_ABCD".

crates for the "IFR_ABCD" cards:
2 per door → 8 total

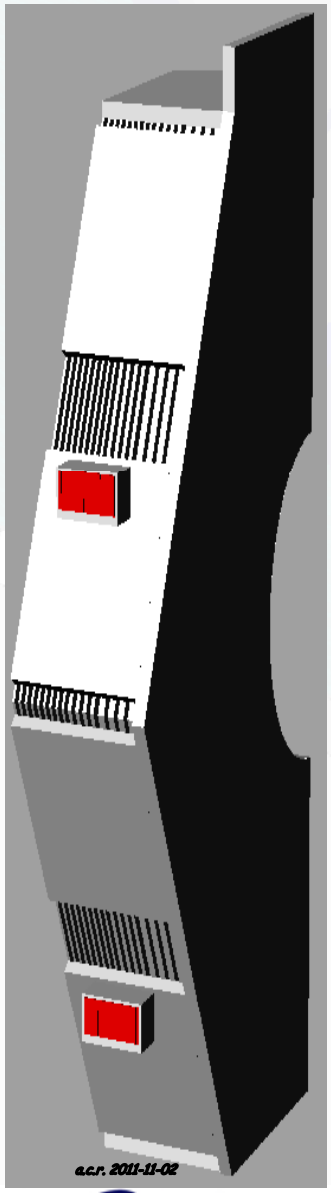


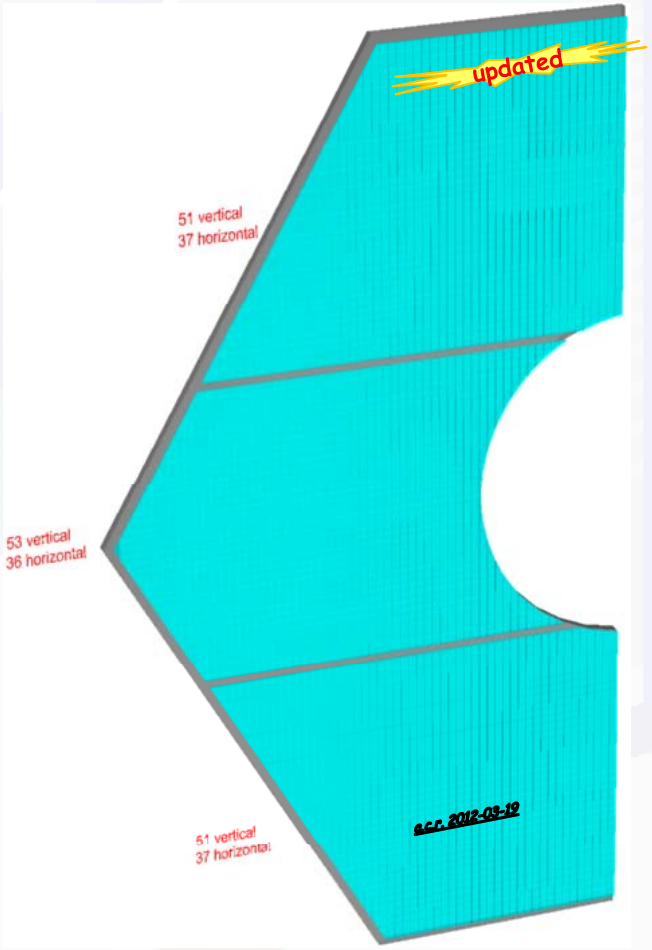


Total of **110** scintillator bars, **5cm** wide, for the **horizontal** coordinate measurement

Total of **155** scintillator bars, **5cm** wide, for the **vertical** coordinate measurement

channel number estimation: endcaps





ENDCAP		
top section	horizontal bars per module:	37
	vertical bars per module:	51
center section	horizontal bars per module:	36
	vertical bars per module:	53
bottom section	horizontal bars per module:	37
	vertical bars per module:	51
AVERAGE channel count per module:		88,4
NO_OF_MOD_PER_LAYER_EC:		3
horizontal bars per layer		110
vertical bars per layer		155
NUMBER OF LAYER PER DOOR		9
NUMBER OF DOORS IN ENDCAPS		4
	+50%	
TOTAL NUMBER OF MODULES IN ENDCAPS:		108
horizontal bars per door:		990
vertical bars per door:		1395
TOTAL HORIZONTAL BARS:		3960
TOTAL VERTICAL BARS:		5580
	+12.3%	
TOTAL CHANNELS IN ENDCAPS:		9540

a.c.r. 2011-11-02

Increment relative to the numbers presented at the nov16/17 ETD meeting at CERN

data rate / data link count estimation: at nominal conditions (trigger rate 150KHz)

BARREL

NUMBER OF CRATES PER SEXTANT	2	NUMBER OF CHANNELS PER CRATE	999
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNEL PER BOARD	83,25
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	2	NUMBER OF 32-CHANNEL PROCESSING UNITS	3
TRIGGER RATE (kHz)	150		
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n:NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (**MOD32**)	10		
EVENT SIZE IN BYTES PER EACH **MOD32** UNIT	40	TOTAL NUMBER OF **MOD32** UNITS	432
	BARREL EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL **MOD32** UNITS)	**17280**	
TOTAL BARREL BANDWIDTH (MB/s)	2592	TOTAL BARREL BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	25,92
TOTAL NUMBER OF DATA LINK	**24**	bandwidth per link (Gbps)	**1,08**

ENDCAP

NUMBER OF CRATES PER DOOR	2	NUMBER OF CHANNELS PER CRATE	1192,5
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNELS PER BOARD	99,375
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	2	NUMBER OF 32-CHANNEL PROCESSING UNITS (**MOD32**) PER BOARD	4
TRIGGER RATE (kHz)	150		
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n:NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (**MOD32**)	10		
EVENT SIZE IN BYTES PER EACH **MOD32** UNIT	40	TOTAL NUMBER OF **MOD32** UNITS	384
	ENDCAP EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL **MOD32** UNITS)	**15360**	
TOTAL ENDCAP BANDWIDTH (MB/s)	2304	TOTAL ENDCAP BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	23,04
TOTAL NUMBER OF DATA LINK	16	**bandwidth per link (Gbps)**	**1,44**

updated

a.c.r. 2011-11-02

+33% due to modularity of data procesing units

data rate / data link count estimation: at higher luminosity (trigger rate 500KHz)

BARREL

NUMBER OF CRATES PER SEXTANT	2	NUMBER OF CHANNELS PER CRATE	999
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNEL PER BOARD	83,25
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	4	NUMBER OF 32-CHANNEL PROCESSING UNITS	3
TRIGGER RATE (kHz)	500		
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n:NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (**MOD32**)	10		
EVENT SIZE IN BYTES PER EACH **MOD32** UNIT	40	TOTAL NUMBER OF **MOD32** UNITS	432
		BARREL EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL **MOD32** UNITS)	**17280**
TOTAL BARREL BANDWIDTH (MB/s)	8640	TOTAL BARREL BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	86,4
TOTAL NUMBER OF DATA LINK	**48**	bandwidth per link (Gbps)	**1,8**

ENDCAP

NUMBER OF CRATES PER DOOR	2	NUMBER OF CHANNELS PER CRATE	1192,5
NUMBER OF BOARDS PER CRATE	12	NUMBER OF CHANNELS PER BOARD	99,375
NUMBER OF DATA LINKS PER CRATE (equal to number of data concentrator/derandomizer buffers)	4	NUMBER OF 32-CHANNEL PROCESSING UNITS (**MOD32**) PER BOARD	4
TRIGGER RATE (kHz)	500		
SAMPLING FREQUENCY (MHz)	50		
SAMPLING CLOCK PERIOD (ns)	20		
W: READOUT WINDOW (ns)	150		
n:NUMBER OF SAMPLES PER TRIGGER	8		
NUMBER OF HEADER/TRAILER WORDS	2		
No. OF 32 BIT WORDS PER TRIGGER PER 32-CHANNEL PROCESSING UNITS (**MOD32**)	10		
EVENT SIZE IN BYTES PER EACH **MOD32** UNIT	40	TOTAL NUMBER OF **MOD32** UNITS	384
		ENDCAP EVENT SIZE in KB (TOTAL NUMBER OF BYTES PER EVENT FOR ALL **MOD32** UNITS)	15360
TOTAL ENDCAP BANDWIDTH (MB/s)	7680	TOTAL ENDCAP BANDWIDTH (Gbps) assuming 8b/10b encoding overhead	76,8
TOTAL NUMBER OF DATA LINK	32	**bandwidth per link (Gbps)**	**2,4**

updated

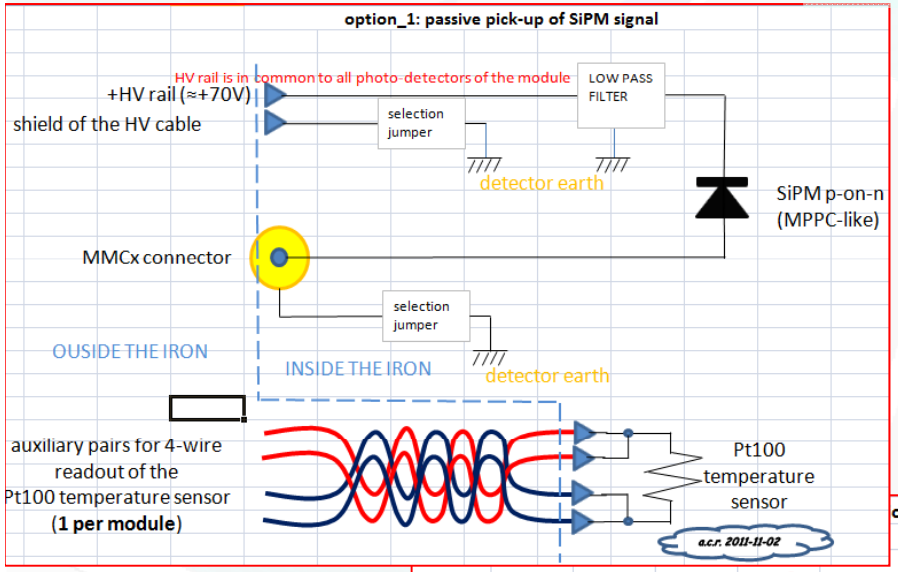
a.c.r. 2011-11-02

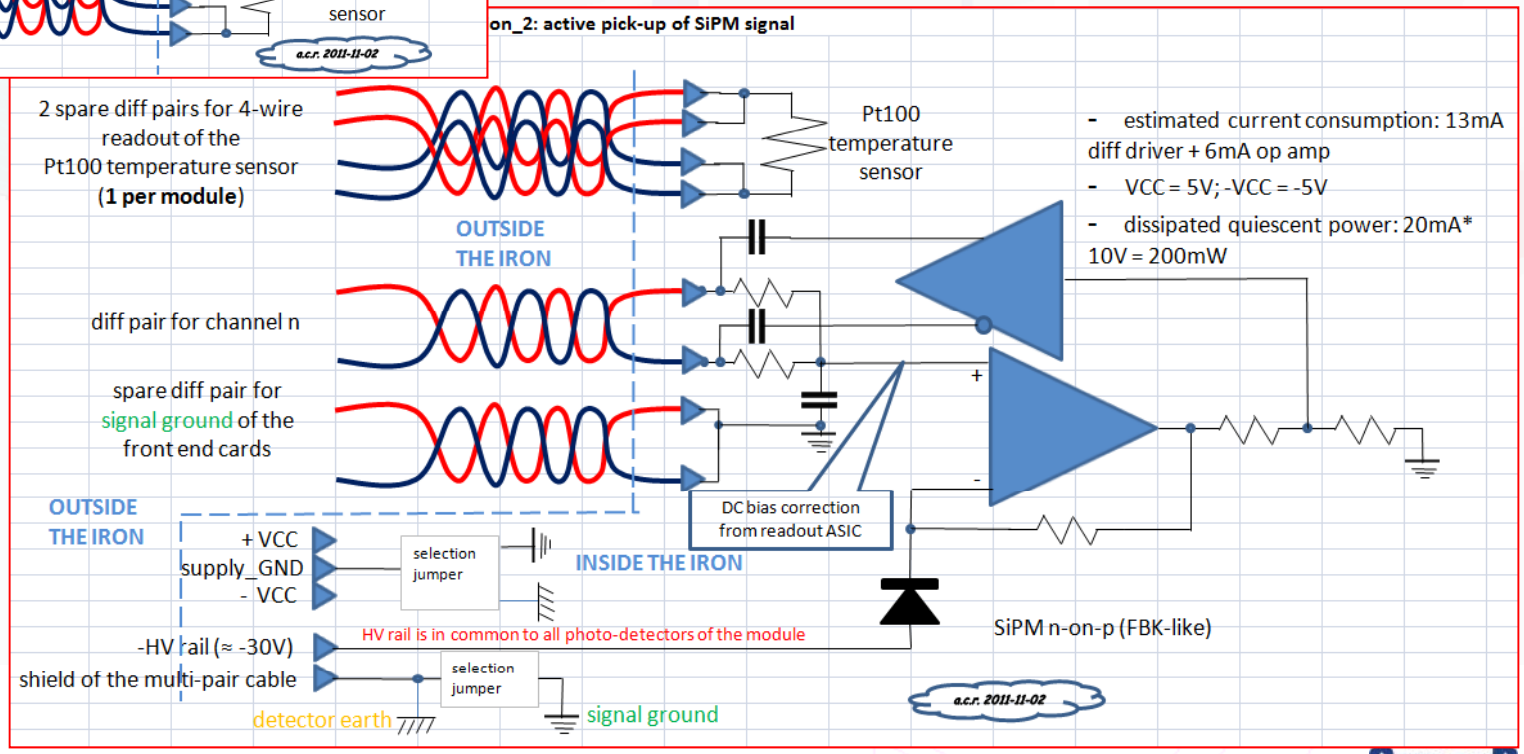
+33% due to modularity of data procesing units

features of the current baseline for the IFR detector design with "binary mode" readout :

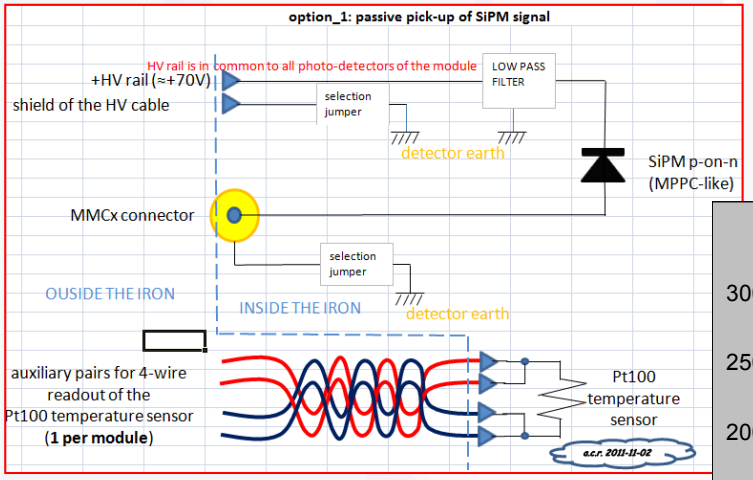
Presented at the nov16/17 ETD meeting at CERN

Single Ended vs active Differential options for "picking-up" the signals from SiPM

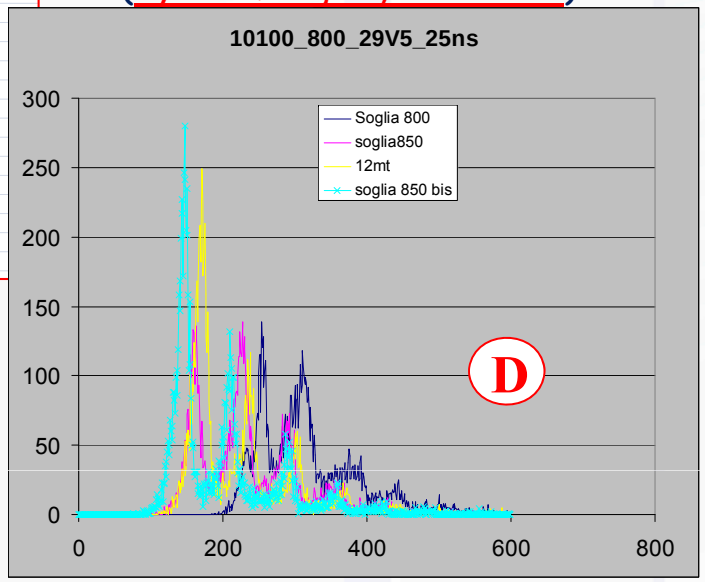




features of the current baseline for the IFR detector design with "binary mode" readout :



Test of Single Ended option for "picking-up" the signals from SiPM (by R. Malaguti, INFN-FE)



USER GUIDE

EASIROC

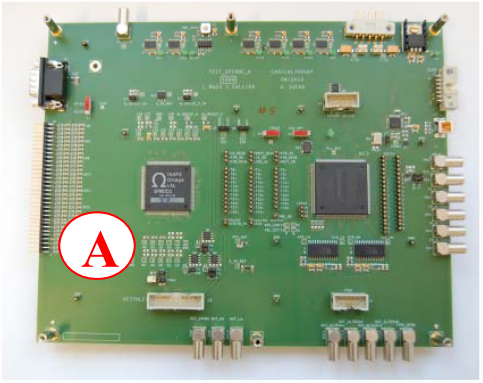
SOFTWARE & TEST BOARD USER GUIDE

Version: 11 April 2011

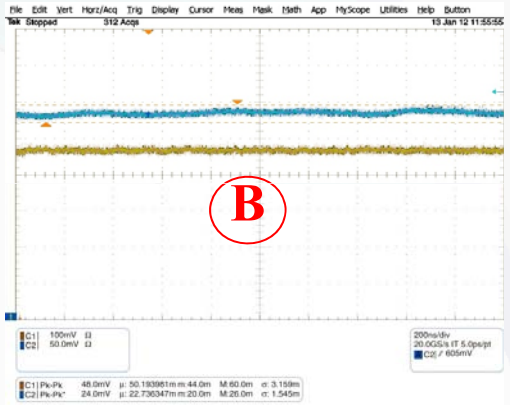
Abstract

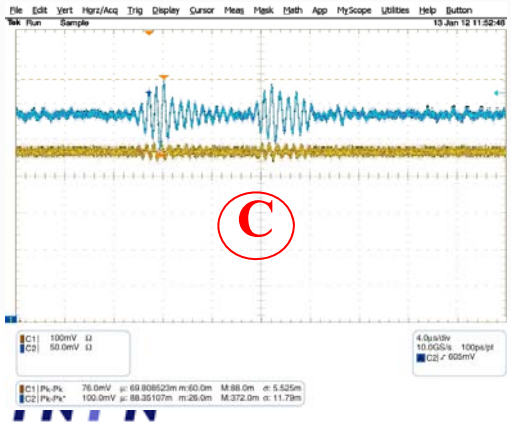
EASIROC (previously SPIROC0), standing for *Extended Analogue Silicon pm Integrated Read Out Chip*, is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors.

This guide explains how to install & use the test board for EASIROC and how to operate with the associated software.



Orsay MicroElectronics Group Associated





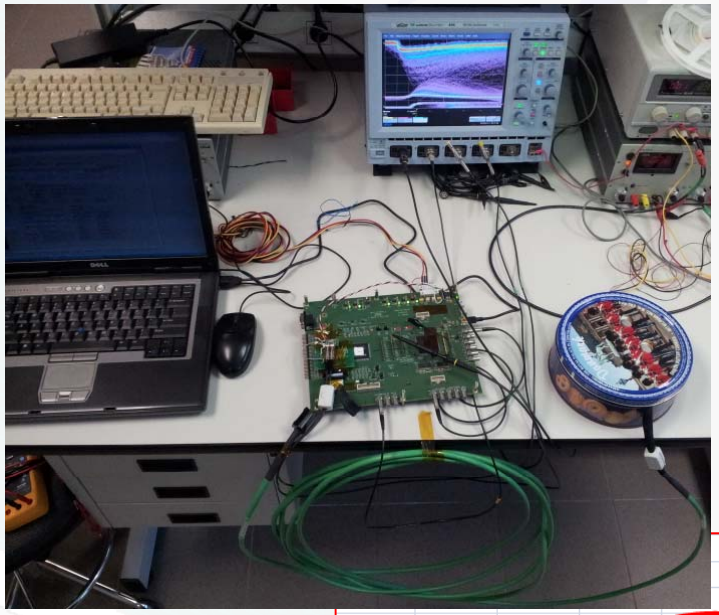
The test was carried out by connecting a **SensL 10100_800** SiPM (biased at 29,5V) to the EASIROC (A) development board and looking at the amplitude histogram of the dark current pulses. The yellow histogram refers to the case in which the SiPM was connected via a 12m long coaxial cable. THERE IS LITTLE DIFFERENCE WITH THE HISTOGRAM OBTAINED WITH A 0.25m LONG CABLE

The waveforms (B) shows the outputs of the LOW_GAIN stage (BLUE trace) and of the fast shaper (LIGHT BROWN trace) with the SensL connected with a 0,25m long cable and UNBIASED.

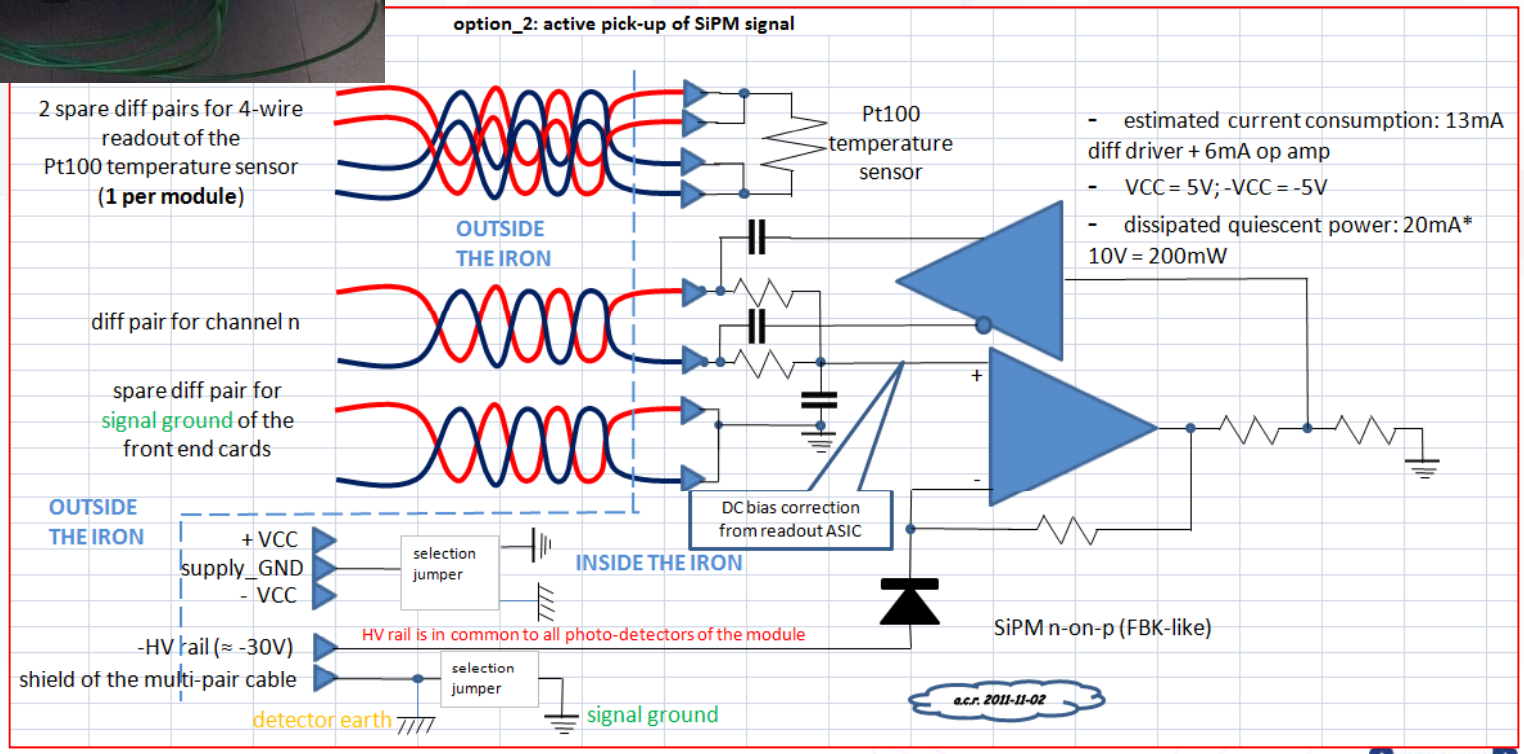
The waveforms (C) shows the outputs of the LOW_GAIN stage (BLUE trace) and of the fast shaper (LIGHT BROWN trace) with the SensL connected with the 12m long cable and UNBIASED. While there is certainly EMI noise pick up this didn't seem to affect the overall outcome of the test.

CAVEAT: only one channel was connected -> pick-up noise might increase with the number of channels connected

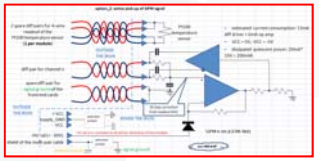
features of the current baseline for the IFR detector design with "binary mode" readout :



Test of active differential option for "picking-up" the signals from SiPM
(by A.C.R., INFN-FE)

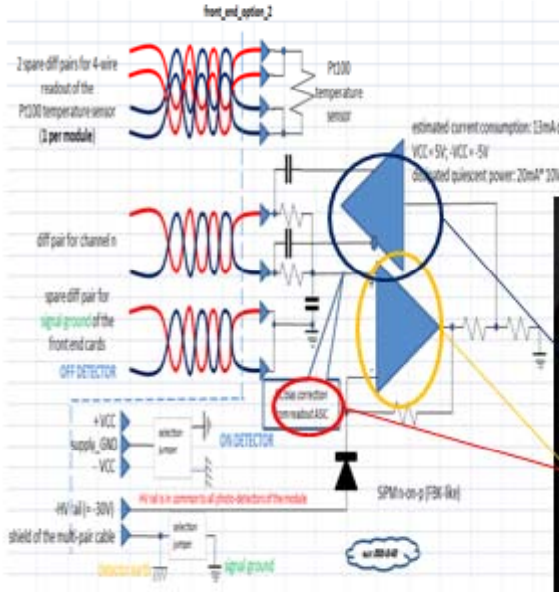


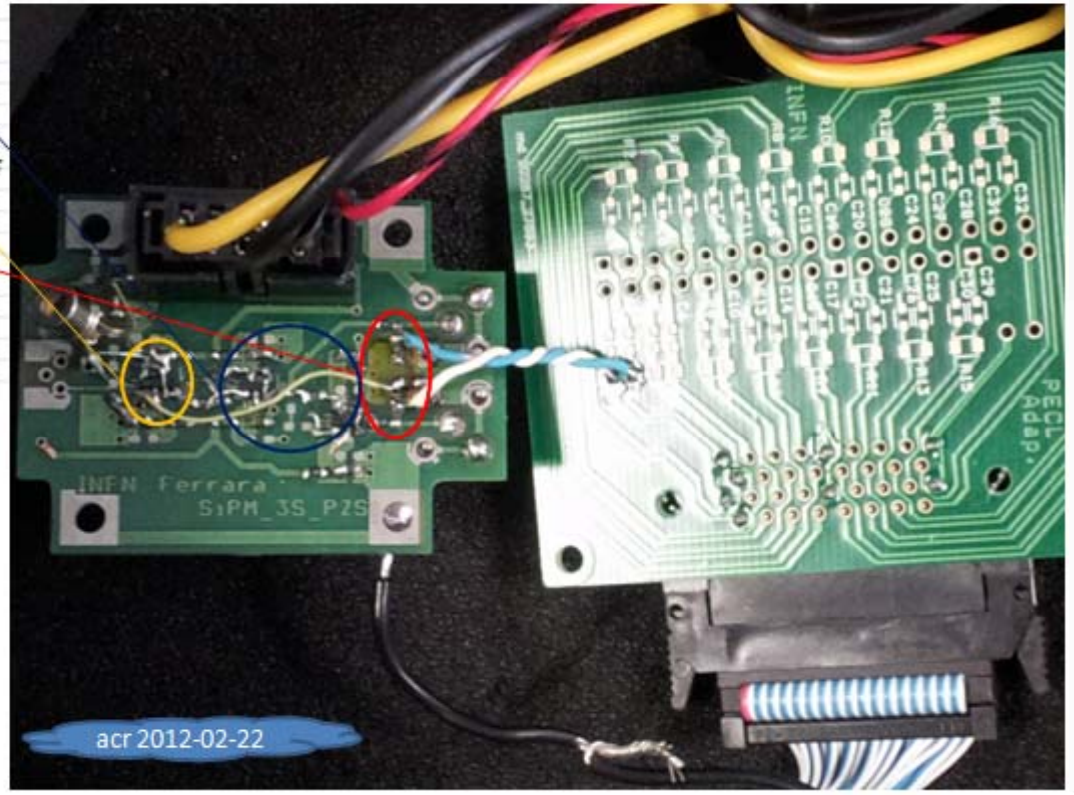
features of the current baseline for the IFR detector design with "binary mode" readout :



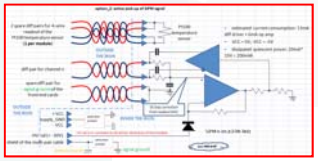
Test of active differential option for "picking-up" the signals from SiPM (by A.C.R., INFN-FE)

buffer/adattatore di polarita' per SiPM: trasmettitore differenziale con recupero del livello in DC di modo comune



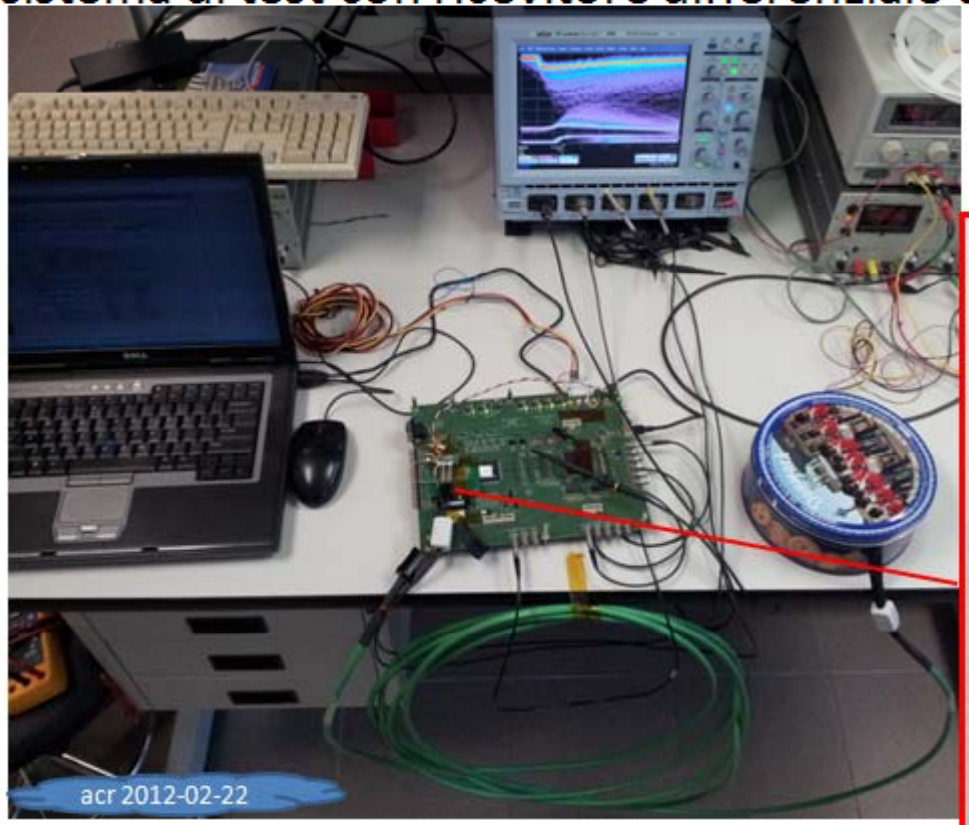


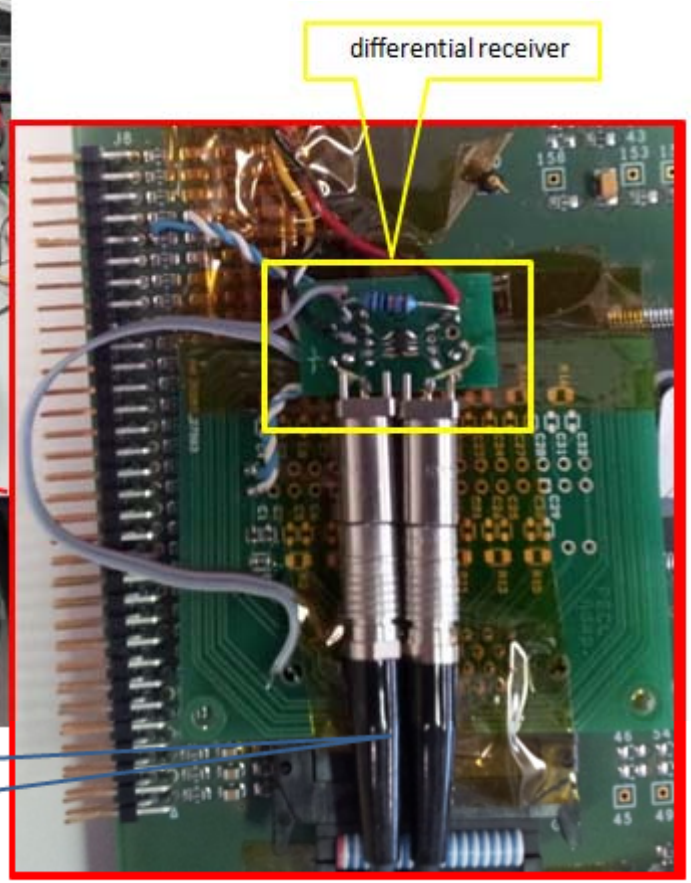
features of the current baseline for the IFR detector design with "binary mode" readout :



Test of active differential option for "picking-up" the signals from SiPM (by A.C.R., INFN-FE)

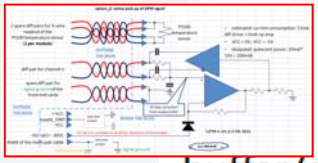
buffer/adattatore di polarita' per SiPM:
sistema di test con ricevitore differenziale applicato alla scheda EASIROC





Coaxial LEMO cables connected to scope (AC coupling, ext 50 Ohm termination) for monitoring the differential signals at the input of the receiver

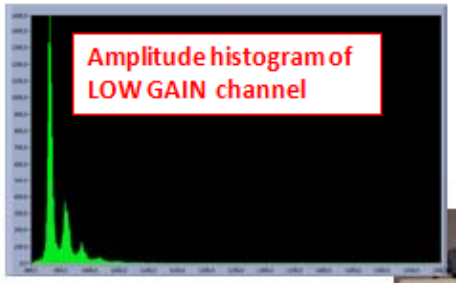
features of the current baseline for the IFR detector design with "binary mode" readout :

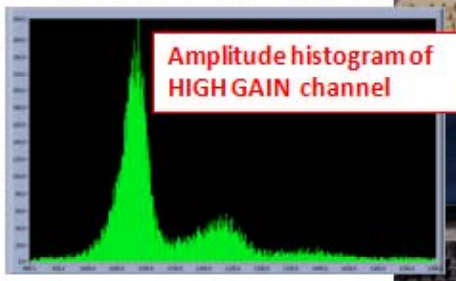


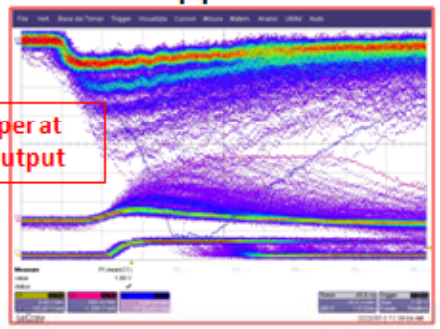
Test of active differential option for "picking-up" the signals from SiPM (by A.C.R., INFN-FE)

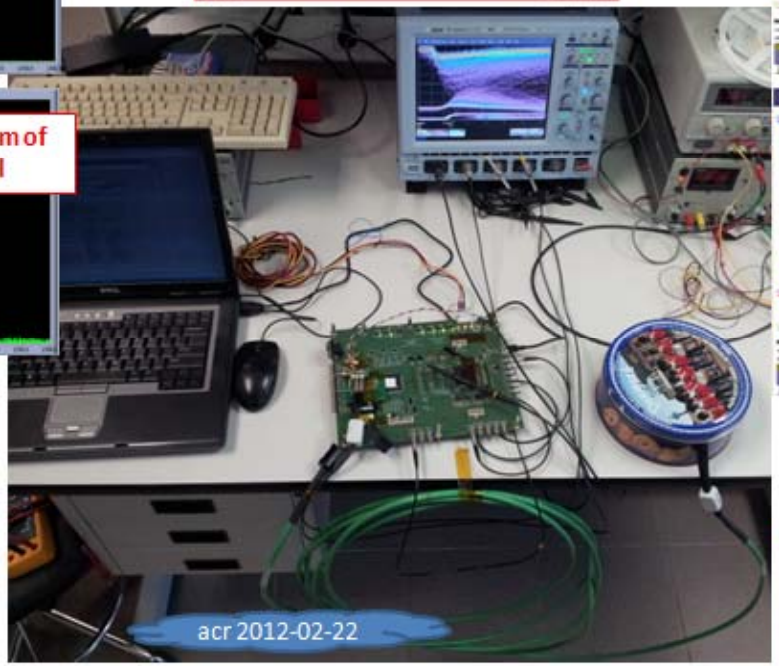
buffer/adattatore di polarita' per SiPM: applicazione alla scheda EASIROC: test results

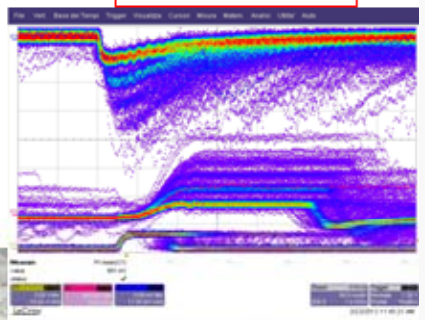
histoprogramming program
by R. Malaguti, May 2011

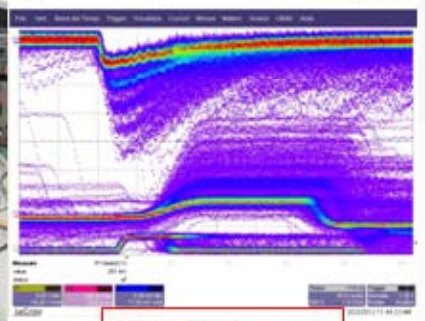






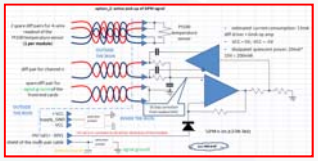






Test results for a reference system **with 8m of shielded twisted pair cable** between driver and receiver

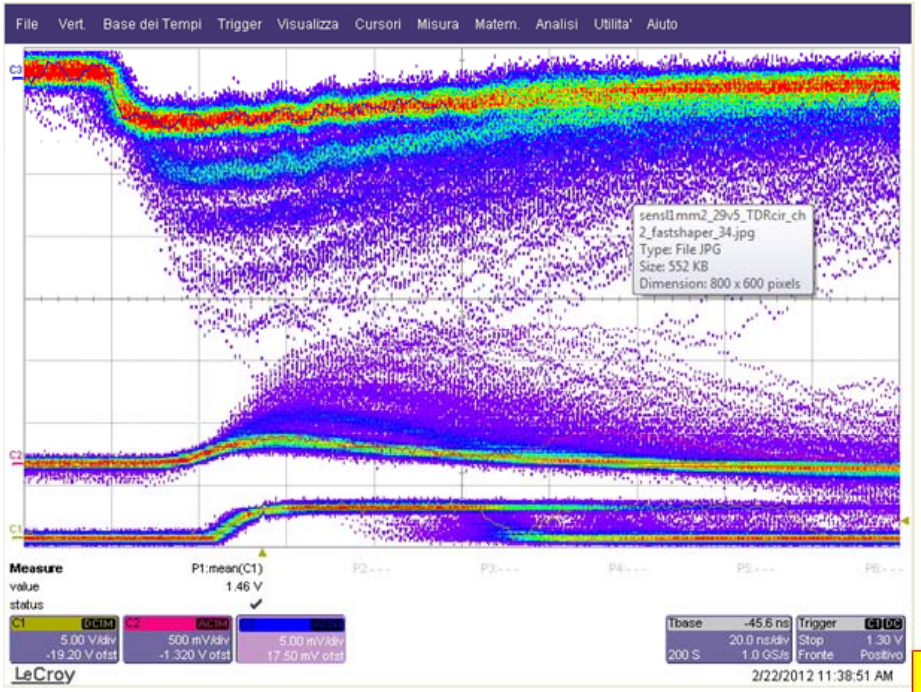
features of the current baseline for the IFR detector design with "binary mode" readout :



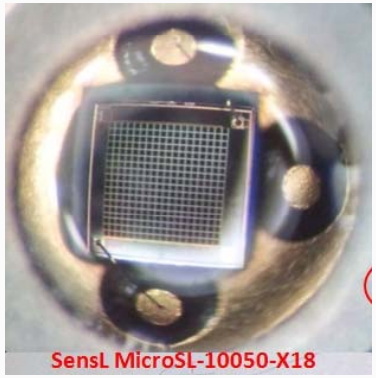
Test of active differential option for "picking-up" the signals from SiPM (by A.C.R., INFN-FE)

buffer/adattatore di polarita' per SiPM: applicazione alla scheda EASIROC: test results

qualche forma d'onda



Test results for a reference system **with 8m of shielded twisted pair cable** between driver and receiver



SensL MicroSL-10050-X18

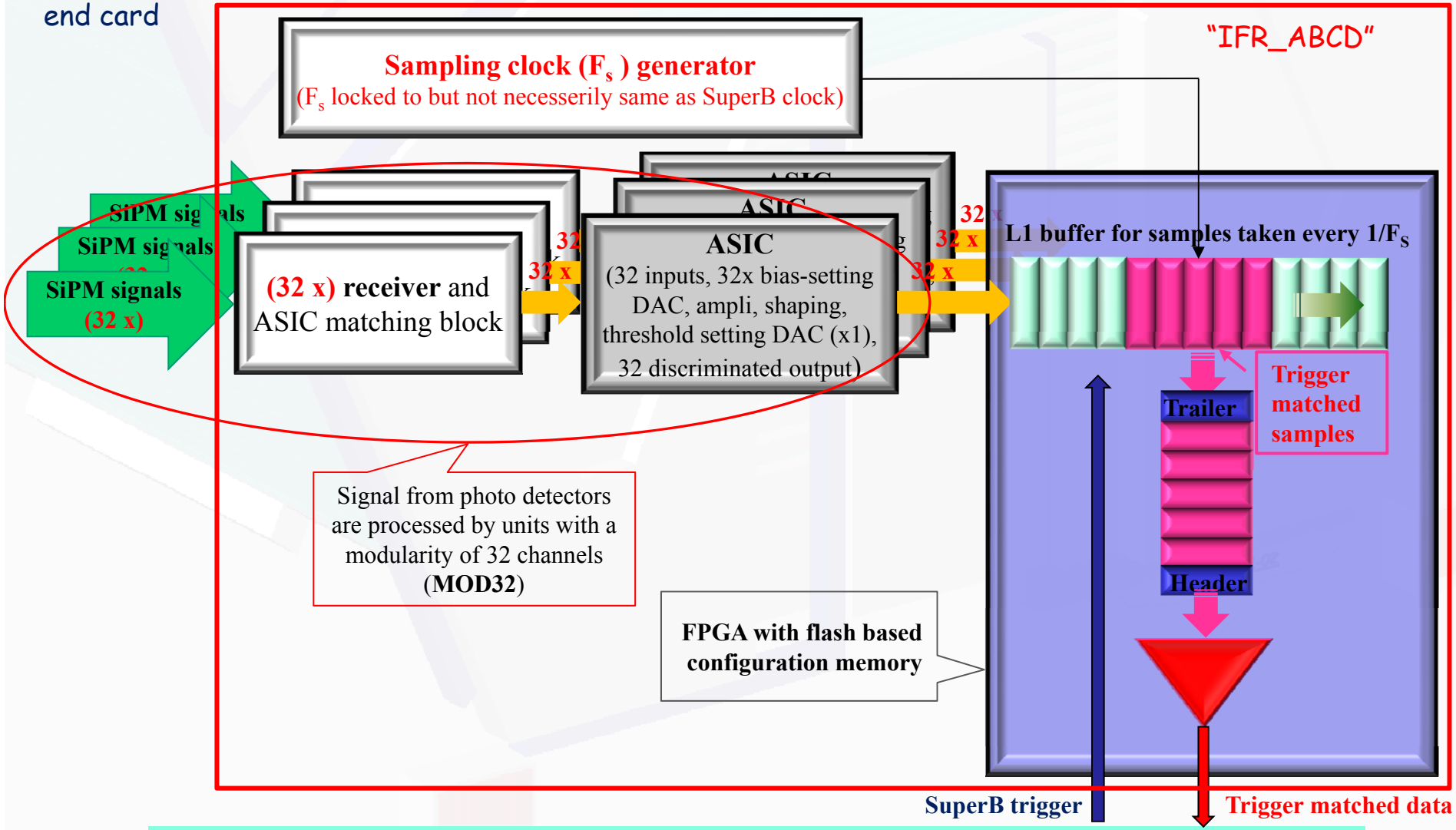
The test was carried out by connecting a **SensL MicroSL-10050-X18** through the proposed active buffer to the EASIROC development board and looking at the amplitude histogram of the dark current pulses.

Also in this configuration the result is that THERE IS LITTLE DIFFERENCE WITH THE HISTOGRAMS OBTAINED by connecting the SiPM to the EASIROC WITH A 0.25m LONG COAXIAL CABLE

features of the current baseline IFR detector design with "binary mode" readout:

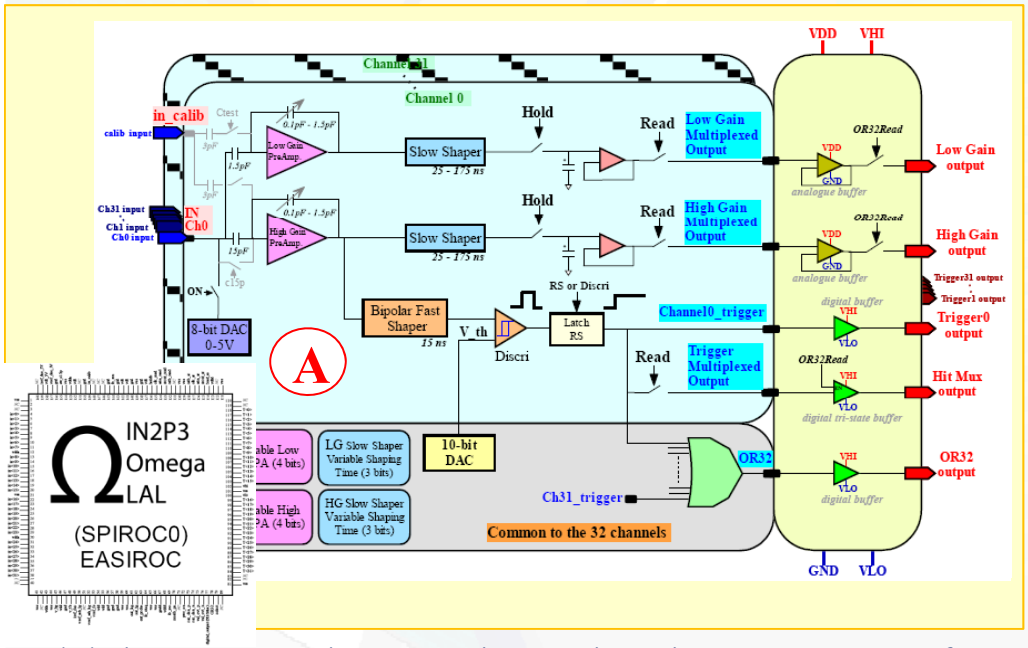
block diagram of the "IFR_ABCD" front end card

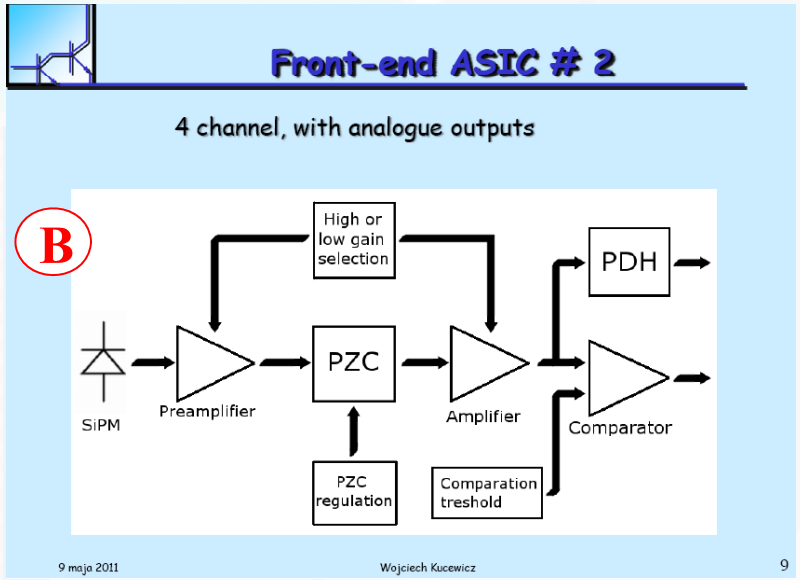
Presented at the nov16/17 ETD meeting at CERN

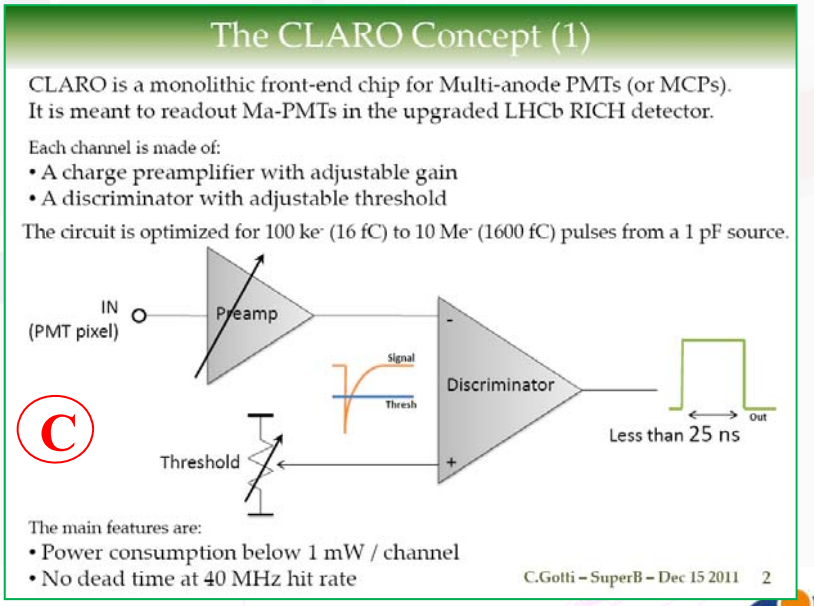


Two "CONCENTRATOR / DATA LINK DRIVER" cards in the "IFR-ABCD" front end crates are connected to the FCTS and to the ROM: they distribute the trigger to the "IFR_ABCD" cards, collect the matched data, merge the streams into the de-randomizer FIFO and drive the data link (1 or 2 per concentrator) toward the ROMs

features of the current baseline IFR detector design with "binary mode" readout: Candidate ASICs at present date







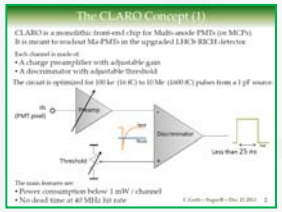
(A)The EASIROC has been designed by the Omega group of LAL and it has been extensively used and tested in Ferrara thanks to evaluation board provided by LAL. It has already described in previous presentations

(B)The RAPSODI ASIC#2 has been designed by **Woitek Kucewicz** of AGH University in Cracov Poland. It has already been introduced in previous presentations

(C)The CLARO ASIC has been designed by **Gianluigi Pessina and Claudio Gotti** and presented at the 2nd SuperB meeting last December.

features of the current baseline IFR detector design with "binary mode" readout:

Candidate ASICs at present date

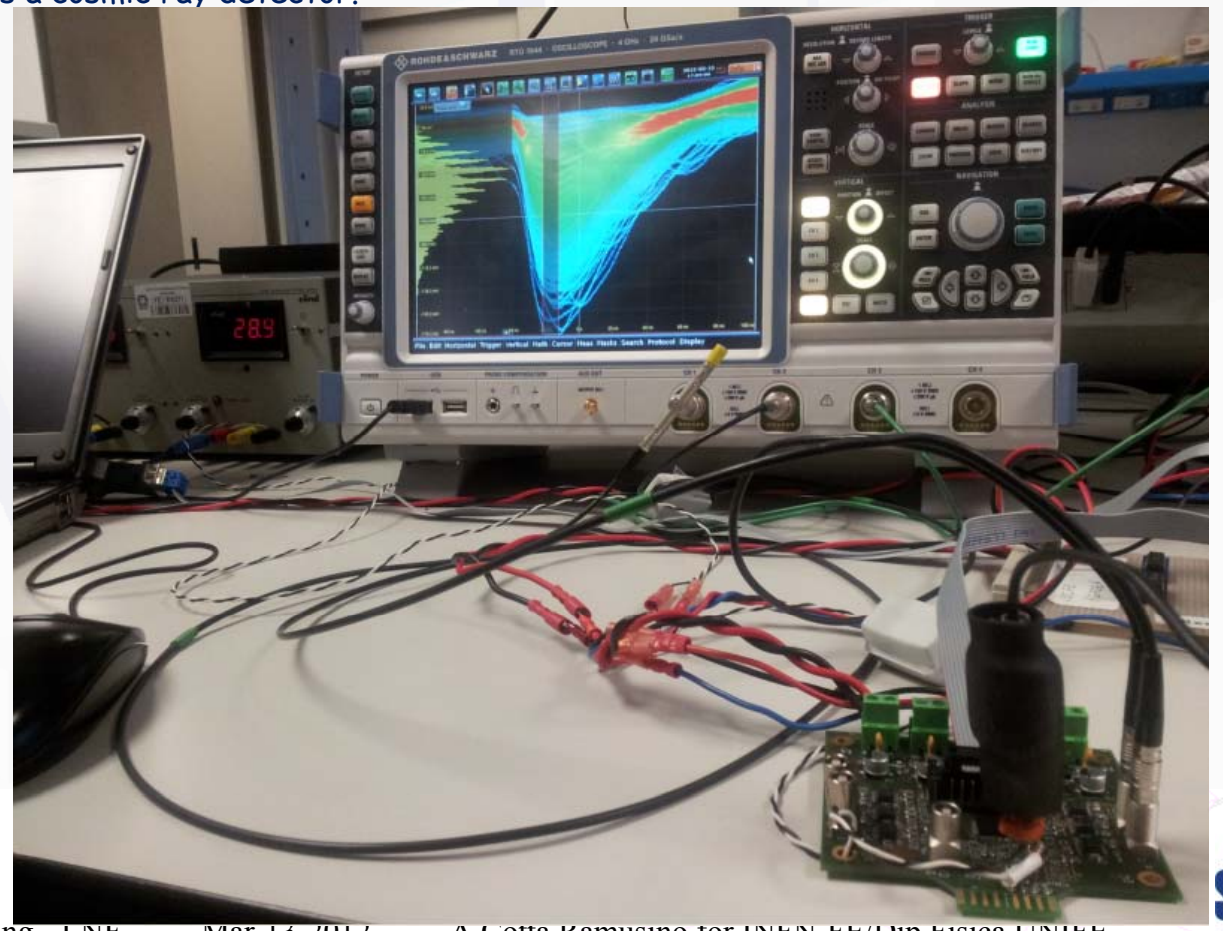


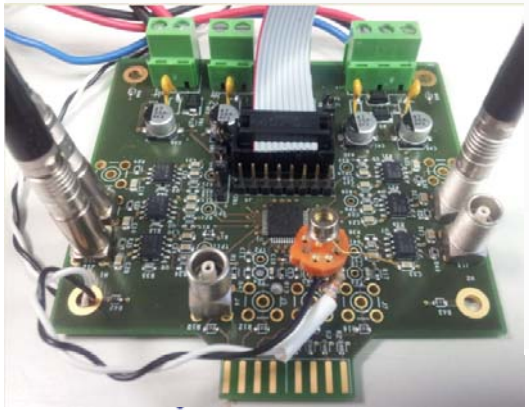
The **CLARO ASIC** has been recently tested in Ferrara on a PCB laid out by R. Malaguti of INFN-Ferrara.

The CLARO was connected to a **SensL MicroSL-10050-X18 1mm²**, directly or through a 1m long coaxial cable. A **SensL MicroSL-30035 9mm²**, was also tested to see the effect of higher input capacitance on the ASIC peaking time and noise performances.

In order to better evaluate the noise performances of the ASIC, a digital scope with a very low noise floor was used (Rohde &Schwarz RTO 1044). The SiPM connected to the ASIC has been first stimulated by photons from a blue LED and then coupled to a scintillator/WLS fiber assembly and operated as a cosmic ray detector.

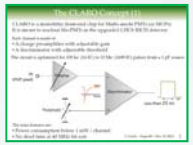
The details of the tests performed on the **CLARO ASIC** are being presented at this meeting by Claudio Gotti.

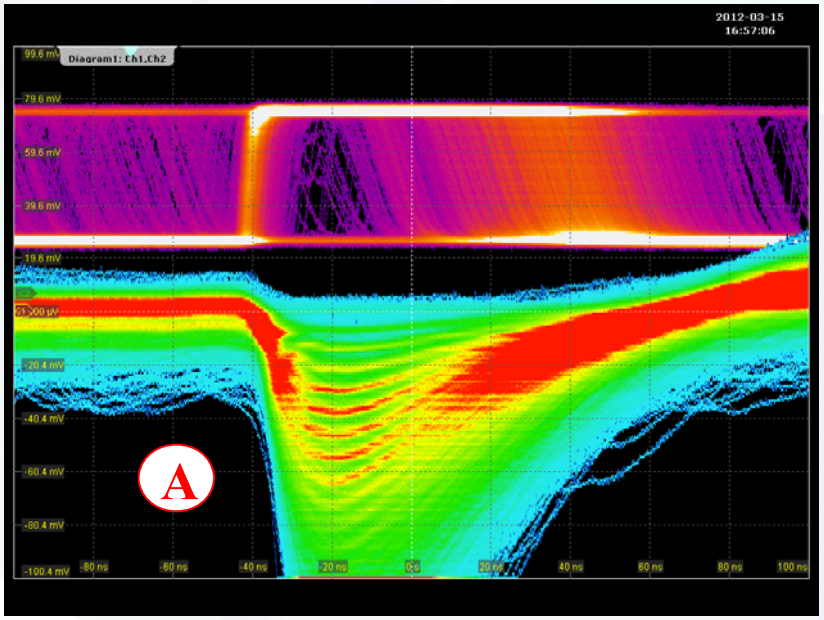


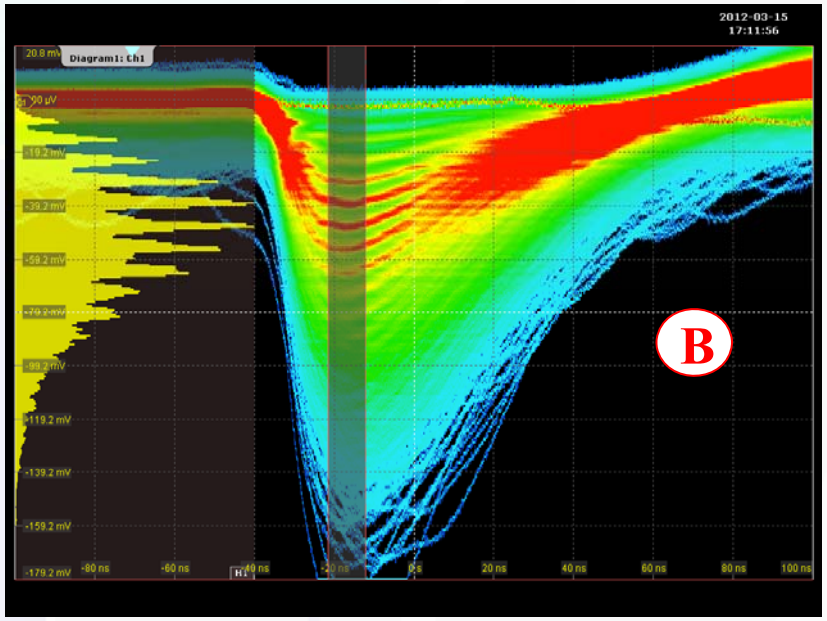


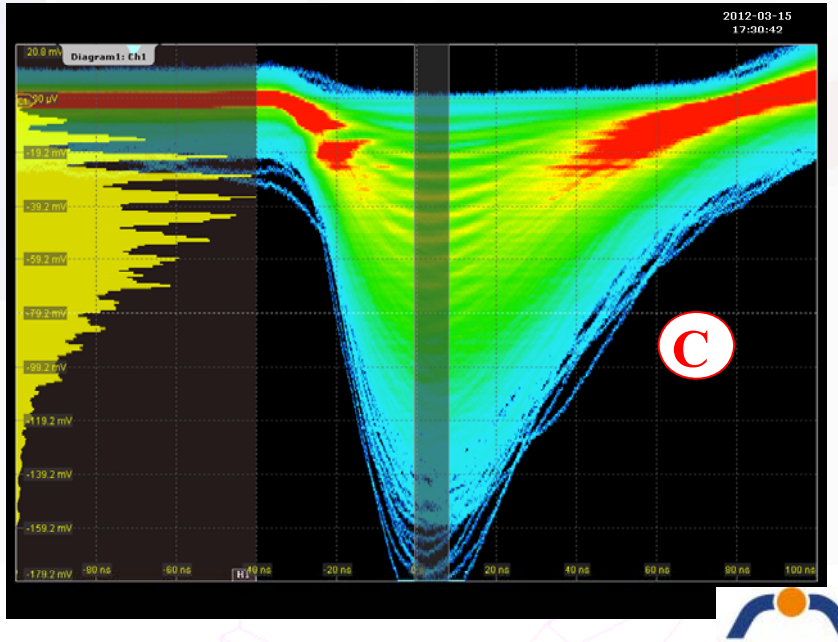
features of the current baseline IFR detector design with "binary mode" readout:

Candidate ASICs at present date









The details of the tests performed on the **CLARO ASIC** are being presented at this meeting by Claudio Gotti.

(A)The CLARO digital and analog outputs

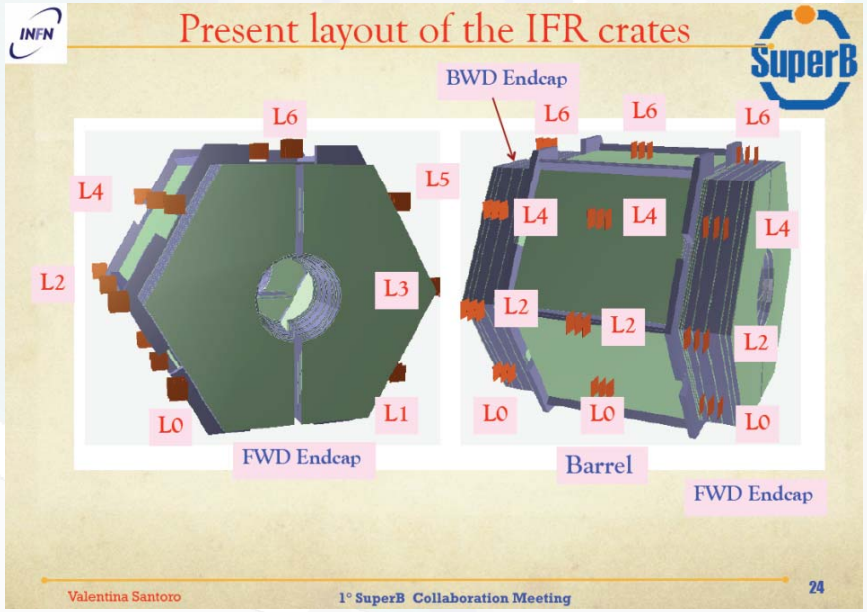
(B)The CLARO ASIC is connected to the SiPM directly

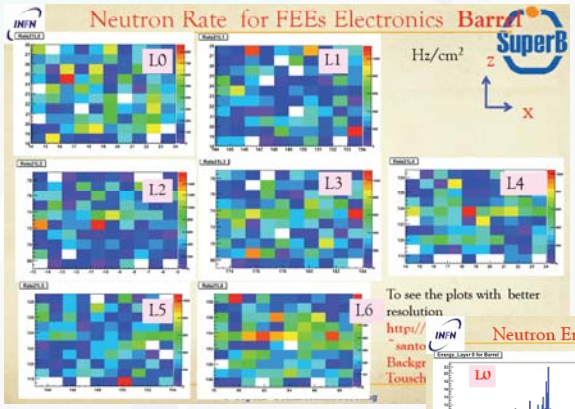
(C)The CLARO ASIC is connected to the SiPM via a 1m long coax cable; the peak is late wrt previous case

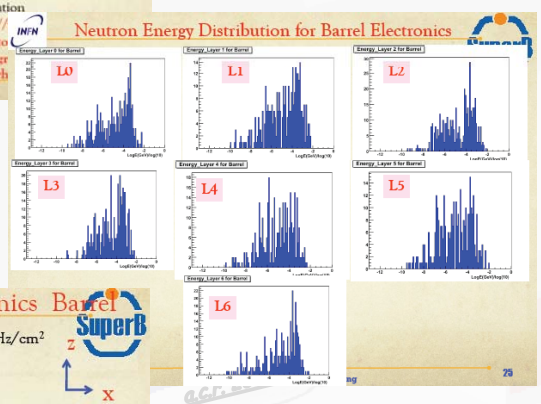
addressing the radiation issues: background rates estimation at the location of IFR front end electronics

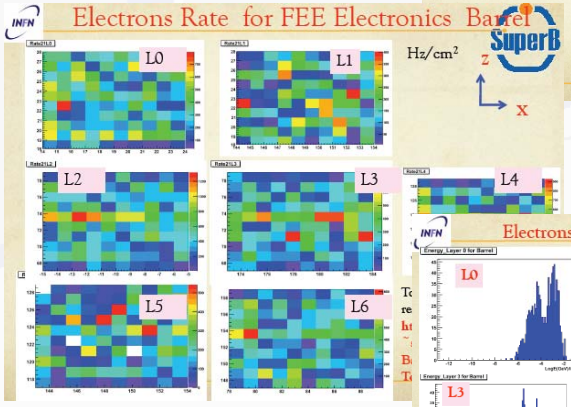
Presented at the nov16/17 ETD meeting at CERN

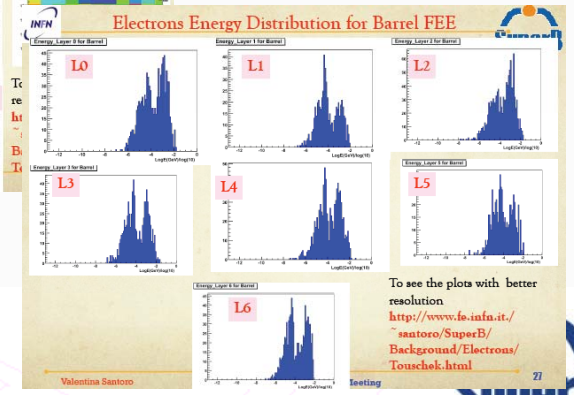
From: "IFR Background Status" Valentina Santoro INFN Ferrara









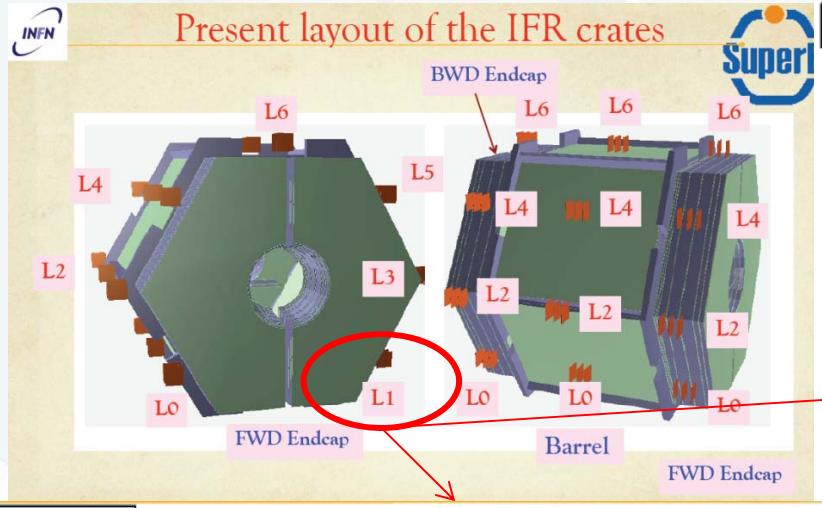


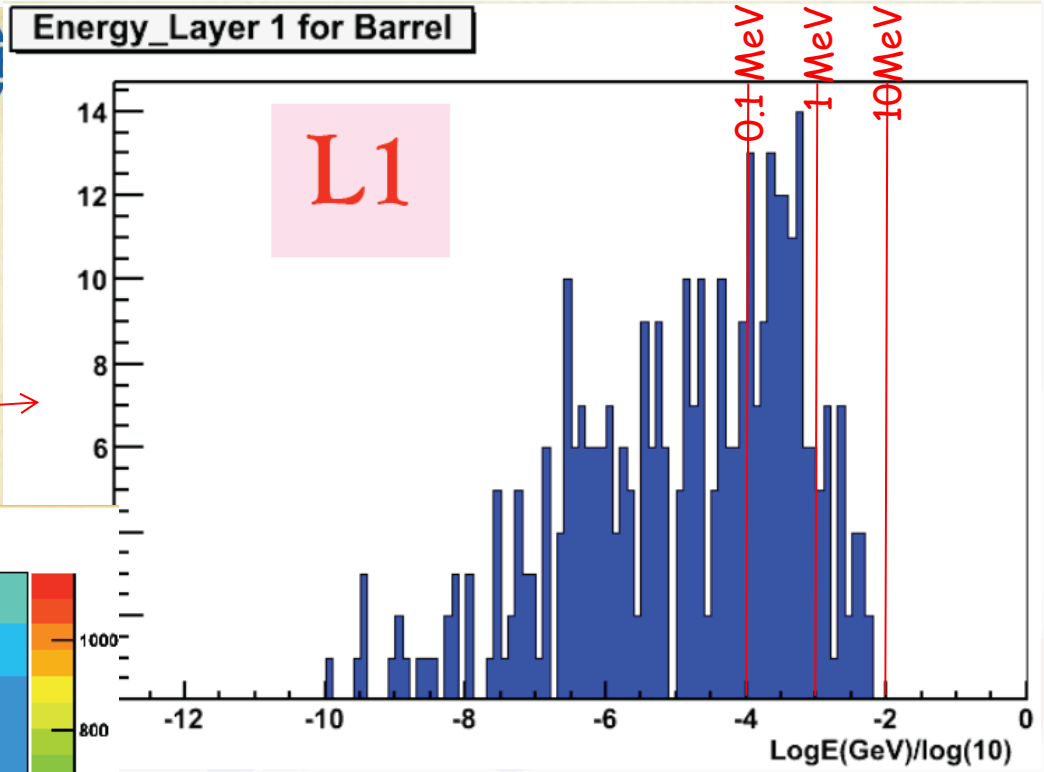
Thanks to this work we have now an estimate of the expected radiation doses at the locations of the front end electronics crates, according to the baseline design.

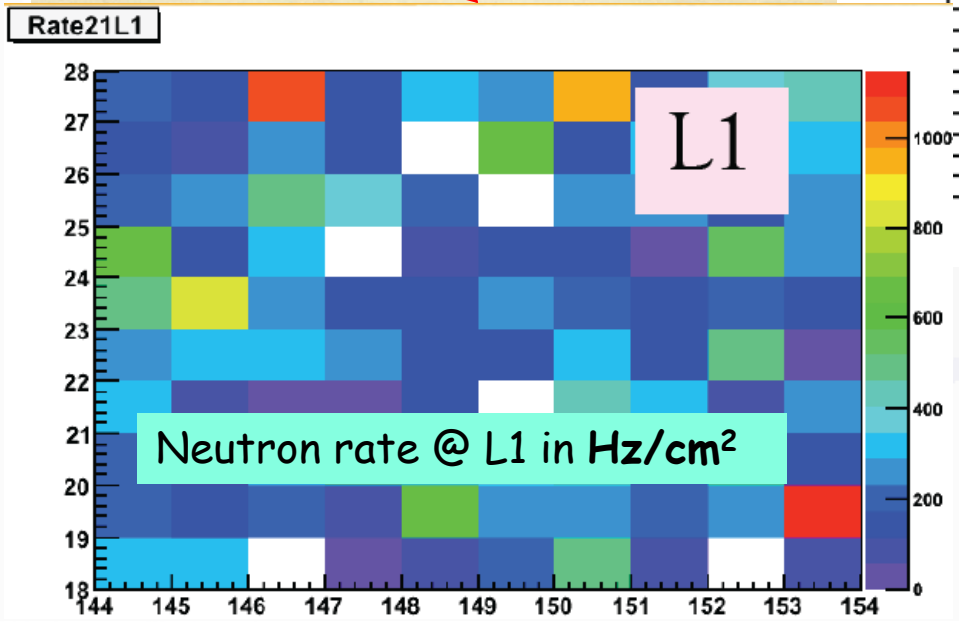
This will allow us to properly plan the irradiation tests of the "compact" front end design based on the EASIROC.

addressing the radiation issues: background rates estimation at the location of IFR front end electronics

From: "IFR Background Status" Valentina Santoro INFN Ferrara







Details of the **neutron energy spectrum** and **neutron rate** expected at location L1

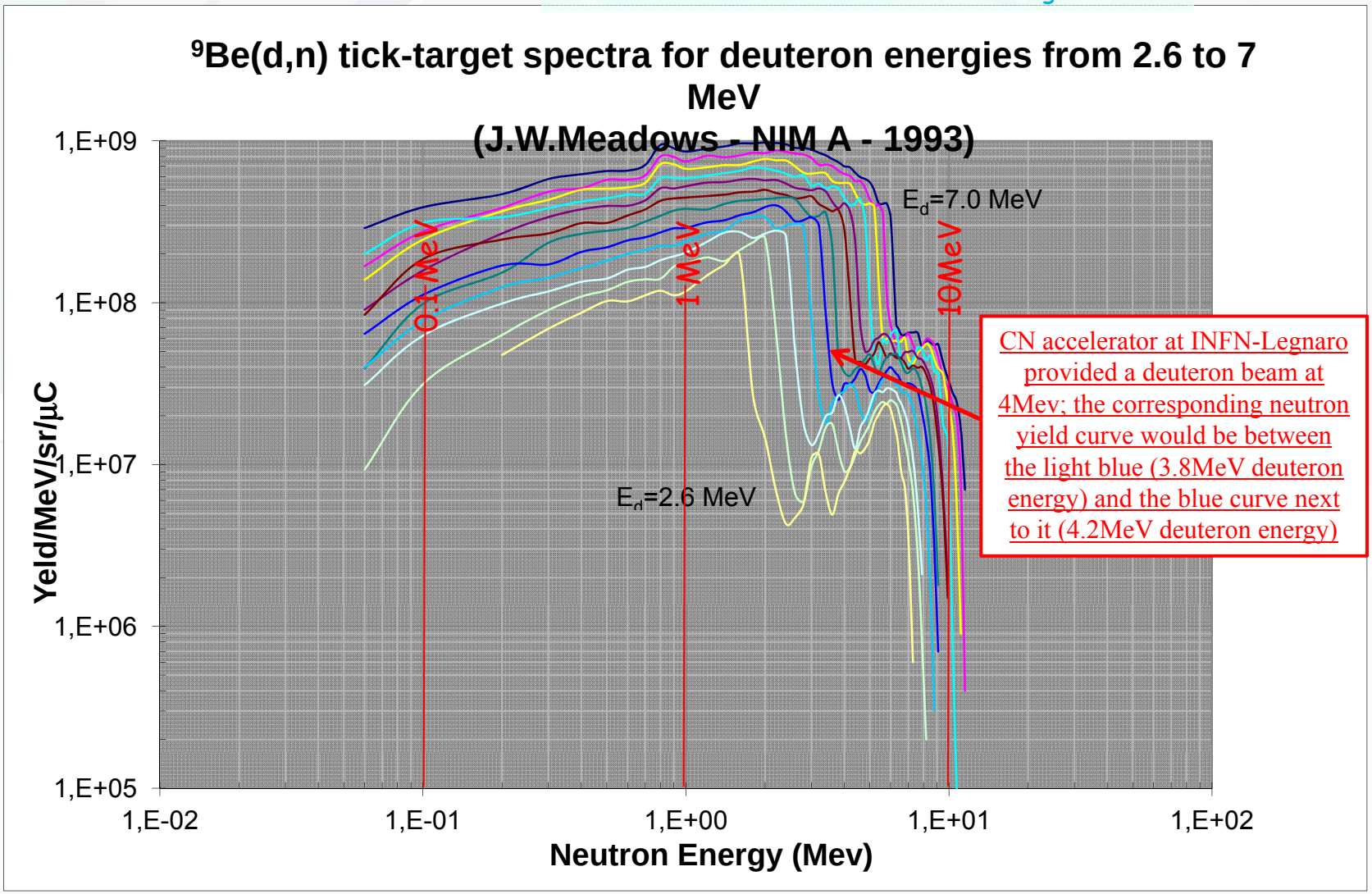
The neutron environment can be partially reproduced exploting the neutron source facility at the CN accelerator of the Legnaro lab of INFN

Assuming 1kHz/cm² ➔ neutron fluence in a year (10^7s) = 10^{10}/cm²

addressing the radiation issues:

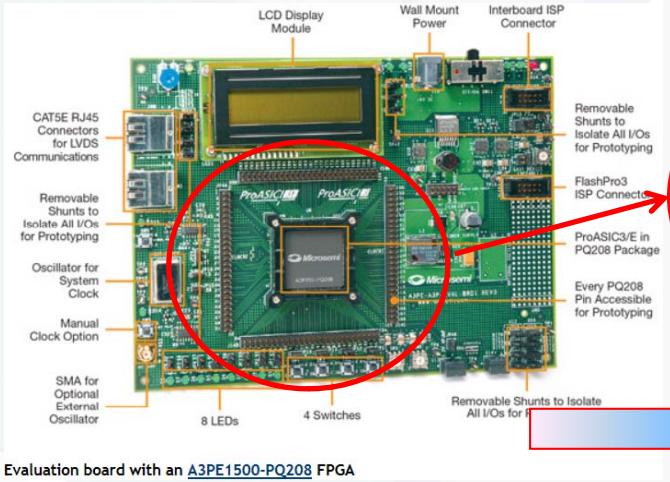
measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro

Presented at the nov16/17 ETD meeting at CERN

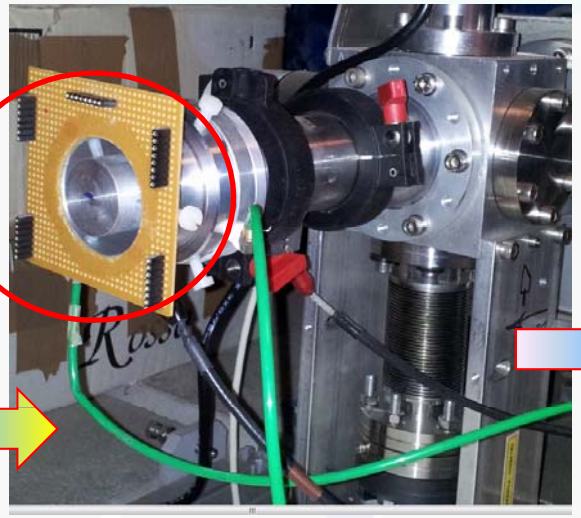


(excel file by Flavio Dal Corso)

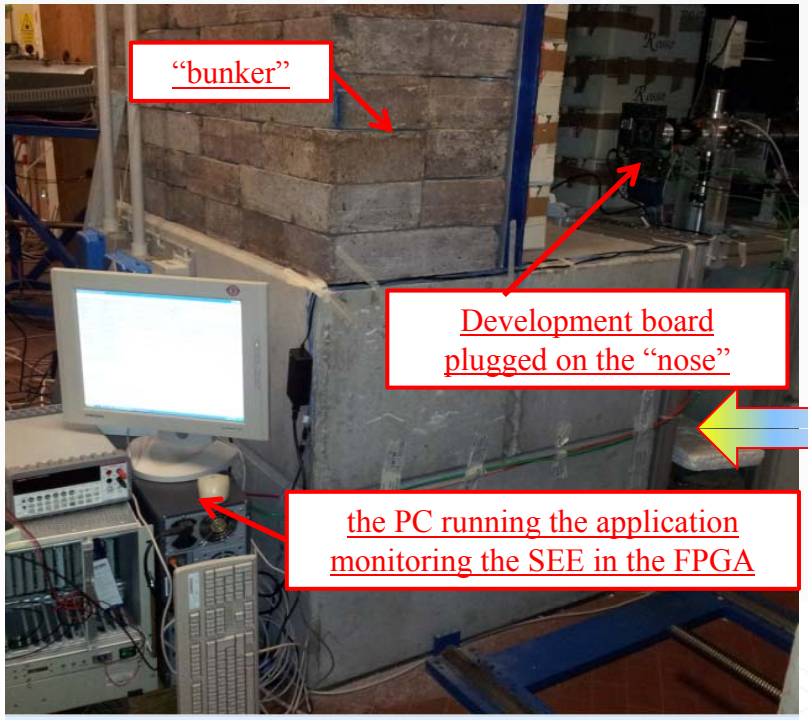
addressing the radiation issues:
measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro



Evaluation board with an A3PE1500-PQ208 FPGA



Presented at the nov16/17 ETD meeting at CERN



Acknowledgements:

We exploited beam time which had been allocated by our colleagues Roberto Stroili and Flavio Dal Corso who also provided the information needed to estimate the neutron flux.

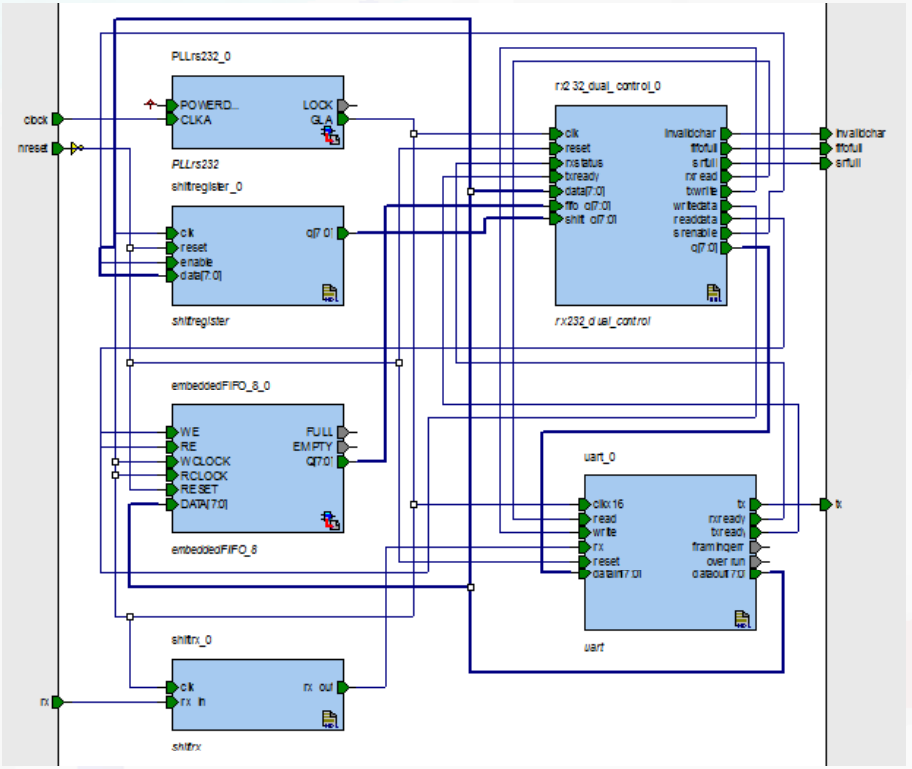
addressing the radiation issues:
measurement of neutron induced SEE in FPGA at the INFN Laboratori Nazionali di Legnaro

Acknowledgements:
The test design developed as his undergraduate thesis work by **Lorenzo De Santis** (University of Ferrara) in the ACTEL device occupied the FPGA for about 98%.

It implemented:
- an embedded FIFO 4096 x 8 based on SRAM cellsm, for a total of **32768 SRAM bits**
- a shift register with 728 cells 8bit wide, for a total of **5824 Flip Flops**
- a UART to load and read back the memory blocks

A PC running a Labview application also provided by Lorenzo was used to repeatedly run the routine of loading known patterns into the structures and reading them back after the test interval.

A typical outcome of the test was that in ½ hour run with 4MeV deuteron energy and 40nA average current we would detect:
- around 36 SRAM bit flip
- between 0 and 2 FLIP FLOP upsets



NO bit flips were detected (nor expected) in the configuration memory (flash-based) of the FPGA: the functionality of the chip was never found impaired

If our estimation of neutron flux at the test facility are correct then for each ½ hour run at 40nA the FPGA has been irradiated with ≈ order of 1*10^10 neutrons (of the same order of the fluence resulting from 1 year of operation in SuperB) →
- **we can use a flash-based FPGA to handle L1 buffering**
- **we should protect the state machines with TRM** but not necessarily the L1 buffer itself: data corruption rate is low

addressing the radiation issues: measurement of neutron induced SEE in FPGA at the INFN-LNL

SOLID ANGLE OMEGA	ACTEL
OMEGA =	1,187020767
alfa (cm)	0,9
beta (cm)	0,9
alfa * beta = (cm^2)	0,81
distance d = (cm)	0,7
denominator (cm^2)	2,64892431

data extracted from the "irraggiamento.xls" spreadsheet by Flavio Dalcorso

integrated irradiation time (sec)	charge (μC)	total errors in the FIFO section of the FPGA design	total errors in the shift register section of the FPGA design
35400	2660	774	20
total Yeld/sr/uC @ Ed=4 Mev	hardness factor @ Ed=4 MeV		
1.02E+09	1.146		

numero totale di neutroni attraverso DUT per tutta la durata del test	3,21E+12
numero di neutroni attraverso 1 cm^2 in per tutta la durata del test = fluenza@DUT	3,97E+12

If the estimation of neutron flux at the CN facility in Legnaro is correct then we have exposed the device to a total flux of ≈ 3,2 * 10^{12} neutrons in about 10 hours, during which we have detected:
-774 errors in the RAM based section of the design
- 20 errors in the shift register instantiated in the FPGA fabric

According to current background simulation results (see Valentina Santoro's http://www.fe.infn.it./~santoro/SuperB/Background/Neutrons/Touschek.html), it would take tens of years of operation for the electronics located around the barrel to collect the 3 * 10^{12} neutrons.

FIFO depth:	4096
Shift Reg. Depth:	728
word width:	8
number of bits:	32768
number of FF:	5824
<numero di bit flip in FIFO> :	774,0000
per Mb:	23620,6055
<numero di bit flip in Shift Reg> :	20,0000
per Million Flip Flop:	3434,0659

vedi: "Overview of iRoC Technologies Report "Radiation Results of the SER Test of Actel FPGA December 2005"

da: "Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances"

nel nostro caso:

cross section per chip: Sigma_C = No_of_errors / (fluence * C) with C= number of chips

reference fluence: fluence at ground level in New York City: fluence_NYC = 14 n/cm^2/hour

FIT: Failure In Time: failures in 10^9 hours. FIT = Sigma_C * fluence_NYC * 10^9

		Sigma_C [cm^2]	ref_fluence/hour	FIT
a3p250-FIFO section	FIFO	1,952E-10	1,400E+01	2,733E+00
a3p250-SHIFT Register section	SHIFT REGISTER	5,044E-12		7,062E-02

definisco:

cross section per FIFO Mb: Sigma_Mb = No_of_errors * 10^6 / (fluence * N_FIFO_bit)

	Sigma_Mb
a3p250: Fifo cross section per Mbit	5,95706E-09

definisco:

cross section per M flipflops: Sigma_Mff = No_of_errors * 10^6 / (fluence * N_flipflops)

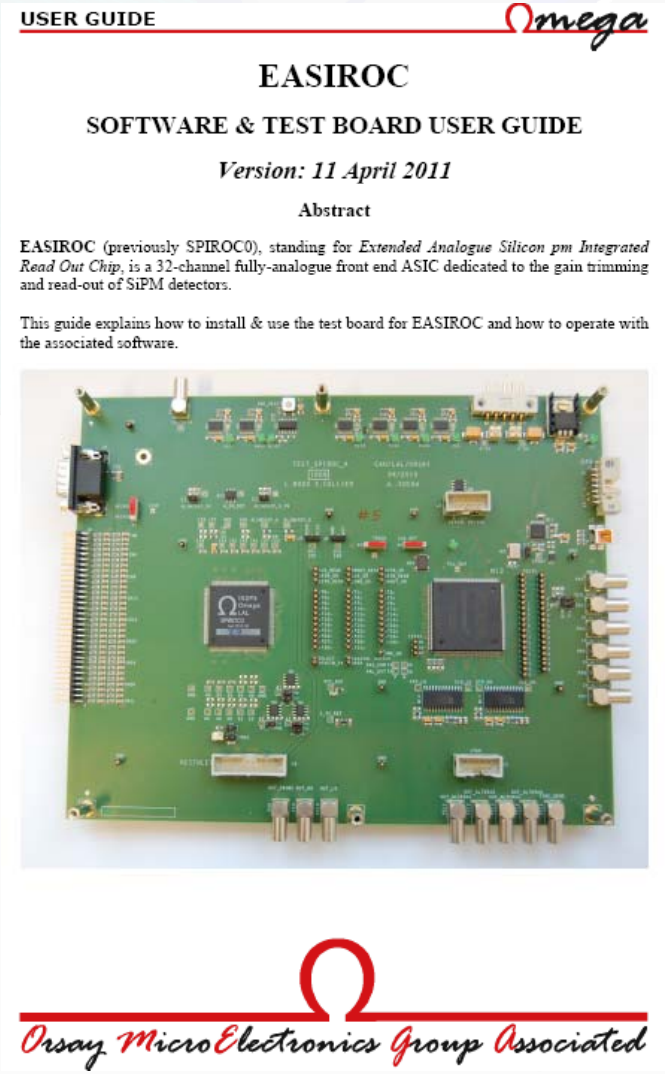
	Sigma_Mff
a3p250: ShiftRegister cross section per Mflipflop	8,66063E-10

FIT (Failure in Time) figure resulting from our test is 20 times smaller than that published by ACTEL for a similar FPGA tested with 14MeV neutrons.

	our test at LNL on a ProASIC3 device a3p250	**IROC test on a ProASIC3 E device a3pE600**
	FIT per million bit of embedded RAM	**FIT per million bit of embedded RAM**
	8,340E+01	**1580**
	FIT per million flip flop	**FIT per million flip flop**
	1,212E+01	**889**
ratios RAMbit errors/FF errors	**6,878E+00**	**1,77727784**

addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro (being planned)

Presented at the nov16/17 ETD meeting at CERN


USER GUIDE

Omega

EASIROC

SOFTWARE & TEST BOARD USER GUIDE

Version: 11 April 2011

Abstract

EASIROC (previously SPIROC0), standing for *Extended Analogue Silicon pm Integrated Read Out Chip*, is a 32-channel fully-analogue front end ASIC dedicated to the gain trimming and read-out of SiPM detectors.

This guide explains how to install & use the test board for EASIROC and how to operate with the associated software.

Orsay MicroElectronics Group Associated

A new test is foreseen at the neutron test facility in Legnaro toward the end of this month. The test is meant to evaluated the SEE rate in the DACs of the EASIROC chip and evaluate the TID dose effects on the analog signal processing units of the ASIC.

We also plan to look for TID effects on the op amps which could be used for the active "pick-up" option mentioned above.

We would stack the ACTEL FPGA board on top of the OMEGA board, in such a way to have correlated measurements failure rate measurements (the FPGA acting as a radiation monitor). In such a way the FPGA would act as some sort of neutron dose monitor, to be checked against the calibration data from the Legnaro facility.

addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: preliminary results

Prior to the irradiation tests:

1) **the EASIROC ASIC provided by LAL/OMEGA was characterized** (thanks to Roberto Malaguti) in order to **record**:

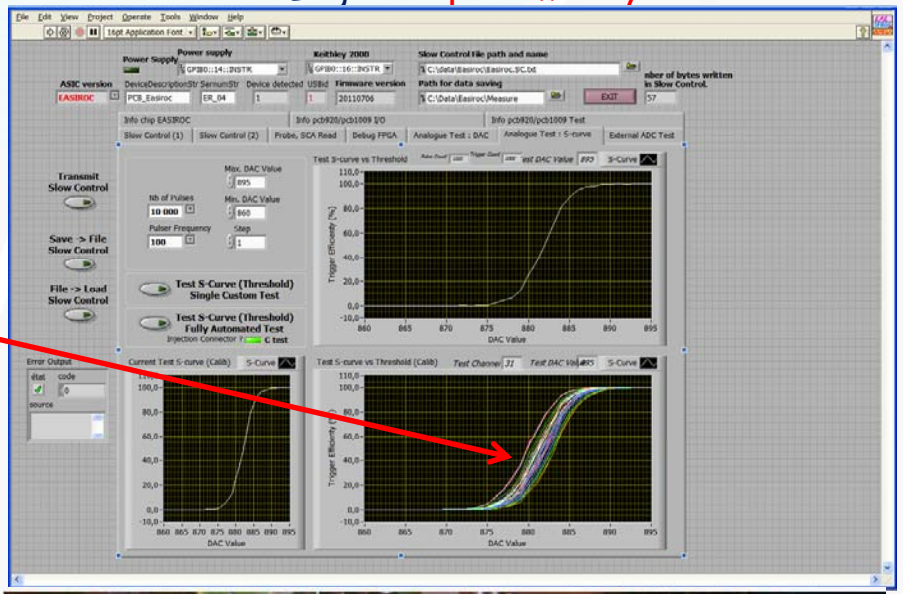
- the transfer curve of the input DACs
- the S-curve for a set of input channels
- the current consumption

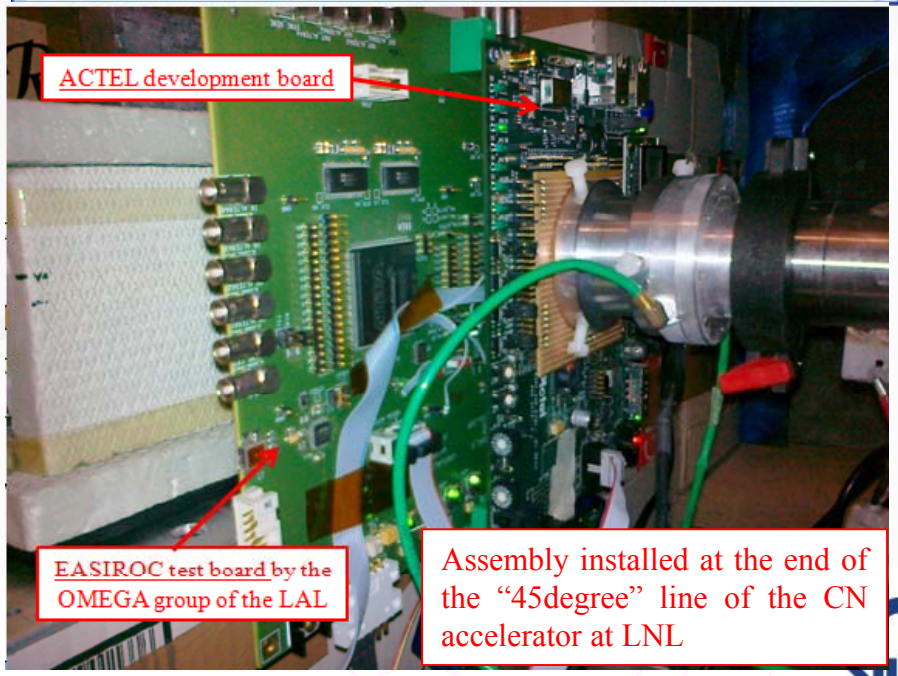
2) the EASIROC test board was **modified to isolate the ASIC from the on-board FPGA** in such a way that the serial programming stream for the initialization of the chip could be provided by a microcontroller board located outside the bunker

3) the firmware for the microcontroller (R.M.) and a Labview program (A.C.R.) were prepared to allow an operator to **periodically send and readback the configuration stream to the configuration registers of the EASIROC (57 words of 8 bit each for a total of 456 bit): these registers were written and checked after a period of about ½ hour to look for SEU**

4) a suitable support was realized to couple the EASIROC board to the FPGA board in such a way that **the FPGA and the ASIC were aligned (and separated by about 13mm)**; the FPGA board was used in this case as a neutron fluence monitor

5) finally a **set of op-amp to be used in the front end differential driver has been fastened on top of the FPGA**





addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: preliminary results

SOLID ANGLE OMEGA	ACTEL	EASIROC
OMEGA =	1,187020767	0,040584586
alfa (cm)	0,9	0,41
beta (cm)	0,9	0,4
alfa * beta = (cm^2)	0,81	0,164
distance d = (cm)	0,7	2
denominator (cm^2)	2,648924 31	16,1632175

	ACTEL	EASIROC
numero totale di neutroni attraverso DUT per tutta la durata del test	**4,96E+12**	**1,69E+11**
numero di neutroni attraverso 1 cm^2 in per tutta la durata del test = fluenza@DUT	**6,12E+12**	**1,03E+12**

data extracted from the "irraggiamento.xls" spreadsheet by Flavio Dalcer...

integrated irradiation time (sec)	charge (μC)	total errors in the FIFO section of the FPGA design	total errors in the shift register section of the FPGA design
60683	4104	752	26
total Yeld/sr/uC @ Ed=4 Mev	hardness factor @ Ed=4 MeV		
1,02E+09	1,146		

If the estimation of neutron flux at the CN facility in Legnaro is correct then we have exposed the devices to a total flux of :

≈ **4.9 * 10 ^{12}** neutrons at the FPGA location

≈ **1.7 * 10 ^{11}** neutrons at the EASIROC location

in about **17** hours, during which we have detected:

- NO SINGLE EVENT EFFECTS HAVE BEEN OBSERVED FOR THE EASIROC

-752 errors in the RAM based section of the design

- 26 errors in the shift register instantiated in the FPGA fabric

(the beam intensity was lower than that of the previous tests because the deuterium bottle became almost exhausted during the last day)

FIFO depth: 4096
Shift Reg. Depth: 728
word width: 8

<numero di bit flip in FIFO> : 752,0000
22949,218
per Mb: 8
<numero di bit flip in Shift Reg> : 26,0000
per Million Flip Flop: 4464,2857

vedi: "Overview of iRoC Technologies Report "Radiation Results of the SER Test of Actel FPGA December 2005"

da: "Radiation Results of the SER Test of Actel, Xilinx and Altera FPGA instances"

cross section per chip: Sigma_C = No_of_errors / (fluence * C) with C= number of chips

reference fluence: fluence at ground level in New York City: fluence_NYC = 14 n/cm^2/hour

FIT: Failure In Time: failures in 10^9 hours. FIT = Sigma_C * fluence_NYC * 10^9

a.c.r. 2011-11-02

nel nostro caso:

ref_fluence/hour 1,400E+01

		Sigma_C [cm^2]	FIT
a3p250-FIFO section	FIFO	1,229E-10	1,721E+00
a3p250-SHIFT Register section	SHIFT REGISTER	4,250E-12	5,950E-02

definisco: cross section per FIFO Mb: Sigma_Mb = No_of_errors * 10^6 / (fluence * N_FIFO_bit)

	Sigma_Mb
a3p250: Fifo cross section per Mbit	3,75131E-09

definisco: cross section per M flipflops: Sigma_Mff = No_of_errors * 10^6 / (fluence * N_flipflops)

	Sigma_Mff
a3p250: ShiftRegister cross section per Mflipflop	7,29738E-10

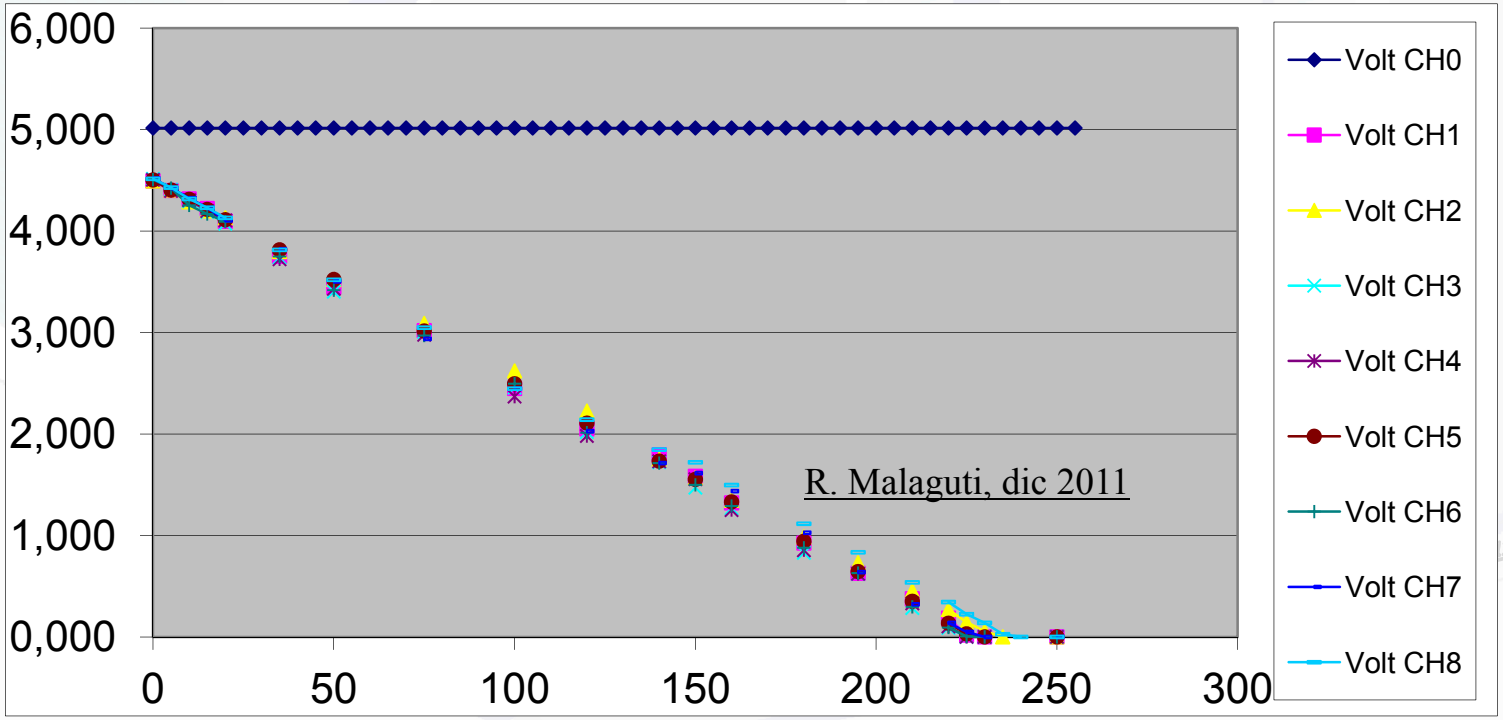
FIT (Failure in Time) figure resulting from our test is **30** times smaller than that published by ACTEL for a similar FPGA tested with 14MeV neutrons.

our test at LNL on a ProASIC3 device a3p250	IROC test on a ProASIC3 E device a3pE600
FIT per million bit of embedded RAM	**FIT per million bit of embedded RAM**
5,252E+01	**1580**
FIT per million flip flop	**FIT per million flip flop**
1,022E+01	**889**
5,141E+00	**1,7**

ratios RAMbit errors/FF errors

addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: preliminary results

- **EASIROC test results:**
  - **integrated neutron fluence at the EASIROC location : ≈ 1.7 * 10 ^{11} neutrons**
  - **TID effects: change in DAC characteristics due to irradiation : undetectable**

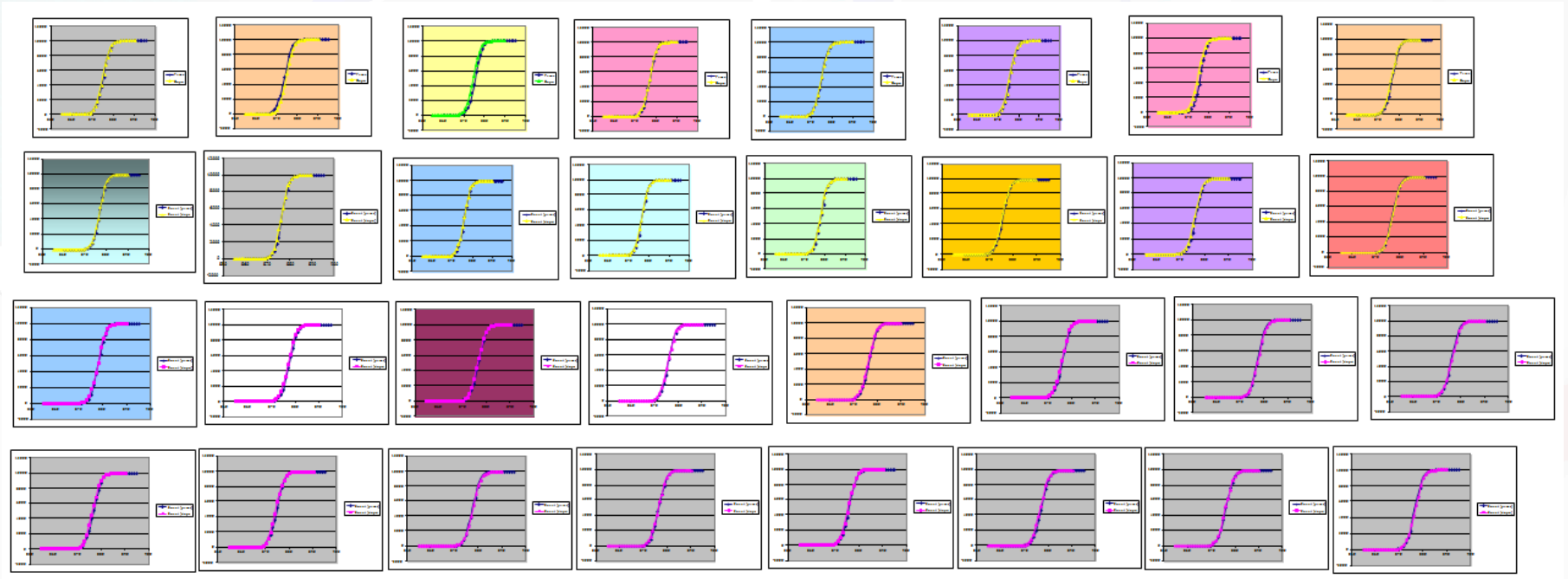


The plot shows the transfer curves, taken BEFORE irradiation, for the input DACs for the channels 0 through 8. Channel 0 was damaged by us at the beginning of the test and can be neglected.

The plots created after irradiation show no detectable differences; just one measurement point, at DAC count 140 for channel 7, was off by 130mV. At all other points the differences were within the systematic error range

addressing the radiation issues: measurement of TID and SEE on the optional front end op-amps and the EASIROC at the INFN Laboratori Nazionali di Legnaro: preliminary results

- **EASIROC test results:**
  - **integrated neutron fluence at the EASIROC location : ≈ 1.7 * 10 ^{11} neutrons**
  - **TID effects: change in S-curves due to irradiation : minor**



R. Malaguti, dic 2011

The plots, by R. Malaguti, show the S-curves, taken BEFORE and AFTER irradiation. In general they shows shifts which could be compatible with systematic errors.
A couple of S-curves are shown in more details on the next slide

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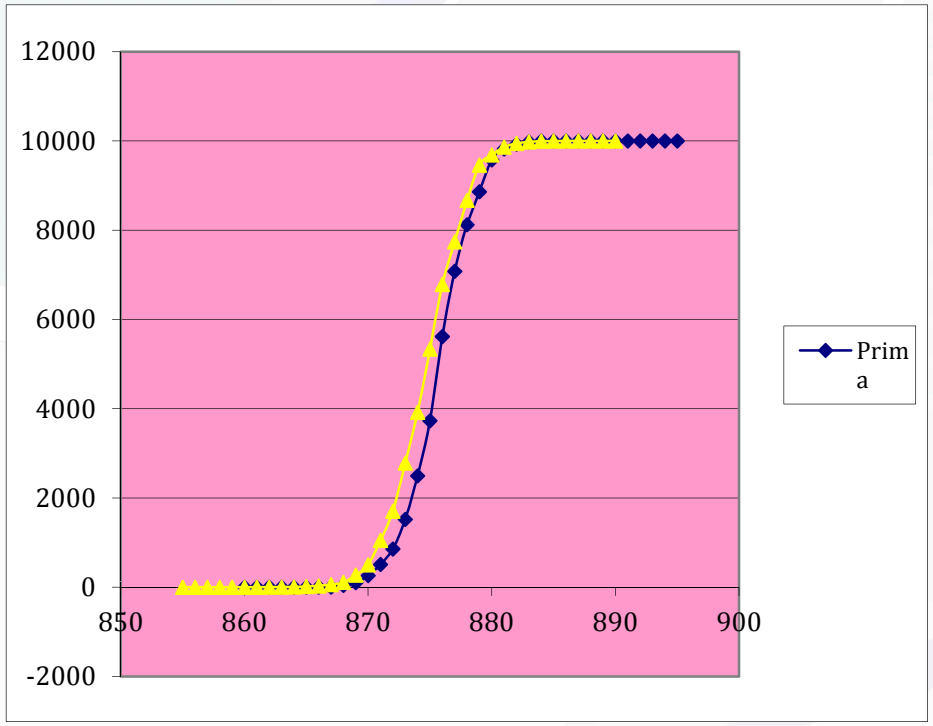

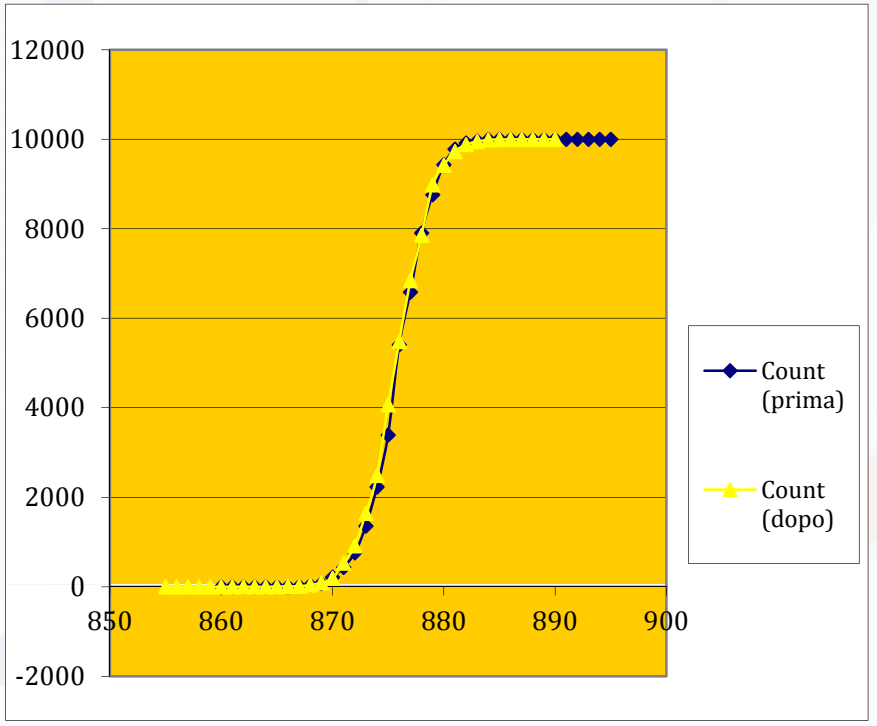

The plots shown are representative of channel with little (**left, channel 6**) or no (**right, channel 13**) difference between BEFORE and AFTER irradiation.

addressing the radiation issues: preparation for next irradiation tests

For the coming irradiation tests we are developing dedicated carrier cards (LEFT) for the EASIROC ASIC and auxiliary cards (RIGHT) to detect (and protect) Single Event LatchUp. The auxiliary card couls be used also for the CLARO and the RAPSODI ASIC#2