

SVT – TDR final phase (I)

- Internal revision of the text started on completed sections (~ 75%)
 - Very few people (2!) sent comments on the written parts!
 - Some of the parallel sessions devoted to TDR reading to get some more feedback.
- Mechanics/Silicon sensor chapter is progressing.
- Background still to be written (only 2 pages + table)
- Still nothing in svn from peripheral electronics fanout layer0!
- Tech Board asked to enter in the final editing phase after this Meeting with the goal to publish by the end of October.
 - Subsystem final readers appointed (Adrian Bevan for SVT). Should work for 2 weeks starting asap.
 - Final editing by the editorial board for 2 more weeks.
- This looks a bit optimistic from the status I see today in svn for SVT but I really hope to have all the sections completed by the end of this meeting.



SVT – TDR final phase (II)

- Need to include budget and schedule for SVT construction and will devote some time in the parallel tomorrow morning to discuss this.
- Budget used for white paper should be revised
 - Need to include costing for quick demounting: nothing there.
 - Refine manpower/cost for technicians and eng. for construction (seems underestimated for some phases)
- Preliminary schedule built looking at BaBar experience + some guess on Layer0 needs and relaxing the final phase of construction w.r.t BaBar.



Main Assumption: Manpower available

- ▶ Assumed **2 main labs** (as in BaBar):
 - ▶ Pisa+UCSB for modules
 - ▶ LBL+(Pisa) SVT Mechanics
 - ▶ Pisa+Trieste Silicon sensors
 - ▶ Pisa+Torino+Ferrara Jigs
 - ▶ LBL+PV+MI On detector electronics
 - ▶ UCSC Off Det. Electronics

Using BaBar SVT Construction Experience + Layer0 needs + more relaxed final phase

	BABAR Experience		comments	SuperB	end date	comments
	months	date		months		
Si sensor design	12	95		12		
Si sensor production test	18	mid 96- end 97		18		
DFA	12-18 months	beg full speed july 97 end 98		18		also L0
chips available		mid 98			mid 2015	prototyping ends in 2 yrs from now. + 6 months production
HDI loading	4	aug 98-nov 98	too hard in 4 months	12 m with 6m chips loading starting when chips available	end 2015	include L0
DFA+HDI L1-2-3	3	sept - nov 98	in UCSB	module assembly in 2 places 3 month for DFA+HDI + 3 months for Module assembly 6 months total	Mar-16	
DFA+HDI L4-5	3	oct-dic 98	in PISA at the same time DFA_HDI bonding/testing and Arch construction (2 teams too hard!!)	module assembly in 2 places 3 month for DFA+HDI + 3 months for Module assembly 6 months total	Mar-16	
Module 1-2-3	2	oc-nov 98	in UCSB	module assembly in 2 places 3 month for DFA+HDI + 3 months for Module assembly 6 months total	mid 2016	
Arch 4-5	3	nov98 jan99	in PISA at the same time DFA_HDI bonding/testing and Arch construction (2 teams too hard!!)	module assembly in 2 places 3 month for DFA+HDI + 3 months for Module assembly 6 months total	mid 2016	
installation on support cones	3	jan-march 99		6 months considering L0 too	end 2016	
installation of SVT	3	march-june 99		3	Mar-17	

UPDATED looking more carefully at BaBar schedule and including Layer0

Item (months) Construction for Baseline (striplets +SVT)	2012 TDR	2013 Design & Protot.	2014	2015	2016	2017 Commissio ning in SuperB
Installation (3)						↔
Final Assembly (6)					↔	
Module Ass. (Arch- SextantStriplets)(3)					↔	
DFA+HDI Ass.(3)					↔	
HDI (12)				↔		
Chip Production (6) Cannot start before 2015				↔		
DFA (18)			↔			
Fanout (15)			↔			
Silicon Sensors (18)			↔			
Off Det Electr. (24)			↔			
Transit. Cards (15)			↔			
Mechanics Support Structure (18-24) Module & Jigs (18)			↔			

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- ▶ Started to fill the Smartsheet document with previous inputs.
 - ▶ Still some inputs on mechanics are needed.
 - ▶ I'll discuss this schedule with the SVT group during this week.