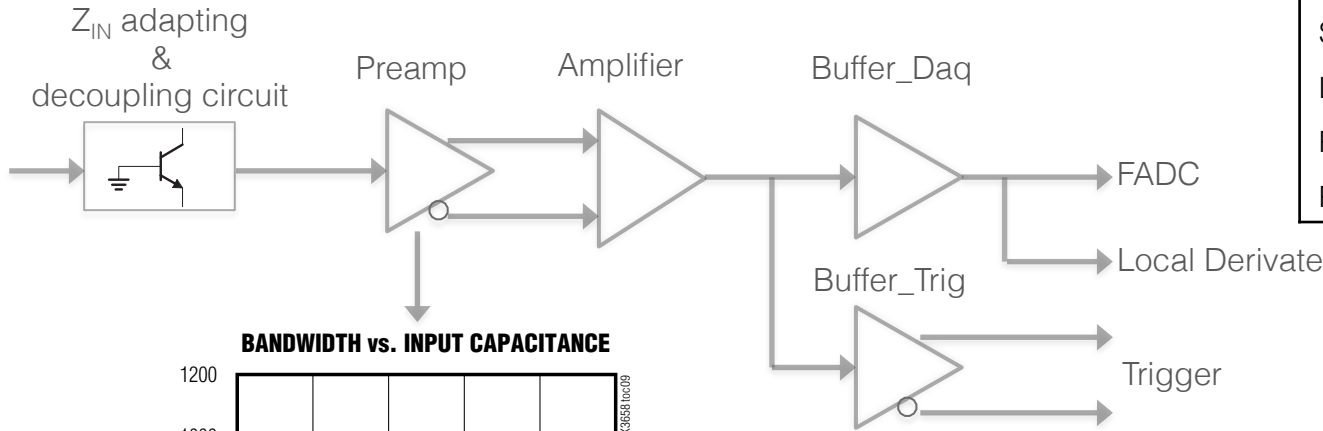


Requirements

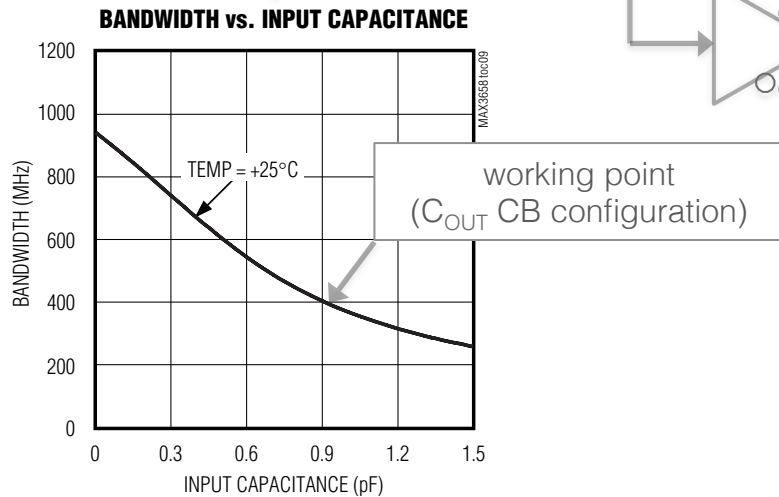
- $BW \approx 350 \text{ MHz}$
- $Gain \geq 5 \text{ mV/fC}$
- $Noise \leq 2000 \text{ erms}$

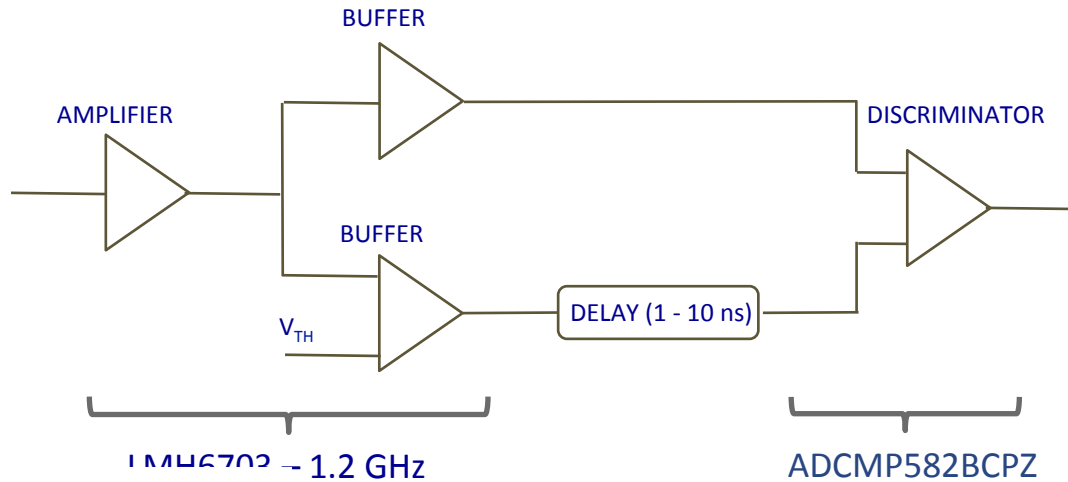
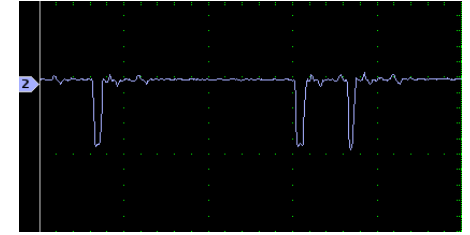
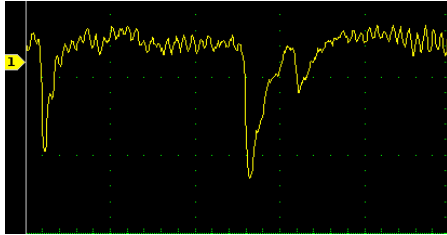
$BW \approx 350 \text{ MHz}$

Z_{IN} decoupling	BFP740 SiGe Transistor (BW > 10 GHz)
Preamp	MAX3658 (BW $\geq 350 \text{ MHz}$)
Amplifier	CLC1606 (BW $\geq 1 \text{ GHz @ G = 2}$)
Buffer_Daq	CLC1606 (BW $\geq 1 \text{ GHz @ G = 2}$)
Buffer_Trig	THS4503 (BW $\geq 370 \text{ MHz @ G = 1}$)



SCHEDULE	
Schematic	OK
Layout	14/09
Prototype	05/10
Production	19/10





Main Features

- VME mechanics
- 8 channels
- Single-ended output
- Differential output
- BW > 500 MHz