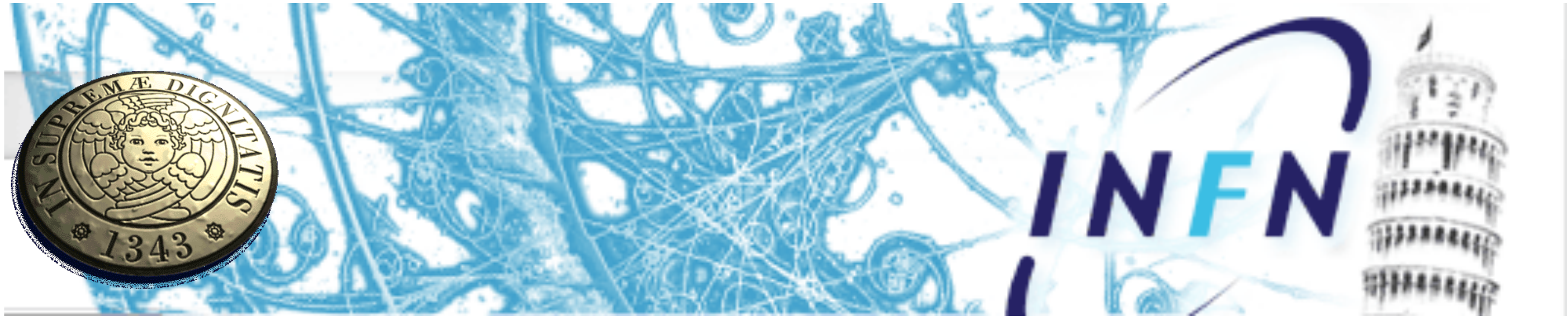
First measurements on the n-irradiated high-Ω INMAPS prototypes

S.Bettarini – F.Morsani – G.Rizzo
Universita' di Pisa & INFN



V SuperB Coll. Meeting - Pisa, SVT Parallel session – 19th September 2012

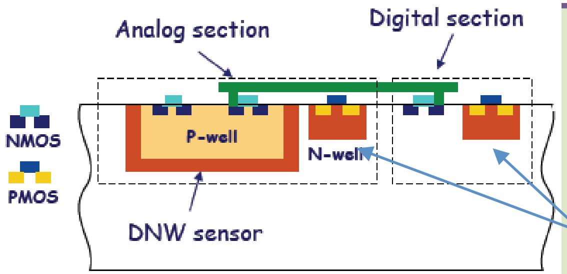
Outline

- Introduction
- INMAPS 3x3 matrices

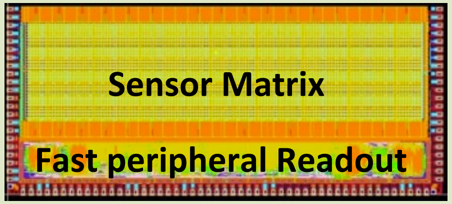
    Analog response to:

    - γ from Fe^{55} (→Gain)
    - Gain calibration for pixel(2,2) by C_{inj}
    - β from Sr^{90} (Charge-colletion→MPV Landau)
- Conclusions

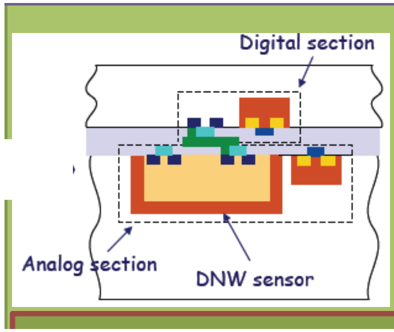
Pixel technologies for SuperB-SVT



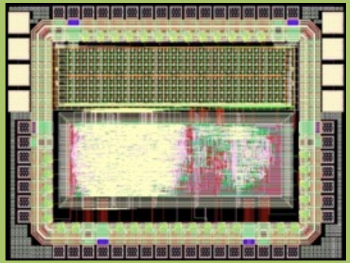
Deep N-well MAPS,
- **In-pixel** front-end electronics (pre, shap, discr).
- **competitive N-well** issue



APSEL4D chip
ST 0.13 um
Beam test **CERN 2008.**
90% efficiency compatible with deep N-well fill factor

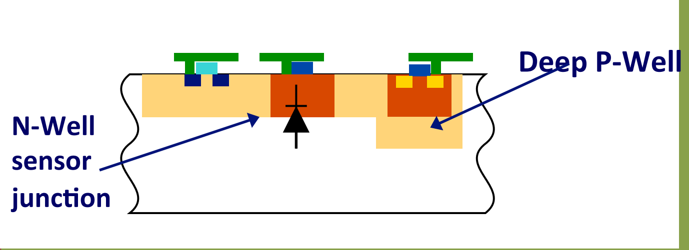


3D MAPS
- **Digital tier: dense pixel digital logic** and peripheral readout
- **In-pixel** analog FE
- **Less competitive N-well issue**

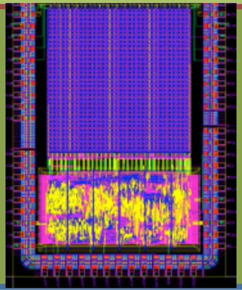


APSEL3D
Tezzaron
Chartered
32x8 matrix

Ongoing tests

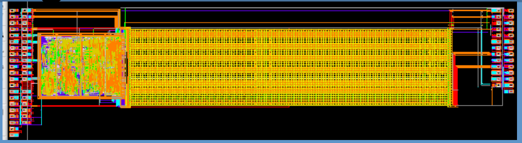


INMAPS technology
- **Deep P-well preventing charge-stealing** by competitive N-wells.
- **High resistivity substrate → more robust against radiation.**

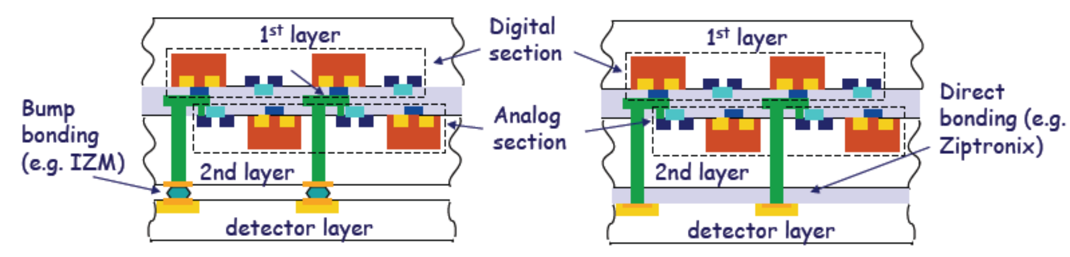


INMAPS 0.18 um
32x32 matrix
submitted July 2011

Hybrid Pixels 50x50 um pitch
- High resistivity, **fully depleted sensor**
- **Fast readout** (analog FE and digital logic at pixel level)

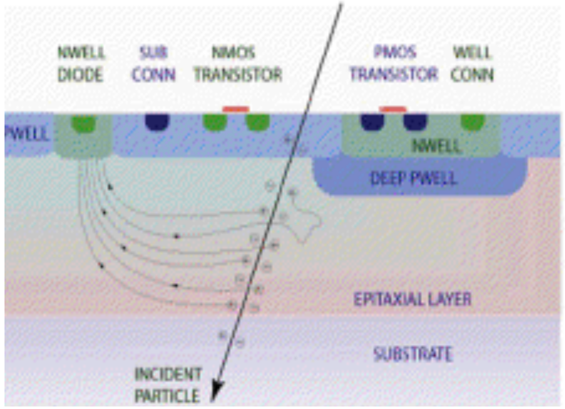


SuperPix0 chip
- **Beam Test** Sept. 2011.
- **Preliminary results presented**



FUTURE… 3D front-end chip
- Dedicated **digital tier**
- **analog tier:** FE electronics.
- **Fully depleted detector** Bump Bonded / Directly Bonded

Why INMAPS



CMOS sensor in the 180nm INMAPS process with high-Ω epilayer

Standard MAPS: poor radiation hardness (important displacement damage observed) could be a showstopper.

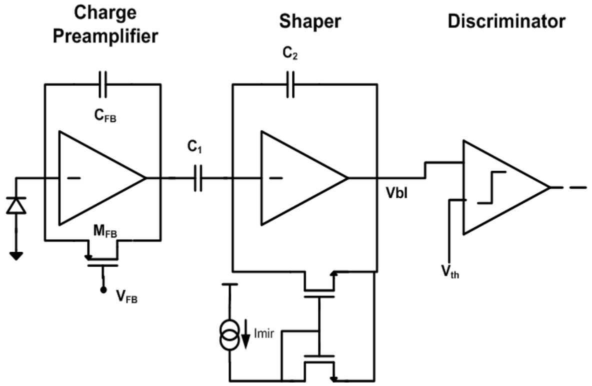
Deep N-well MAPS: charge collection is affected by the parasitic N-wells. It can be avoided with a buried P-type layer (deep P-well)

Further improvement on charge collection by means of high resistivity epitaxial layer (~1 kOhm cm).
Our High-Ω chips delivered in mid june.

A high-resistivity, fully depleted sensing layer with analog CMOS front-end is the solution we are pursuing.

INMAPS developments for the Layer0

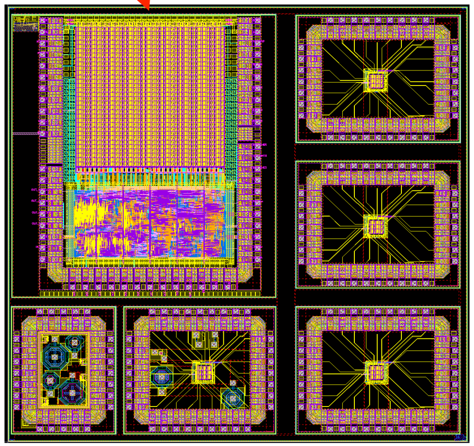
- Small N-well collecting diodes with small input capacitance and low power consumption.
- The forth-well prevents charge stealing by the parasitic N-wells (→ efficiency benefit).
- Implemented the digital architecture as in the latest APSEL chips, to cope with the high bkg rates.

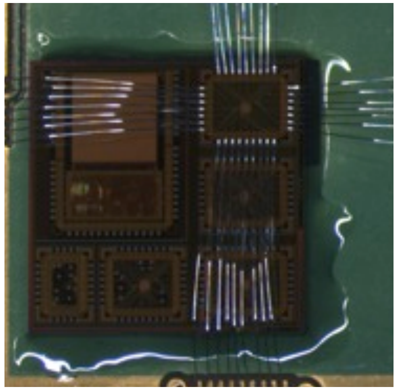


Apsel4well - Post Layout Simulation	
Charge sensitivity	930 mV/fC
t_p @ 800 injected electrons	240 ns
ENC (C_D = 30 fF)	26 e-
Threshold dispersion	23 e-
NLI (@ 2000e-)	1%
Analog Power consumption	18 μW/pixel
Pixel pitch	50 μm

32x32 matrix with sparsified digital readout architecture

3x3 analog matrices with different diodes configurations

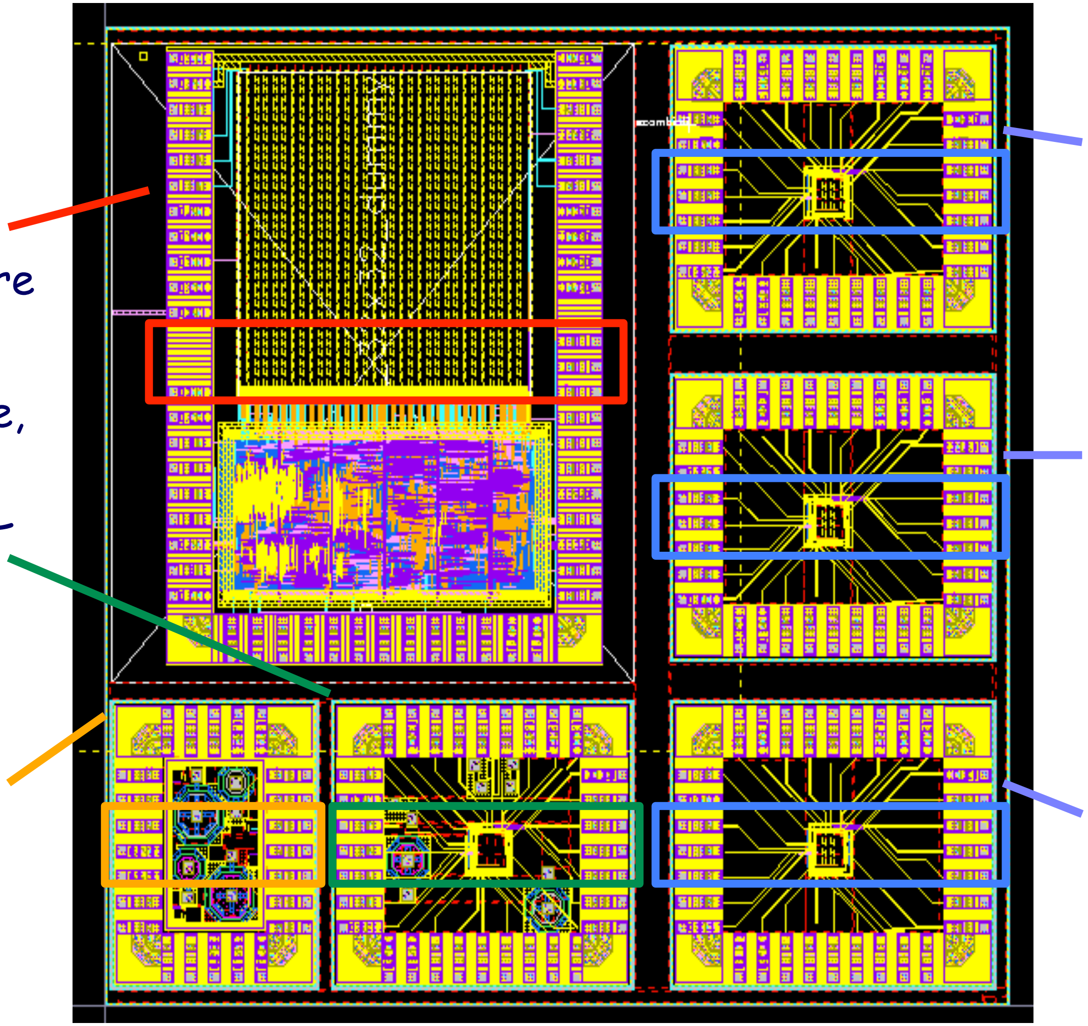




INMAPS Chip (5x5 mm^2)

The INMAPS CHIP

In 3x3 matrices all the analog outputs are available and an injection capacitor is connected to the central pixel



32x32 matrix (4-diode pixels) with sparsified digital readout architecture

3x3 matrix, 4-diode, no DPW, preampli input device with EL structure, Nw/Pepi diodes and accumulator capacitors

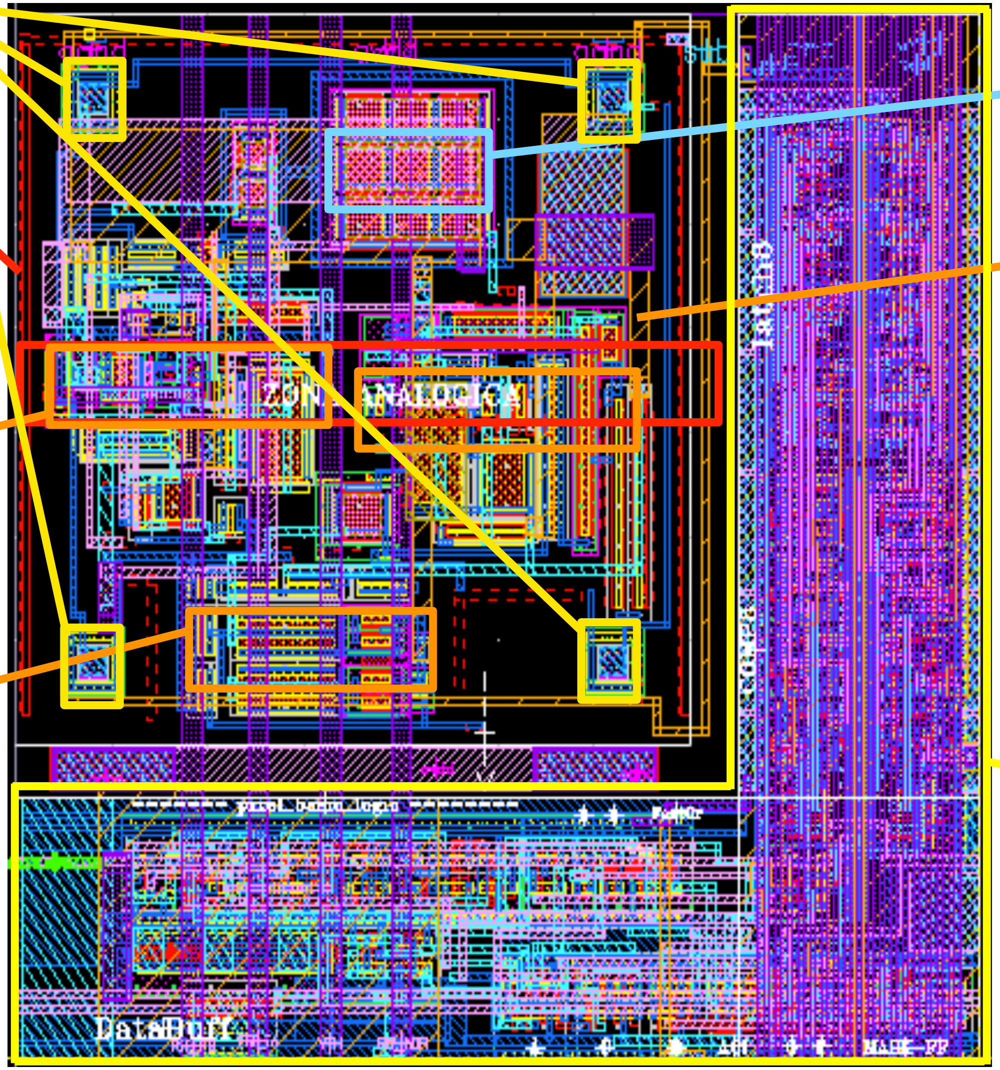
Nw/Pepi diodes, single channels

3x3 matrix, 4-diode pixels, DPW, preampli input device with EL structure

3x3 matrix 4-diode pixels, DPW, preampli input device with open structure

3x3 matrix 2-diode pixels, DPW, preampli input device with EL structure

INMAPS CELL



Collecting diodes

Analog section

Charge preamplifier

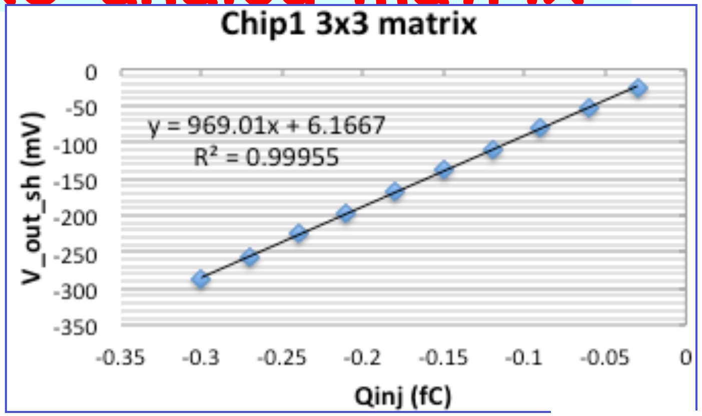
Discriminator

Differentiating capacitor (at the shaper input)

Shaper

Digital section

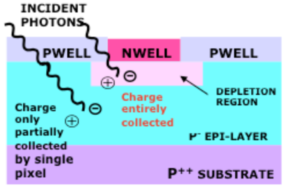
Low-Ω and epi=5 um
INMAPS RESULTS: 3x3 analog matrix



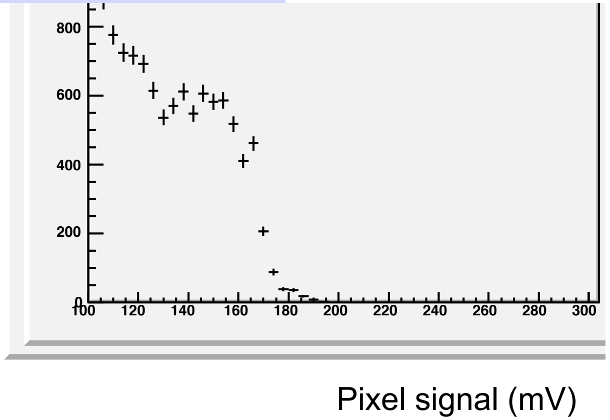
Noise and gain measured in 3x3 analog matrix in good agreement with PLS:

- ENC = 30 e- (~20% dispersion)
- Gain=920 mV/fC (~10% dispersion)

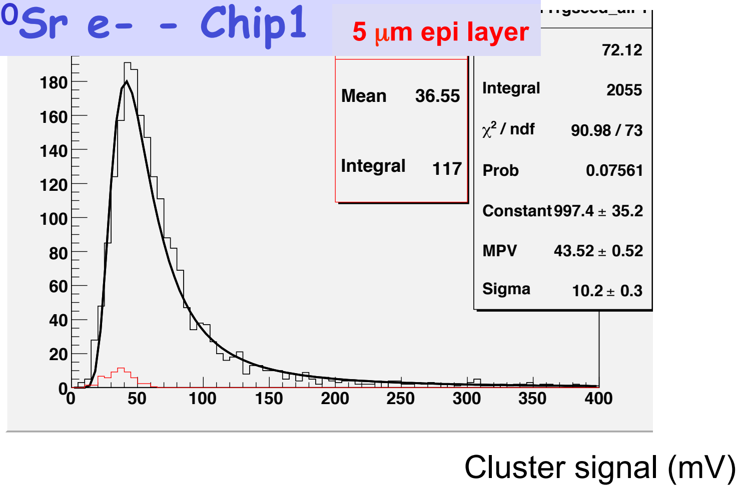
- Response to radioactive source
  - **^{55}Fe γ**: 5.9keV photo peak hardly visible due to very small diode area.
    - Charge totally collected for γ interaction in the depleted volume below the diode. Partial collection elsewhere. End point (5.9 keV + 3 σ noise) used for gain evaluation (agreement within 10% with Cinj)
  - **^{90}Sr e-** signal cluster: MPV ~ 350 e-, compatible with 5 um epi layer of first chips → chips with 12 um epi layer (standard & high resistivity) available since June.



^{55}Fe γ - Chip1



^{90}Sr e- - Chip1



Neutron Irradiation in Lubiana

We decided to irradiate at least 2 naked (i.e. not mounted on carrier) chips for each step:

- Trust on chip uniformity
- Avoid waiting for radiation quarantine
- Have soon a rough response for both Low-Ω and High-Ω chips (irradiation time~some days)
- Postpone a more accurate irradiation campaign

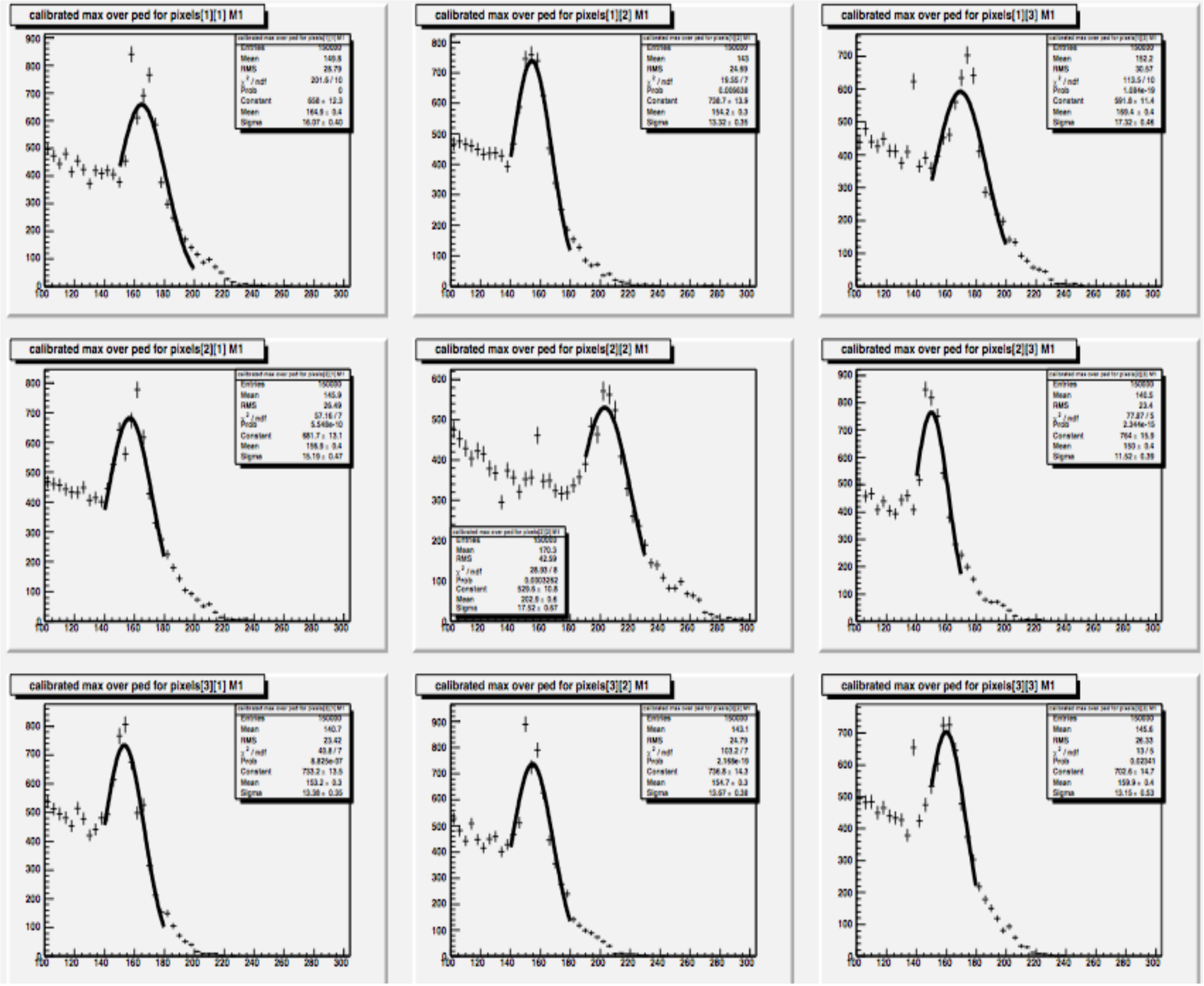
Step	fluence [n/cm2]	Chip Low Ω		Chip High Ω	
0	0		31,32		41,42
1	2.0E+12	1L,2L,3L	53,52,51	1H,2H,3H	63,62,61
2	7.4E+12	4L,5L	54,55	4H,5H	64,65
3	2.7E+13	6L,7L	56,57	6H,7H	66,67
4	1.0E+14	8L,9L	58,59	8H,9H	68,69

Test in Pisa

- Rad. sources spectra requires a lot of time for each chip:
  - Some hours for Fe55
  - A whole day for Sr90
    - (source + no-source acquisitions)
- We focused on High-Ω chips (Low-Ω chips were sent to PV to optimize test-time), observing:
  - Fe55 peak reduces after first steps of radiation (the depleted region decreases)
  - MPV Landau shrinks

- Still to fully understand the mechanism at work!

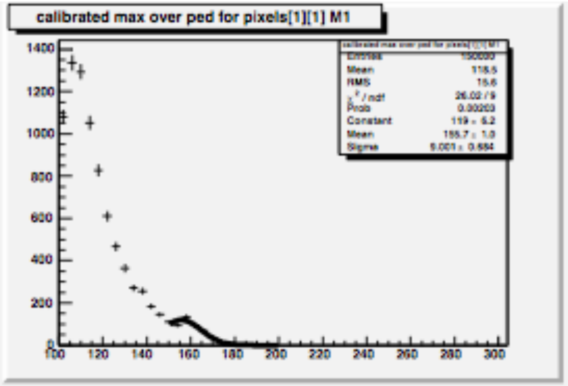
Fe55 spectra not irr.(chip42)

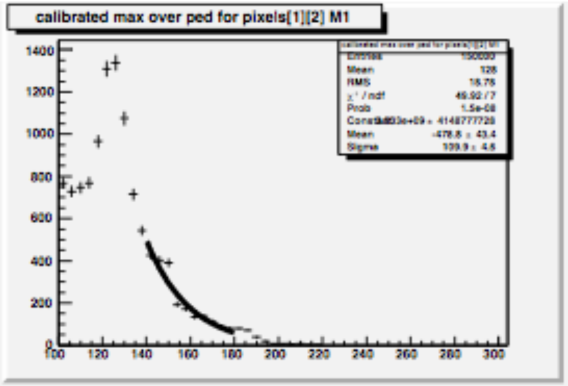


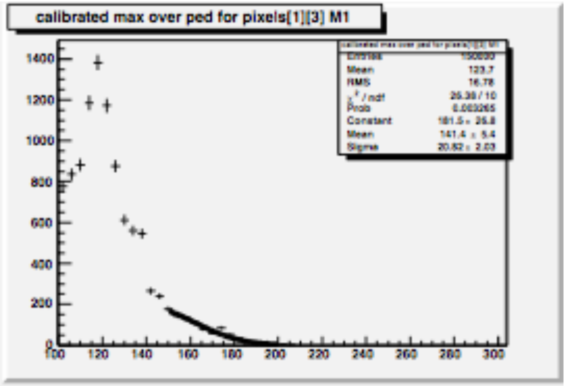
pixel	Mean[mV]	Sigma[mV]
[1,1]	165	16
[1,2]	154	13
[1,3]	169	17
[2,1]	157	15
[2,2]	203	18
[2,3]	150	12
[3,1]	153	13
[3,2]	155	14
[3,3]	160	13

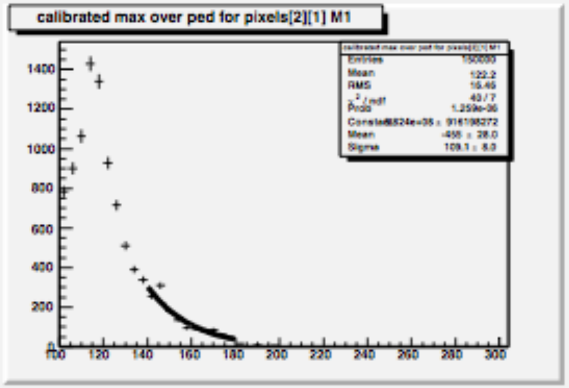
<Mean>=
163+-15 mV
<Sigma>=
15+-2 mV

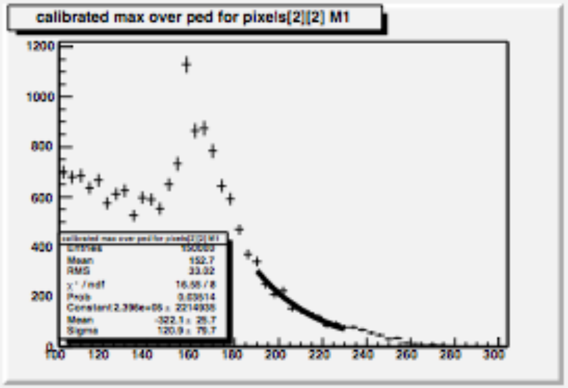
Fe55 spectra irr. step1 (chip62)

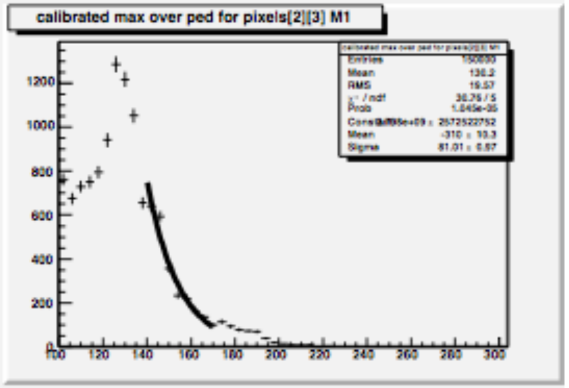


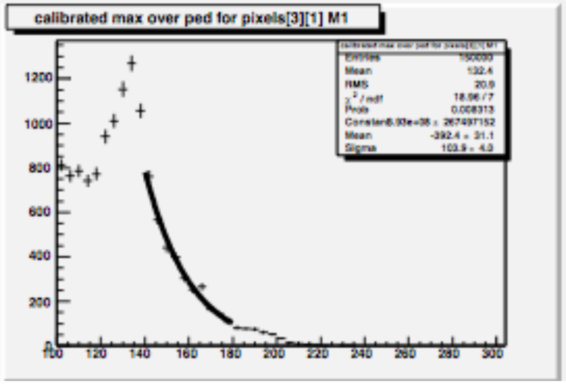


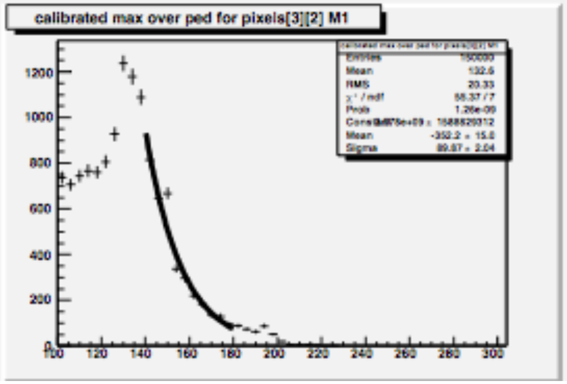


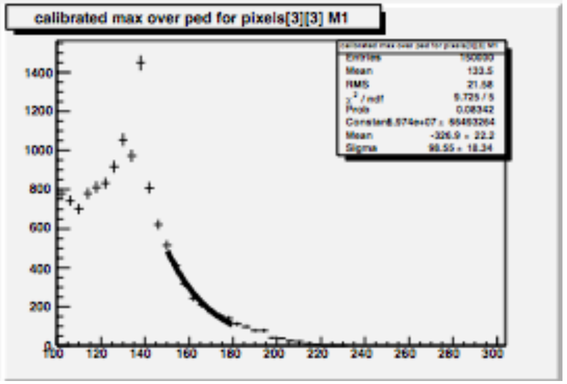




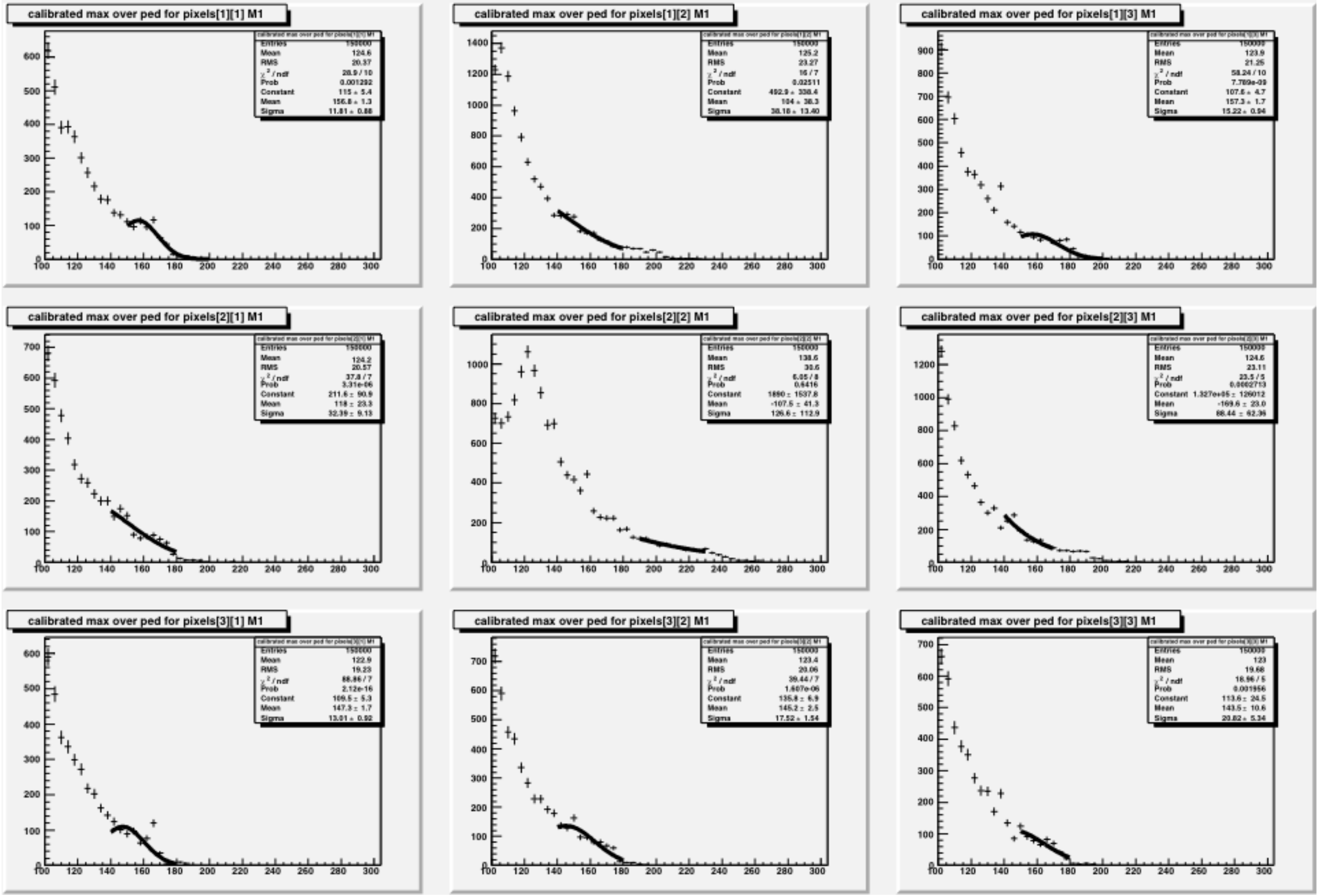




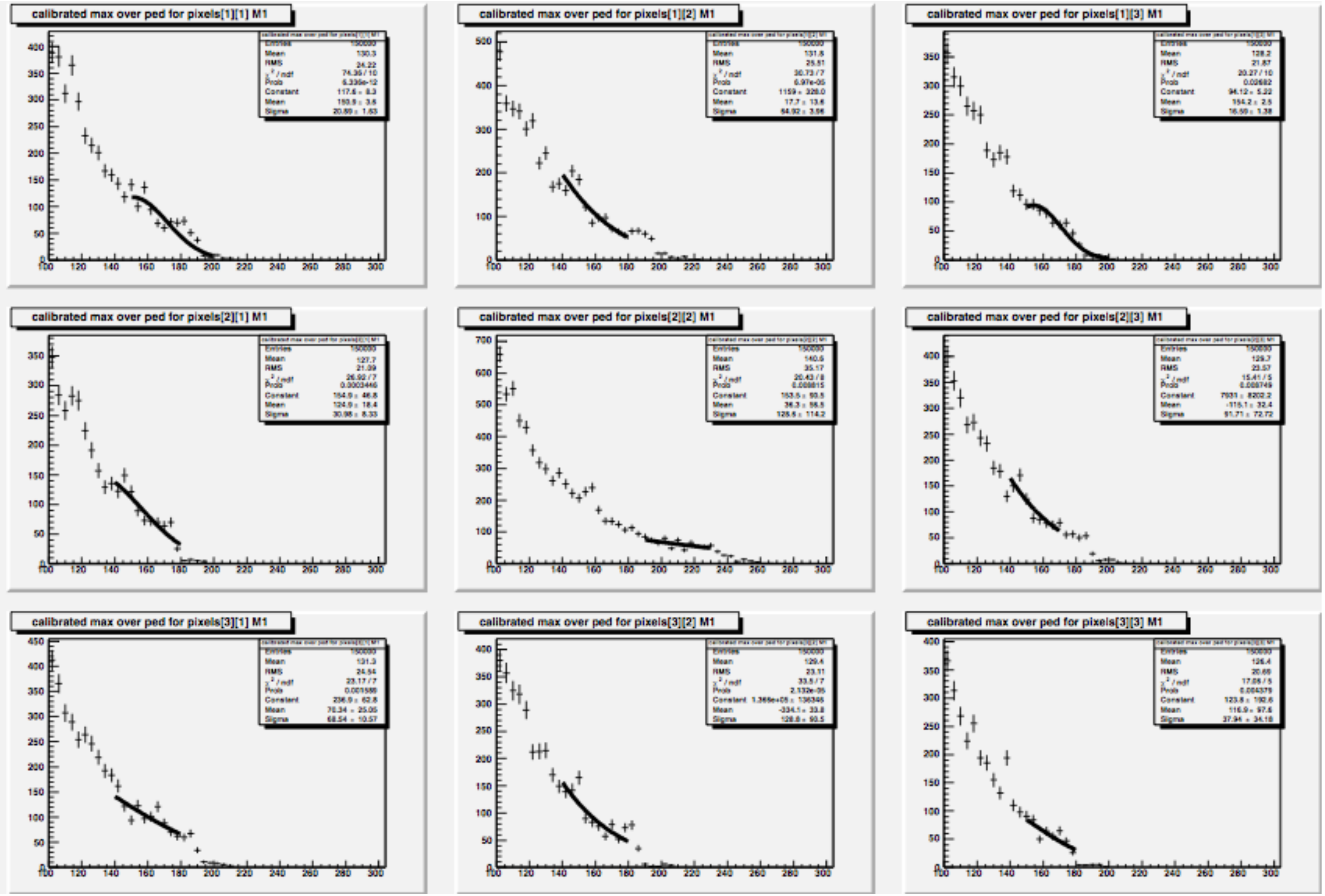




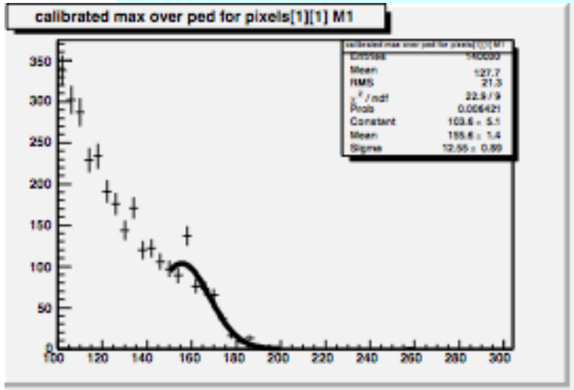
Fe55 spectra irr. step2 (chip64)

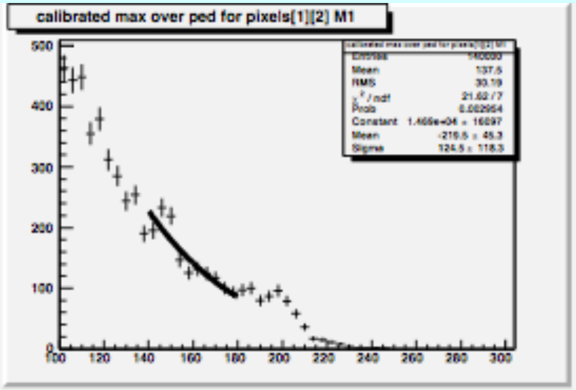


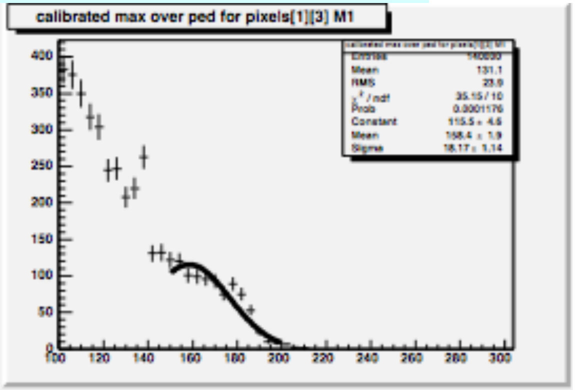
Fe55 spectra irr. step3 (chip66)

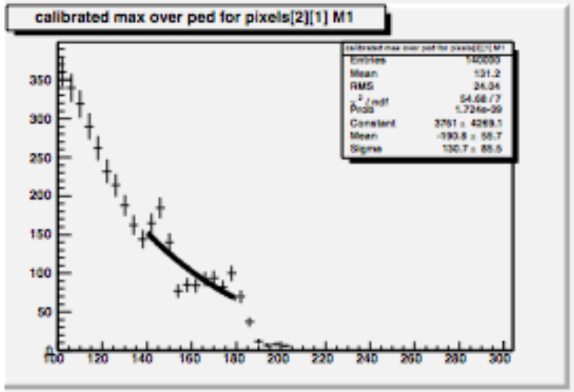


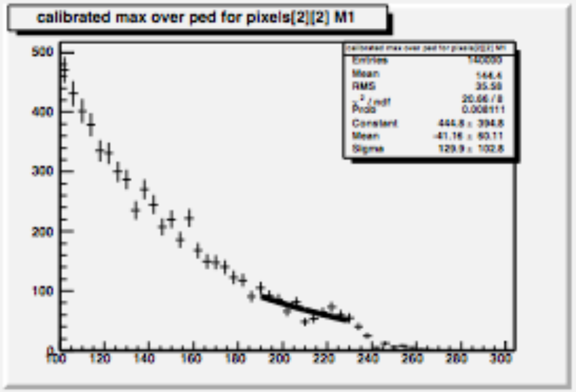
Fe55 spectra irr. step4 (chip68)

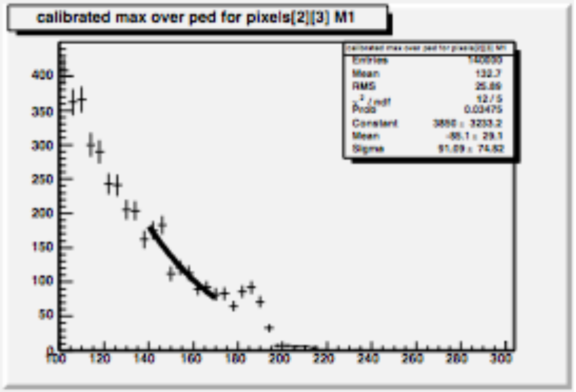


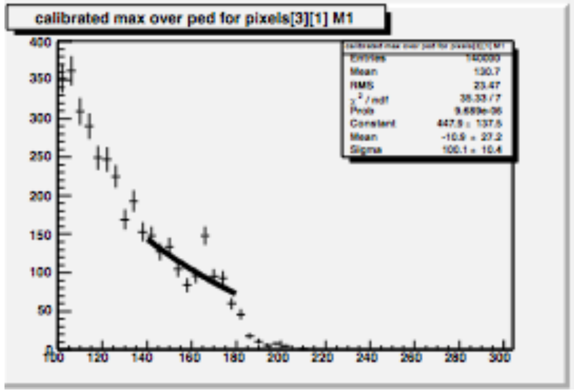


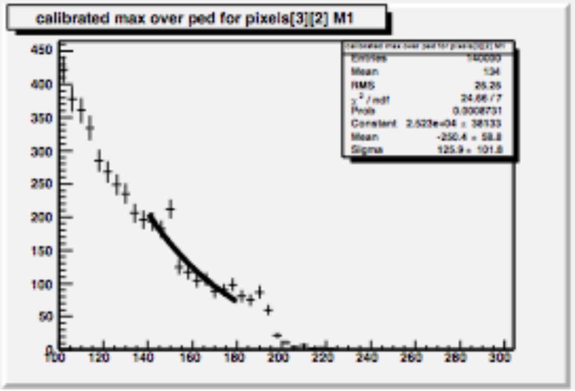


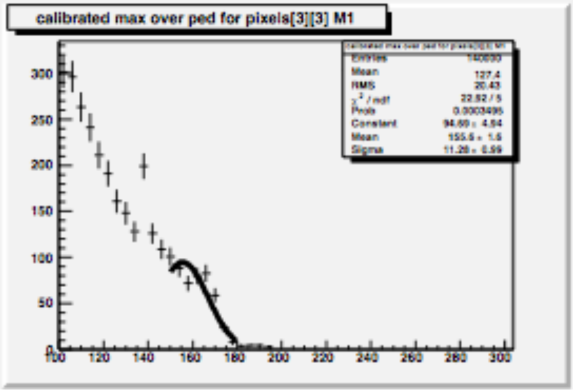




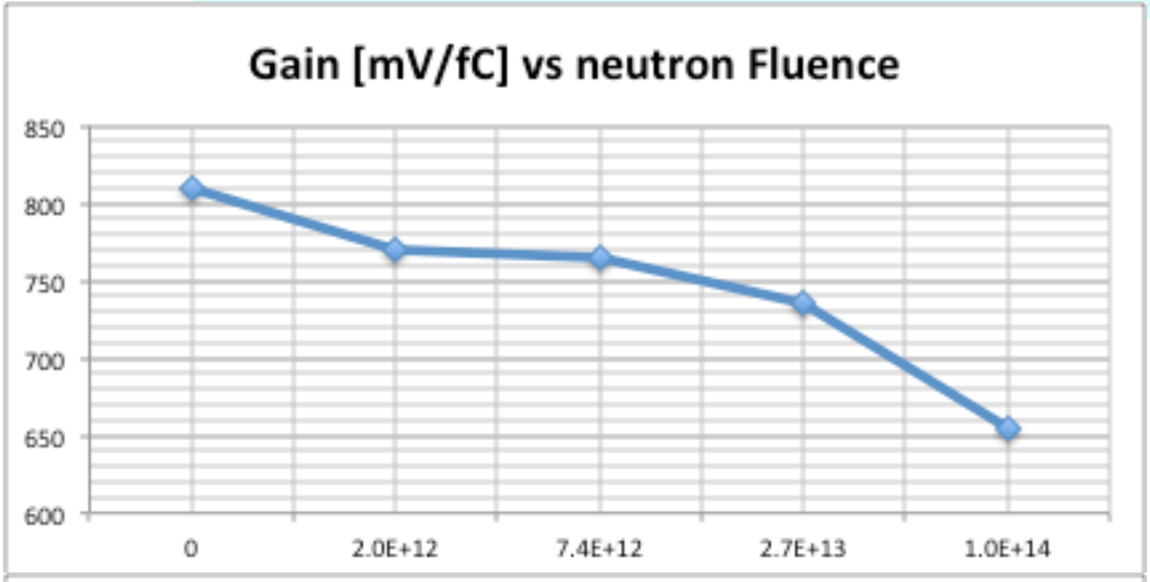


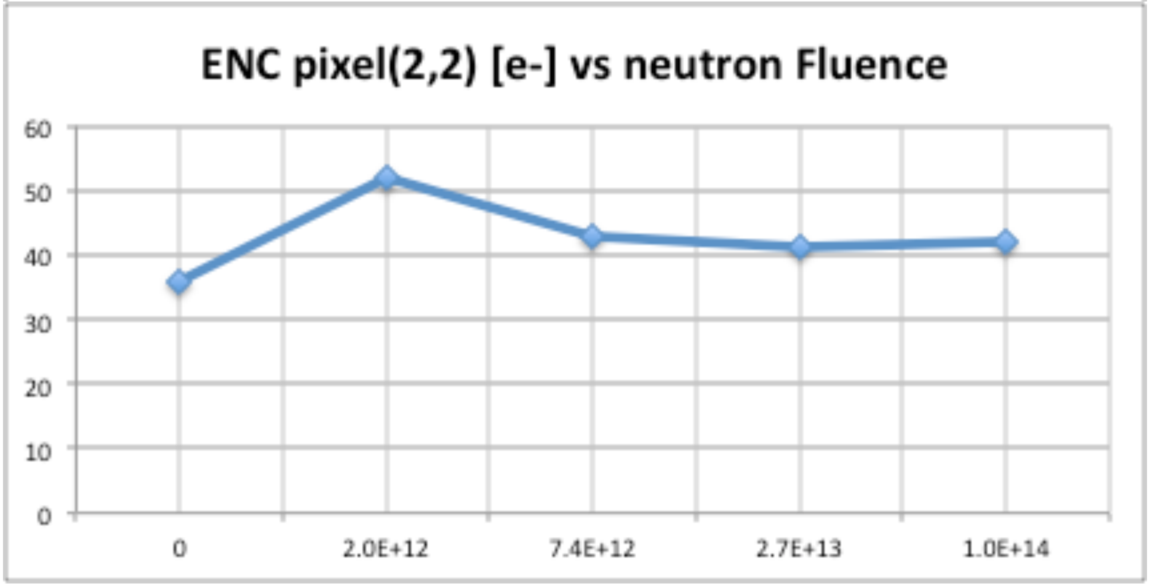






What about the Gain through C_{inj}?





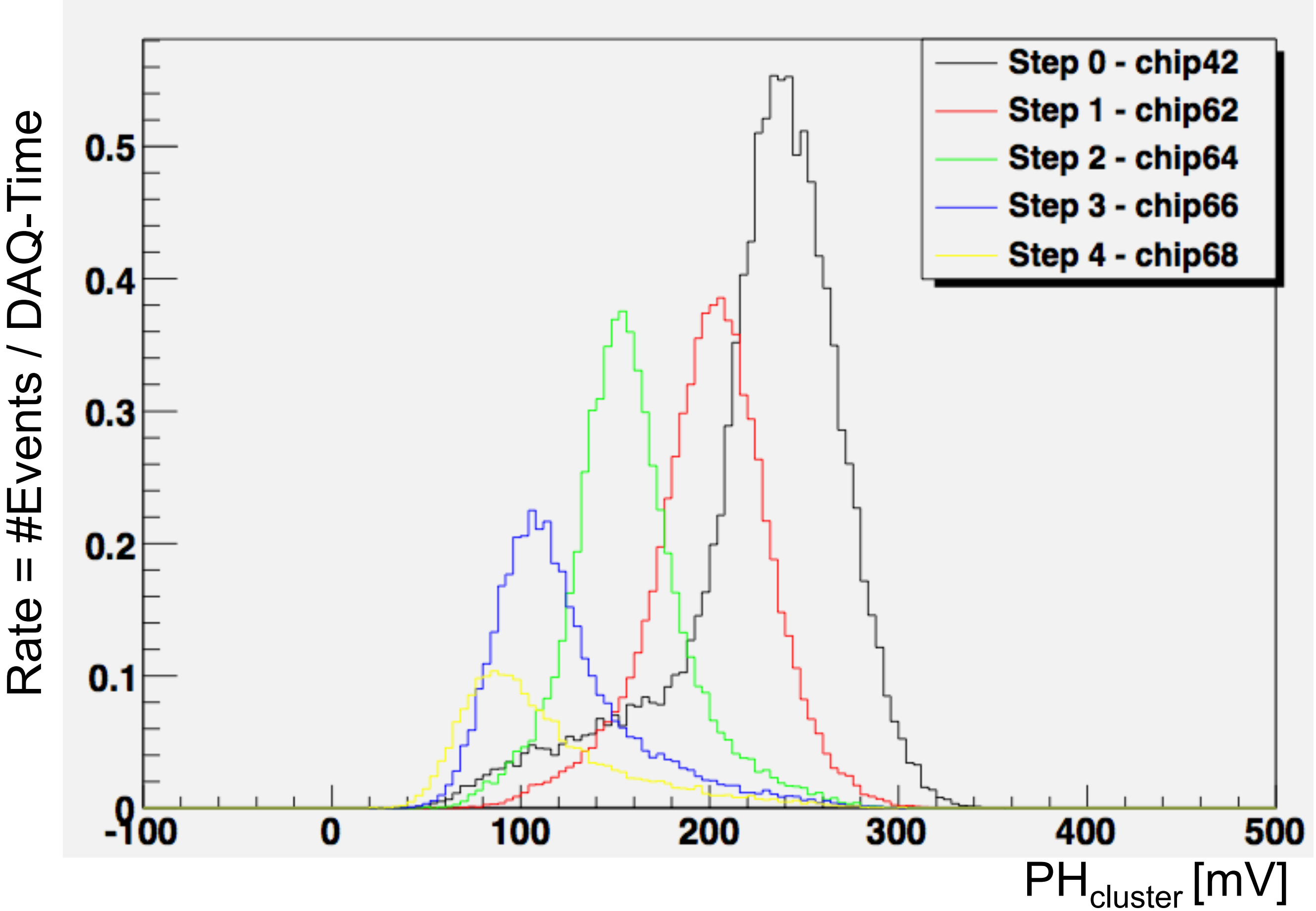
A ~20% decrease in Gain measured with C_{inj} is observed. This is a feature of the high-Ω chips
(not on low-Ω chips).

Fe55 Results/Comments

- The photo-peak becomes less evident as the fluence increases
- The "peak" drifts to the left, meaning that some charge is "lost" by each pixel, instead the end-point of the spectrum seems less affected;
- The Gain calibration is not straightforward…

  (in the following no conversion attempted Pulse height [mV] → Charge [e-])
- C_{inj} calibration →-20% Gain
- Possible to recover summing up the charge of the central pixel (seed, maximum) with the charge of the other 8 pixel providing the $PH_{cluster}$?

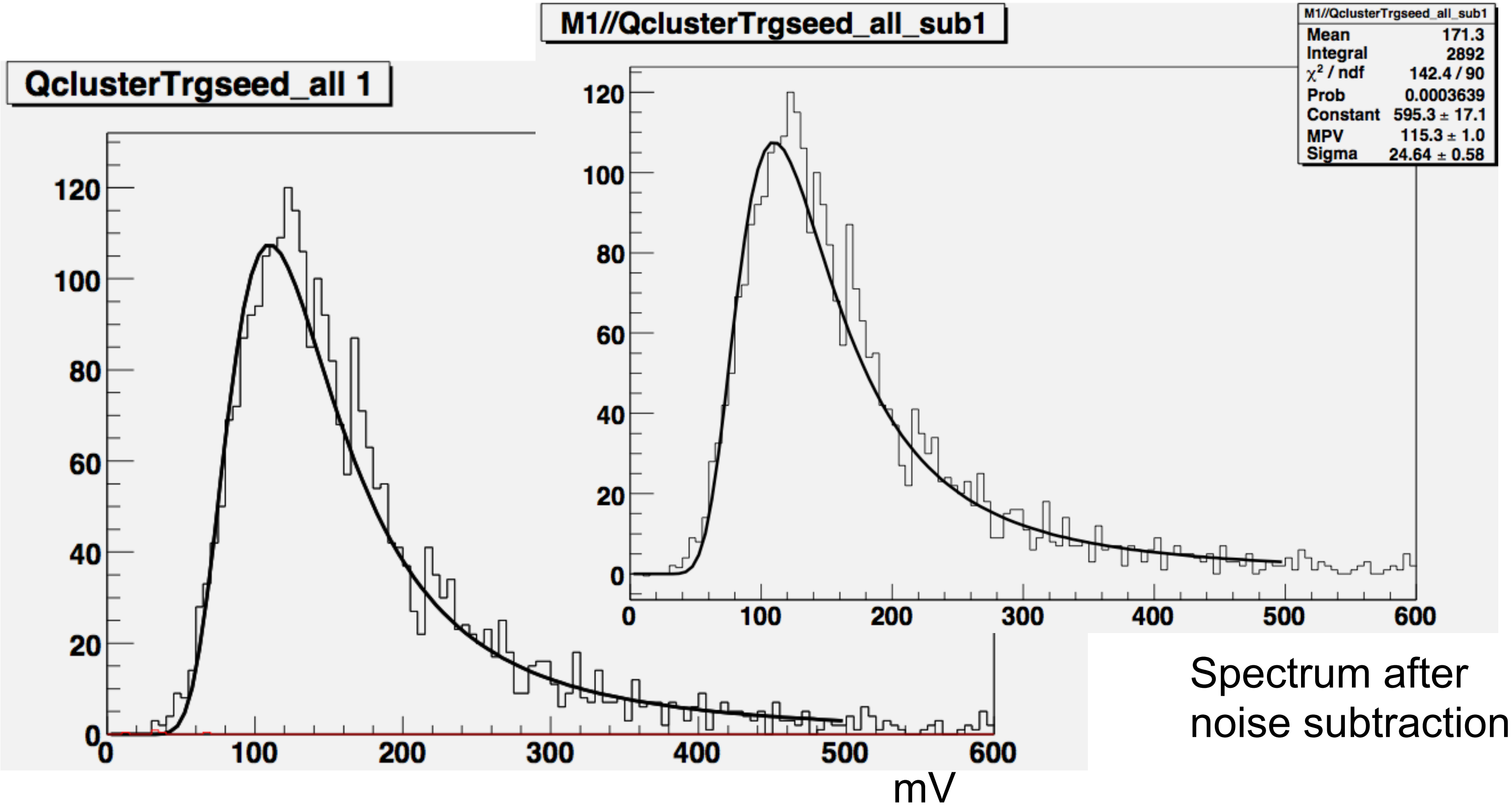
PH$_{cluster}$



Due to radiation damage, the charge is no longer completely collected.
Furthermore the rates decrease with irradiation.
Some mechanism is at work, by decreasing the size of depleted region around our tiny electrodes and affecting the lifetime of the minority carriers.

Sr90 spectrum not irr.(chip42)

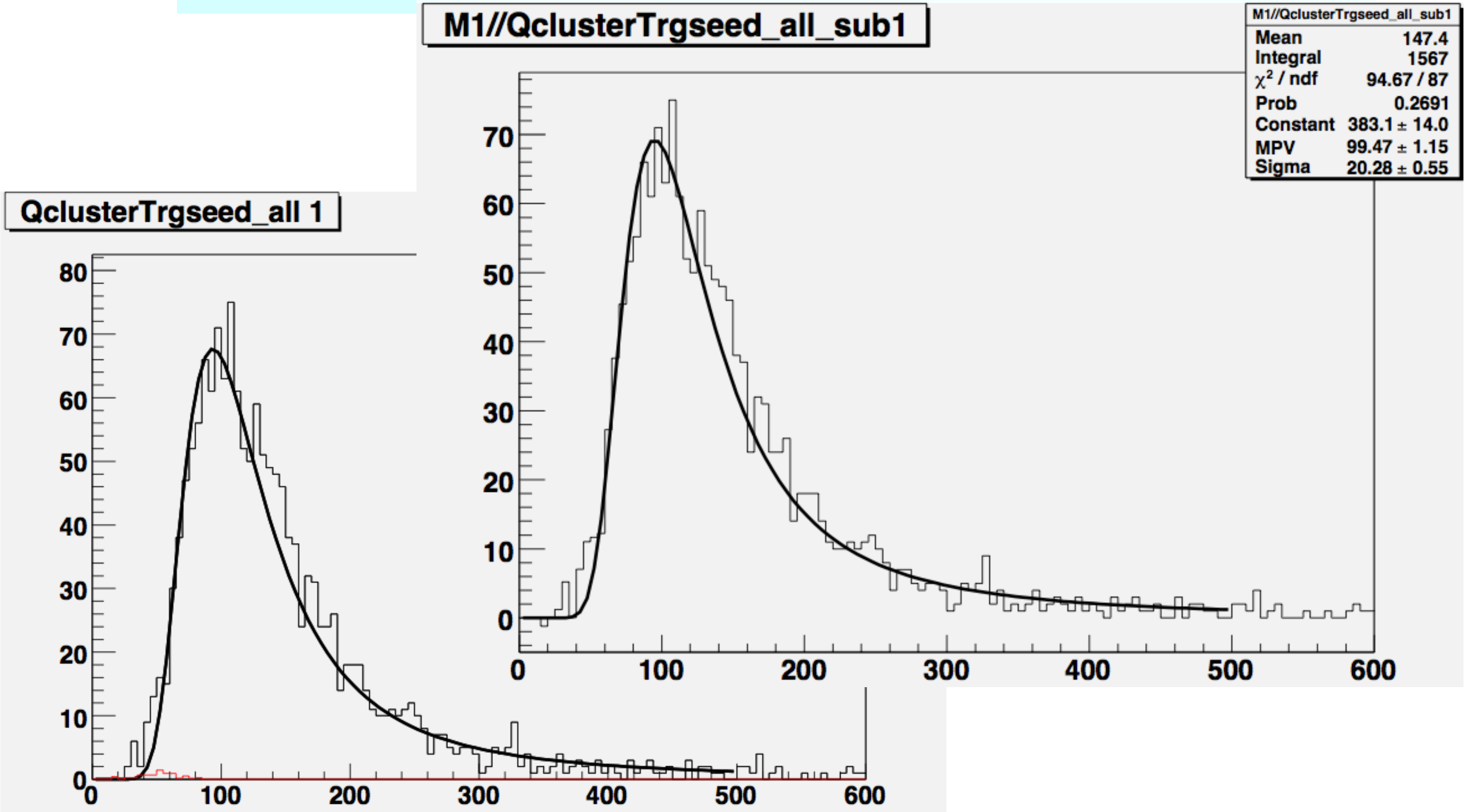
Trigger=4$\sigma_{[2,2]}$ above pedestal after (1 τ_{peak}) the scintillator fires
Analysis= V[2,2,]@τ_{peak} >5$\sigma_{[2,2]}$ and $Q_{cluster}$[mV] = Σ V[i,j]@τ_{peak}



Spectrum after noise subtraction ⬆

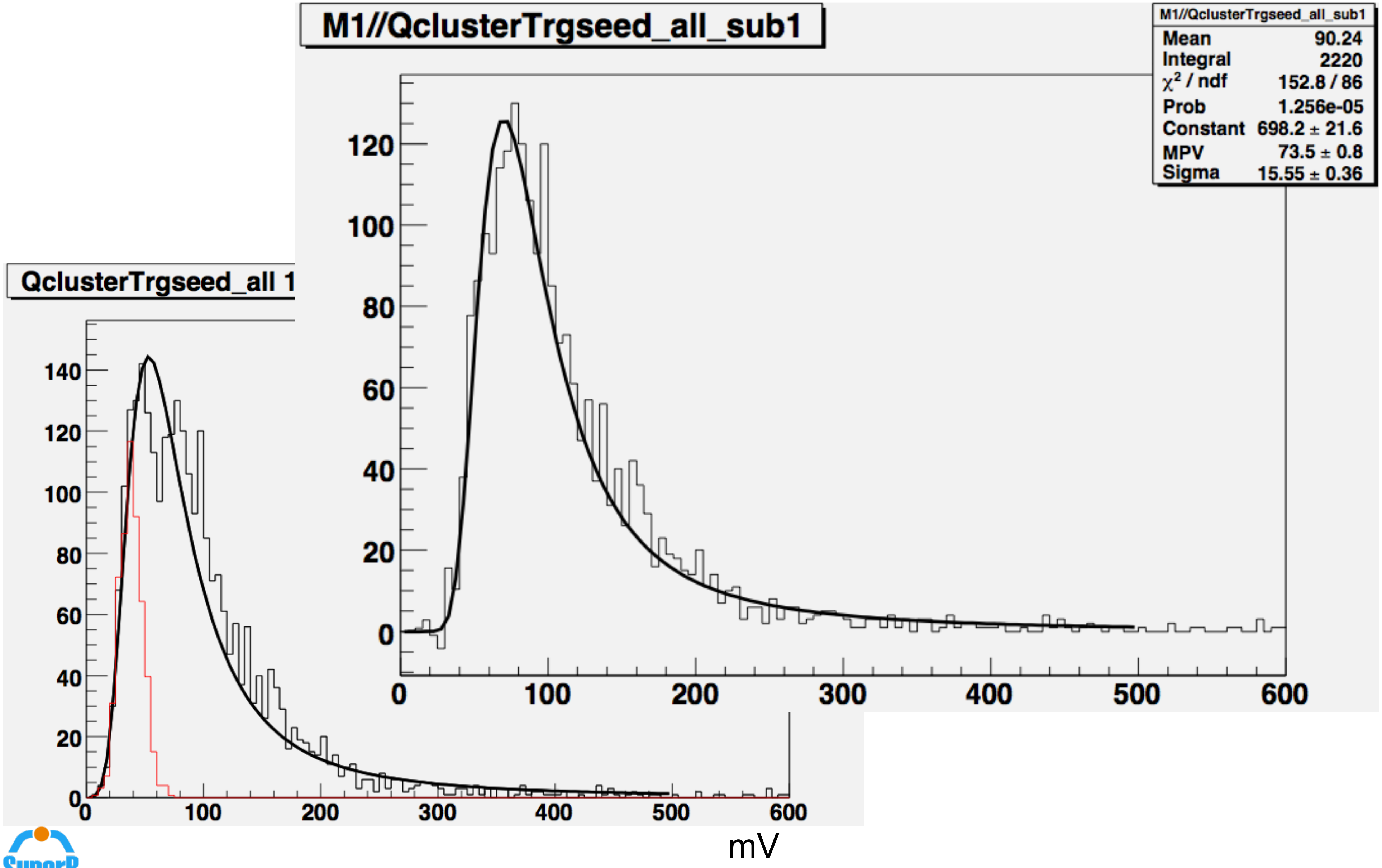
Noise events (in red) taken w/o source with a pulser firing at the same frequency of the scintillator in the source spectrum.

Sr90 spectrum step 1 (chip62)

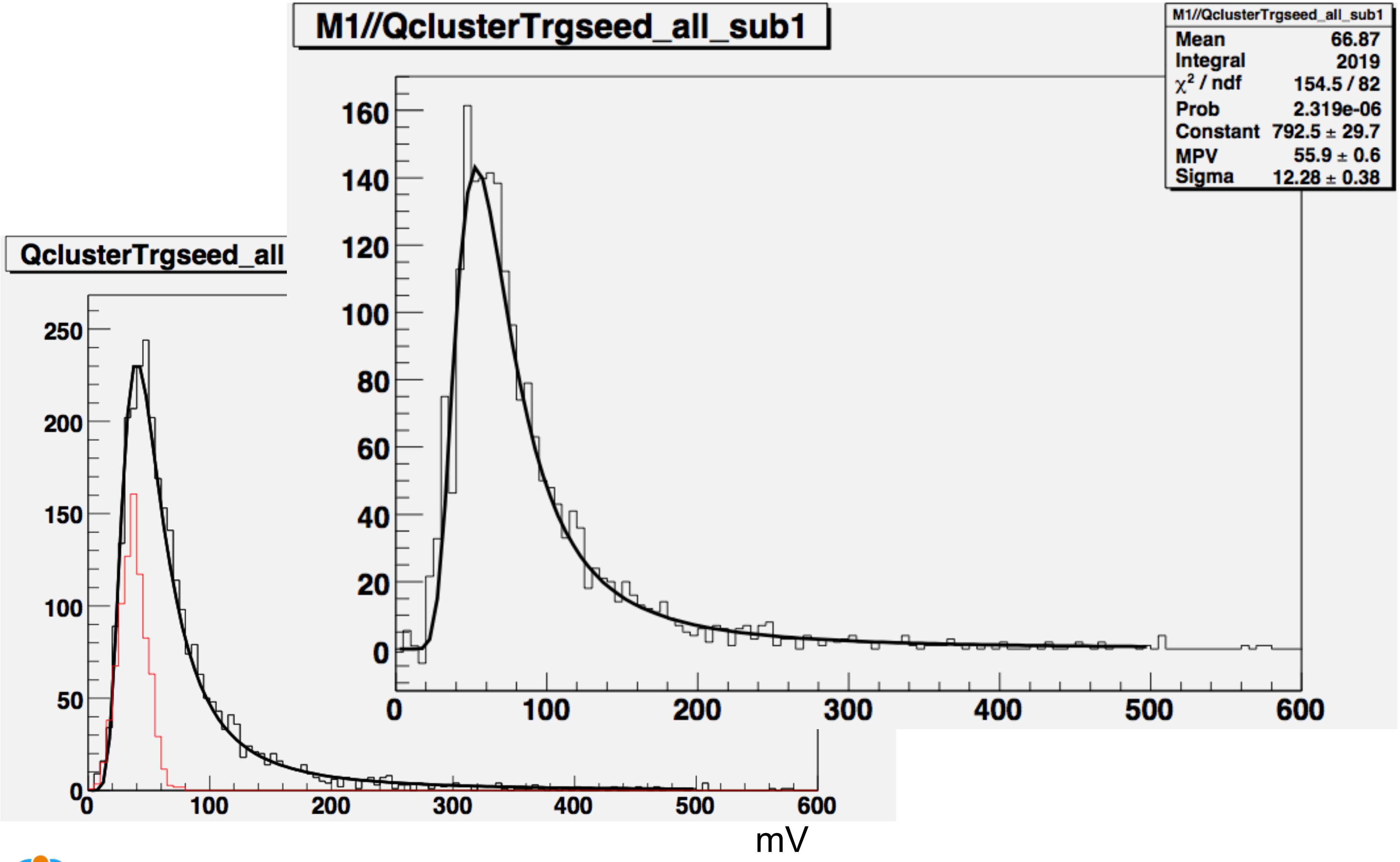


mV

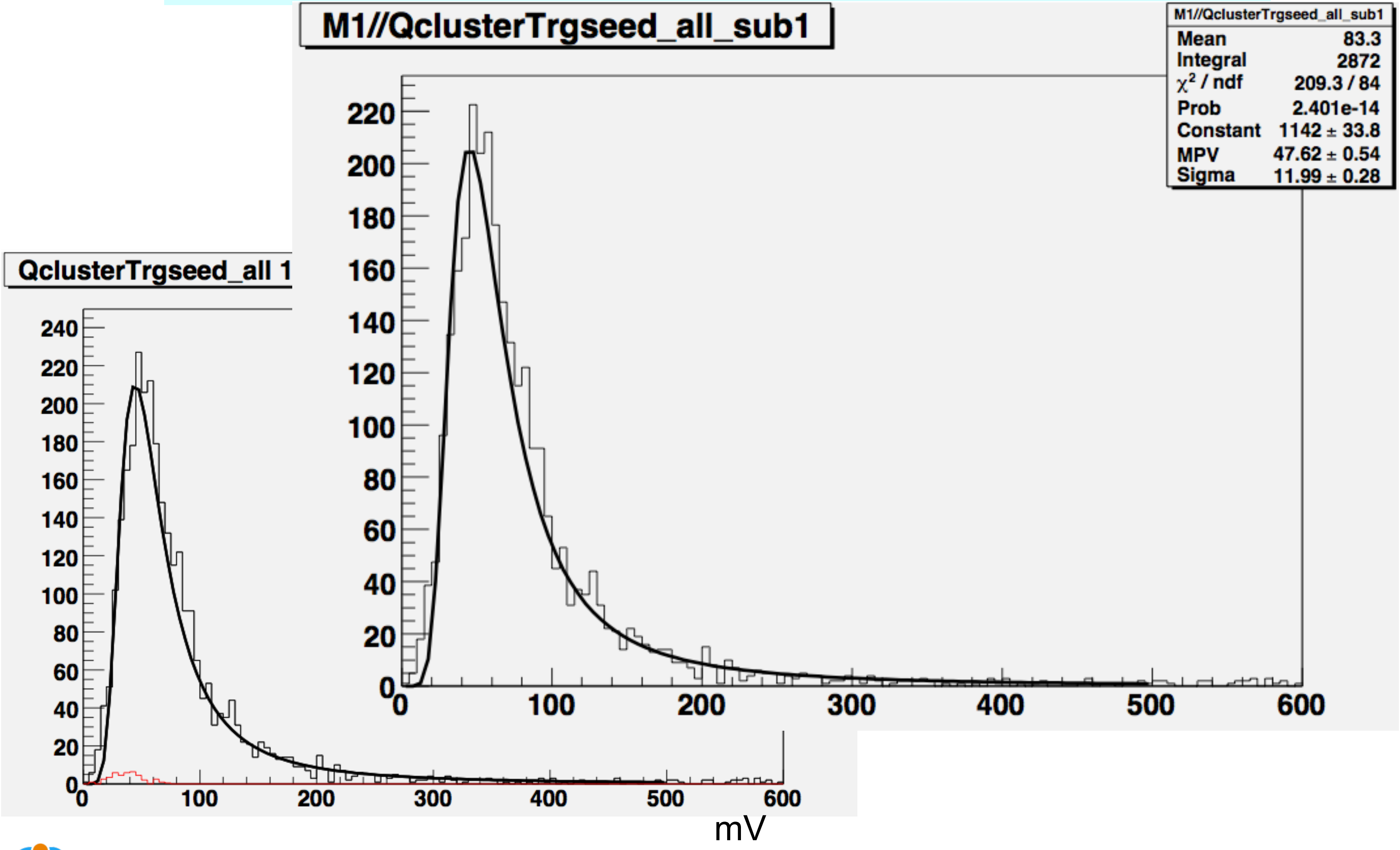
Sr90 spectrum step 2 (chip64)



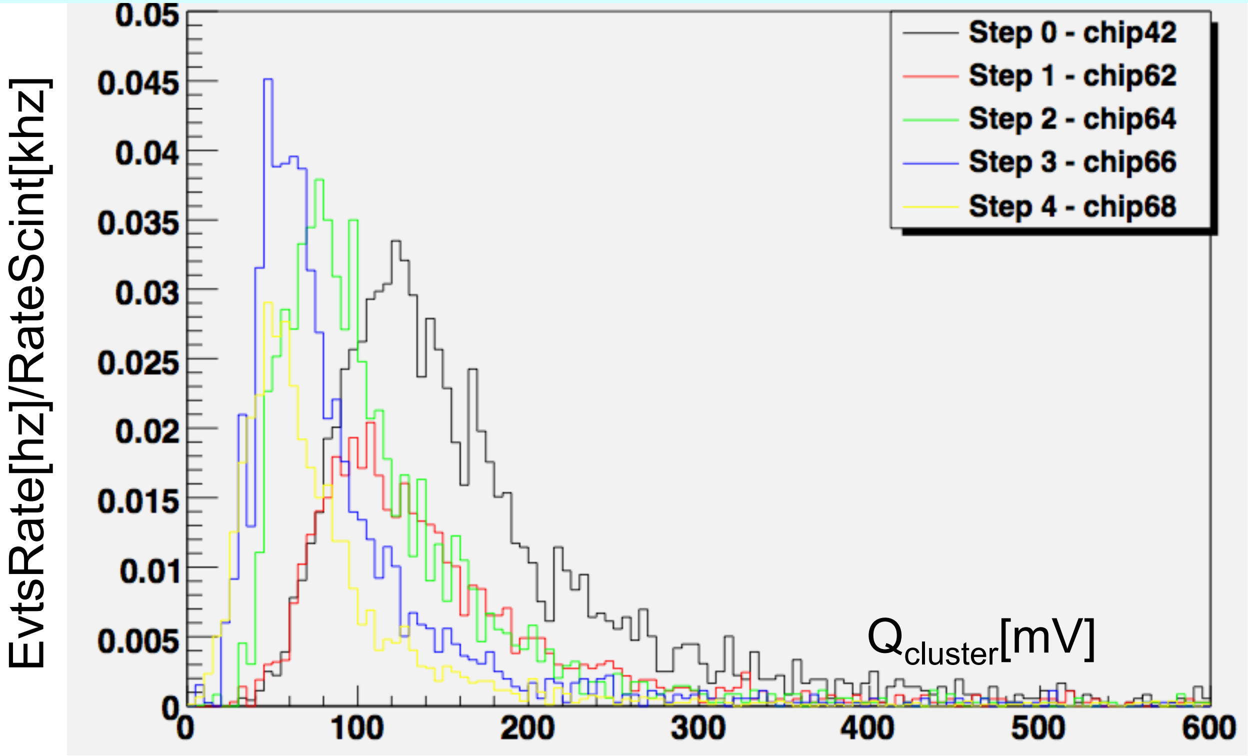
Sr90 spectrum step 3 (chip66)



Sr90 spectrum step 4 (chip68)



Comparison: Evts.Rate/RateScintillator



Note:

The PHs are naively summed up (they should be first converted in charge[e-] by a G calibration and then summed!). This effect may be important because of the different gains of the 9 pixels, even if the central pixel dominates the cluster charge.

C_{inj} present only on pixel[2,2,].

Conclusions

- The other 4 chips are under test this week
  (…they are confirming the results!)
- The Gain calibration may be performed by considering the end-point of the Fe^{55} spectrum (assuming that the endpoint corresponds to ~ $E\gamma+3\ \sigma_{noise}$) and checked with C_{inj} results on the central pixel.
- MPVs must be converted in charge (e-): the gain decreases (as Cinj calibration indicates) and the final results in charge are better than they appear now in pulse height.
- To do: tests on the 8 Low-W chips
- When the whole picture is complete, try to model the underlying damage mechanism.
- Learn the lesson to improve the design (electrodes' layout/ dimension, "more" enclosed transistors, …) for the next INMAPS submission.